Modeling and Control of a Three-Phase Five-Port Partially Isolated DC–DC Converter for DC-Powered Commercial Buildings

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***Abstract*—Integrating low-voltage, high-power energy sources and energy storage devices into medium voltage (e.g., 380 V) dc microgrids presents significant challenges due to the need for high-current and high-gain power conversion. This paper proposes a five-port, partially-isolated dc–dc converter to efficiently interface solar photovoltaics (PV), battery, fuel cell, and supercapacitor with a 380 V dc bus. At the core of the proposed topology is a current-fed asymmetrical three-phase triple active bridge structure, which results in a higher order system, making its modeling and controller design challenging. To address this, a simplified small-signal modeling approach and a proportional–integral controller-based control scheme are proposed, enabling seamless operation of the converter under any energy management scheme (EMS). Further, a limiter-based novel autonomous power adjustment strategy is introduced to manage substantial load/PV power variations between consecutive EMS updates. The topology reduces power conversion stages, requires 4% fewer semiconductor switches, uses 20% fewer magnetic cores per phase and port compered to existing equivalent fully-isolated and partially-isolated converters. It also lowers the load bus voltage undershoot/overshoot by almost 10 times for the same percentage of load change. The experimental validation on a 2 kW laboratory-scale prototype confirms the effectiveness of the control strategy and overall system performance.**

***Index Terms*—DC microgrid, energy storage integration, multiport converter (MPC), renewable energy integration, triple active bridge converter (TAB), zero-voltage switching (ZVS).**

I. Introduction

GROWING environmental concerns and depletion of fossil fuel reserves have accelerated the adoption of renewable energy sources (RESs), such as solar photovoltaics (PV), fuel cells (FC), and energy storage systems (ESSs), such as batteries and supercapacitors (SC) in direct current microgrids (DCMGs). By combining higher energy density of batteries with higher power density and long lifespan of SC, a hybrid ESS enhances DCMGs performance both in steady state and transient conditions, despite fluctuating solar PV and variable load demands [1]. It also extends battery life by reducing its' frequent charge-discharge operations. Similarly, hydrogen FC offer high energy density and sustained power generation with sufficient hydrogen storage. Hence, replacement of polluting and noisy diesel generator with clean, silent FC ensures reliable support when PV generation is insufficient for critical loads. At the same time, electricity consumption is shifting increasingly toward dc, such as multimedia systems, LED lighting, and electric vehicles. Even, refrigerators, fans, and air-conditioning systems, are transitioning to brushless dc motors for enhanced speed control and energy efficiency. Thus, integration of these RESs and ESSs technologies paves the way for developing a reliable, energy efficient and eco-friendly dc-powered microgrid for commercial buildings in the long term [2], [3], [4].

Typically separate dc–dc converters connect the solar PV, FC, battery and SC to the 380 V dc bus while a bidirectional ac–dc converter links the utility grid. A central controller oversees all local controllers via communication links, enabling centralized monitoring, data analysis, and energy management for optimized microgrid performance [5]. However, instead of separate converter based architecture, a multiport converter (MPC)-based integration strategy as shown in Fig. 1 is increasingly being preferred due to fewer power conversion stages, reduced component count, lower cost and communication overhead, and easier control [6], [7]. In general, MPCs are categorized into three types, namely, 1) nonisolated, 2) fully isolated, and 3) partially isolated.

Galvanic isolation is usually necessary for medium to high-power/voltage applications, such as commercial building microgrids, to ensure voltage matching and user safety. Hence, nonisolated topologies, which are typically restricted to low voltage/low power applications are not discussed in this article.

In the fully isolated category, authors in [8], [9], [10], and [11] proposed triple active bridge (TAB) multiport converter (MPC) topologies. All ports in these topologies are bidirectional and can function as either voltage-fed [8], [9], [11] or current-fed

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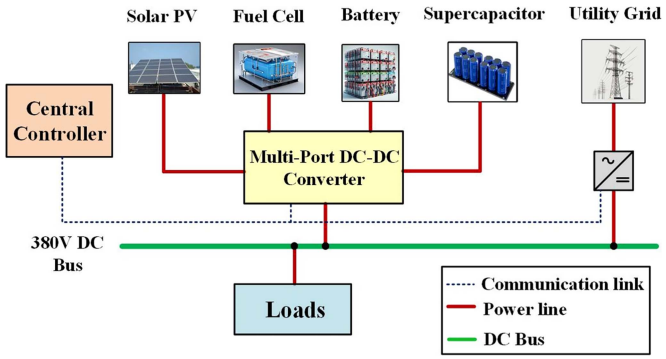


Fig. 1. Proposed multiport DC–DC converter-based structure focuses on the integration of RESs and ESSs.

(CF) ports [10], with power flow managed through a multiwinding high-frequency transformer (MW-HFT). The MW-HFT provides voltage matching among dc buses, soft-switching operation, and galvanic isolation. However, adding more ports (especially beyond three [12]) requires additional windings in the MW-HFT, increasing design complexity, component count, and control complexity due to increased coupling effects in power flow. In contrast, the authors in [13] and [14] presented a fully isolated three-port converter using two dual-active-bridge (DAB) [15] converters. Here, the secondary sides of each DAB are connected to separate core-based HFTs to form the third port, allowing decoupled power flow through each port. However, this approach increases the number of two-winding HFTs and semiconductor components as the power level and number of ports rise.

Among the three topological classifications, the partially isolated MPC structure offers higher number of ports with fewer components, higher efficiency, and power density. A DAB-based partially isolated three-port converter is proposed in [16], integrating PV and battery in a single efficient nonisolated stage using a full-bridge CF structure. It ensures galvanic isolation for the load port via a two-winding HFT. Compared to [8], the nonisolated PV-battery connection enables shared semiconductor switches and magnetic paths, reducing components while maintaining the same number of ports. However, it requires the PV voltage to be lower than the battery voltage, which results in higher conduction loss in the long cable of the low voltage PV. Further, Vettuparambil et al. [17] proposed a DAB-based four-port partially-isolated dc–dc converter with a split dc bus structure at the HFT's primary side, eliminating the voltage constraint between the PV and the battery seen in [16]. However, this configuration suffers from even-order harmonic-related conduction losses in the transformer windings and requires complex modulation techniques. Kurm and Agarwal [18] introduced a DAB-based partially isolated four-port converter, which integrates a SC and solar PV via a nonisolated boost converter on the primary side, along with a battery. This setup reduces rapid charging/discharging of battery from intermittent PV generation and load variations. However, the low SC voltage limits PV voltage, and its isolation from the load port prevents it from effectively leveraging its superior transient performance to regulate the load bus voltage. Since FC systems typically operate below 70 V [19] and SC below 60 V [20], delivering higher power demands increased current, complicating high-efficiency operation.

To address PV, battery, FC, and SC integration challenges, our previous work [21] proposes a three-phase high-power partially isolated five-port dc–dc converter for commercial building applications. The multiphase asymmetrical triple active bridge (A-TAB) topology employs three-leg and six-leg interleaved boost-integrated active bridges with a multiwinding HFT. A switched-capacitor six-leg boost converter connects the SC to the load-side converter for tight voltage regulation, while series dc-link capacitors enable high-voltage PV integration, facilitating power transfer through shared switches and HFT. However, Mondal et al. [21] is limited to the steady-state simulation results, and zero-voltage switching (ZVS) analysis of the converter. On the other hand, Mallick et al. [22] focused on a hybrid model predictive control-based energy management scheme (EMS) and experimental verification of the same using the topology from [21]. A comprehensive dynamic modeling, along with the development of a suitable control schemes for the multiphase multiport converter itself and experimental verification of both steady-state and transient performance, is presented neither in [21] nor in [22].

In general, modeling of the current-fed full-bridge triple-active bridge (CF-TAB) converter in time domain is highly challenging due to its numerous steady-state operating modes, which arise from its five degrees of freedom: these are duty cycles of three active bridges and two phase shift angles. Therefore, a frequency-domain modeling approach [23], [24] is often employed to accurately determine the steady-state voltages and currents in transformer windings. However, the detailed plant-based controller design approach for the full-bridge CF-TAB converter, while considering its full degrees of freedom, remains limited in the literature [10]. Although, Biswas et al. [10] accounted for complete control flexibility, it gives less emphasis on duty ratio control due to its negligible effect on converter dynamics, given the slow variations in FC and battery voltages. This limitation results in poor regulation of dc-link voltages during transients. In addition, the control strategy in [10] relies on feedforward compensation to mitigate the coupling effect among dc-link voltages, thereby increasing implementation complexity.

To simplify the control structure, this work shows that the coupling among dc-link voltages is negligible and can be disregarded. This results in a reduced-order system realization, where feedforward terms are eliminated. To achieve effective regulation of dc-link voltages while maintaining independent control over battery and FC ports, the duty cycle control bandwidth is set higher than that of phase shift control to minimize significant interactions [25]. In adition, a decoupling matrix is systematically formulated to mitigate the coupling effects of phase shift angles in regulating dc-link voltages.

Furthermore, while the proposed converter normally operates under an EMS as presented in [22] with power reference commands typically updating at 15 min intervals [26], [27], it is also essential that it is able to autonomously maintain

TABLE I
FEATURES OF VARIOUS MULTIPORT DC–DC CONVERTER TOPOLOGIES AND THEIR CONTROL

Method	Advantages	Disadvantages
Fully-Isolated [8], [9], [10], [11], [12], [13], [14]	• Voltage matching among DC buses (In particular with CF structure). • Galvanic Isolation among ports and ZVS operation. Specifically, wide soft-switching region due to use of series-resonant tank in [9]. • Scalable for medium to high power applications. • Decoupled power flow among ports reported in [13], [14].	• Design complexity of the MW-HFT increases with port count and power level. Furthermore, HFT cores and switch count increase more significantly with number of ports and phases in [13], [14] than in [8], [9], [10], [11], [12]. • System performance is highly sensitive to parameter variations in [9]. • Modeling and power flow control complexity increases beyond three ports due to multiple phase-shift controls and associated coupling.
Partially-Isolated Converter for RESs and ESSs integration [16], [17], [18]	• Galvanic isolation of the load port. • Non-isolated PV-battery integration increases battery charging efficiency using excess PV power. • Sharing of semiconductor switches and magnetic paths reduces component count per port and per phase. • Modeling and control complexity is moderate due to predominantly DAB-based topologies.	• Limited to PV and battery integration with low PV voltage; FC and SC integration with PV & battery has not been reported. • In [17], high even-order harmonic conduction losses require a complex modulation scheme in the control strategy, which degrades transient performance. Additionally, rapid charging/discharging of the battery is unavoidable. • The isolation from load port in [18] prevents SC from effectively utilizing its transient performance in load bus voltage regulation.
Proposed	• Supports integration of low-voltage, high-power FC and SC, and relatively high-voltage battery bank. Also enables direct high-voltage PV integration for medium/high-power applications, improving battery charging efficiency using excess PV power. • Sharing of semiconductor switches and magnetic paths reduces component count per port and per phase. Further, non-isolated, common-ground SC integration at the load side enables faster double-loop control structure for regulating the load bus voltage, achieving fast transient response. • Reduced-order model simplifies controller design. Control scheme ensures smooth power sharing among ports under any EMS. • Limiter-based autonomous power adjustment between EMS updates enhances reliability and robustness against large, unpredictable load variations and error in PV power forecast.	• High number of inductor cores increases core losses and limits power density. • Light load efficiency is typically low due to multi-phase converter structure. • The wide variation in PV MPP voltage leads to loss of voltage matching in A-TAB, increasing conduction losses in the switches & the HFT.

power balance in response to sudden and significant load and PV power variations (for example, greater than 50% of rated load) occurring between consecutive EMS updates. Therefore, as an extension of [21] and [22], this article makes the following contributions:

1) Detailed small signal modeling and a control scheme are developed to ensure smooth power distribution among different ports of the power converter under any EMS.
2) Implementation of a limiter-based novel power adjustment strategy in the control scheme to address the challenges of managing large and unpredictable load variation between consecutive EMS updates to increases reliability and robustness of the overall system.

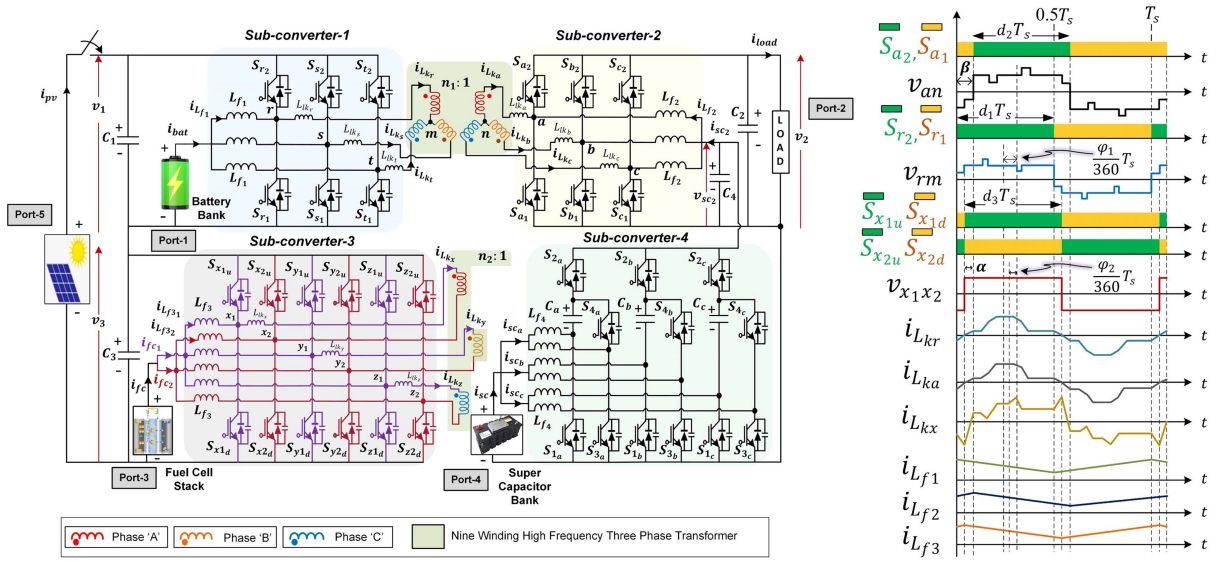
Table I summarizes the key features of various multiport dc–dc converters, highlighting the advantages and disadvantages of the proposed system compared to existing alternatives.

The rest of this article is organized as follows. Section II investigates the steady-state operating principle and frequency domain modeling of the converter. Small-signal modeling and control strategy are discussed in Section III. The effectiveness of the proposed converter and its control strategy are experimentally verified through the steady state and transient results on a scaled-down 2 kW laboratory prototype using real RES and ESSs in Section IV. Finally, Section V concludes this article.

II. PROPOSED TOPOLOGY

A. Topology Description

Fig. 2(a) presents the circuit diagram of the proposed five-port dc–dc converter, comprising four subconverter units. The battery, FC, SC, and solar PV are connected to ports 1, 3, 4, and 5, respectively, while port 2 serves as a 380 V dc load bus. All ports, except ports 3 and 5, support bidirectional power flow. Subconverters 1 and 2 utilize three-leg boost interleaved structures interfaced with two sets of three-windings of the three-phase HFTs, while subconverter 3 employs a six-leg structure, connecting to the other set of three-windings. This forms a novel three-phase CF partially isolated A-TAB topology, enabling single-stage integration of energy sources with necessary galvanic isolation. Since the PV shares the same converter units with the battery and the FC, ports 1, 3, and 5 cannot output peak power simultaneously to avoid exceeding the power limits of subconverters 1 and 3. The power rating of subconverter 2 determines the overall power rating of the five-port dc–dc converter.



(a) (b)

Fig. 2. (a) Schematic of the proposed five-port DC–DC converter and (b) key operating waveforms.

B. Operating Principle and Frequency Domain Modeling of A-TAB

Fig. 2(b) presents typical waveforms of the gate drive signals of Phase "A" switches, the voltages across and the currents through the transformer windings for fixed phase shift angles (ϕ_1 and ϕ_2) and a 50% duty ratio. The duty ratios d_1, d_2, and d_3 correspond to the top switches of subconverters 1, 2, and 3, respectively. The phase shift angles ϕ_1 and ϕ_2, control the power transfer through the HFT. In addition, α and β represent the phase displacement of switches S_{r_2} and S_{x1_u} relative to switch S_{a_2}, expressed as $\alpha = \phi_2 + \pi(d_3 - d_2)$ and $\beta = \phi_1 + \pi(d_1 - d_2)$.

The proposed TAB structure has five control variables: d_1, d_2, d_3, ϕ_1, and ϕ_2, resulting in a large number of operating modes. Therefore, based on the trigonometric Fourier series analysis, the mathematical expressions of the voltages between the switched node points and the neutral points of subconverters 1 and 2 (v'_{rm} and v_{an}) and the transformer winding voltage of subconverter 3 ($v'_{\text{x}_1\text{x}_2}$) are given by (1), (2), and (3), where, $k \in \mathbb{Z}_0^+$ and $\mathbb{Z}_0^+$ denotes the set of nonnegative integer numbers (including zero), and $d_w = \min(d_3, (1-d_3))$. The variable N represents Nth order harmonic and $\theta = \omega t = 2\pi f_s$, where f_s denotes the switching frequency. Specifically, we have

$$v_{\text{an}}(\theta) = \begin{cases} 0 & \text{if } N = 6k \\ \sum_{N=3,9,15,\ldots}^{\infty} \sqrt{2} v'_{x_N} \cos\left[N(\theta+\phi_2)\right] & \text{if } N = 6k+3 \\ \sum_{N=1,2,4,\ldots}^{\infty} \sqrt{2} v_{a_N} \cos(N\theta) & \text{if } N \neq 3k \end{cases} \quad (1)$$

$$v'_{\text{rm}}(\theta) = \begin{cases} 0 & \text{if } N = 6k \\ \sum_{N=3,9,15,\ldots}^{\infty} \sqrt{2} v'_{x_N} \cos\left[N(\theta+\phi_2)\right] & \text{if } N = 6k+3 \\ \sum_{N=1,2,4,\ldots}^{\infty} \sqrt{2} v'_{r_N} \cos\left[N(\theta+\phi_1)\right] & \text{if } N \neq 3k \end{cases} \quad (2)$$

$$v'_{\text{x}_1\text{x}_2}(\theta) = \begin{cases} 0 & \text{if } N = 2k \\ \sum_{N=1,3,5,\ldots}^{\infty} \sqrt{2} v'_{x_N} \cos\left[N(\theta+\phi_2)\right] & \text{if } N = 2k+1 \end{cases} \quad (3)$$

$$\text{where } v_{a_N} = \frac{\sqrt{2} v_2}{N\pi} \sin(N\pi d_2) \quad (4)$$

$$v'_{r_N} = \frac{\sqrt{2} v'_1}{N\pi} \sin(N\pi d_1) \quad (5)$$

$$v'_{x_N} = (-1)^{N+1} \frac{2\sqrt{2} v'_3}{N\pi} \sin^2\left(\frac{N\pi}{2}\right) \sin(N\pi d_w). \quad (6)$$

In (4)–(6), v_1, v_2, and v_3 are the dc-bus voltages across the clamp capacitors C_1, C_2, and C_3, respectively. The apostrophe ($'$) indicates that the variable is referenced to the subconverter 2 side transformer winding. The turns ratio between the transformer windings are denoted as n_1 (subconverters 1 and 2) and n_2 (subconverters 2 and 3), as illustrated in Fig. 2(a). Based on (1)–(6), it is to be noted that

$$v'_1 = \frac{v_1}{n_1} = v_2, \qquad v'_3 = \frac{v_3}{n_2} = \frac{v_2}{2} \quad (7)$$

needs to be followed to ensure voltage matching and the ranges of variation of ϕ_1 and ϕ_2 are equal at the nominal operating condition. This is necessary to avoid excessive rms currents flow through the transformer windings. The three-phase power flow relationships among ports are described by (8)–(11) and depicted in Fig. 3. For all ports except the load, power flowing out of the port is considered to be positive while at the load port, positive power flows into the port. From power balance condition, we have

$$p_1 = p_{\text{bat}} + \frac{v_1}{(v_1+v_3)} p_{\text{pv}} \quad (8)$$

$$p_3 = p_{\text{fc}} + \frac{v_3}{(v_1+v_3)} p_{\text{pv}} \quad (9)$$

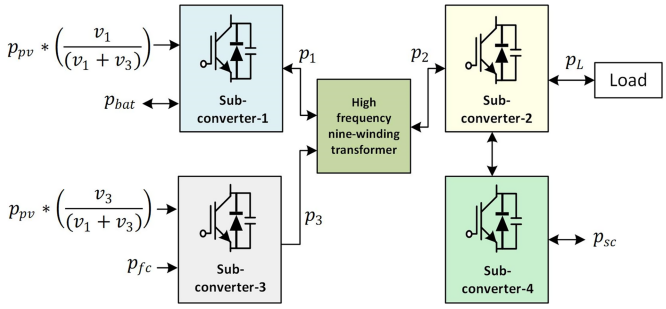


Fig. 3. Simplified power flow diagram of the proposed five-port converter.

$$p_2 = p_1 + p_3 \tag{10}$$

$$p_{\mathrm{L}} = p_2 + p_{\mathrm{sc}}. \tag{11}$$

Based on the delta equivalent transformer model of the proposed A-TAB, discussed in detail in [21], the three-phase power flows through the HFT can be expressed in terms of the dc-bus voltages (v_1, v_2, and v_3), duty ratios (d_1, d_2, and d_3) and the phase shift angles (ϕ_1 and ϕ_2) as follows:

$$p_1 = \sum_{m=1}^{\infty} E_m \sin(m\pi d_1)\sin(m\pi d_2)\sin(m\phi_1) + \sum_{n=1}^{\infty} F_n \sin(n\pi d_1)\sin(n\pi d_w)\sin\left(n(\phi_1-\phi_2)\right) \tag{12}$$

$$p_2 = \sum_{m=1}^{\infty} E_m \sin(m\pi d_1)\sin(m\pi d_2)\sin(m\phi_1) + \sum_{n=1}^{\infty} G_n \sin(n\pi d_2)\sin(n\pi d_w)\sin(n\phi_2) \tag{13}$$

$$p_3 = \sum_{n=1}^{\infty} \left[G_n \sin(n\pi d_2)\sin(n\pi d_w)\sin(n\phi_2) - F_n \sin(n\pi d_1)\sin(n\pi d_w)\sin\left(n(\phi_1-\phi_2)\right)\right] \tag{14}$$

$$\text{where } E_m = \frac{6v_1v_2}{(m^3\pi^2 X_{L_k} n_1)} \tag{15}$$

$$F_n = \frac{12v_1v_3}{(n^3\pi^2 X_{L_k} n_1 n_2)} \tag{16}$$

$$G_n = \frac{12v_2v_3}{(n^3\pi^2 X_{L_k} n_2)} \tag{17}$$

$m = 1, 2, 4, 5, 7, 8, 10, 11\ldots$; $n = 1, 5, 7, 11\ldots$. X_{L_k} represents the delta equivalent leakage reactance. Equations (12)–(14) show that the harmonic power decreases as fast as m^3 and n^3. Hence, computation up to 15 harmonics gives accurate enough results.

TABLE II
VOLTAGE GAIN AND INDUCTOR CURRENT IN DIFFERENT OPERATION MODES OF ONE CELL OF SUB CONVERTER 4

Cases	Mode	Duty Ratio * (d_4)	Output Voltage	Average Inductor Current
I	Boost	> 0.5	$v_{\mathrm{sc}_2} = \frac{2v_{\mathrm{sc}}}{(1-d_4)}$	$I_{L_1} = I_{L_2} = \frac{I_o}{(1-d_4)}$
II	Boost	< 0.5	$v_{\mathrm{sc}_2} = \frac{v_{\mathrm{sc}}}{(1-d_4)^2}$	$I_{L_1} = \frac{d_4 I_o}{(1-d_4)^2}$ $I_{L_2} = \frac{I_o}{(1-d_4)^2}$ Note: $I_{L_2} > I_{L_1}$
III	Buck	< 0.5	$v_{\mathrm{sc}} = d_4^2 v_{\mathrm{sc}_2}$	$I_{L_1} = (1-d_4) I_{\mathrm{sc}_a}$ $I_{L_2} = d_4 I_{\mathrm{sc}_a}$ Note: $I_{L_2} > I_{L_1}$
IV	Buck	> 0.5	$v_{\mathrm{sc}} = \frac{d_4 v_{\mathrm{sc}_2}}{2}$	$I_{L_1} = I_{L_2} = \frac{I_{\mathrm{sc}_a}}{(1-d_4)}$

* d_4 denotes the duty ratio of each leg bottom switch of sub-converter 4.

C. Operation of Subconverter 4

Integrating an extralow-voltage, high-power-density SC into a 380 V dc bus requires a significant voltage gain, typically between 7 and 12 times, which is achieved through the cascaded operation of subconverters 2 and 4 in the proposed topology. Subconverter 4 boosts the SC voltage (36–56 V) to 190 V, subsequently subconverter 2 raises it to 380 V. Conventional bidirectional buck–boost converters are inefficient in providing the required first-stage voltage gain (3.5–6 times). Therefore, the proposed topology employs a series capacitor-based interleaved high-gain nonisolated bidirectional three-phase dc–dc converter. Each phase unit in subconverter 4 consists of two current-carrying switch legs operating 180° out of phase, with complementary gate pulses [28]. With three units operating in parallel and in interleaved fashion with a 120° phase shift, input current handling capacity is increased while ripple current is reduced. The interleaved operation results in four distinct operational cases for each phase unit, detailed in our previous work [29] with output voltage and average inductor current expressions provided in Table II.

III. Small Signal Modeling and Control Scheme

It is desired that the proposed five-port converter be able to manage smooth power distribution among multiple energy sources and storage devices, while tightly regulating the dc-bus voltages. This section discusses the small signal modeling followed by the design of a suitable control scheme for the converter for this purpose.

Since the objective of the small signal modeling is to capture the dynamics of the system, which is much slower than the switching frequency, the switching ripple on inductor currents and capacitor voltage are removed by averaging all the variables over one switching cycle [30].

A. Small Signal Modeling of A-TAB

The relevant switching cycle average variables for modeling and controller design of the A-TAB are defined as follows:

1) State variables $\mathbf{x}$: $[\langle i_{\text{bat}}\rangle\ \langle i_{\text{fc}}\rangle\ \langle i_{\text{sc}_2}\rangle\ \langle v_1\rangle\ \langle v_2\rangle\ \langle v_3\rangle]^\top$.
2) Output variables $\mathbf{y}$: $[\langle i_{\text{bat}}\rangle\ \langle i_{\text{fc}}\rangle\ \langle i_{\text{sc}_2}\rangle\ \langle v_1\rangle\ \langle v_2\rangle\ \langle v_3\rangle]^\top$.
3) Control inputs $\mathbf{u}$: $[\langle d_1\rangle\ \langle d_2\rangle\ \langle d_3\rangle\ \langle \phi_1\rangle\ \langle \phi_2\rangle]^\top$.
4) Independent disturbance inputs $\mathbf{z}$: $[\langle v_{\text{bat}}\rangle\ \langle v_{\text{fc}}\rangle\ \langle v_{\text{sc}_2}\rangle\ \langle i_{\text{pv}}\rangle]^\top$.

Here, the symbol $\langle\rangle$ signifies switching cycle average values. It is to be noted that the transformer winding currents are not considered as state variables as their average values over one switching cycle are zero even in the transient scenario.

Kirchhoff's voltage law equations involving the inductor and the power balance equation involving the dc-link capacitors node of subconverter 1, 2 and 3 are as follows:

$$\frac{1}{3}L_{f_1}\frac{\mathrm{d}\langle i_{\text{bat}}\rangle}{\mathrm{d}t} = \langle v_{\text{bat}}\rangle - \frac{1}{3}r_{L_{f_1}}\langle i_{\text{bat}}\rangle - \langle d_1\rangle\langle v_1\rangle \tag{18}$$

$$C_1\frac{\mathrm{d}\langle v_1\rangle}{\mathrm{d}t} + \frac{\langle p_1\rangle}{\langle v_1\rangle} = \frac{\langle v_{\text{bat}}\rangle\langle i_{\text{bat}}\rangle}{\langle v_1\rangle} - \frac{1}{3}\left[L_{f_1}\frac{\langle i_{\text{bat}}\rangle}{\langle v_1\rangle}\frac{\mathrm{d}\langle i_{\text{bat}}\rangle}{\mathrm{d}t} + r_{L_{f_1}}\frac{\langle i_{\text{bat}}\rangle^2}{\langle v_1\rangle}\right] + \langle i_{\text{pv}}\rangle \tag{19}$$

$$\frac{1}{3}L_{f_2}\frac{\mathrm{d}\langle i_{\text{sc}}\rangle}{\mathrm{d}t} = \langle v_{\text{sc}_2}\rangle - \frac{1}{3}r_{L_{f_2}}\langle i_{\text{sc}_2}\rangle - \langle d_2\rangle\langle v_2\rangle \tag{20}$$

$$C_2\frac{\mathrm{d}\langle v_2\rangle}{\mathrm{d}t} - \frac{\langle p_2\rangle}{\langle v_2\rangle} = \frac{\langle v_{\text{sc}_2}\rangle\langle i_{\text{sc}_2}\rangle}{\langle v_2\rangle} - \frac{1}{3}\left[L_{f_2}\frac{\langle i_{\text{sc}_2}\rangle}{\langle v_2\rangle}\frac{\mathrm{d}\langle i_{\text{sc}_2}\rangle}{\mathrm{d}t} + r_{L_{f_2}}\frac{\langle i_{\text{sc}_2}\rangle^2}{\langle v_2\rangle}\right] - \frac{\langle v_2\rangle}{R_o} \tag{21}$$

$$\frac{1}{6}L_{f_3}\frac{\mathrm{d}\langle i_{\text{fc}}\rangle}{\mathrm{d}t} = \langle v_{\text{fc}}\rangle - \frac{1}{6}r_{L_{f_3}}\langle i_{\text{fc}}\rangle - \langle d_3\rangle\langle v_3\rangle \tag{22}$$

$$C_3\frac{\mathrm{d}\langle v_3\rangle}{\mathrm{d}t} + \frac{\langle p_3\rangle}{\langle v_3\rangle} = \frac{\langle v_{\text{fc}}\rangle\langle i_{\text{fc}}\rangle}{\langle v_3\rangle} - \frac{1}{6}\left[L_{f_3}\frac{\langle i_{\text{fc}}\rangle}{\langle v_3\rangle}\frac{\mathrm{d}\langle i_{\text{fc}}\rangle}{\mathrm{d}t} + r_{L_{f_3}}\frac{\langle i_{\text{fc}}\rangle^2}{\langle v_3\rangle}\right] + \langle i_{\text{pv}}\rangle \tag{23}$$

where R_o denotes the load resistance connected across port 2. In order to design controller, linearization is performed by introducing perturbations to the state variables, output variables, control inputs, and disturbance inputs around a steady-state operating point (i.e., $\widetilde{\mathbf{x}} = \mathbf{x} - \mathbf{X}$, $\widetilde{\mathbf{y}} = \mathbf{y} - \mathbf{Y}$, $\widetilde{\mathbf{u}} = \mathbf{u} - \mathbf{U}$ and $\widetilde{\mathbf{z}} = \mathbf{z} - \mathbf{Z}$). The resulting linearized small-signal state-space equations of the converter are represented using small-signal variables, denoted by $\sim$ above the variable names. The state-space equations are expressed as follows:

$$\dot{\widetilde{\mathbf{x}}} = \mathbf{A}\widetilde{\mathbf{x}} + \mathbf{B}\widetilde{\mathbf{u}} + \mathbf{M}\widetilde{\mathbf{z}} \tag{24}$$

$$\widetilde{\mathbf{y}} = \mathbf{H}\widetilde{\mathbf{x}} \tag{25}$$

where

$$\mathbf{A} = \begin{bmatrix} -\frac{r_{L_{f_1}}}{L_{f_1}} & 0 & 0 & -\frac{3D_1}{L_{f_1}} & 0 & 0 \\ 0 & -\frac{r_{L_{f_3}}}{L_{f_3}} & 0 & 0 & 0 & -\frac{6D_3}{L_{f_3}} \\ 0 & 0 & -\frac{r_{L_{f_2}}}{L_{f_2}} & 0 & -\frac{3D_2}{L_{f_2}} & 0 \\ a_1 & 0 & 0 & b_1 & -w_{v_2}^{p_1} & -w_{v_3}^{p_1} \\ 0 & 0 & a_2 & w_{v_1}^{p_2} & b_2 & w_{v_3}^{p_2} \\ 0 & a_3 & 0 & -w_{v_1}^{p_3} & -w_{v_2}^{p_3} & b_3 \end{bmatrix} \tag{26}$$

$$\mathbf{B} = \begin{bmatrix} -\frac{3V_1}{L_{f_1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{6V_3}{L_{f_3}} & 0 & 0 \\ 0 & -\frac{3V_2}{L_{f_2}} & 0 & 0 & 0 \\ q_1 & -w_{d_2}^{p_1} & -w_{d_3}^{p_1} & -w_{\phi_1}^{p_1} & -w_{\phi_2}^{p_1} \\ w_{d_1}^{p_2} & q_2 & w_{d_3}^{p_2} & w_{\phi_1}^{p_2} & w_{\phi_2}^{p_2} \\ -w_{d_1}^{p_3} & -w_{d_2}^{p_3} & q_3 & -w_{\phi_1}^{p_3} & -w_{\phi_2}^{p_3} \end{bmatrix} \tag{27}$$

$$\mathbf{M} = \begin{bmatrix} \frac{3}{L_{f_1}} & 0 & 0 & 0 \\ 0 & \frac{6}{L_{f_3}} & 0 & 0 \\ 0 & 0 & \frac{3}{L_{f_2}} & 0 \\ \frac{I_{\text{bat}}}{C_1V_1} & 0 & 0 & \frac{1}{C_1} \\ 0 & 0 & \frac{I_{\text{sc}_2}}{C_2V_2} & 0 \\ 0 & \frac{I_{\text{fc}}}{C_3V_3} & 0 & \frac{1}{C_3} \end{bmatrix}. \tag{28}$$

Here, $\mathbf{H}$ is an identity matrix of 6×6. It is be noted that the uppercase letters in (26)–(38) represent the steady-state values of each variables at an operating points around which linearization is performed. Certain elements of the matrices $\mathbf{A}$ and $\mathbf{B}$ are defined separately as given below:

$$w_{d_j}^{p_i} = \frac{1}{C_iV_i}\frac{\partial p_i}{\partial d_j}\bigg|_{\mathbf{op}} \quad i = 1,2,3 \text{ and } j = 1,2,3 \tag{29}$$

$$w_{v_j}^{p_i} = \frac{1}{C_iV_i}\frac{\partial p_i}{\partial v_j}\bigg|_{\mathbf{op}} \quad i = 1,2,3 \text{ and } j = 1,2,3 \tag{30}$$

$$w_{\phi_k}^{p_i} = \frac{1}{C_iV_i}\frac{\partial p_i}{\partial \phi_k}\bigg|_{\mathbf{op}} \quad i = 1,2,3 \text{ and } k = 1,2 \tag{31}$$

$$a_i = \frac{V_{S_i} - (m_i)r_{L_{f_i}}I_{S_i}}{C_iV_i} \quad i = 1,2,3 \tag{32}$$

$$b_i = \frac{I_{\text{pv}}}{C_iV_i} + \frac{D_iI_{S_i}}{C_iV_i} - w_{v_i}^{p_i} \quad i = 1,3 \tag{33}$$

$$b_2 = \frac{D_2I_{\text{sc}_2}}{C_2V_2} + w_{v_2}^{p_2} - \frac{2}{C_2R_o} \tag{34}$$

$$q_i = \frac{I_{S_i}}{C_i} + (-1)^i w_{d_i}^{p_i} \quad i = 1,2,3 \tag{35}$$

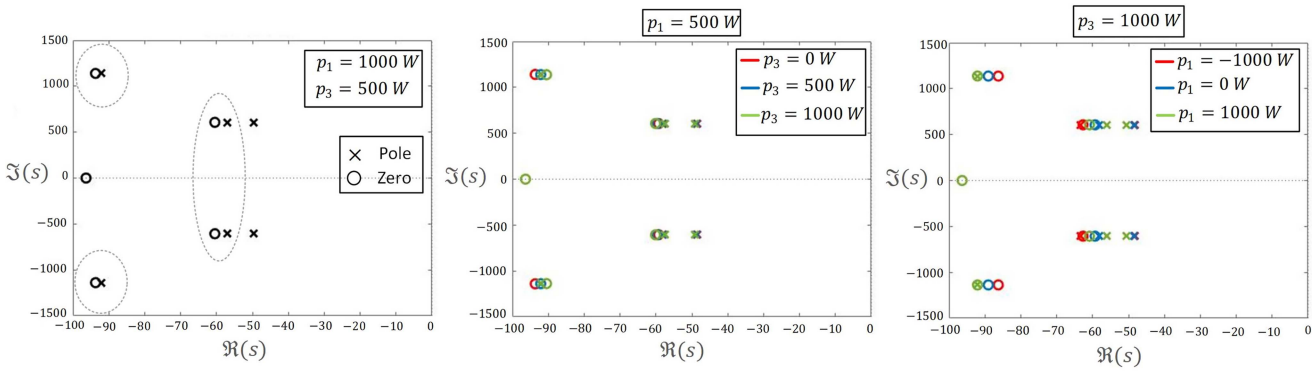


Fig. 4. (a) Pole-zero plot of $\langle \tilde{v_1} \rangle(s)/\langle \tilde{\phi_1} \rangle(s)$ for a given operating point and variation of their position with the operating points: when, (b) p_1 fixed and p_3 varies, and (c) p_3 fixed and p_1 varies.

where I_{S_i}, V_{S_i}, and m_i of (32)–(35) are defined as

$$I_{S_1} = I_{\text{bat}}, \quad I_{S_2} = I_{\text{sc}_2}, \quad I_{S_3} = I_{\text{fc}} \tag{36}$$

$$V_{S_1} = V_{\text{bat}}, \quad V_{S_2} = V_{\text{sc}_2}, \quad V_{S_3} = V_{\text{fc}} \tag{37}$$

$$m_1 = \quad m_2 = \frac{1}{3} \quad \text{and} \quad m_3 = \frac{1}{6}. \tag{38}$$

The parameters L_{f_i} $(i = 1, 2, 3)$ denote the filter inductance values, while the corresponding series resistances are represented by $r_{L_{f_i}}$ $(i = 1, 2, 3)$. Subscript "**op**" denotes the operating point used for the controller design.

As an example, based on the state-space model given in (24)–(38), the pole-zero plot of the control-to-output transfer function, $\langle \tilde{v_1} \rangle(s)/\langle \tilde{\phi_1} \rangle(s)$, generated using MATLAB, is shown in Fig. 4(a). The parameters used for this plot are the same as those used for the experimental setup described in Section IV. It is important to note that since the dynamics of PV is inherently slow it is not considered in Fig. 4 for simplicity. The operating point of controller design is as follows: $p_1 = p_{\text{bat}} = 1000\,\text{W}$, $p_3 = p_{\text{fc}} = 500\,\text{W}$, $p_2 = 1500\,\text{W}$, $p_{\text{sc}} = 500\,\text{W}$, $V_{\text{bat}} = 220\,\text{V}$, $V_{\text{fc}} = 48\,\text{V}$, $V_{\text{sc}_2} = 190\,\text{V}$, $V_{\text{sc}} = 40\,\text{V}$, $V_1 = 440\,\text{V}$, $V_2 = 380\,\text{V}$, $V_3 = 96\,\text{V}$, $I_{\text{bat}} = 4.54\,\text{A}$, $I_{\text{fc}} = 10.41\,\text{A}$, $I_{\text{sc}_2} = 2.63\,\text{A}$, $I_{\text{pv}} = 0\,\text{A}$, $D_1 = D_2 = D_3 = 0.5$, and $D_4 = 0.58$. The phase shift angles are: $\phi_1 = 11.7^\circ$, $\phi_2 = 9.4^\circ$, which are calculated based on (12) and (14). By examining Fig. 4(a), it can be inferred that two complex-conjugate pole pairs are approximately canceled by nearby zeros, as highlighted by the dashed circles. Moreover, the relative positions of these pole-zero pairs remain very close, even with variations of operating points, as shown in Fig. 4(b) and (c). Similar pole-zero cancellation behavior is observed across all other transfer functions. It can be shown that the mathematical expressions for the resulting second order open-loop transfer functions are obtained from the sixth-order system [defined in (24)] by eliminating the elements of (26) defined in (30). This essentially converts the original sixth order system to three decoupled second order systems by eliminating the effect of the dynamics of two dc-link voltages among v_1, v_2, and v_3 on the third. As a result, this leads to a simplified representation of the system dynamics. The corresponding second order open-loop transfer functions are presented below:

$$\frac{\langle \tilde{i}_{\text{bat}} \rangle}{\langle \tilde{d}_1 \rangle}(s)\Big|_{\substack{\langle \tilde{d}_i \rangle = 0 \\ \langle \tilde{\phi}_j \rangle = 0}} = -\frac{\left(s + \frac{D_1 I_{\text{bat}}}{C_1 V_1} - \frac{D_1 w_{d_1}^{p_1}}{V_1} - b_1\right)}{\frac{L_{f_1}}{3V_1}\Upsilon(s)}, \; {}^{i=2,3}_{j=1,2} \tag{39}$$

$$\frac{\langle \tilde{v}_1 \rangle}{\langle \tilde{\phi}_1 \rangle}(s)\Big|_{\substack{\langle \tilde{d}_i \rangle = 0 \\ \langle \tilde{\phi}_j \rangle = 0}} = -\frac{\left(s + \frac{r_{L_{f_1}}}{L_{f_1}}\right) w_{\phi_1}^{p_1}}{\Upsilon(s)}, \quad {}^{i=1,2,3}_{j=2} \tag{40}$$

$$\frac{\langle \tilde{i}_{\text{fc}} \rangle}{\langle \tilde{d}_3 \rangle}(s)\Big|_{\substack{\langle \tilde{d}_i \rangle = 0 \\ \langle \tilde{\phi}_j \rangle = 0}} = -\frac{\left(s + \frac{D_3 I_{\text{fc}}}{C_3 V_3} - \frac{D_3 w_{d_3}^{p_3}}{V_3} - b_3\right)}{\frac{L_{f_3}}{6V_3}\Psi(s)}, \; {}^{i=1,2}_{j=1,2} \tag{41}$$

$$\frac{\langle \tilde{v}_3 \rangle}{\langle \tilde{\phi}_2 \rangle}(s)\Big|_{\substack{\langle \tilde{d}_i \rangle = 0 \\ \langle \tilde{\phi}_j \rangle = 0}} = -\frac{\left(s + \frac{r_{L_{f_3}}}{L_{f_3}}\right) w_{\phi_2}^{p_3}}{\Psi(s)}, \quad {}^{i=1,2,3}_{j=1} \tag{42}$$

$$\frac{\langle \tilde{v}_2 \rangle}{\langle \tilde{d}_2 \rangle}(s)\Big|_{\substack{\langle \tilde{d}_i \rangle = 0 \\ \langle \tilde{\phi}_j \rangle = 0}} = -\frac{(I_{\text{sc}_2} + C_2 w_{d_2}^{p_2})(f_1 - s)}{C_2 \Gamma(s)}, \quad {}^{i=1,3}_{j=1,2} \tag{43}$$

$$\frac{\langle \tilde{i}_{\text{sc}_2} \rangle}{\langle \tilde{d}_2 \rangle}(s)\Big|_{\substack{\langle \tilde{d}_i \rangle = 0 \\ \langle \tilde{\phi}_j \rangle = 0}} = -\frac{\left(s + \frac{D_2 I_{\text{sc}_2}}{C_2 V_2} + \frac{D_2 w_{d_2}^{p_2}}{V_2} - b_2\right)}{\frac{L_{f_2}}{3V_2}\Gamma(s)}, \; {}^{i=1,3}_{j=1,2} \tag{44}$$

$$\frac{\langle \tilde{v}_2 \rangle}{\langle \tilde{i}_{\text{sc}_2} \rangle}(s)\Big|_{\substack{\langle \tilde{d}_i \rangle = 0 \\ \langle \tilde{\phi}_j \rangle = 0}} = \frac{(f_1 - s)}{\left(s + \frac{D_2 I_{\text{sc}_2}}{C_2 V_2} + \frac{D_2 w_{d_2}^{p_2}}{V_2} - b_2\right) f_2}, \; {}^{i=1,3}_{j=1,2} \tag{45}$$

where

$$\Upsilon(s) = s^2 + \left(\frac{r_{L_{f_1}}}{L_{f_1}} - b_1\right) s - \frac{b_1 r_{L_{f_1}}}{L_{f_1}} + \frac{D_1(3V_{\text{bat}} - r_{L_{f_1}} I_{\text{bat}})}{C_1 V_1 L_{f_1}} \tag{46}$$

$$\Psi(s) = s^2 + \left(\frac{r_{L_{f_3}}}{L_{f_3}} - b_3\right)s - \frac{b_3 r_{L_{f_3}}}{L_{f_3}} + \frac{D_3(6V_{\rm fc} - r_{L_{f_3}} I_{fc})}{C_3 V_3 L_{f_3}} \tag{47}$$

$$\Gamma(s) = s^2 + \left(\frac{r_{L_{f_2}}}{L_{f_2}} - b_2\right)s - \frac{b_2 r_{L_{f_2}}}{L_{f_2}} + \frac{D_2(3V_{\rm sc_2} - r_{L_{f_2}} I_{\rm sc_2})}{C_2 V_2 L_{f_2}} \tag{48}$$

$$f_1 = \frac{(3V_{\rm sc_2} - 2r_{L_{f_2}} I_{\rm sc_2} - w_{d_2}^{p_2} r_{L_{f_2}} C_2)}{L_{f_2}(I_{\rm sc_2} + C_2 w_{d_2}^{p_2})} \tag{49}$$

$$f_2 = \frac{3V_2 C_2}{L_{f_2}(I_{\rm sc_2} + C_2 w_{d_2}^{p_2})}. \tag{50}$$

The accuracy of the reduced-order model is verified later in this section. Moreover, the elimination of the elements of (26), defined in (30), leads to the following linearized dynamic equations for the state variables $\langle\tilde{v_1}\rangle$ and $\langle\tilde{v_3}\rangle$:

$$C_1\dot{\langle\tilde{v_1}\rangle} = -g_1\langle\tilde{v_1}\rangle + C_1\left(a_1\langle\tilde{i_{\rm bat}}\rangle + \tilde{u_1} + \tilde{z_1}\right) - \tilde{\Theta_1} \tag{51}$$

$$C_3\dot{\langle\tilde{v_3}\rangle} = -g_3\langle\tilde{v_3}\rangle + C_3\left(a_3\langle\tilde{i_{\rm fc}}\rangle + \tilde{u_2} + \tilde{z_2}\right) - \tilde{\Theta_2} \tag{52}$$

$$\text{where } g_i = -C_i b_i, \qquad i = 1, 3 \tag{53}$$

$$\tilde{u_1} = q_1\langle\tilde{d_1}\rangle - w_{d_2}^{p_1}\langle\tilde{d_2}\rangle - w_{d_3}^{p_1}\langle\tilde{d_3}\rangle \tag{54}$$

$$\tilde{u_2} = q_3\langle\tilde{d_3}\rangle - w_{d_2}^{p_3}\langle\tilde{d_2}\rangle - w_{d_1}^{p_3}\langle\tilde{d_1}\rangle \tag{55}$$

$$\tilde{z_1} = \frac{I_{\rm bat}}{C_1 V_1}\langle\tilde{v_{\rm bat}}\rangle + \frac{1}{C_1}\langle\tilde{i_{\rm pv}}\rangle \tag{56}$$

$$\tilde{z_2} = \frac{I_{\rm fc}}{C_3 V_3}\langle\tilde{v_{\rm fc}}\rangle + \frac{1}{C_3}\langle\tilde{i_{\rm pv}}\rangle \tag{57}$$

$$\tilde{\Theta_1} = C_1\left(w_{\phi_1}^{p_1}\langle\tilde{\phi_1}\rangle + w_{\phi_2}^{p_1}\langle\tilde{\phi_2}\rangle\right) \tag{58}$$

$$\tilde{\Theta_2} = C_3\left(w_{\phi_1}^{p_3}\langle\tilde{\phi_1}\rangle + w_{\phi_2}^{p_3}\langle\tilde{\phi_2}\rangle\right). \tag{59}$$

According to the control strategy (discussed later in this section), the battery current ($i_{\rm bat}$) and FC current ($i_{\rm fc}$) are controlled through the duty ratios (d_1 and d_3) of their respective subconverters, while the dc-link voltages (v_1, v_3) are regulated via phase shift angles (ϕ_1, ϕ_2). The current control loops in subconverters 1, 2, and 3 are designed to be faster than the voltage control loops to ensure minimal interaction between voltage and current loops.

Hence, $\langle\tilde{i_{\rm bat}}\rangle$ and $\langle\tilde{i_{\rm fc}}\rangle$ become zero in (51) and (52), and $\tilde{u_1}$ and $\tilde{u_2}$ become constant disturbances, which are ignored along with $\tilde{z_1}$ and $\tilde{z_2}$ for simplicity. Therefore, (51) and (52) can be written in Laplace domain as

$$(C_1 s + g_1)\langle\tilde{v_1}\rangle(s) = -\tilde{\Theta_1}(s) \tag{60}$$

$$(C_3 s + g_3)\langle\tilde{v_3}\rangle(s) = -\tilde{\Theta_2}(s). \tag{61}$$

Here, $\tilde{\Theta_1}$ and $\tilde{\Theta_2}$ are generated from the v_1 and v_3 voltage loop proportional–integral (PI) controllers, respectively. Moreover,

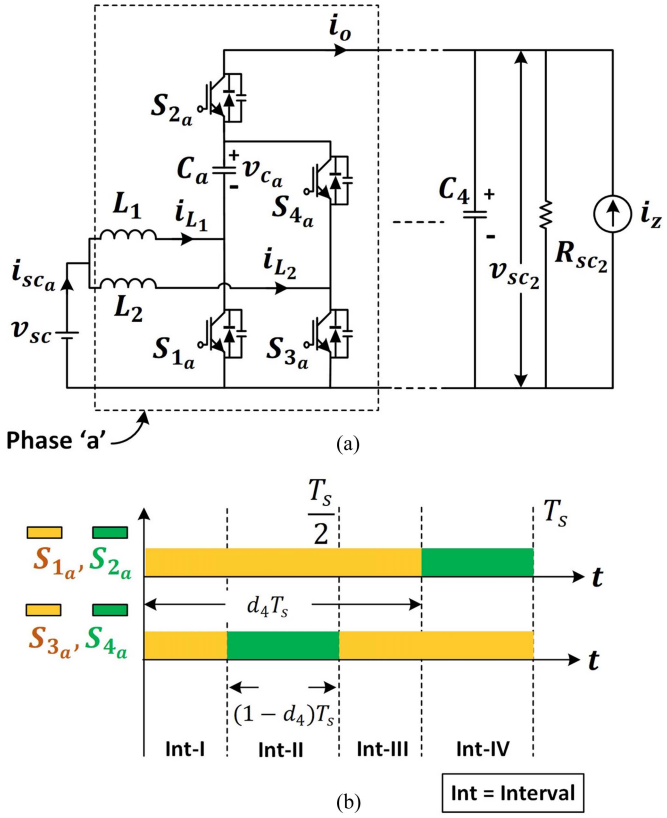


Fig. 5. Phase "a" unit of subconverter 4. (a) Schematic diagram. (b) Gate pulses for $d_4 > 0.5$.

(58)–(61) reveals that $\tilde{v_1}$ and $\tilde{v_3}$ are linearly dependent on both the phase shift angles. Therefore, decoupled control over dc-link voltages v_1 and v_3 is achieved through (62), which compensates the coupling effect of the phase shift angles ϕ_1 and ϕ_2 on both v_1 and v_3

$$\begin{bmatrix}\langle\tilde{\phi_1}\rangle\\ \langle\tilde{\phi_2}\rangle\end{bmatrix} = \begin{bmatrix}C_1 w_{\phi_1}^{p_1} & C_1 w_{\phi_2}^{p_1}\\ C_3 w_{\phi_1}^{p_3} & C_3 w_{\phi_2}^{p_3}\end{bmatrix}^{-1}\begin{bmatrix}\tilde{\Theta_1}\\ \tilde{\Theta_2}\end{bmatrix} = \underbrace{\begin{bmatrix}e_{11} & e_{12}\\ e_{21} & e_{22}\end{bmatrix}}_{\rm E}\begin{bmatrix}\tilde{\Theta_1}\\ \tilde{\Theta_2}\end{bmatrix}. \tag{62}$$

Here, **E** denotes the decoupling matrix.

B. Small Signal Modeling of Subconverter 4

For the small-signal modeling of subconverter 4, phase "a" unit of subconverter 4 is considered, as shown in Fig. 5(a). The key variables are defined as follows:

1) State variables: i_{L_1}, i_{L_2}, and v_{c_a}.
2) Output variables: i_o and $i_{{\rm sc}_a}$.
3) Control inputs: d_4.
4) Independent disturbance inputs: $v_{\rm sc}$.

For small-signal modeling, case-I from Table II is selected since subconverter 4 primarily operates in case-I or case-IV for this application. A single switching period is divided into four intervals, with intervals I and III being identical, collectively referred to as "intervals I–III". The durations of intervals II and

IV are $(1-d_4)T_s$, while that of intervals I–III is $(2d_4-1)T_s$ as shown in Fig. 5(b). The state equations for intervals I–III are

$$\underbrace{\begin{bmatrix}\dot{i}_{L_1}\\ \dot{i}_{L_2}\\ \dot{v}_{c_a}\end{bmatrix}}_{\dot{\boldsymbol{x}}} = \underbrace{\begin{bmatrix}-\frac{r_{L_1}}{L_1} & 0 & 0\\ 0 & -\frac{r_{L_1}}{L_1} & 0\\ 0 & 0 & 0\end{bmatrix}}_{\mathbf{A_1}} \underbrace{\begin{bmatrix}i_{L_1}\\ i_{L_2}\\ v_{c_a}\end{bmatrix}}_{\boldsymbol{x}} + \underbrace{\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_2}\\ 0\end{bmatrix}}_{\mathbf{K_1}} v_{\text{sc}}$$

$$i_{\text{sc}_a} = \underbrace{\begin{bmatrix}1 & 1 & 0\end{bmatrix}}_{\mathbf{Q_1}}\boldsymbol{x}, \quad i_o = \underbrace{\begin{bmatrix}\mathbf{O}_{1\times 3}\end{bmatrix}}_{\mathbf{W_1}}\boldsymbol{x} \tag{63}$$

where $\mathbf{O}$ signifies null matrix. Similarly, the state matrices for the other two intervals can be obtained as follows:

$$\mathbf{A_2} = \begin{bmatrix}-\frac{r_{L_1}}{L_1} & 0 & 0\\ 0 & -\frac{r_{L_2}}{L_2} & -\frac{1}{L_2}\\ 0 & \frac{1}{C_a} & 0\end{bmatrix}, \begin{matrix}\mathbf{K_2}=\mathbf{K_1}\\ \mathbf{Q_2}=\mathbf{Q_1}\\ \mathbf{W_2}=\mathbf{W_1}\end{matrix} \tag{64}$$

$$\text{and } \mathbf{A_4} = \begin{bmatrix}-\frac{r_{L_1}}{L_1} & 0 & \frac{1}{L_1}\\ 0 & -\frac{r_{L_2}}{L_2} & 0\\ -\frac{1}{C_a} & 0 & 0\end{bmatrix}, \begin{matrix}\mathbf{K_4}=\mathbf{K_1}\\ \mathbf{Q_4}=\mathbf{Q_1}\\ \mathbf{W_4}=\begin{bmatrix}1 & \mathbf{O}_{1\times 2}\end{bmatrix}\end{matrix}. \tag{65}$$

Averaging of the aforementioned matrices over a switching cycle leads to the switching cycle average model of a unit cell of subconverter 4 as follows:

$$\begin{aligned}\langle\dot{\boldsymbol{x}}\rangle &= \mathbf{A}_{\text{avg}}\langle\boldsymbol{x}\rangle + \mathbf{K}_{\text{avg}}\langle v_{\text{sc}}\rangle\\ \langle i_{\text{sc}_a}\rangle &= \mathbf{Q}_{\text{avg}}\langle\boldsymbol{x}\rangle, \text{ and } \langle i_o\rangle = \mathbf{W}_{\text{avg}}\langle\boldsymbol{x}\rangle.\end{aligned} \tag{66}$$

Here, (67) provides the coefficient matrices of (66)

$$\underbrace{\zeta_{\text{avg}} = \zeta_1(2d_4-1) + (\zeta_2+\zeta_4)(1-d_4)}_{\zeta=\mathbf{A},\mathbf{K},\mathbf{Q},\mathbf{W}}. \tag{67}$$

Since subconverter 4 comprises of three such unit cell connected in parallel, (68) must hold at the output capacitor node over a switching cycle as follows:

$$C_4\langle\dot{v}_{\text{sc}_2}\rangle + \frac{\langle v_{\text{sc}_2}\rangle}{R_{\text{sc}_2}} = 3\langle i_o\rangle + \langle i_z\rangle. \tag{68}$$

Here, i_z denotes the independent disturbance inputs at the output of subconverter 4. By combining (66) with (68) and eliminating $\langle i_o\rangle$, one can have the augmented state space average model as follows:

$$\begin{aligned}\langle\dot{\boldsymbol{x}}_{\text{aug}}\rangle &= \mathbf{A}_{\text{aug}_{\text{avg}}}\langle\boldsymbol{x}_{\text{aug}}\rangle + \mathbf{K}_{\text{aug}_{\text{avg}}}\langle v_{\text{sc}}\rangle + \mathbf{M}\langle i_z\rangle\\ \langle i_{\text{sc}_a}\rangle &= \mathbf{Q}_{\text{aug}_{\text{avg}}}\langle\boldsymbol{x}_{\text{aug}}\rangle, \text{ and } \langle v_{sc_2}\rangle = \mathbf{F}\langle\boldsymbol{x}_{\text{aug}}\rangle.\end{aligned} \tag{69}$$

Here, the augmented state variable vector is given as, $\langle\dot{\boldsymbol{x}}_{\text{aug}}\rangle = [\langle\dot{\boldsymbol{x}}\rangle \ \langle v_{sc_2}\rangle]^{\text{T}}$ and the coefficient matrices of (69) are given as follows:

$$\underbrace{\zeta_{\text{aug}_{\text{avg}}} = \zeta_{1_{\text{aug}}}(2d_4-1) + (\zeta_{2_{\text{aug}}}+\zeta_{4_{\text{aug}}})(1-d_4)}_{\zeta=\mathbf{A},\mathbf{K},\mathbf{Q}}$$

$$\mathbf{M} = \begin{bmatrix}\mathbf{O}_{1\times 3} & \frac{1}{C_4}\end{bmatrix}^{\text{T}}, \quad \mathbf{F} = \begin{bmatrix}\mathbf{O}_{1\times 3} & 1\end{bmatrix} \tag{70}$$

where $\mathbf{A}_{\mathbf{i}_{\text{aug}}} = \begin{bmatrix}\mathbf{A_i} & \mathbf{O}_{3\times 1}\\ \mathbf{O}_{1\times 3} & -\frac{1}{C_4 R_{sc_2}}\end{bmatrix}$, $(i=1,2)$

$$\mathbf{A}_{\mathbf{4}_{\text{aug}}} = \begin{bmatrix}\mathbf{A_4} & \begin{bmatrix}-\frac{1}{L_1}\\ \mathbf{O}_{2\times 1}\end{bmatrix}\\ \begin{bmatrix}\frac{3}{C_4} & \mathbf{O}_{1\times 2}\end{bmatrix} & -\frac{1}{C_4 R_{sc_2}}\end{bmatrix}$$

$$\mathbf{K}_{\mathbf{i}_{\text{aug}}} = \begin{bmatrix}\mathbf{K_i}\\ 0\end{bmatrix} \text{ and } \mathbf{Q}_{\mathbf{i}_{\text{aug}}} = \begin{bmatrix}\mathbf{Q_i} & 0\end{bmatrix}, \ (i=1,2,4). \tag{71}$$

By applying perturbations to the state variables, output variables, control inputs, and disturbance inputs in (69) around a steady state operating point, the small-signal switching average model of subconverter 4 is derived, as presented in (72), with corresponding coefficient matrices provided in the appendix

$$\begin{aligned}\langle\tilde{\dot{\boldsymbol{x}}}_{\text{aug}}\rangle &= \mathbf{A_s}\langle\tilde{\boldsymbol{x}}_{\text{aug}}\rangle + \mathbf{K_s}\langle\tilde{v}_{\text{sc}}\rangle + \mathbf{M}\langle\tilde{i}_z\rangle + \mathbf{G}\langle\tilde{d}_4\rangle\\ \langle\tilde{i}_{\text{sc}_a}\rangle &= \mathbf{Q_s}\langle\tilde{\boldsymbol{x}}_{\text{aug}}\rangle \text{ and } \langle\tilde{v}_{\text{sc}_2}\rangle = \mathbf{F}\langle\tilde{\boldsymbol{x}}_{\text{aug}}\rangle.\end{aligned} \tag{72}$$

Subsequently, the transfer function required for designing the controller of subconverter 4 can be obtained from the following equations:

$$\frac{\langle\tilde{v}_{\text{sc}_2}(s)\rangle}{\langle\tilde{d}_4(s)\rangle} = \mathbf{F}\left(s\,\mathbf{I_{4\times 4}} - \mathbf{A_s}\right)^{-1}\mathbf{G} \tag{73}$$

$$\frac{\langle\tilde{i}_{\text{sc}_a}(s)\rangle}{\langle\tilde{d}_4(s)\rangle} = \mathbf{Q_s}\left(s\,\mathbf{I_{4\times 4}} - \mathbf{A_s}\right)^{-1}\mathbf{G} \tag{74}$$

$$\frac{\langle\tilde{v}_{\text{sc}_2}(s)\rangle}{\langle\tilde{i}_{\text{sc}_a}(s)\rangle} = \frac{(73)}{(74)}. \tag{75}$$

To validate the accuracy of the derived small-signal model of A-TAB and subconverter 4, a set of Bode plots of the proposed five-port dc–dc converter are obtained using the "impulse response analysis" tools in "PLECS Standalone" simulation software by using the operating point given in Section III-A. The results, shown in Fig. 6, demonstrate that the derived small signal model accurately captures the converter dynamics up to half of the switching frequency.

C. Control Strategy

Fig. 7 illustrates the control block diagram of the proposed five-port dc–dc converter. It uses PI-based two-loop control structures: an outer voltage loop and an inner current loop for both subconverters 2 and 4, as shown in Fig. 7(a) and (f), respectively. The smooth current profile due to the interleaved boost inductors enables the inner current loops to achieve bandwidths as fast as approximately one-tenth of the switching frequency, allowing the outer voltage loops to maintain fast response times. Outputs of the current loops generate the required duty ratio signals (d_2^* for subconverter 2, and $d_{4_a}^*$, $d_{4_b}^*$, and $d_{4_c}^*$ for the respective phases of subconverter 4). These duty ratio signals are then compared with the carrier-based modulation signals

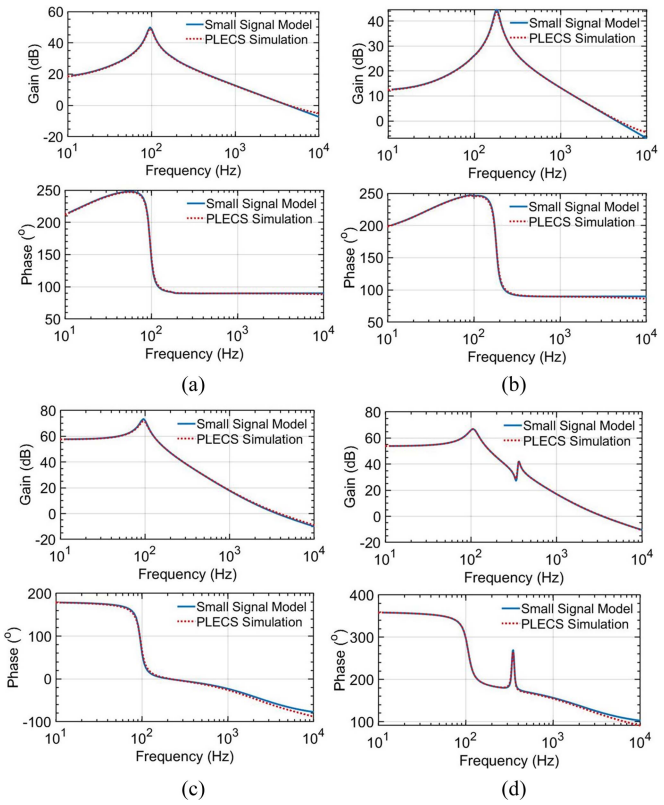


Fig. 6. Frequency response verification of the proposed five-port DC–DC converter with PLECS simulation. Bode plot of transfer functions (a) $\frac{\tilde{\langle v_1 \rangle}}{\tilde{\langle \phi_1 \rangle}}(s)$ of (40), (b) $\frac{\tilde{\langle v_3 \rangle}}{\tilde{\langle \phi_2 \rangle}}(s)$ of (42), (c) $\frac{\tilde{\langle v_2 \rangle}}{\tilde{\langle d_2 \rangle}}(s)$ of (43), and (d) $\frac{\tilde{\langle v_{sc_2} \rangle}}{\tilde{\langle d_4 \rangle}}(s)$ of (73).

and subsequently generate the pulsewidth modulation pulses required to drive the switches. To effectively harness the forecasted PV power under any irradiance conditions, a PV power controller is utilized. This controller uses a PI compensator-based slow power control loop, as illustrated in Fig. 7(d). The control loop generates the required dc-link reference voltage commands, v_1^* and v_3^*, which are tracked by the decoupled voltage controller [shown in Fig. 7(e)], with the decoupling matrix defined in (62). The decoupled control loops calculate the necessary phase shift angles (ϕ_1^* and ϕ_2^*) to facilitate smooth power transfer through the HFT, while maintaining the dc-link voltages at their respective reference values (v_1^* and v_3^*). To achieve controlled power sharing of the battery and FC, individual current control loops [see Fig. 7(b) and (c)] generate duty ratio signals (d_1^*, $d_{3_1}^*$, and $d_{3_2}^*$) to drive subconverters 1 and 3. Subconverter 3 employs two distinct current loops to ensure balanced phase currents: one controls the leading leg switches [see ■ in Fig. 2(a)], and the other controls the lagging leg switches (■). Furthermore, the two-loop structure of subconverter 2, depicted in Fig. 7(a), includes a limiter to keep sourcing and sinking currents within subconverter 4's rated limits. Similarly, the current loops in subconverters 1 and 3 [see Fig. 7(b) and (c)] incorporate limiters to regulate current at port-1 and port-3, ensuring power flow remains within the rated capacity.

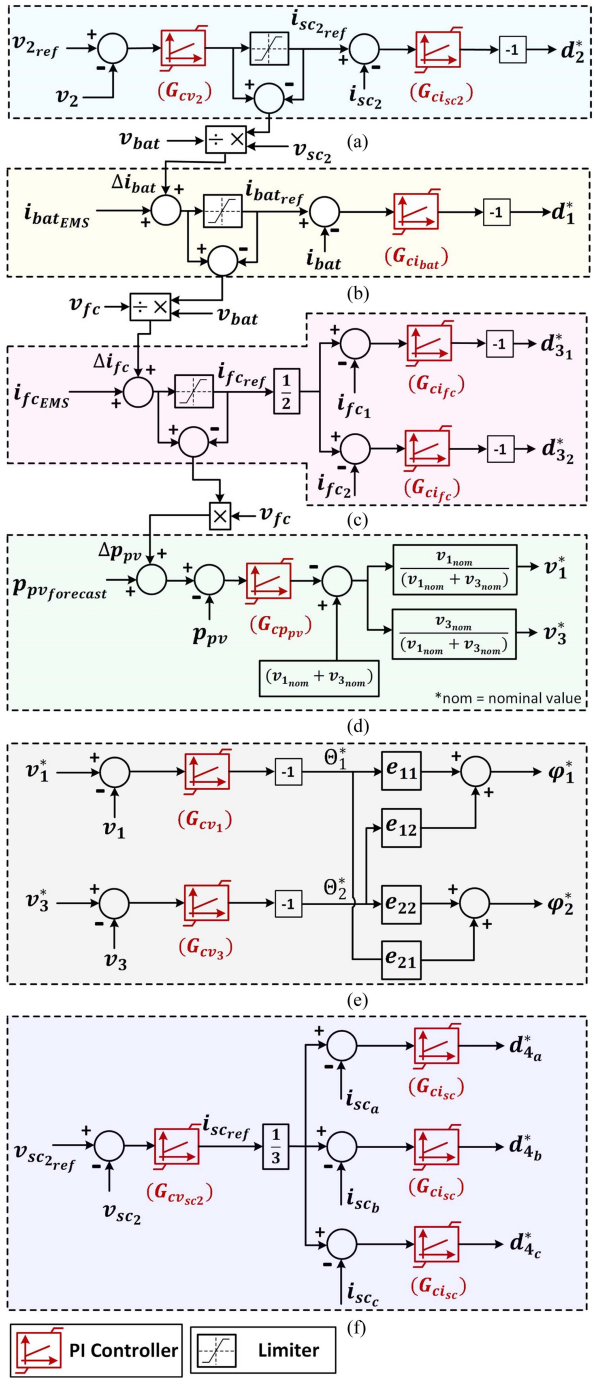


Fig. 7. Overall control block diagram of the proposed five-port DC–DC converter. (a) Nested-loop structure of subconverter 2. (b) Current controller of subconverter 1. (c) Current controller of subconverter 3. (d) Power controller of solar PV. (e) Decoupled phase shift controller. (f) Nested-loop structure of subconverter 4.

The proposed topology, designed for dc-powered commercial buildings with RES and ESSs, operates under an EMS [22]. The EMS functions as a supervisory controller, providing reference signals for battery current ($i_{\text{bat}_{\text{EMS}}}$), FC current ($i_{\text{fc}_{\text{EMS}}}$), and forecasted PV power ($p_{\text{pv}_{\text{EMS}}}$), which the local controller follows. During normal operation, errors in PV forecasts or prediction in load demand is smoothly managed by the EMS

using the SC bank. However, unexpected large errors, such as increasing load demand due to sudden grid outage cause the SC current to reach its limit, resulting in a power imbalance in the system and compromised load bus voltage regulation. To address these challenges and enhance system performance, a robust power adjustment mechanism is incorporated into the control scheme via the signal links $\triangle i_{\text{bat}}$, $\triangle i_{\text{fc}}$, and $\triangle p_{\text{pv}}$, as illustrated in Fig. 7(b)–(d), respectively. Specifically, the output of the limiter block of the inner current loop in subconverter 2 is subtracted from the input of the limiter. The resulting difference is then multiplied by the v_{sc_2} and subsequently divided by v_{bat} to generate the necessary adjustment current reference signal, $\triangle i_{\text{bat}}$, which is added with the reference signal $i_{\text{bat}_{\text{EMS}}}$ provided by the EMS for the current loop of sub-converter 1. Similarly, the current adjustment signal $\triangle i_{\text{fc}}$ and power adjustment signal $\triangle p_{\text{pv}}$ are realized from the limiter block of battery and FC current loops, respectively. This adjustment signals override the EMS commands to maintain power balance in the system.

Remark 1: It is reasonable to assume that the forecast PV power data provided by any forecasting algorithms [31], [32] or commercially available tools [33] (typically with a 15-min resolution) is accessible to the EMS. In addition, the actual measured PV power, denoted as p_{pv} in Fig. 7(d), is available to the EMS at each update interval. Based on both the forecast and actual PV power data, the EMS generates the PV power reference signal $p_{\text{pv}_{\text{EMS}}}$, which is then provided to the control loop in Fig. 7(d). The system tracks this reference signal, maintaining power balance despite minor forecast errors, which are managed through timely charge/discharge operations of the SC. However, if the forecast error is significant enough to cause the SC current to reach its limit, the proposed override operation, as discussed in Sections III-C and IV, ensures power balance is maintained.

The following section validates the proposed topology and its control scheme through experimental studies.

TABLE III
SYSTEM SPECIFICATIONS

Parameter	Value	Parameter	Value
v_{bat}	200–240 V	v_1	398–460 V
v_{fc}	43–54 V	v_3	86–100 V
v_{sc}	36–56 V	v_{pv}	485–560 V
v_{sc_2}	190 V	v_2	380 V
L_{f_1},L_{f_2}	3 mH	L_{f_3}/L_{f_4}	380 μH/704 μH
L_{lk_r},L_{lk_s},L_{lk_t}	82 μH	L_{lk_a},L_{lk_b},L_{lk_c}	62 μH
L_{lk_x},L_{lk_y},L_{lk_z}	16 μH	$C_{\text{DC block}}$[1]	70 μF
C_1,C_2,C_4	676 μF	C_3	3016 μF
C_a,C_b,C_c	117 μF	f_s	20 kHz
$P_{\text{port 1,3,4,5}}$	1 kW	$P_{\text{port 2}}$	2 kW
Filter inductors			
	L_{f_1},L_{f_2}	L_{f_3}	L_{f_4}
Ferrite core:[2]	E-65/32/27	E-55/28/25	E-65/32/27
No. of turns:	85	28	40
Peak Current:	3 A	6 A	6 A
Litz wire:[2]	50 strands	100 strands	100 strands
Air gap:	1.6 mm	1.1 mm	1.5 mm
High frequency transformer (1-phase 3-windings)			
	Winding 1	Winding 2	Winding 3
No. of turns:	38	33	17
kVA rating:	0.613 kVA	0.905 kVA	0.642 kVA
RMS Voltage:	220 V	190 V	96 V
Litz wire:[2]	50 strands	50 strands	100 strands
Ferrite core:[2]		E-65/32/27	

[1] DC blocking capacitor at transformer windings.
[2] Cosmo Ferrite (CF139 material); 38 SWG Litz wire.

IV. Experimental Results and Discussion

In order to verify the operation of the proposed five-port dc–dc converter, a laboratory-scale 2 kW prototype is developed, and its various parameters are provided in Table III. Since the required device voltage rating is higher, Infineon IKW40N120T2FKSA1 IGBT switches are used for subconverters 1 and 2, while subconverters 3 and 4 utilize IKW20N65ET7XKSA1 IGBT switches due to high current rating. Subconverters 1, 3, and 4 are rated for 1 kW each, while subconverter 2 is designed to operate up to 2 kW. The three-phase multiwinding HFT is realized using three single-phase, three-winding HFTs. The design details of each single-phase HFT unit are provided in Table III. Here,"winding no." refers to the windings connected to subconverters 1–3, respectively. Based on (13), the leakage inductance value (L_k) is selected as 185 μH to transfer 2 kW power at phase shift angles, $\phi_1 = \phi_2 = 15^\circ$ for a switching frequency of 20 kHz. The dc-link voltages are considered to be at their nominal values ($v_1 = 440$ V, $v_2 = 380$ V, $v_3 = 96$ V), with a 50% duty ratio. Subsequently, the required externally connected leakage inductance values for each phase of the respective windings are determined as, $L_{lk_r} = n_1^2(L_k/3)$, $L_{lk_a} = L_k/3$, and $L_{lk_x} = n_2^2(L_k/3)$. These are given in Table III, where n_1 and n_2 are found from (7). A design approach similar to that outlined in [34] is followed for selecting the filter capacitances (C_1, C_2, C_3, and C_4) and series capacitances (C_a, C_b, and C_c) of subconverter 4, ensuring less than 1% ripple voltage of their rated values. The filter inductors L_{f_1} and L_{f_2} are chosen to limit ripple current to below 15%, while L_{f_3} and L_{f_4} are designed with less than 2% ripple current of their rated values. This effectively suppresses ripple voltage across the dc-link capacitors and minimizes ripple currents at various CF ports (ports 1, 3, and 4). Notably, in order to avoid excessive filter inductance at port 1 due to its higher voltage and lower current rating, a higher ripple current ($< 15\%$) is considered, compared to ports 3 and 4. The photograph of the developed prototype is presented in Fig. 8. The proposed control scheme is implemented on an AMD Artix 7 FPGA (XC7A50T1FGG484C) and programmed using the Verilog HDL. The Raspberry Pi is utilized to implement the EMS algorithm and provide the EMS commands to FPGA as discussed in our prior work [22].

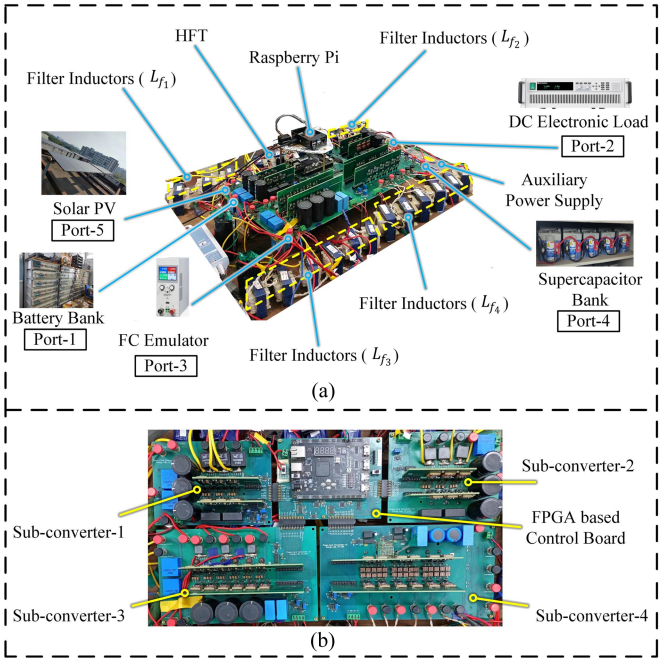


Fig. 8. Laboratory scale prototype of the proposed five-port DC–DC converter. (a) Overall system view. (b) Top view of power and control board.

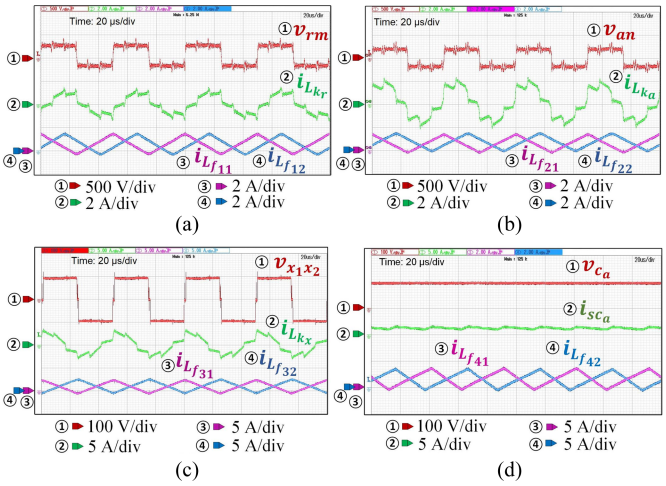


Fig. 9. Steady-state waveforms at nominal voltage levels with load power of 830 W. Transformer winding voltage, transformer winding current, and filter inductor current of two interleaved phases for (a) subconverter 1, (b) subconverter 2, and (c) subconverter 3. (d) voltage across the series capacitor and the filter inductor currents of one unit cell of subconverter 4.

Fig. 9 presents the steady-state experimental results of the proposed converter under a load demand of 830W. In this study, all dc-link voltages are maintained at their nominal rated values: $v_1 = 440$ V, $v_2 = 380$ V, $v_3 = 96$ V, and $v_{sc_2} = 190$ V. The duty cycles for subconverters 1–3 are approximately 0.5, while the duty cycle for subconverter 4 is set to 0.58 to regulate the respective dc-link voltages corresponding to the port voltages: $v_{bat} = 220$ V, $v_{fc} = 48$ V, and $v_{sc} = 40$ V. The battery discharges at 1.81 A, and the FC supplies 5.6 A of current. Solar PV contributes approximately 100 W of power, with the remaining power demand balanced by the SC to meet the total load. It can be observed that the waveforms of the transformer currents ($i_{L_{kr}}$, $i_{L_{k_a}}$, and $i_{L_{k_x}}$) corresponding to subconverters 1–3 exhibit approximately symmetric patterns, as the duty ratios are set to 0.5. The influence of reflected triplen harmonics on the per-phase winding voltages, v_{rm} and v_{an}, is evident in Fig. 9(a) and (b). This behavior differs from that of the symmetrical TAB structure [11], where conventional six-step voltage waveforms typically appear. This verifies the theoretical analysis presented in Section II. Furthermore, the current through the filter inductors in all CF ports maintains an interleaved operation, which reduces the ripple current at the respective ports.

Based on the ZVS analysis presented in [21], Fig. 10(a)–(c) illustrate the ZVS characteristics of subconverters 1–3, respectively, under varying operating conditions. Here, the ZVS plane, p_1 and p_3 are normalized with respect to the rated power of subconverters 1 and 3, respectively, as referenced in Fig. 3. It can be observed that subconverter 2 exhibits the widest ZVS range, while subconverter 3 has the narrowest. Under light load conditions (approximately < 160 W), all switches operate with ZVS, as shown in Fig. 10(d) and (e). However, as the contributions from the battery and FC increase, subconverters 1 and 3 shift to hard-switching operation. In contrast, subconverter 2 continues to maintain ZVS when the power drawn from the SC remains low, as indicated in the ZVS plots in Fig. 10(a)–(c). This behavior is further supported by the experimental results in Fig. 10(f) and (g), where the battery and FC supply approximately 586 W and 552 W, respectively, while the SC draws only about 20 W for a total load of 941 W. Specifically, the bottom switches of subconverter 1 lose ZVS operation with increasing battery power share, while both the leading and lagging leg bottom switches of subconverter 3 experience hard turn-ON behavior as the FC contribution increases.

Figs. 11 and 12 illustrates the dynamic performance of the proposed five-port converter under step changes in the battery and FC current references, respectively. The controller parameters, including PI gain values (k_p, k_i), bandwidth, and phase margin for each control loop of Fig. 7, are summarized in Table IV. These parameters are designed using the corresponding linearized plant models, also provided in the table, based on the operating points described in Section III-A. The "PID Tuner" tool in MATLAB Simulink is used to calculate the k_p, k_i values ensuring a sufficient phase margin (greater than 60°) and gain margin above 20 dB. As shown in Fig. 11(a) and (b), a battery current step from 0.5 to 3 A and vice versa is applied at 220 V with a 150 W load. The high-bandwidth battery current controller (1.6 kHz) effectively tracks the reference by adjusting subconverter 1's duty cycle. The phase-shift controller regulates the dc-link voltages (v_1 and v_3) and transfers increased battery power to the load, as evident from the rise in transformer currents ($i_{L_{kr}}$ and $i_{L_{k_a}}$) in Fig. 11(b). Meanwhile, the nested loop control structure of subconverters 2 and 4 controls the charging/discharging operation of the SC, ensuring power balance and regulates the load bus voltage v_2 at 380 V with minimal transient effects, as shown in Fig. 11(b). Similarly, Fig. 12(a) and (b) illustrates the transient response during a step change in the FC current reference from 1 A to 10 A at 48 V with a 150 W load. The FC current controller, with a lower bandwidth

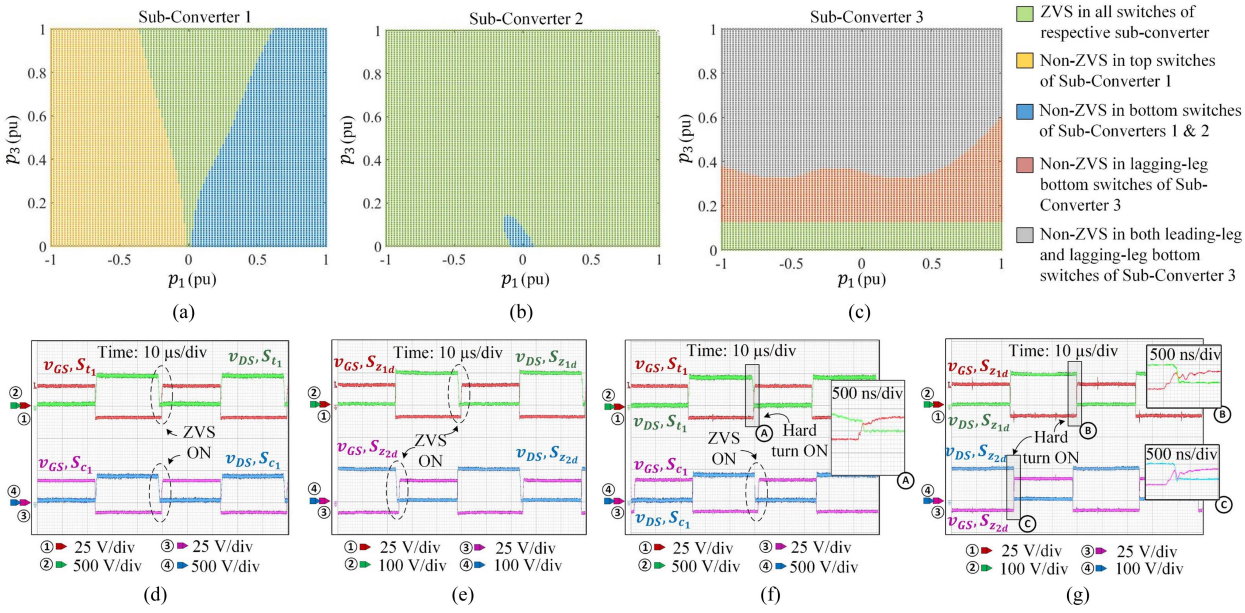


Fig. 10. (a), (b), (c) ZVS region of subconverters 1–3 on p_1–p_3 plane at $p_{pv} = 0$, $p_{sc} = 30$ W and 50% duty ratio. Experimental verification of ZVS turn-ON of all switches under light load conditions. (d) Bottom switches of subconverters 1 and 2. (e) Subconverter 3. Hard turn-ON under high load conditions. (f) Subconverter 1, while subconverter 2 maintain ZVS. (g) Subconverter 3.

TABLE IV
PI GAIN OF PI CONTROLLERS (SHOWN IN FIG. 7) FOR THE EXPERIMENTAL SETUP

PI controller	$G_{C_{v_2}}$	$G_{C_{i_{sc_2}}}$	$G_{C_{i_{bat}}}$	$G_{C_{i_{fc}}}$	$G_{C_{v_{sc_2}}}$	$G_{C_{i_{sc}}}$	$G_{C_{v_1}}$	$G_{C_{v_3}}$
Proportional Gain (k_p)	0.73	0.033	0.016	0.004	0.8	0.045	0.166	0.759
Integral Gain (k_i)	20	7.11	10	1.37	60	10	4.51	25.78
Phase margin	83°	89.3°	85.7°	87.3°	86°	89.3°	83.7°	82.4°
Bandwidth	130 Hz	2 kHz	1.6 kHz	750 Hz	100 Hz	2 kHz	55 Hz	57 Hz
Plant	(45)	(44)	(39)	(41)	(75)	(74)	(60)	(61)

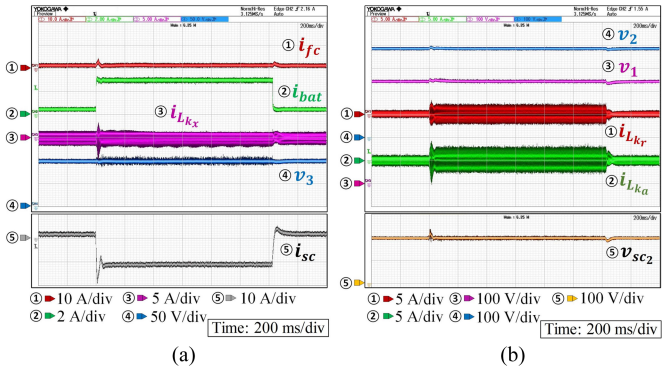


Fig. 11. Transient response at 220 V battery, 48 V FC with 150 W load. (a) Battery current step (0.5 A → 3 A → 0.5 A) under fixed 1 A FC current, showing impacts on transformer current $i_{L_{k_x}}$, DC-link voltage v_3, and SC current. (b) DC-link voltages v_1 and v_{sc_2}, load bus voltage v_2, and transformer current $i_{L_{k_r}}$ and $i_{L_{k_a}}$.

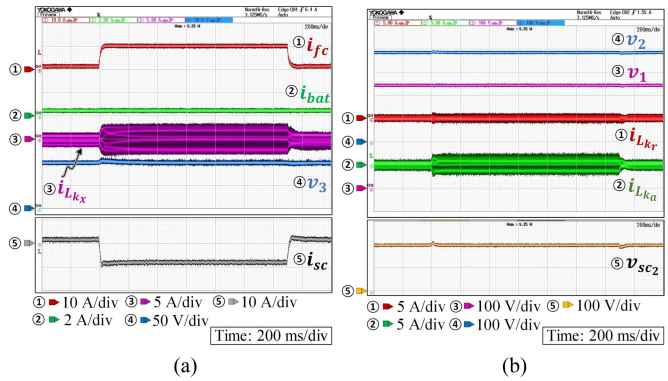


Fig. 12. Transient response at 220 V battery, 48 V FC with 150 W load. (a) FC current step (1 A → 10 A → 1 A under fixed 0.5 A battery current. Its' effect on transformer current $i_{L_{k_x}}$, DC-link voltage v_3, and SC current. (b) DC-link voltages v_1 and v_{sc_2}, load bus voltage v_2, and transformer current $i_{L_{k_r}}$ and $i_{L_{k_a}}$.

of 750 Hz to emulate the FC slow dynamics, effectively tracks the reference. The decoupled phase-shift controller regulates phase shift angles to transfer increased FC power to the load. As shown in Fig. 12(a) and (b), transformer currents ($i_{L_{k_x}}$ and $i_{L_{k_a}}$) of subconverters 3 and 2 rise as the FC current reaches 10 A. Similar to the battery current transient, SC minimizes the impact on the load bus voltage.

Fig. 13 illustrates the load transient performance of the five-port converter. The load changes from 150 W (7.5%) to 1123 W

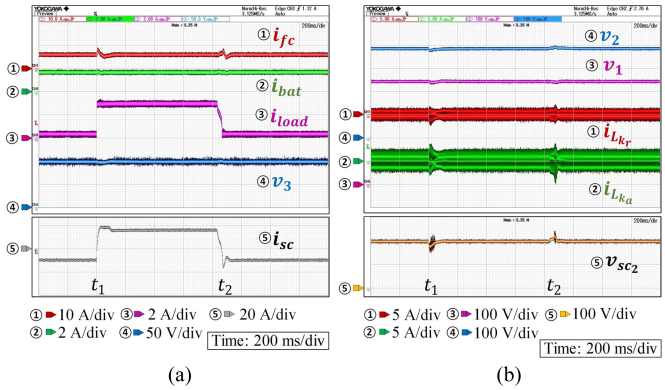


Fig. 13. Transient response during step change in load power: 150 W → 1123 W → 150 W. (a) Status of battery current, FC current, SC current and DC-link voltage v_3. (b) Status of load bus voltage v_2, DC-link voltages v_1 and v_{sc_2}, and transformer currents $i_{L_{kr}}$ and $i_{L_{ka}}$.

(56.15%) at t_1 and returns to 150 W at t_2. During this transition, battery and FC power contributions remain constant at 410 W (1.86 A at 220 V) and 315 W (6.56 A at 48 V), respectively. The fast response of the SC (operating around 40 V) maintains the load bus voltage at 380 V with a maximum overshoot of 2.63% and a settling time of 50 ms. In addition, other dc-link voltages remain well-regulated, with v_{sc_2} experiencing approximately 10% overshoot and a 50 ms settling time.

Fig. 14 presents the experimental demonstration of the override operation discussed in Section III-C. The power share references from the EMS are assumed to remain constant, as load changes are considered to occur between two consecutive EMS updates, necessitating override operation. The maximum power outputs for port-1 and port-3 are limited to 300 W each, while the SC port (port-4) is restricted to 250 W. These power limits are arbitrarily chosen for this case study. In practical scenarios, limits are determined based on battery and SC state of charge, FC level of hydrogen, and the power ratings of respective subconverter units. As shown in Fig. 14, the controller is turned ON at t_1, enabling the converter to track forecasted PV power (340 W). Meanwhile, the battery and FC share 108 W ($i_{\text{bat}} = 0.49$ A at 220 V) and 63 W ($i_{\text{fc}} = 1.31$ A at 48 V), respectively, as per EMS commands for a 290 W load. At t_2 instant first load change occurs (290 W to 500 W), among a series of increasing load changes as shown in Fig. 14(a). This is taken care of by the SC to maintain power balance in the system. However, the change in load power at t_3 (500 W to 800 W) causes the SC power share to hit its' upper limit and makes it essential for the battery to increase its' power share despite unchanged EMS commands. A further load change at t_4 (800 W to 1000 W) causes power share for the battery to hit its upper limit. The requirement of additional load power is compensated by the FC, increasing its' power share despite unchanged EMS commands. Even further load change (1000 W to 1200 W) at t_5 instance necessitates PV power shares to increase since FC hits its' power share limit as shown in Fig. 14(b). The applied load power is reduced after t_6 and system returns back to the state of interval t_2–t_3 after t_7 and start following the EMS commands again. The verification of power balance through out this case study is confirmed by the tight regulation of load bus voltage (v_2) to 380 V and the output voltage of sub-converter 4 (v_{sc_2}) to 190 V as shown in Fig. 14(c). Conversely, the variation in the dc-link voltage v_1 and v_3 is necessary to control PV port power output. This override operation proves useful in practical scenarios, such as a sudden utility grid fault, which significantly increases load demand on the multiport converter in no time. It is also applicable after sudden decrease in load demand, which drives subconverter 2 to its lower limit, requiring the battery, FC, and PV power shares to adjust independently of EMS commands to maintain system power balance. In addition, if a significant deviation in PV power from forecasted values causes the SC current to reach its limit, the override operation helps preserve power balance in the system. Thus, the proposed override operation enhances the dc microgrid controller's reliability and robustness.

TABLE V
COMPARISON OF THE PROPOSED MULTIPORT CONVERTER WITH A EQUIVALENT POWER RATED SEPARATE CONVERTER STRUCTURE

Topology	No. of Transformer Core	No. of Inductor Core	No. of Switches
Separate converter structure [35], [36]	9	15	48
Proposed Multiport converter	3	18	36

Fig. 15 presents the measured efficiency (the ratio of net output power to net input power) of the proposed five-port converter for different power share scenarios. The efficiency is higher when the battery and SC share near-rated power. Efficiency decreases with increased FC power share due to higher conduction and switching losses in subconverter 3. In addition, Fig. 16 shows the simulated loss breakdown for battery and SC operation near rated power (operating point ★ in Fig. 15). The total loss is approximately 130 W for a 1800 W load. Semiconductor losses account for 65%, with 34% from conduction losses and 31% from switching losses, primarily during IGBT turn-OFF events. Therefore, replacing IGBTs in subconverters 3 and 4 with MOSFETs could reduce both conduction and switching losses, improving efficiency. The remaining losses are distributed as 26% in inductors and 9% in transformers.

Table V compares the proposed system with a separate converter-based structure of equivalent power rating. In the referenced separate converter setup, the battery is connected to the load bus via the converter from [35], while the FC and SC are interfaced using two converters as reported in [36]. The solar PV is connected to the series-configured dc-link capacitor of the battery and FC converter, similar to the proposed topology. As shown in the table, the proposed design reduces the number of switches and overall magnetic core requirements. Moreover, its integrated structure also simplifies control and reduces communication overhead. Table VI compares the proposed system with similar existing multiport converters, showing a 20% reduction in transformer cores and a 4% reduction in number of switches per phase per port, along with enhanced transient performance,

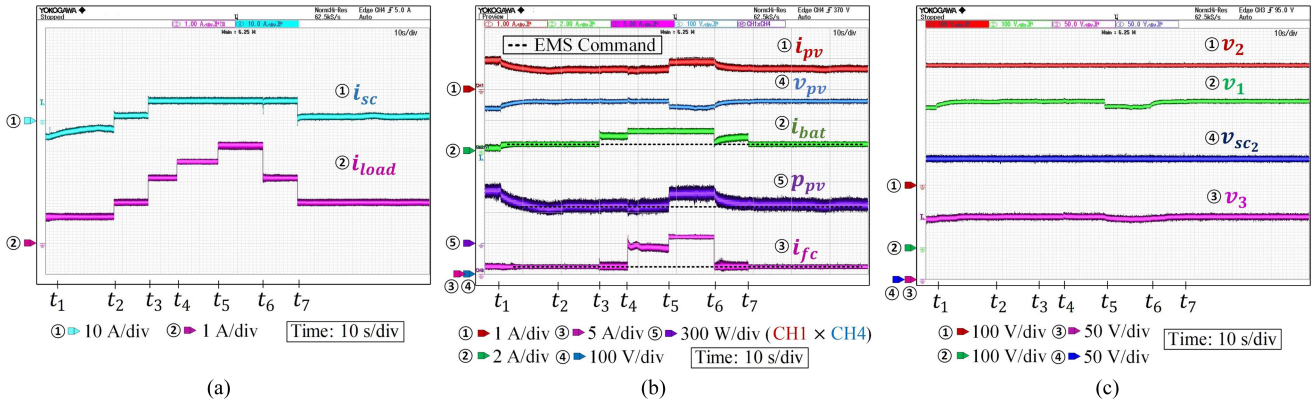


Fig. 14. Override operation. (a) Port-4 current and load profile. (b) Waveform of port-1, port-3, and port-5 currents and PV power shares. (c) Status of load bus voltage (v_2) and other DC-bus voltages v_1, v_3, and v_{sc_2}.

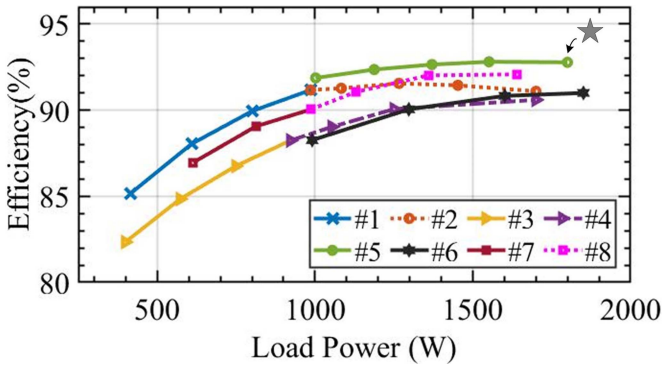


Fig. 15. Efficiency plot of the experimental prototype at different operating conditions with $v_{bat} \approx 219\,V$, $v_{fc} \approx 47\,V$, and $v_{sc} \approx 43\,V$. **(1)** $p_{fc} \approx 100\,W$, $p_{pv} = 0\,W$, $p_{sc} \approx 0\,W$, and p_{bat} : $399\,W \rightarrow 991\,W$. **(2)** $p_{bat} \approx 991\,W$, $p_{pv} = 0\,W$, $p_{sc} \approx 0\,W$, and p_{fc} : $98\,W \rightarrow 936\,W$. **(3)** $p_{bat} \approx 100\,W$, $p_{pv} = 0\,W$, $p_{sc} \approx 0\,W$, and p_{fc} : $393\,W \rightarrow 954\,W$. **(4)** $p_{fc} \approx 954\,W$, $p_{pv} = 0\,W$, $p_{sc} \approx 0\,W$, and p_{bat} : $100\,W \rightarrow 920\,W$. **(5)** $p_{bat} \approx 898\,W$, $p_{pv} = 0\,W$, $p_{fc} \approx 99\,W$, and p_{sc} : $100\,W \rightarrow 940\,W$. **(6)** $p_{fc} \approx 935\,W$, $p_{pv} = 0\,W$, $p_{bat} \approx 99\,W$, and p_{sc} : $93\,W \rightarrow 914\,W$. **(7)** $p_{pv} \approx 514\,W$, $p_{sc} \approx 0\,W$, $p_{bat} \approx 99\,W$, and p_{fc} : $95\,W \rightarrow 495\,W$. **(8)** $p_{pv} \approx 514\,W$, $p_{sc} \approx 0\,W$, $p_{fc} \approx 495\,W$, and p_{bat} : $101\,W \rightarrow 590\,W$.

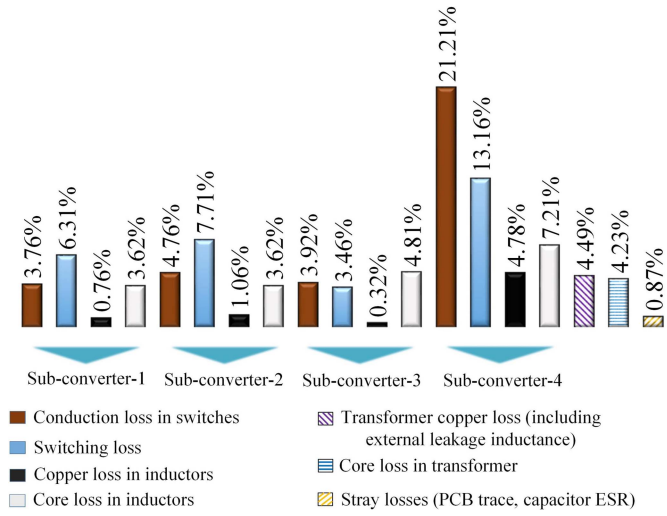


Fig. 16. Approximate loss breakdown of the proposed five-port converter for the operating point ★ as marked in efficiency plot (Fig. 15): $p_{load} \approx 1800\,W$, $p_{bat} \approx 898\,W$, $p_{fc} \approx 99\,W$, $p_{pv} = 0\,W$ and $p_{sc} \approx 940\,W$. The measured efficiency is 92.78%.

such as reduction of undershoot/overshoot by almost 10 times for the same percentage of load change. It is worth mentioning that the hardware implementation of the proposed topology is primarily intended to demonstrate the proof of concept, rather than to optimize for power density or cost at this stage. In addition, the detailed information on system cost and power density are not available for the topologies referenced for comparison. Therefore, a quantitative comparison of system cost and power density are kept beyond the scope of this article.

Remark 2: To assess the stability of the proposed system, the closed-loop state-space models of both the A-TAB and subconverter 4 are derived using the small signal model presented in Section III and chosen PI controller gain values listed in Table IV, following a similar approach to the stability analysis presented in [37]. Fig. 17 illustrates the variation in the locations of the closed-loop poles for the original system described by (24) (for the A-TAB) and (72) (for subconverter 4), under varying disturbance input values. As shown in Fig. 17(a), all closed-loop poles have negative real parts, indicating system stability. Furthermore, the variation in the closed-loop pole locations of the A-TAB with changes in independent disturbance input, such as PV current (i_{pv}) is minimal, particularly for the dominant poles, as highlighted in the zoomed view in Fig. 17(a). A similar trend is observed for subconverter 4 as well in Fig. 17(b), where all closed-loop poles have negative real parts and exhibit negligible shifts in their locations, even under a full swing of the independent disturbance input i_z. This analysis signifies negligible deviation in system's transient responses from the controller's designed operating points. Thus, despite the presence of several controllers and control loops (in Fig. 7), the overall system remains stable across a wide range of operating conditions.

V. Conclusion

This article proposes a novel integration strategy of solar PV, battery, FC and SC through a five-port integrated dc–dc converter structure. Compared to existing separate converter as

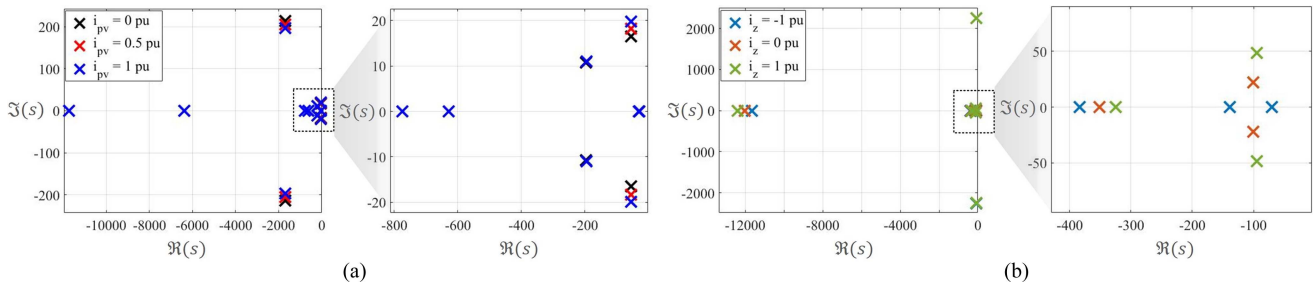


Fig. 17. Closed-loop pole locations for (a) A-TAB under varying PV current (i_{pv}) and (b) subconverter 4 under variation of disturbance input i_z.

TABLE VI
COMPARISON OF PROPOSED AND REPORTED MULTI-PORT CONVERTERS

MPC Architecture	Fully-Isolated [12]	Partially-Isolated [18]	Proposed Work
Port count/Phase count	4/1	4/1	5/3
No. of Transformer Core ÷ (Phase × Port)	0.25	0.25	0.20
No. of Inductor Core ÷ (Phase × Port)	1.00	0.75	1.20
No. of Switch ÷ (Phase × Port)	4.00	2.50	2.40
PV to Load	Isolated	Isolated	Isolated
SC to Load	Isolated	Isolated	Non-Isolated
Peak Efficiency	95.4%	94.3%	92.78%
Switch Type	SiC-MOSFET	Si-MOSFET	Si-IGBT
No. of Power Conversion Stages*	α = 1, β = 1, – ζ = 1.	α = 1, β = 1, γ = 2, –	α = 1, β = 1, γ = 2, ζ = 1.
Load Bus Voltage	160 V	100 V	380 V
Load Change (W)	730→928	80→350	150→1123
Overshoot/Undershoot (%)**	10	26	2.63
Settling time (ms)	50	80	50
Control Complexity	High	Medium	Medium

* α :PV to load,β :PV to battery,γ : SC to load,ζ :FC to load.
** Percentage value with respect to respective load bus voltage.

well as fully isolated/partially isolated multiport converter-based systems, it uses fewer switches, magnetic cores and power conversion stages. A detailed small signal model and control strategy is developed to achieve tight regulation of dc-bus voltages ($< 5\%$ overshoot/undershoot). The experimental results verify that the proposed topology can effectively allocates power share among diverse RESs and energy storage devices, irrespective of the specific energy management framework in place. In addition, the developed control scheme has the capability to override energy management commands when necessary, ensuring tight regulation of the load bus voltage and balance in power distribution within the system, even under substantial load variations, such as $> 50\%$ of rated load. Therefore, this topology is particularly suitable for dc microgrid-based commercial buildings application, where a 380 V load bus is prevalent, and there is a wide range of source and storage voltages to manage. However the proposed topology does come with certain limitations. 1) The wide variation in PV array voltage increases rms current through transformer windings and switches due to the voltage mismatch in A-TAB. This increases conduction losses. 2) Higher number of magnetic cores increases core losses and reduces power density. 3) Low light-load efficiency due to multiphase converter structure. Therefore, the future work includes: 1) Topological decoupling between PV array and series connected dc-link capacitor of subconverters 1 and 3 without adding significant power conversion stages; 2) realization of integrated magnetic structure to reduce core size and core loss; and 3) inclusion of phase shedding strategy to improve light load efficiency.

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APPENDIX

The coefficient terms of (72) are as follows:

$$\underbrace{\zeta_s = \zeta_{1_{\text{aug}}}(2D_4 - 1) + (\zeta_{2_{\text{aug}}} + \zeta_{4_{\text{aug}}})(1 - D_4)}_{\zeta = \mathbf{A},\mathbf{K},\mathbf{Q}}$$

$$\mathbf{G} = (2\mathbf{A}_{1_{\text{aug}}} - \mathbf{A}_{2_{\text{aug}}} - \mathbf{A}_{4_{\text{aug}}})\boldsymbol{X} + (2\mathbf{K}_{1_{\text{aug}}} - \mathbf{K}_{2_{\text{aug}}} - \mathbf{K}_{4_{\text{aug}}})V_{\text{sc}}$$

$$\boldsymbol{X} = -\mathbf{A_s}^{-1}(\mathbf{K_s}V_{\text{sc}} + \mathbf{M}I_z). \tag{76}$$

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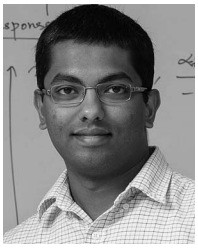

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