Identification of Phase Shift Variables to Match Multiobjective Optimization Strategy for EPS Modulated Dual Active Bridge DC–DC Converter

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***Abstract*—The modulation techniques of dual active bridge dc–dc converter with higher degrees of freedom give opportunities for optimization. This article investigates the effect of three existing optimization strategies that aim at minimizing current stress, backflow power, and reactive power delivered by the leading H-bridge terminal of the converter. The study leads to proposing a novel optimization strategy to simultaneously achieve multiple objectives, while ensuring reduced complexity in the control algorithm. The proposed strategy aims to minimize the reactive power seen by the equivalent leakage inductance of the high-frequency transformer, which is the difference in reactive power delivered by the leading and lagging H-bridge terminals of the converter. The steady-state performance of the converter is improved by attaining zero voltage switching for all the switches in a wider power range with reduced backflow power and current stress. Experimental results are presented to validate the theoretical analysis and effectiveness of the proposed optimization strategy.**

***Index Terms*—Backflow power, current stress, dual active bridge converter (DABC), extended phase shift (EPS) modulation, optimization, reactive power, zero voltage switching (ZVS).**

I. Introduction

RECENT advancements in power electronic technologies led to extensive inclusion of dc–dc converters in energy storage systems, electric vehicle applications, microgrids, more electric aircraft etc. The dual active bridge dc–dc converter (DABC) proposed in [1] has evolved as a potential choice among isolated bidirectional dc–dc converters due to its extendable soft-switching range, high-frequency operation and symmetric structure. The achievement of zero voltage switching (ZVS) without any additional components makes it appropriate in applications that demand high efficiency and high power density [2], [3].

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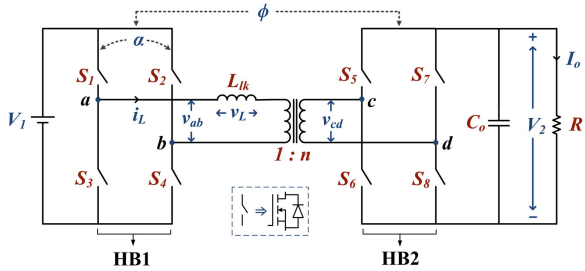

Fig. 1. Circuit diagram of DAB converter.

Moreover, the galvanic isolation and bidirectional power transfer capability enable the converter to be efficiently interfaced with battery packs and supercapacitors [4], [5]. The typical structure of a DABC, which is depicted in Fig. 1, consists of a primary H-bridge (HB1) and a secondary H-bridge (HB2) interconnected through a high-frequency transformer (HFT) with turns ratio, n. The equivalent leakage inductance of HFT (L_{lk}) acts as the energy transfer element. The power flow in DABC is controlled by the phase shift delay between the alternating voltages at H-bridge terminals (ab and cd) which is attained using different modulation techniques.

Conventionally, single phase shift (SPS) modulation employs an external phase shift delay (ϕ) between the H-bridge voltages to control the output voltage and power flow in the circuit. With a single degree of freedom, SPS is simple and easy to implement. However, if the input–output voltage gain value (V_2/V_1) deviates from the turns ratio, the converter would be prone to lose ZVS. In addition, there is limited control over current stress, backflow power and conduction losses with this technique. The control flexibility can be improved by providing an internal phase shift delay (α) between the legs of either one H-bridge or both the H-bridges along with the external phase shift delay. Consequently, advanced modulation techniques, such as extended phase shift (EPS) [6], dual phase shift (DPS) [7] and triple phase shift (TPS) [8] controls with higher degrees of freedom were introduced. In these techniques, multiple combinations of α and ϕ deliver the same power at the same voltage levels as that in SPS. Hence, the selection of appropriate control variables

can be based on a specific optimization strategy aiming at the minimization of reactive power, backflow power, current stress or the RMS value of HFT current.

The literature has reported several optimization algorithms using EPS [9], [10], [11], [12], [13], DPS [7], [14] and TPS [15], [16], [17], [18], [19], [20], [21], [22], [23], [24]. The proposed methods in [14], [15], and [16] optimize the current stress, while the RMS current of HFT is minimized in [17]. The optimization methods aiming at reducing the backflow power are presented in [7], [18], and [19]. All these methods are single-objective optimization schemes, hence, their shortcomings can be compensated by addressing multiple objective optimization schemes. The approaches proposed in [9] and [10] reduce the backflow power, while ensuring a minimized peak HFT current. However, the efficiency of the converter remains low if soft switching is not ensured for all switches. In [11], [12], [20], and [21] the proposed schemes aim at achieving ZVS and extending its range in addition to minimizing the RMS current of HFT. Optimization algorithms based on asymmetric duty modulation that minimizes the peak current along with improving soft switching are presented in [25] and [26]. Although the degree of freedom increases with such modulation scheme, time domain analysis is adopted for formulating the optimization function, making it dependent on voltage conversion ratio and mode of operation. In DABC, the conditions for achieving ZVS turn-ON and minimizing backflow power contradict each other. A negative HFT current at the switching instant is required to ensure soft-switching, whereas the backflow power increases with the magnitude of this negative HFT current. This dilemma has been addressed in [13] and [22], and optimal methods to achieve ZVS with minimum backflow power have been developed. A few literature consider the backflow power as an analogous parameter of the reactive power [7], [18], [27]. Despite being a dc–dc converter, a reactive power flow exists in DAB due to the high-frequency ac link, where alternating H-bridge voltage interacts with HFT current. The optimization method that aims at minimization of reactive power and achievement of ZVS is presented in [23], [24], and [28]. These works consider the reactive power delivered by the leading H-bridge terminals for optimization.

All the works mentioned above propose various algorithms for implementing the intended optimization strategy. The current literature lacks a horizontal analysis of the response of DABC toward different optimization strategies. This gap in the existing literature motivates a focused comparative study on the effect of various optimization strategies, specifically, minimization of current stress, backflow power and reactive power on the converter parameters, employing EPS modulation technique. Moreover, this study leads to the necessity of a new optimization strategy by which multiple objectives are realized. Hence, this article proposes a strategy that improves the performance of DABC by minimizing the reactive power seen by the leakage inductance of HFT. The proposed strategy consequently reduces the backflow power, attains zero voltage switching and reduces the current stress of the circuit.

The rest of this article is organized as follows. Section II briefly covers two operating modes of EPS modulation, while Section III elaborates on the existing optimization strategies using this modulation scheme. The proposed optimization strategy is discussed in Section IV, followed by a comparative study with the existing optimization schemes. Section V provides the experimental validation and analysis of the results obtained. Finally, Section VI concludes this article.

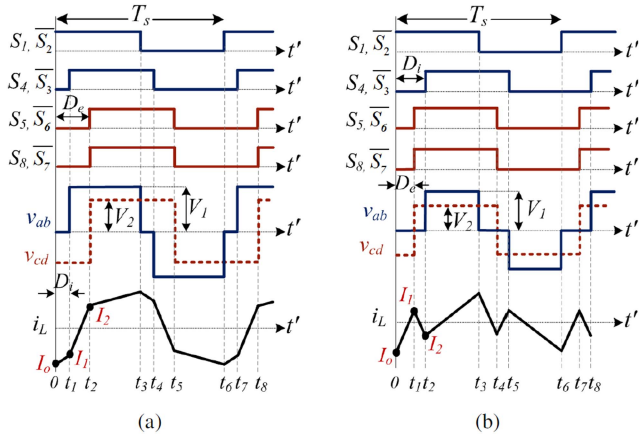

Fig. 2. (a) Mode 1 ($0 < D_i < D_e < 1$) and (b) Mode 2 ($0 < D_e < D_i < 2D_e$) of EPS modulation ($t' = 2t/T_s$).

II. Operating Modes of EPS Modulation

Among the advanced modulation techniques of DABC that use multiple control variables, the EPS modulation technique, which is initially presented in [29] grabs wider attention of researchers. In EPS modulation, apart from the external phase shift angle ϕ, either HB1 or HB2 is given an internal phase shift α, making one among the H-bridge terminal voltages (v_{ab} or v_{cd}) a three-level waveform and the other a two-level waveform.

As illustrated in Fig. 2, two modes of operation are feasible in EPS modulation according to the position of the rising edge of the switching pulses. Considering the switching pulse of S_1 as the reference, the switching pulse of S_5 lags behind S_4 in mode 1, while the switching pulse of S_5 leads S_4 in mode 2. The two modes are mathematically described as $0 < D_i < D_e < 1$ for mode 1 and $0 < D_e < D_i < 2D_e$ for mode 2. Here, the phase shift angles ϕ and α are represented in terms of phase shift ratio D_e and D_i, respectively, where $D_e = \phi/\pi$ and $D_i = \alpha/\pi$. T_s represents the switching period.

The expressions for HFT current (i_L) for mode 1 at the switching instants $t = 0$, t_1 and t_2 are given in (1) [30]. As the HFT current possesses half-wave symmetry in the steady state, the expressions of I_0, I_1 and I_2 (as indicated in Fig. 2) are sufficient for the analysis

$$I_0 = -\frac{V_2}{4nf_sL_{lk}}[k - 1 + 2D_e - kD_i]$$
$$I_1 = -\frac{V_2}{4nf_sL_{lk}}[k - 1 + 2D_e - kD_i - 2D_i]$$
$$I_2 = \frac{V_2}{4nf_sL_{lk}}[1 - k - kD_i + 2kD_e]. \quad (1)$$

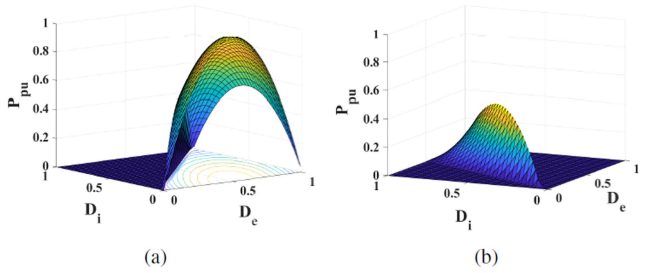

Fig. 3. Variation of power flow in (a) Mode 1 and (b) Mode 2.

TABLE I
IDEAL CONDITIONS FOR ACHIEVING ZVS TURN-ON

	Mode 1	Mode 2
S_1 and S_2	$I_0 < 0$	$I_0 < 0$
S_3 and S_4	$I_1 < 0$	$I_2 < 0$
S_5 – S_8	$I_2 > 0$	$I_1 > 0$

Here, k is the voltage conversion ratio defined as $k = \frac{nV_1}{V_2}$, where V_1 and V_2 are amplitudes of voltage waveforms of V_{ab} and V_{cd}, respectively, and f_s is the switching frequency. Then, the transferred power in mode 1 is formulated as

$$P = \frac{V_1 V_2}{2nf_s L_{lk}} \left[D_e(1 - D_e) + \frac{D_i}{2}(2D_e - D_i - 1) \right]. \quad (2)$$

Similarly, the HFT current at the switching instants $t = 0$, t_1 and t_2 for mode 2 are expressed as (3)

$$I_0 = -\frac{V_2}{4nf_s L_{lk}}[k - 1 - kD_i + 2D_e]$$
$$I_1 = -\frac{V_2}{4nf_s L_{lk}}[k - 1 - kD_i]$$
$$I_2 = -\frac{V_2}{4nf_s L_{lk}}[k - 1 - kD_i - 2D_e + 2D_i]. \quad (3)$$

The expression for transferred power in mode 2 is derived as

$$P = \frac{V_1 V_2}{2nf_s L_{lk}} \left[\frac{(1 - D_i)(2D_e - D_i)}{2} \right] \quad (4)$$

where the constraint $D_e > D_i/2$ is to be satisfied for the forward flow of power.

Considering the maximum power that can be achieved using SPS modulation as the base value, the transferred power, P can be normalized as $P_{pu} = P/P_{\max}$, where $P_{\max} = nV_1V_2/(8f_sL_{lk})$ [30]. The 3-D curves of normalized power for two modes are shown separately in Fig. 3. It is inferred that although the operation of mode 1 spans throughout the power range, it is predominantly realized in medium to higher power levels. In contrast, mode 2 is realized only in medium to lower power levels.

The criteria for achieving soft switching vary for each mode. The ideal conditions for attaining ZVS turn-ON for the switches in HB1 and HB2 in each mode are given in Table I [30].

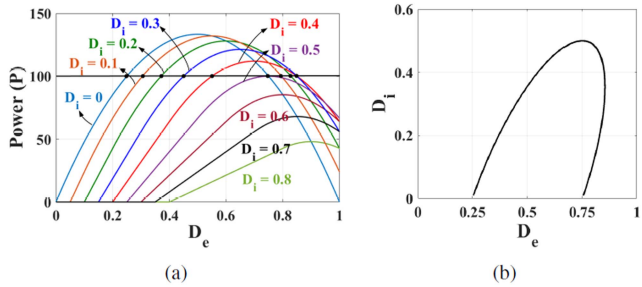

Fig. 4. (a) Variation in power transfer with D_e for different values of D_i, and (b) variation in D_i and D_e for a specific power transfer.

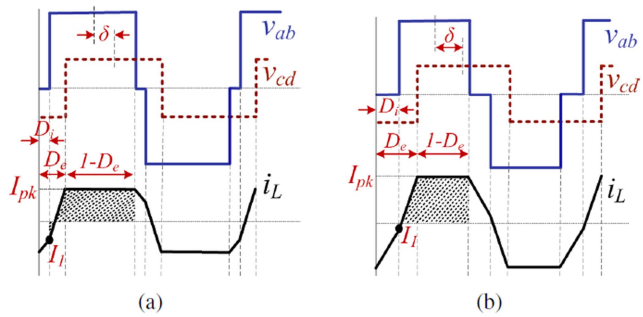

Fig. 5. Effect of change in D_i: (a) lower D_i and (b) higher D_i.

III. OPTIMIZATION STRATEGIES AND COMPARISON

A. Scope of Optimization

The power curve shown in Fig. 3 depicts a many-to-one mapping of D_e and D_i to P for two modes of operation. A detailed illustration of power variation for different values of D_e and D_i is given in Fig. 4(a). With two degrees of freedom, multiple combinations of D_e and D_i deliver the desired power (e.g., $P = 100$ W) in EPS modulation. Fig. 4(b) gives the variation of D_i with respect to D_e for delivering this power. Out of numerous combinations of D_e and D_i, the choice of appropriate phase shift variables can be made to achieve an optimization goal. The effect of different ranges of phase shift variables can be comprehensively explained using Fig. 5, in which both the steady-state waveforms deliver equal power (the hatched area represents the forward power). While delivering a fixed output power, when D_i is increased, D_e also increases as inferred from Fig. 4. As represented in Fig. 5(a), the zero voltage duration of v_{ab} is less for low D_i. Although this results in backflow power, the switching instant current I_1 will be sufficiently high to ensure soft switching. As D_i is increased, the magnitude of I_1 reduces and the switch tends to lose ZVS turn-ON. Moreover, a shrinkage of the interval $1 - D_e$ raises the peak of i_L to maintain the forward power. Hence, even though an increase in D_i results in reduced backflow power, it leads to a higher peak current and loss of soft-switching capability. In EPS modulation, determining an appropriate value of D_i remains a primary research focus.

B. Existing Optimization Strategies

This section presents three optimization strategies reported in the literature - optimization of current stress, backflow power and

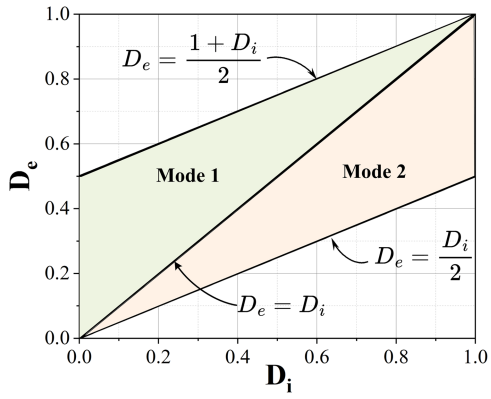

Fig. 6. Range of D_e and D_i in Mode 1 and Mode 2.

reactive power, hereafter indicated as *Minimum* I_{pk}, *Minimum* P_b, and *Minimum* Q_s, respectively. The conditions adopted for the analysis include the range of D_e and D_i that is determined based on (a) the mode of operation and (b) the phase angle between the fundamental components of v_{ab} and v_{cd}. This phase angle is expressed as

$$\delta = \pi \left[D_e - \frac{D_i}{2} \right]. \tag{5}$$

Fig. 6 represents the range of phase shift variables of each mode, with boundary conditions as mentioned in the previous section. To ensure a monotonic relation with P, the angle δ is limited to 90°, introducing an additional constraint $D_e < (1 + D_i)/2$. This eliminates the negative-slope region of the power curve given in Fig. 4(a); hence, the variation in Fig. 4(b) will become unidirectional. As stated previously, different combinations of phase shift variables D_e and D_i deliver a constant power. The values of various parameters of the converter, such as peak current (I_{pk}), backflow power (P_b), reactive power (Q_s) and the number of switches attaining ZVS (N_{zvs}) corresponding to each possible combination of phase shift variables are plotted in Fig. 7 for $k = 1$ and $P = 80$ W.

1) Minimization of Backflow Power (Minimum P_b): The optimization strategy, *Minimum* P_b refers to minimizing the backflow power either by minimizing the area of the backward flow of energy [13] or by reducing the magnitude of the switching instant current that contributes to negative power flow [22] [e.g., I_1 in Fig. 2(a) and I_2 in Fig. 2(b)]. The backflow power obtained corresponding to each possible combination of D_e and D_i is indicated in Fig. 7(b). The phase shift variables that give $P_b = 0$ can be chosen as optimal phase shift variables D_{i_opt} and D_{e_opt}. Since many combinations of D_e and D_i deliver zero backflow power, an auxiliary criterion, such as minimum peak current consideration is required for the appropriate selection of these variables. Also, Fig. 7(a) conveys that whenever $P_b = 0$, ZVS is lost for two switches as the conditions in Table I are not satisfied. Switches S_3 and S_4 always lose ZVS turn-ON with *Minimum* P_b.

2) Minimization of Current Stress (Minimum I_{pk}): Current stress refers to the peak value of HFT current in DABC. The largest among the three switching instant currents $(I_0, I_1, I_2$ as indicated in Fig. 2) is decided by the voltage conversion ratio $(k = \frac{nV_1}{V_2})$ and the mode of operation. The optimization strategy *Minimum* I_{pk} aims to optimize the peak value of i_L. As inferred from Fig. 7(d), the D_{i_opt} and D_{e_opt} for *Minimum* I_{pk} can ensure ZVS turn-ON for all the switches. However, the expression of I_{pk} differs depending on the voltage conversion ratio and the mode of operation, as given in Table II. To apply the optimization strategy in the entire power range, the identification of modes and k is necessary. Depending on the modes and k values, the objective function for optimization has to be updated each time. This complicates the control algorithm in *Minimum* I_{pk}. The algorithmic flowchart representing the implementation procedures for *Minimum* I_{pk} is depicted in Fig. 8.

TABLE II
EXPRESSION FOR PEAK CURRENT

k	Mode	I_{pk}
$k > 1$	1	$I_0 = -\frac{V_2}{4nf_sL_{lk}}[k - 1 + 2D_e - kD_i]$
	2	$I_0 = -\frac{V_2}{4nf_sL_{lk}}[k - 1 + 2D_e - kD_i]$ for $\lvert k - 1 + 2D_e - kD_i\rvert > \lvert k - 1 - kD_i\rvert$
		$I_1 = -\frac{V_2}{4nf_sL_{lk}}[k - 1 - kD_i]$ for $\lvert k - 1 - kD_i\rvert > \lvert k - 1 + 2D_e - kD_i\rvert$
$k < 1$	1	$I_2 = \frac{V_2}{4nf_sL_{lk}}[1 - k - kD_i + 2kD_e]$
	2	$I_1 = -\frac{V_2}{4nf_sL_{lk}}[k - 1 - kD_i]$

3) Minimization of Reactive Power (Minimum Q_s): The power flow in DABC is analogous to the power flow between two voltage buses in a transmission line of the power system. Hence, reactive power evolves due to the interaction of HFT current and H-bridge terminal voltages. The Fourier series representation of v_{ab} and v_{cd} including all odd harmonic components are given as

$$v_{ab}(t) = \sum_{h=1,3,5}^{\infty} \frac{4V_1}{h\pi} \cos\left(\frac{h\alpha}{2}\right) \sin(h\omega t) \tag{6}$$

$$v_{cd}(t) = \sum_{h=1,3,5}^{\infty} \frac{4V_2}{h\pi} \sin h(\omega t - \delta) \tag{7}$$

where $\alpha = \pi D_i$ and $\omega = 2\pi f_s$. The reactive power generated at the sending end of the power system is equivalent to that generated at the leading H-bridge of DABC (i.e., HB1). It is obtained by

$$Q_s = \frac{V_{1f}\left(V_{1f} - \frac{V_{2f}}{n}\cos\delta\right)}{\omega L_{lk}}. \tag{8}$$

Here, V_{1f} and V_{2f} are RMS values of fundamental components of v_{ab} and v_{cd}, respectively. From (6) and (7),

$$V_{1f} = \frac{2\sqrt{2}V_1}{\pi}\cos\left(\frac{\alpha}{2}\right);\ V_{2f} = \frac{2\sqrt{2}V_2}{\pi}. \tag{9}$$

Considering the fundamental harmonics alone, Q_s with EPS modulation takes the form

$$Q_s = \frac{8V_1}{\pi^2 L_{lk}\omega}\cos\left(\frac{\alpha}{2}\right)\left[V_1\cos\left(\frac{\alpha}{2}\right) - \frac{V_2\cos\delta}{n}\right]. \tag{10}$$

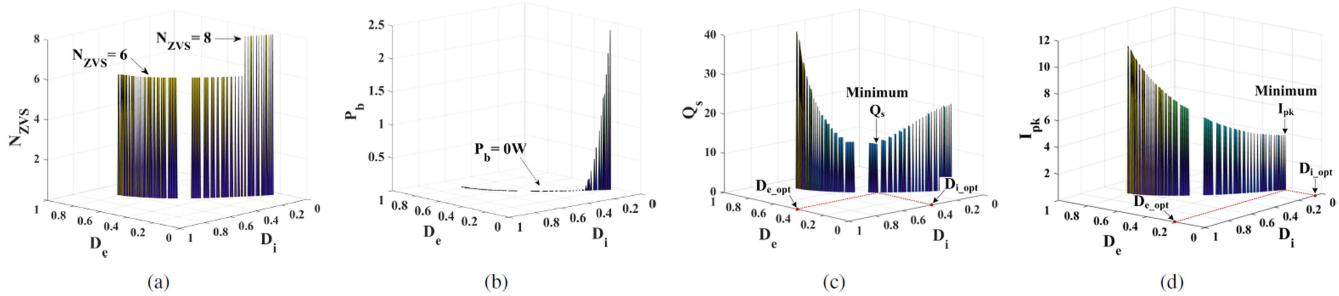

Fig. 7. Values of various parameters of DABC obtained corresponding to each possible combination of D_e and D_i (a) N_{zvs}, (b) P_b, (c) Q_s and (d) I_{pk}.

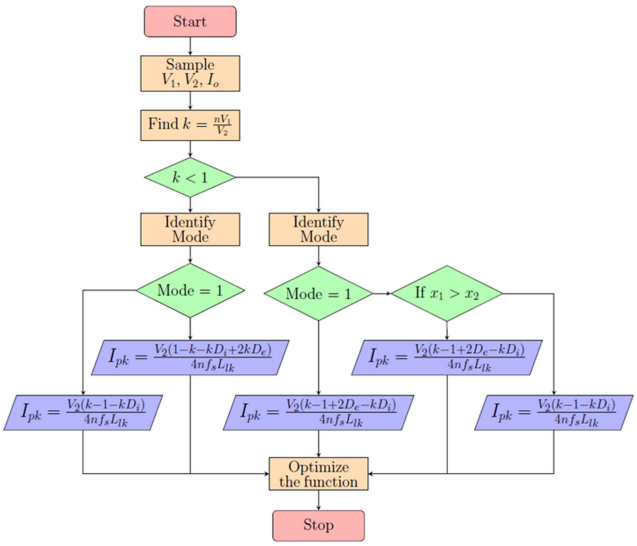

Fig. 8. Typical flowchart for *Minimum* I_{pk} strategy; ($x_1 = k - 1 + 2D_e - kD_i$ and $x_2 = k - 1 - kD_i$).

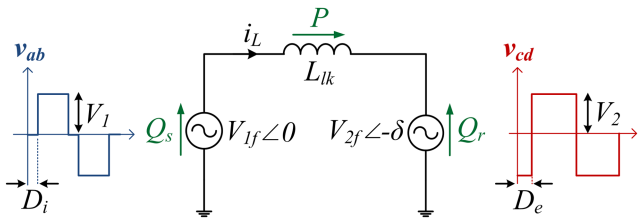

Fig. 9. Power system equivalent of DABC.

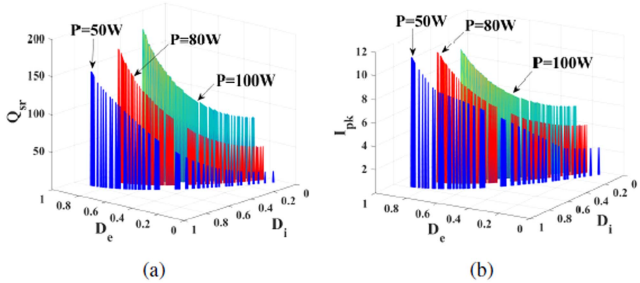

Fig. 10. Possible values of (a) Q_{sr} and (b) I_{pk} for different power levels.

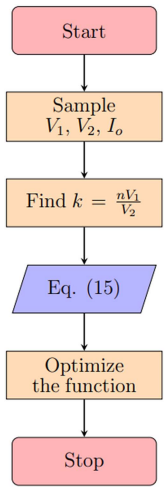

Fig. 11. Typical flowchart for *Minimum* Q_{sr} strategy.

The optimization strategy *Minimum* Q_s refers to minimizing this reactive power. With fundamental harmonic approach-based modeling, the expression for Q_s is unique for both modes, and the complexity in implementation is reduced. Fig. 7(c) shows the reactive power corresponding to each possible combination of D_e and D_i. The optimum values D_{i_opt} and D_{e_opt} that provide minimum Q_s fall in the region where $N_{ZVS} = 6$. Higher value of D_{i_opt} leads to the loss of ZVS turn-ON for two switches, as explained in Section III-A A. From [31], minimization of (8) using the Lagrange multiplier method with a desired output power as the constraint gives the relation between phase shift variables as

$$\delta = \cos^{-1}\left(\frac{V_2}{2nV_1\cos\left(\frac{\alpha}{2}\right)}\right). \tag{11}$$

The effectiveness of *Minimum* Q_s based on (11) is inspected toward the end of the next section.

IV. Proposed Optimization Strategy

The comparative study of the three existing schemes led to the necessity of a more effective and easily implementable optimization strategy to improve the performance of the converter. This section presents a novel optimization strategy that aims to minimize the reactive power seen by the leakage inductance of HFT.

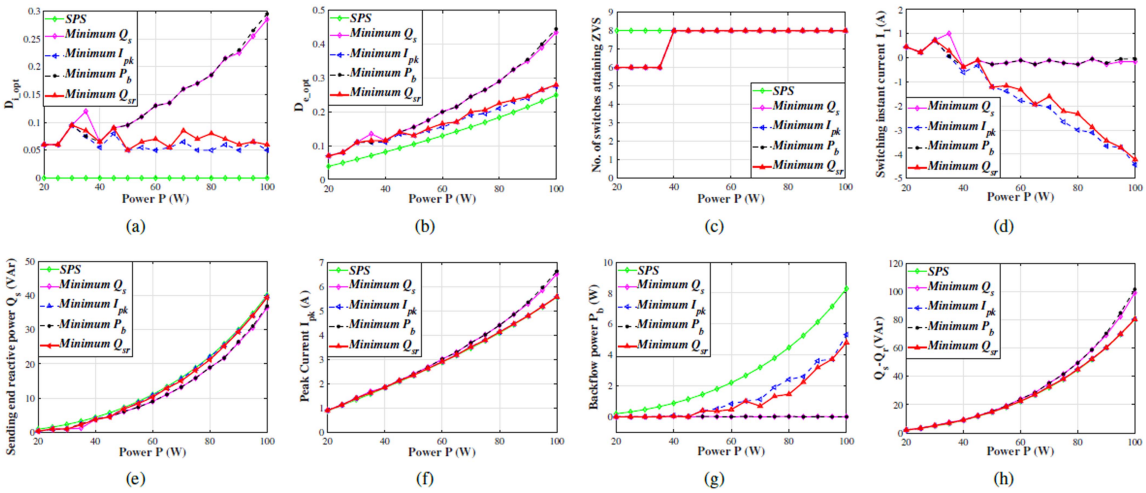

Fig. 12. Variations in (a) optimal D_i, (b) optimal D_e, (c) no. of switches attaining ZVS, (d) switching instant current I_1, (e) sending end reactive power (Q_s), (f) peak current (I_{pk}), (g) backflow power (P_b) and (h) Q_s-Q_r across power levels for different optimization strategies.

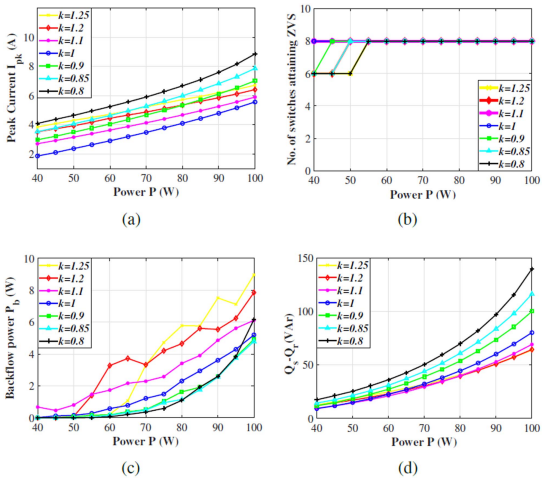

Fig. 13. Variations in (a) peak current (I_{pk}), (b) number of switching attaining ZVS, (c) backflow power (P_b) and (d) Q_s-Q_r for different values k.

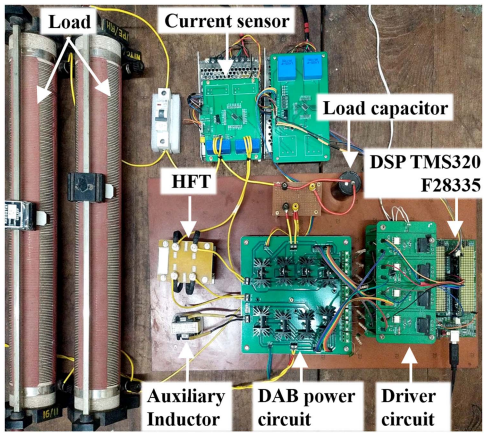

Fig. 14. Experimental set-up of DABC.

A. *Proposed Optimization Strategy (Minimum Q_{sr})*

The power flow between two voltage buses through a transmission line in the power system forms the fundamental operating principle of a DABC, as depicted in Fig. 9. The phase difference of two voltage buses influences the magnitude and direction of power flow between them. These sinusoidal bus voltages are analogous to pulse width modulated H-bridge voltages, v_{ab} and v_{cd} of DABC. With v_{ab} and v_{cd}, the active power transferred from source to load is formulated as

$$P = \frac{V_{1f}V_{2f}\sin\delta}{n\omega L_{lk}} = \frac{8V_1V_2}{n\pi^2\omega L_{lk}}\cos\left(\frac{\alpha}{2}\right)\sin\delta. \tag{12}$$

The reactive power represented as Q_s in Fig. 9 is generated at the sending end of DABC and is expressed in (8). On the other hand, the reactive power generated at the receiving end or that generated at the lagging H-bridge (HB2) can be formulated as

$$Q_r = \frac{V_{2f}\left(V_{1f}\cos\delta - \frac{V_{2f}}{n}\right)}{n\omega L_{lk}}. \tag{13}$$

Substituting V_{1f} and V_{2f} from (9), (13) becomes

$$Q_r = \frac{8V_2}{\pi^2 L_{lk}\omega}\left[V_1\cos\left(\frac{\alpha}{2}\right)\cos\delta - \frac{V_2}{n}\right]. \tag{14}$$

The proposed optimization strategy considers the reactive power seen by L_{lk} (Q_{sr}), which is obtained by solving the difference between Q_s and Q_r (i.e., $Q_{sr} = Q_s - Q_r$). Thus, from (8) and (14), the proposed optimization index is expressed as (15), and the strategy is called *Minimum Q_{sr}*

$$Q_{sr} = \frac{8}{\pi^2 L_{lk}\omega}\left[V_1^2\cos^2\left(\frac{\alpha}{2}\right) + \frac{V_2^2}{n^2} - \frac{2V_1V_2}{n}\cos\delta\cos\left(\frac{\alpha}{2}\right)\right]. \tag{15}$$

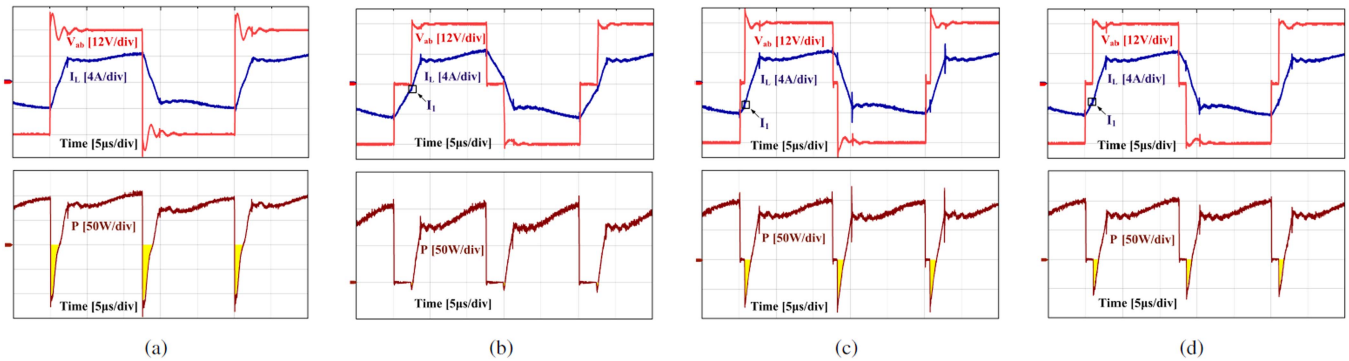

Fig. 15. Steady state waveforms of output voltage of HB1 v_{ab}, HFT current i_L and power P using (a) SPS modulation and optimization strategies (b) *Minimum* Q_s, (c) *Minimum* I_{pk}, and (d) *Minimum* Q_{sr} for $k = 1$ and $P = 80$ W.

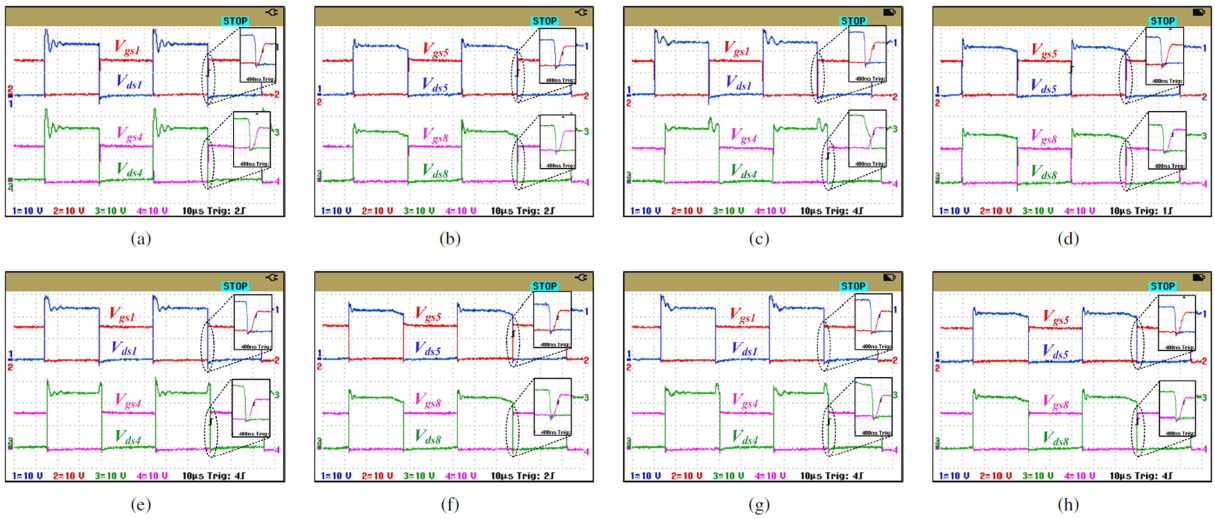

Fig. 16. Waveforms of gate-source voltage V_{gs}, drain-source voltage V_{ds} of all switches (a)–(b) with SPS modulation, (c)–(d) with *Minimum* Q_s, (e)–(f) with *Minimum* I_{pk} and (g)–(h) with *Minimum* Q_{sr} for $k = 1$ and $P = 80$ W. (a), (c), (e), (g) represent S_1 and S_4, and (b), (d), (f), (h) represent S_5 and S_8.

Fig. 17. Power loss components (in Watts) for output power of 80 W.

Fig. 18. Steady state waveforms of HFT current i_L, V_{ds} and V_{gs} with the proposed optimization strategy for (a) $k = 0.9$ and (b) $k = 1.1$.

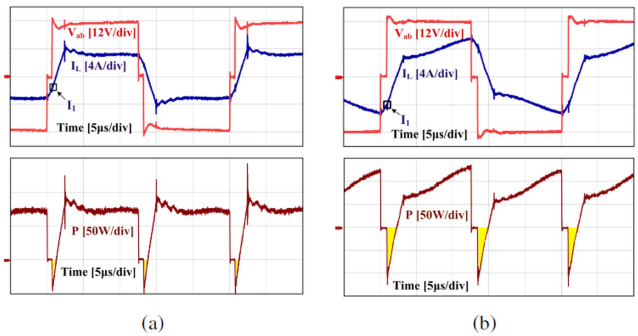

Fig. 19. Steady state waveforms of v_{ab}, HFT current i_L and power P with the proposed optimization strategy for (a) $k = 0.9$ and (b) $k = 1.1$.

Minimization of the proposed parameter Q_{sr}, while ensuring the flow of desired active power P can be achieved by employing the Lagrange multiplier method (LMM). The Lagrange optimization function is formulated as

$$L(D_i, D_e) = Q_{sr}(D_i, D_e) - \lambda(P - P^*) \tag{16}$$

where λ is the Lagrangian multiplier and P^* is the reference power. The optimal values of D_i and D_e are obtained by solving the following condition

$$\nabla Q_{sr}(D_i, D_e) = \lambda \nabla (P - P^*). \tag{17}$$

Here, ∇ indicates the gradient operation. Hence, the relation between the phase shift variables is obtained as

$$\delta = \cos^{-1}\left(\frac{V_2}{nV_1 \cos\left(\frac{\alpha}{2}\right)}\right). \tag{18}$$

Substituting (5) and $\alpha = \pi D_i$ in (18), it becomes

$$D_e = \frac{1}{\pi}\cos^{-1}\left(\frac{V_2}{nV_1 \cos\left(\frac{\pi D_i}{2}\right)}\right) + \frac{D_i}{2}. \tag{19}$$

The values of Q_{sr} and I_{pk} corresponding to possible combinations of D_i and D_e that give different power levels are shown in Fig. 10. It is deduced that the region of minimum Q_{sr} aligns with the region of minimum I_{pk}. Therefore, the response of the converter that employs the proposed *Minimum* Q_{sr} strategy will be similar to that of *Minimum* I_{pk}. However, similar to the *Minimum* Q_s condition, since Q_{sr} is unique for both the modes and any voltage conversion ratio, the proposed strategy will also lack complexity in the control algorithm. Fig. 11 presents the algorithmic flowchart outlining the implementation procedure for *Minimum* Q_{sr}. A comparison with Fig. 8 demonstrates the reduced implementation complexity of the proposed approach relative to the *Minimum* I_{pk} strategy.

B. Analytical Comparison of Proposed Strategy With Existing Methods

The response to the existing and proposed optimization strategies for various power levels ranging from 20 to 100 W at $k = 1$ with input voltage 24 V is given in Fig. 12. The response with conventional SPS modulation is also compared as it is generally employed in the control logic when the voltage conversion ratio is unity. Fig. 12(a) and 12(b) indicate the optimal phase shift variables D_{i_opt} and D_{e_opt} for each optimization strategy. Since the variations in the proposed parameter Q_{sr} and I_{pk} are identical for different power levels, the optimal phase shift variables of the proposed strategy remain closer to that of *Minimum* I_{pk}. At the same time, Fig. 7(b) and 7(c) show that the values of P_b and Q_s corresponding to different combinations of D_i and D_e vary differently. However, the phase shift variables that deliver the minimum Q_s simultaneously ensure that the P_b is reduced to zero. Because, as mentioned in Section III A, the minimum value of P_b (i.e., $P_b = 0$) is obtained when D_i is higher. Hence, the optimal phase shift variables of *Minimum* Q_s and *Minimum* P_b will be relatively the same as indicated in Fig. 12(a), 12(b) and 12(g).

The soft switching capability of *Minimum* Q_s strategy is examined using Fig. 12(c) and 12(d). The former indicates that, with the optimal values of D_i and D_e, all switches achieve ZVS turn-ON at medium to high power levels. However, the switching instant current I_1 is insufficient to discharge the parasitic capacitance across switches S_3 and S_4 [13]. Consequently, achieving complete ZVS turn-ON becomes practically challenging, while applying the *Minimum* Q_{sr} strategy.

Alternatively, as illustrated in Fig. 10(a), the minimum value of Q_{sr} is obtained for lower values of D_i. Fig. 12(d) confirms that this ensures a sufficiently large magnitude of I_1 to facilitate soft switching. Therefore, complete ZVS turn-ON is achieved using the proposed *Minimum* Q_{sr} strategy at medium to high power levels. Moreover, an appropriate choice of D_i significantly reduces P_b compared to SPS modulation, which is inferred from Fig. 12(g). The effect of these optimization strategies on peak current can be validated using Fig. 12(f). The proposed strategy ensures a minimized I_{pk} compared with *Minimum* Q_s strategy.

These responses can also be explained by the relation between optimal phase shift variables obtained using LMM. Let α_s and α_{sr} be the optimal inner phase shift angles corresponding to the minimization of Q_s and Q_{sr}, respectively. From (11), α_s is formulated as

$$\alpha_s = 2\cos^{-1}\left(\frac{V_2}{2nV_1 \cos\delta}\right). \tag{20}$$

The inner phase shift angle with the proposed strategy derived from (18) is expressed as

$$\alpha_{sr} = 2\cos^{-1}\left(\frac{V_2}{nV_1 \cos\delta}\right). \tag{21}$$

From (20) and (21), it is identified that for same δ, α_s is greater than α_{sr} ($\alpha_s > \alpha_{sr}$). This emphasizes the advantages of the proposed strategy over *Minimum* Q_s on the grounds of the inferences made from Fig. 5.

C. Performance Evaluation With Nonunity k

The performance of the proposed control strategy has been evaluated through the response of DABC parameters for different values of k. The effect on P_b, I_{pk}, number of switches attaining ZVS and Q_{sr} when k is varied between 0.8 and 1.25 for the output power ranging from 40 to 100 W are recorded in Fig. 13. In DABC, the peak current of HFT is the minimum when the k is unity, and it increases as k deviates from this optimal point, as shown in Fig. 13(a). The proposed control strategy effectively generates lower values of D_i, enabling ZVS turn-ON in maximum number of switches. This is further supported by Fig. 13(b), which confirms that all switches conserve soft switching capability from half-load to full-load conditions across varying values of k. In addition, although backflow power increases with k, the proposed control strategy effectively limits the maximum P_b to just 9% of the rated power, as depicted in Fig. 13(c).

V. Experimental Results and Discussions

To validate the effectiveness of the proposed optimization scheme, an experimental prototype of DABC is set up, as shown in Fig. 14. The digital control board TMS320F28335 is used to generate the switching pulse for MOSFET IRFP250 N. Table III includes the converter parameters. Experimental validation for

TABLE III
CONVERTER PARAMETERS

Converter Specifications	Symbol	Value
Input voltage	V_i	24 V
Output voltage	V_o	24 V
Rated output power	P	100 W
Switching frequency	f_s	20 kHz
Transformation ratio of HFT	n	1
Leakage Inductance	L_{lk}	27 μH

TABLE IV
COMPARISON OF OPTIMIZATION STRATEGIES

	D_{i_opt}	D_{e_opt}	Pb (W)	I_{pk} (A)	N_{ZVS}	Complexity
SPS	0	0.183	2.012	4.08	8	Low
Min. Q_s	0.185	0.29	0.065	4.2	6	Medium
Min. I_{pk}	0.05	0.21	1.422	3.9	8	High
Min. Q_{sr}	0.08	0.225	0.875	4.08	8	Medium

the analysis given in Fig. 12 for power $P = 80$ W is provided in this section. Since the optimization strategies *Minimum* Q_s and *Minimum* P_b generate the same optimal values of D_e and D_i, the experimental results of the former alone are included. Table IV has the optimal values of D_i and D_e using each scheme.

The steady-state waveforms of v_{ab}, i_L and instantaneous power (P) for delivering 80 W at $k = 1$ employing SPS modulation and the aforementioned optimization strategies are shown in Fig. 15. The area in the power waveform that contributes to the backward flow of power (P_b) is highlighted in yellow. The achievement of ZVS using the optimization strategies is validated by analyzing the waveforms of gate-source voltage V_{gs} and drain-source voltage V_{ds} of one switch in each leg of both the H-bridges. A switch loses ZVS turn-ON capability when V_{gs} and V_{ds} overlap, indicating nonzero power consumption at the switching instant. These observations are consolidated in Table IV.

Unity voltage conversion ratio $(k = 1)$ made all switches achieve soft switching in SPS modulation. However, as verified by Fig. 15(a), since the SPS modulation lacks a zero-voltage period in v_{ab}, a considerably high backflow power is incurred, leading to reduced efficiency. A reduction in backflow power is achieved by employing the EPS modulation optimization strategies, which introduce an inner phase delay in HB1. As denoted in (20) and (21) in the previous section, D_{i_opt} $(= \alpha/\pi)$ for *Minimum* Q_s is larger than that for *Minimum* Q_{sr}. A higher D_{i_opt} leads to reduced backflow power but increases the peak value of HFT current (I_{pk}). Thus, Fig. 15(b) verifies the inferences obtained from Fig. 5. However, a higher D_{i_opt} affects the soft-switching capability of the switches. In *Minimum* Q_s, since the switching instant current I_1 is insufficient to discharge the parasitic capacitance across S_3 and S_4, the ZVS turn-ON is lost for these switches. The overlap of V_{gs4} and V_{ds4} in Fig. 16(c) validates the same. In contrast, a lower D_{i_opt} reduces I_{pk} and provides a sufficiently high switching instant current I_1. This facilitates the achievement of ZVS turn-ON in all 8 switches with *Minimum* I_{pk} and the proposed strategy *Minimum* Q_{sr}.

Different power loss components are calculated corresponding to each optimization strategy based on [32] and are illustrated in Fig. 17 for an output power of 80 W. It is deduced that the proposed strategy yields minimum losses, verifying the inferences obtained above. The soft switching capability of the proposed optimization strategy is checked for $k = 0.9$ and $k = 1.1$ at $P = 80$ W, representing a boost and buck operation, respectively, and are given in Fig. 18. Due to sufficient magnitude of switching instant current I_1, switches S_3 and S_4 attain ZVS turn-ON. The backflow power for each condition is shown in Fig. 19.

Based on the experimental findings, it can be concluded that the proposed optimization approach performs better than SPS modulation and *Minimum* Q_s in terms of reduced P_b and soft switching capabilities, respectively. It is also preferred over *Minimum* I_{pk} due to its ease of implementation.

VI. CONCLUSION

The existence of multiple combinations of phase shift variables for delivering a desired output power enables optimization of DABC parameters. This article presents a comparative study of three widely employed optimization strategies that minimize the peak current of HFT, backflow power and sending-end reactive power. Based on the analysis performed, the need for a more effective and easily implementable optimization strategy for the efficient operation of the converter is identified. Hence, an optimization strategy that minimizes the reactive power seen by the leakage inductance of HFT is proposed in this article. The optimal phase shift variables identified by the proposed strategy enhance the steady-state performance of the converter in terms of current stress, backflow power and soft switching, while ensuring easy implementation. The theoretical analysis provided in the article has been validated experimentally. The study indicates that due to a significant reduction in backflow power, the proposed optimization strategy is capable of replacing SPS control even when the voltage conversion ratio is moderately away from unity.

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