Enhancing Buck Converter Efficiency by Using GaN/Si Hybrid Switches to Suppress Dynamic ON-State Resistance

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***Abstract*—In this work, it is demonstrated that the buck converter using a GaN/Si hybrid switch can achieve an even higher power conversion efficiency than the one using a pure-GaN switch with the same ratings. By replacing one of the dual paralleled GaN HEMTs with a Si superjunction MOSFET having the same voltage rating yet a slightly higher resistance, the total conduction loss, however, is significantly decreased. This is accomplished through suppressing the dynamic ON-state resistance peculiar to GaN HEMTs. Optimizing the gate timing between the GaN and the Si devices within the hybrid switch enables exceptional low-loss performance. Both device-level and system-level demonstrations are performed. The experimental results prove that the p-GaN gate HEMT/Si MOSFET hybrid switch increases the efficiency by 2% and 3%, respectively, when compared to its pure-GaN and pure-Si counterparts, at an output power of 240 W and a switching frequency of 500 kHz.**

***Index Terms*—Dynamic resistance, efficiency, GaN, hybrid, turn ON.**

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I. Introduction

THE GaN power high electron mobility transistors (HEMTs) have emerged as an important branch in the power semiconductor market. The fast-switching speed and low specific ON-resistance make them an ideal choice for high-frequency and high-efficiency power conversion. However, these devices often encounter the issue of dynamic ON-state resistance degradation (also known as current collapse), which is mainly induced by the charge trapping effect [1], [2], [3], [4], [5], [6]. The charge trapping effect can be caused by surface traps as well as bulk traps in GaN buffer layers. During high-voltage OFF-state, hot electrons could be injected to the epitaxial surface, where they are trapped by surface states [7]. The vertically drifting electrons can be captured by the buffer traps [8]. The decharging time constant for both surface states and bulk traps is often longer than the device switching period. When the device turns ON again, the negatively charged surface traps and bulk traps can deplete the two-dimensional electron gas (2DEG), thereby reducing the 2DEG carrier concentration and increasing R_{ON}. Consequently, the GaN HEMT under high-frequency continuous switching exhibits a higher resistance than that during its static ON-state. The conduction losses in a GaN-based converters are actually much higher than those predicted based on specified R_{ON} in the datasheet (or curve tracer). At the device-level, technologies for suppressing dynamic R_{ON} can be categorized into two types. The first type aims at minimizing charge trapping effects at the device surface, including the field-plate optimization [9] and surface passivation technique [10]. These techniques are effective and have been applied in commercial GaN power devices. The second type aims at minimizing charge trapping effects in the GaN buffer layer [11], [12], which are caused by the deep-level defects. However, blocking several hundred or even higher volts between the drain and source often requires the intentional inclusion of deep-level defects (e.g., carbon) in the GaN buffer layer to suppress bulk leakage [13]. Consequently, there exists a tradeoff relationship between reducing leakage current and suppressing dynamic R_{ON} degradation. This explains the fact that dynamic R_{ON} degradation still exists in the state-of-the-art commercial GaN power HEMTs to various degrees. At the system-level, the degree of dynamic R_{ON} degradation is also influenced by

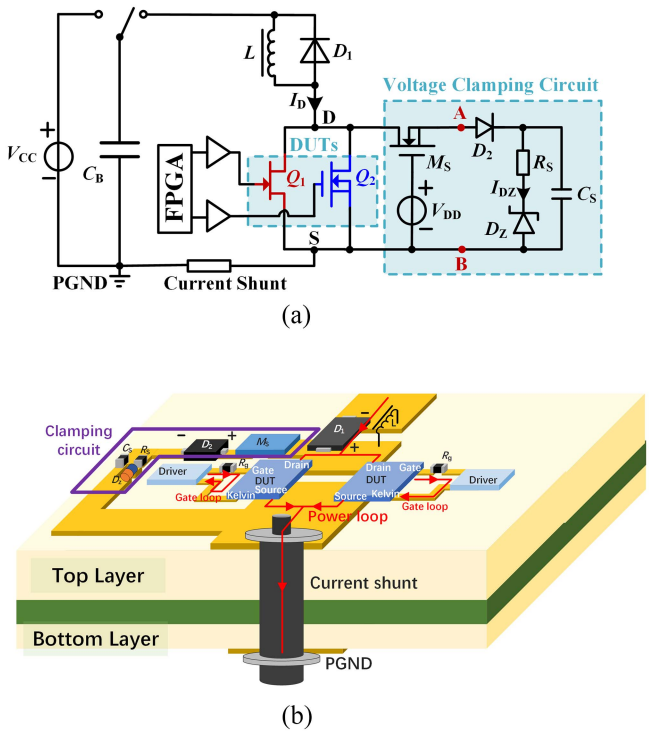


Fig. 1. Test setup for dynamic R_{ON} characterization. (a) Circuit diagram. (b) Top view of the PCB for power loop.

the switching conditions including load current [14], OFF-state gate/drain voltage [15], [16], [17], OFF-state stress time [18], switching frequency [19], gate resistor [20] and switching mode (i.e., hard-switching or soft-switching) [21]. Consequently, it becomes a highly intricate task to accurately estimate and minimize dynamic R_{ON} for GaN HEMTs.

The hybrid switch has been an attractive solution as it combines the advantages of different types of devices. In particular, the SiC MOSFET/Si IGBT hybrid switch [22], [23], [24], [25], [26], [27] inherits the merits of both Si IGBTs (large current handling capability and low cost) and SiC MOSFETs (low switching loss and high switching frequency), obtaining an increasing popularity in electric vehicle applications. Nevertheless, the GaN/Si hybrid switch received much less attention.

The GaN/Si hybrid switch often refers to a single switch formed by paralleled GaN and Si devices. This is quite different from the more frequently reported GaN/Si hybrid topology. The hybrid topology employs GaN devices as a subset of switches while using Si devices as the remaining switches, thereby enhancing the overall topology efficiency, such as a GaN/Si hybrid multilevel topology ANPC converter in [28] and a GaN/Si hybrid multilayer stacked architecture (MSC-PoL VRM) in work [29].

To date, a GaN HEMT/Si MOSFET hybrid switch was demonstrated in a zero-voltage switching application in work [30] and its transient analysis was presented in work [31]. However, there have been no reports regarding the hard-switching performance of the GaN HEMT/Si MOSFET hybrid switch. Hard-switching scenarios based on GaN devices are also relatively common in practical applications, such as point-of-load (POL) power supplies. The most prevalent topology in POL systems is the buck converter [32]. More importantly, the critical dynamic R_{ON} issue was never taken into consideration in previous investigations upon GaN/Si hybrid switches. More in-depth device-level characterizations are still necessary.

To sum up, the key advancements of this work are as follows.

1) It is demonstrated that a GaN/Si hybrid switch can achieve a higher efficiency than a pure-GaN switch in a buck converter, which was never revealed before.
2) The dynamic R_{ON} behaviors for GaN/Si hybrid switches are extensively investigated. The underlying mechanisms by which the hybrid switch suppresses the dynamic R_{ON} degradation are revealed.
3) GaN/Si hybrid switches configured with both p-GaN gate HEMTs and cascode GaN HEMTs are investigated. Previous studies have focused exclusively on hybrid switches configurated with p-GaN gate HEMTs, without involving cascode GaN HEMT configurations.
4) GaN/Si hybrid switches are implemented in hard-switching applications. Previous studies have been confined to the zero-voltage turn-on applications.

The rest of this article is organized as follows: Section II presents the test setup and design considerations for the dynamic R_{ON} characterization. Section III presents the performance of p-GaN gate HEMT/Si MOSFET hybrid switch. Section IV presents the performance of Cascode GaN HEMT/Si MOSFET hybrid switch. Section V concludes the whole work.

II. Test Setup and Design Considerations

Fig. 1(a) shows the circuit diagram for a double-pulse setup utilized in the measurement of dynamic R_{ON}. Q_1 and Q_2 are the devices under test (DUTs). Depending on the selection of device models, Q_1 and Q_2 can be configured to form a hybrid switch or a pure-GaN switch or a pure-Si switch. V_{CC} is the dc-link voltage. D_1 (IDW40G120C5B) provides a freewheeling path for the inductor current. The total drain current (I_D) of the DUTs is monitored using a 0.1 Ω coaxial shunt (SSDN-10). Fig. 1(b) shows the top view of the printed circuit board (PCB) for power loop. The coaxial shunt is positioned at the source side of the DUTs. The ON-state voltage of the DUTs can be precisely obtained by measuring V_{AB} thanks to the voltage clamping circuit [33].

The PCB for the clamping circuit module is shown in Fig. 2(a). D_Z is a Zener diode (ZM4733A, 5.1 V/1 W) used for stabilizing V_{AB} when the DUTs are at OFF-state. R_S limits the surge I_{DZ} [see Fig. 2(b)] and protect D_Z during turn-OFF transients. D_2 (RBR20BM30A) is a Schottky Diode used for isolation. C_S is used to reduce the voltage spikes for V_{AB} during turn-OFF transients, as shown in Fig. 2(c) and (d). In this experiment, R_S and C_S are set to 1000 Ω and 100 nF, respectively.

The voltage clamping circuit described in [34] is adopted in this article. M_S (IPD60R180P7S) is a Si MOSFET with similar voltage rating as the DUTs. The gate voltage of M_S is biased at V_{DD} (7.6 V) and its threshold voltage ($V_{th,MS}$) is 3.5 V. When

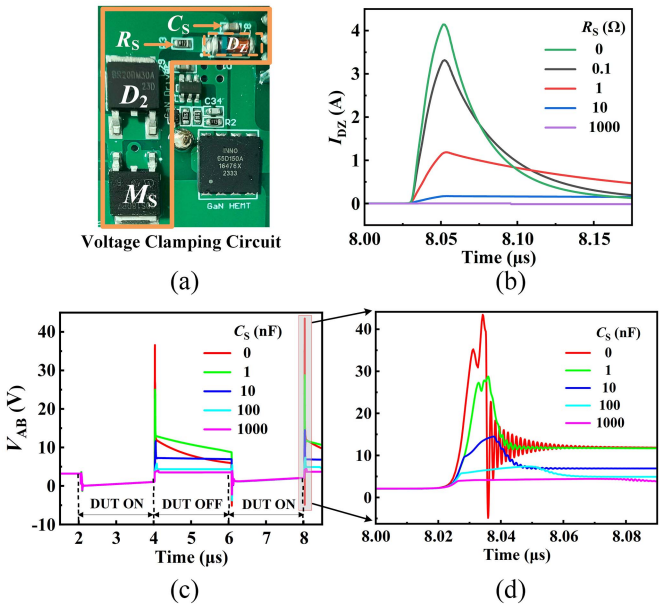


Fig. 2. Design of the voltage clamping circuit. (a) Top view of the PCB for voltage clamping circuit. (b) Simulated waveforms of I_{DZ} when using different resistance values for R_S. (c) Simulated waveforms of V_{AB} when using different capacitance values for C_S. (d) Enlarged waveforms of V_{AB} during turn-OFF.

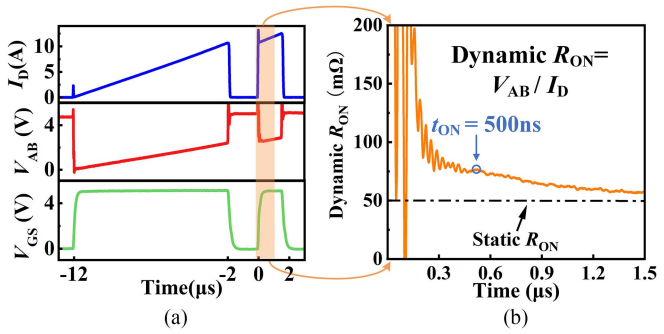


Fig. 3. Dynamic R_{ON} measurement and extraction. (a) Measured I_D, V_{AB} and V_{GS} waveforms of DUTs. (b) Dynamic R_{ON} transients extracted from the highlighted time slot in (a).

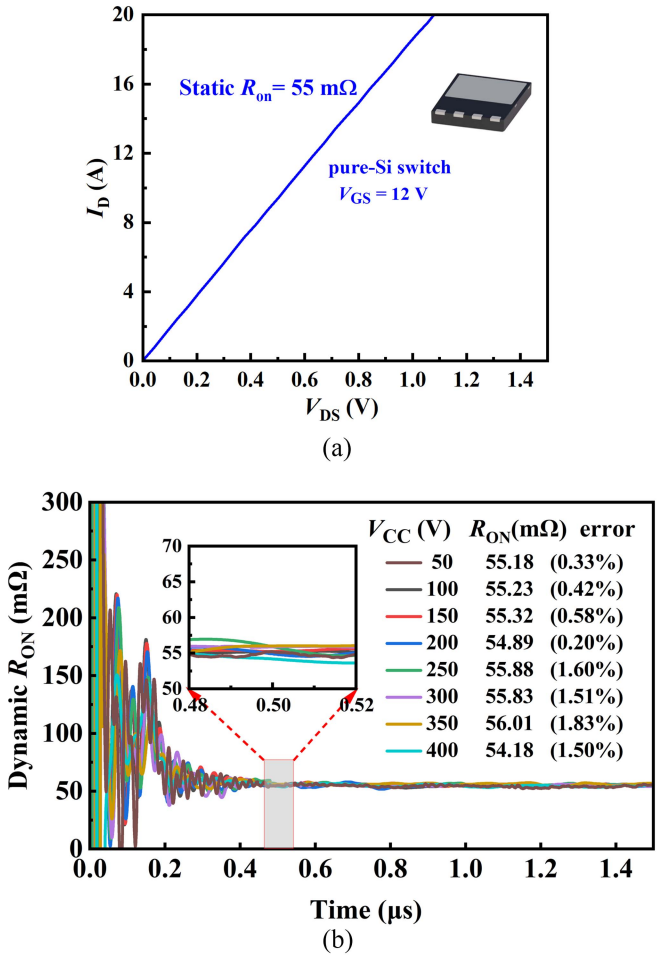


Fig. 4. Accuracy validation of the measured results using a pure-Si switch. (a) Measured static R_{ON} by Keysight B1505A semiconductor parameter analyzer. (b) Measured dynamic R_{ON} transients switching from different V_{CC}. (I_D = 10 A).

the DUTs are at OFF-state, V_{AB} is clamped at (V_{DD}-$V_{th,MS}$). When the DUTs are at ON-state, M_S turns on and $V_{AB} = V_{DS}$. At OFF-state, M_S prevents the high voltage at DS from appearing at AB. This enables the oscilloscope to measure the ON-state voltage at AB with a high resolution.

Fig. 3 shows the method for extracting dynamic R_{ON} of the DUTs in the double-pulse setup. The DUTs are switched on twice throughout the entire test. The interval between the two pulses is 1 μs. Dynamic R_{ON} is calculated after the DUTs are switched ON in the second time [see the time slot highlighted in Fig. 3(a)]. The dynamic R_{ON} decreases gradually from a maximum to a constant value and remains higher than the static R_{ON} in the following hundreds of microseconds.

Given that dynamic $R_{ON} = V_{AB}/I_D$, the extraction of dynamic R_{ON} should be performed until both V_{AB} and I_D waveforms have stabilized with no oscillations observed. According to IEC 63373-2022 [35], to ensure the extracted dynamic R_{ON} value is sufficiently accurate, it is also required to measure dynamic R_{ON} in < 1 μs after switching. In order to simultaneously satisfy both requirements, dynamic R_{ON} at 500 ns after switching are extracted in this experiment to quantify the degradation. By adjusting the duration of the first ON-state pulse, the dynamic R_{ON} switching at different drain currents can be measured and extracted (e.g., a 10-μs pulse facilitates a drain current of 10 A).

In the double-pulse test, the entire testing process lasts only a few microseconds, so that the heat generated is very small (approximately several μJ), which basically excludes the effect of temperature on the dynamic R_{ON} degradation.

The measurement accuracy of the double-pulse setup is validated with a pure-Si switch (two paralleled IPL65R130CFD7). Since silicon-based devices do not exhibit dynamic R_{ON} degradation [15], the dynamic R_{ON} should equal the static R_{ON}. The static R_{ON} is measured with a Keysight B1505A Power Device Analyzer, which is an industry-standard instrument for precise semiconductor parameter extraction. The measured static R_{ON} is 55 mΩ, as shown in Fig. 4(a). The measured dynamic R_{ON} values from double-pulse setup exhibit a range of 54.1 to 56.2 mΩ when V_{CC} varies from 50 to 400 V, as illustrated in Fig. 4(b). The

TABLE I
PARAMETERS FOR HYBRID-I [36], [37]

Device types / Parameters	Hybrid-I (p-GaN HEMT/Si MOSFET)	
	Q_1	Q_2
Technology	*p*-GaN gate	SJ MOSFET
Ratings	650 V/ 104 mΩ	650 V/ 110 mΩ
Vendor	Innoscience	Infineon
Threshold voltage	1.7 V	4 V
Gate driver	LM5114	SI8261BCC -C-ISR

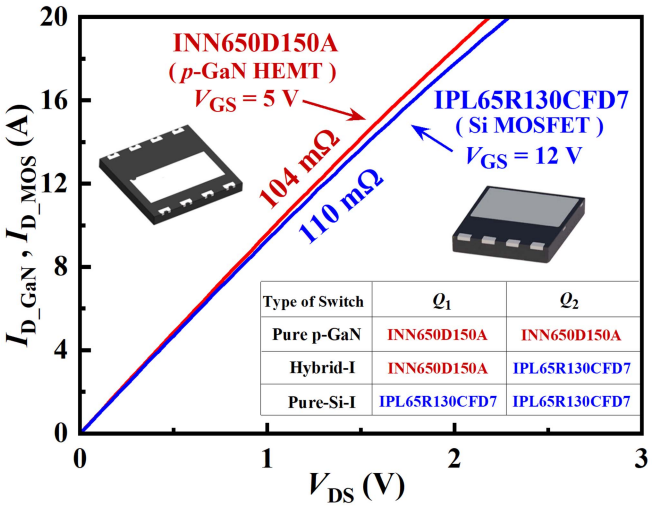


Fig. 5. Output characteristic curves for the DUTs measured by Keysight B1505A semiconductor parameter analyzer.

below 2% deviation between static and dynamic measurements demonstrates the high accuracy of the proposed configuration.

Currently, there are two mainstream commercial device types in the GaN power device market: the p-GaN HEMTs and Cascode GaN HEMTs. In this article, both device types are investigated within a hybrid switch. The p-GaN HEMT/Si MOSFET hybrid switch is designated as Hybrid-I. The Cascode GaN HEMT/Si MOSFET hybrid switch is designated as Hybrid-II.

III. HYBRID-I

In this section, the p-GaN HEMT/Si MOSFET hybrid switch (Hybrid-I) is investigated. For comparison, two paralleled p-GaN HEMTs (designated as a pure p-GaN switch) and two paralleled Si MOSFETS (designated as a pure-Si-I switch) are also tested. Table I shows the detailed parameters for devices used to form Hybrid-I. The resistance extracted from curve tracer for the p-GaN HEMT (104 mΩ) is slightly lower than that for the Si MOSFET (110 mΩ), as shown in Fig. 5. During the test, the p-GaN HEMT and the Si MOSFET are switched on with V_{GS} = 5 and 12 V, respectively, and switched OFF with V_{GS} = 0 V.

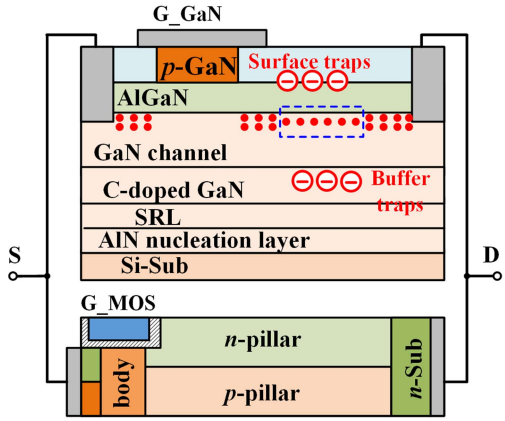


Fig. 6. Reduced 2DEG density caused by the negative-charged traps for the GaN HEMT inside a hybrid switch.

A. Dynamic ON-Resistance

Fig. 6 shows the schematic with the cross-sections of the devices inside the hybrid switch. The stress-relief-layer of the GaN HEMT serves to relief the stress caused by lattice mismatch and difference in thermal expansion coefficient between Si and GaN materials. The superjunction (SJ) structure has alternating n-pillar and p-pillar, which are homogeneous silicon materials with only different doping types. The dynamic R_{ON} degradation in GaN power HEMTs is induced by electron trapping, which typically occurs at two key locations: the AlGaN barrier layer surface and the buffer layer [7], [8]. At OFF-state, the channel hot electrons can be captured by the surface traps and the vertically drifting electrons can be captured by the buffer traps. At ON-state, the negative-charged traps cannot de-trap the captured electrons immediately and thus deplete the 2DEG, leading to increased resistance. Moreover, the charging of deep-level traps may increase with E-field strength in GaN devices [8], [11]. For the Si-based SJ MOSFET, the depletion region across the *n*-pillar and *p*-pillar at OFF-state can be quickly recovered to neutral region when switched to the ON-state. The Si MOSFET is fabricated on a homogeneous silicon wafer with highly mature processes. The common defect-related traps in heterojunction semiconductor devices are nearly negligible in silicon devices [15].

Dynamic R_{ON} transients switched from different OFF-state voltages (V_{CC}) are measured. Fig. 7(a) shows the measurement results over time. Fig. 7(b) shows a partially enlarged view of Fig. 7(a). For a more intuitive comparison, the dynamic R_{ON} values extracted at 500 ns after switching are normalized in Fig. 7(c). Both the hybrid switch and pure p-GaN switch exhibit increased dynamic R_{ON} when V_{CC} increases from 50 to 250 V, but the Si MOSFET effectively lowers down the R_{ON} since the current carried by the Si MOSFET is not subject to the trapping effect. Particularly, the dynamic R_{ON} of the hybrid switch is 22.37% lower than the pure GaN switch under the same condition (V_{CC} = 250 V). The ratio of dynamic R_{ON} to static R_{ON} reaches its maximum value when V_{CC} is between 250 and 300 V, and then drops as V_{CC} continues to increase. This can be explained by the leaky-dielectric model [11], [38].

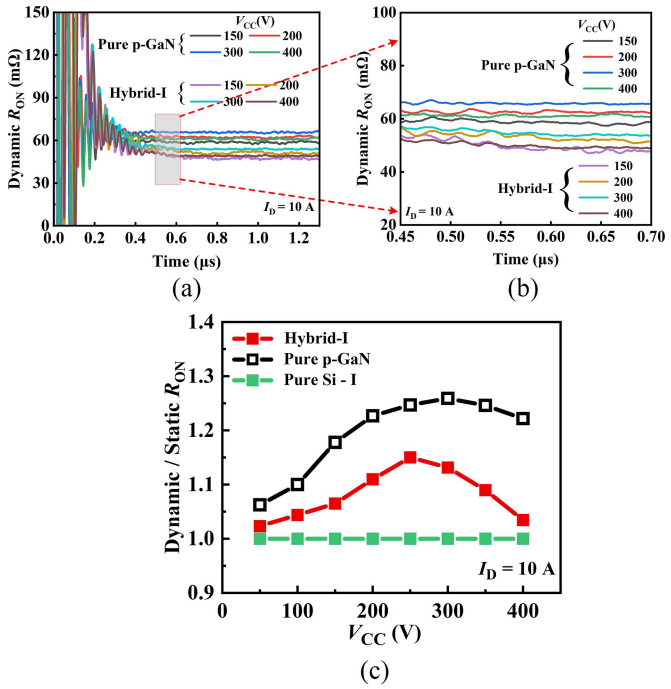


Fig. 7. Dynamic R_{ON} comparison. (a) Measured dynamic R_{ON} transients of the pure p-GaN switch and hybrid switch directly after switching from different OFF-state voltages (V_{CC} = 150, 200, 300, 400 V, I_D = 10 A). (b) Enlarged view of (a). (c) Dynamic / static R_{ON} value as a function of V_{CC}.

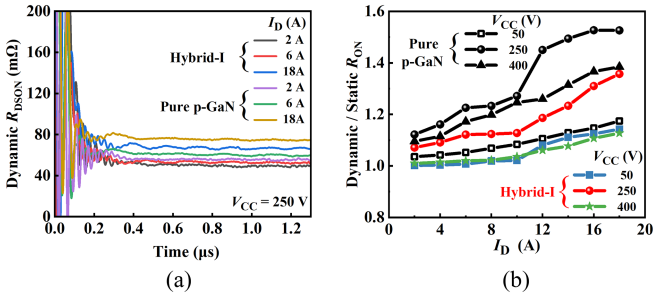


Fig. 8. (a) Measured dynamic R_{ON} transients for I_D = 2 A, 6 A and 18 A. (b) Dynamic / static R_{ON} value as a function of I_D.

Dynamic R_{ON} transients switched from different ON-state currents (I_D) are measured. Fig. 8 shows the impact of I_D on the dynamic R_{ON} for the investigated switches. For all switches, the dynamic R_{ON} increases with I_D. For a more intuitive comparison, the dynamic R_{ON} values extracted at 500 ns after switching are normalized in Fig. 8(b). Compared to the pure p-GaN switch, the dynamic R_{ON} for the hybrid switch is significantly suppressed over a wide range of I_D.

Fig. 9 shows the impact of T_{on_delay} on the dynamic R_{ON} for Hybrid-I. T_{on_delay} is defined as the turn-ON signals' delay time between the GaN HEMT and the MOSFET, as shown in the insets of Fig. 9(a). T_{on_delay} was well calibrated and can be accurately controlled by the FPGA controller. When $T_{on\_delay} > 0$, the GaN HEMT turns ON earlier than the MOSFET. The drain current is all carried by the GaN HEMT during the delay time. This

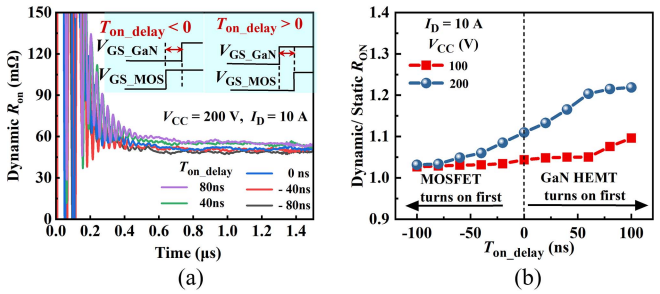


Fig. 9. Impact of T_{on_delay} on the dynamic R_{ON} for Hybrid-I. (a) Measured dynamic R_{ON} transients with different T_{on_delay}. (b) Dynamic / static R_{ON} value as a function of T_{on_delay}.

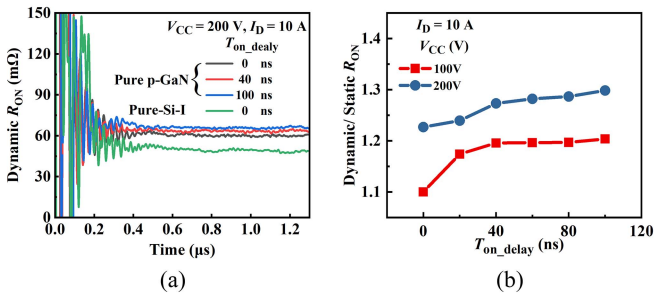


Fig. 10. Impact of T_{on_delay} on the dynamic R_{ON} for the pure p-GaN switch. (a) Measured dynamic R_{ON} transients with different T_{on_delay}. (b) Dynamic / static R_{ON} value as a function of T_{on_delay}.

overloaded drain current leads to an increase in dynamic R_{ON}, as already illustrated in Fig. 8. When $T_{on\_delay} < 0$, the MOSFET turns ON earlier than the GaN HEMT. The drain current is all carried by the MOSFET during the delay time. The GaN HEMT turns on with a small drain current and thus exhibits reduced dynamic R_{ON}.

Fig. 10 shows the impact of T_{on_delay} on the dynamic R_{ON} for the pure p-GaN switch. Since the two parallelled GaN HEMTs are identical, it does not matter which one turns on first. The dynamic R_{ON} increases with T_{on_delay}. The GaN HEMT that turns on earlier has to carry an over-loaded current during the delay-time, which leads to an increase in dynamic R_{ON}. The pure p-GaN switch has the lowest dynamic R_{ON} when both devices turn on simultaneously (T_{on_delay} = 0), as shown in Fig. 10(b).

Fig. 11 shows the ratio of dynamic R_{ON} to static R_{ON} as functions of V_{CC} and I_D when T_{on_delay} = –140, –40, 0, and 40 ns, respectively. Both Fig. 11(a) and (b) indicate that a negative T_{on_delay} can further enhance the advantage of the hybrid switch over the pure p-GaN switch in terms of dynamic R_{ON} suppression.

B. Turn-ON and Turn-OFF Losses

There are four different gate control patterns for a hybrid switch, as shown in Fig. 12. The turn-ON and turn-OFF gate signals' delay time between the GaN HEMT and the MOSFET are defined as T_{on_delay} and T_{off_delay}, respectively. The test circuit for extracting and measuring turn-ON and turn-OFF losses

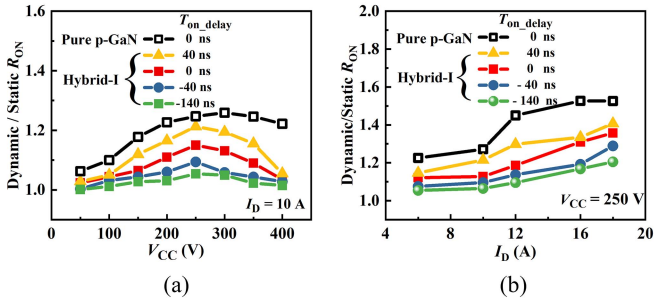


Fig. 11. Measured dynamic / static R_{ON} value as a function of (a) V_{CC} and (b) I_D with $T_{on\_delay} = -140$, -40, 0, and 40 ns.

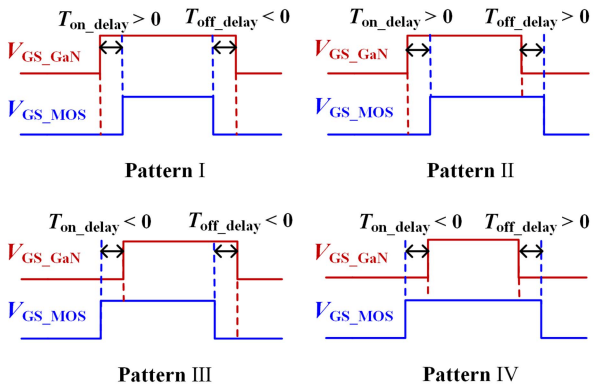
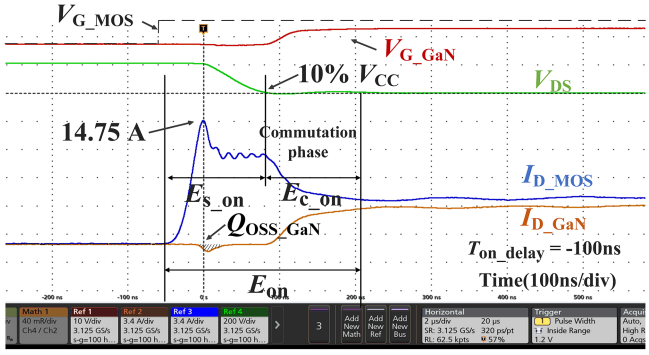
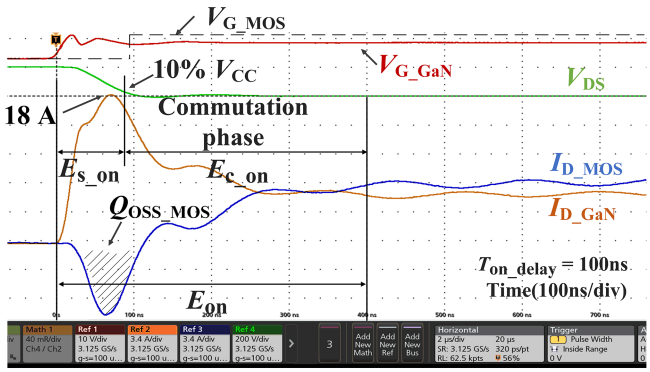


Fig. 12. Gate control patterns for a hybrid switch.



(a)



(b)

Fig. 13. Turn-ON waveforms for Hybrid-I. (a) $T_{on\_delay} = -100$ ns. (b) $T_{on\_delay} = 100$ ns.

is also based on the double-pulse setup shown in Fig. 1. Coaxial shunts are employed on each parallel branch to detect the current I_{D_GaN} and I_{D_MOS}. The currents I_{D_GaN} and I_{D_MOS} are the currents of the GaN HEMT branch and the Si MOSFET branch in the hybrid switch, respectively. The critical signals are monitored using a 12-bit digital oscilloscope (MSO44) with a bandwidth of 20 MHz.

Fig. 13(a) and (b) show the measured turn-ON waveforms when $T_{on\text{-}delay}$ takes –100 and 100 ns, respectively. The total turn-ON loss (E_{on}) for a hybrid switch consists of two parts: E_{s_on} and E_{c_on} ($E_{on} = E_{s\_on} + E_{c\_on}$). E_{s_on} represents the loss calculated from the moment when I_D ($I_D = I_{D\_GaN} + I_{D\_MOS}$) begins to rise to the moment when V_{DS} drops to $10\%V_{CC}$. E_{c_on} represents the loss during the commutation phase, which is calculated from the moment when $V_{DS} = 10\%V_{CC}$ until I_D is stabilized. E_{c_on} is usually much smaller than E_{s_on} because V_{DS} has decreased to a relatively low value during the commutation phase.

The turn-ON current peak value of the GaN HEMT in Fig. 13(b) is 18 A, much higher than that (14.75 A) of the Si MOSFET in Fig. 13(a). This can be explained by the discharging process shown in Fig. 14. The transistor that turns ON first needs to carry the discharging current of the other transistor that have not yet turned on. Since the Si MOSFET has much higher C_{DS} than the GaN HEMT, the discharging current when $T_{on\_delay} > 0$ is thus higher than that when $T_{on\_delay} < 0$. Consequently, a positive T_{on_delay} increases the turn-ON overshoot in GaN

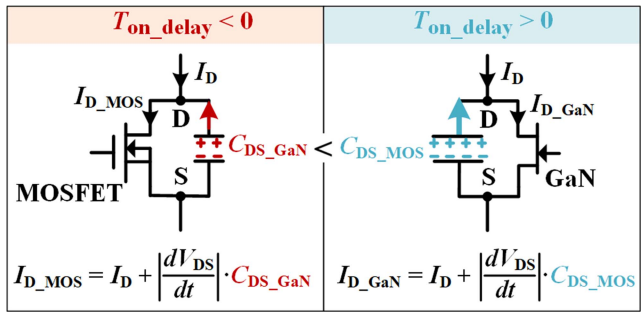


Fig. 14. Discharging current induced by C_{DS} during turn-ON transient.

HEMT, which further leads to more pronounced dynamic R_{ON} degradation.

Although a higher discharging current is observed when $T_{on\_delay} > 0$, a smaller E_{on} can still be achieved compared to that with $T_{on\_delay} < 0$, as shown in Fig. 15. The minimum turn-ON loss of the hybrid switch is obtained at the turn-ON gate signal's delay time of approximately 20 ns.

Fig. 16 illustrates the dependence of E_{on} and dynamic R_{ON} on T_{on_delay}. More negative T_{on_delay} is favorable to decrease the dynamic R_{ON} but results in higher E_{on}. There exists a trade-OFF relationship between dynamic R_{ON} and E_{on}. The selection of T_{on_delay} for achieving a minimum overall loss largely

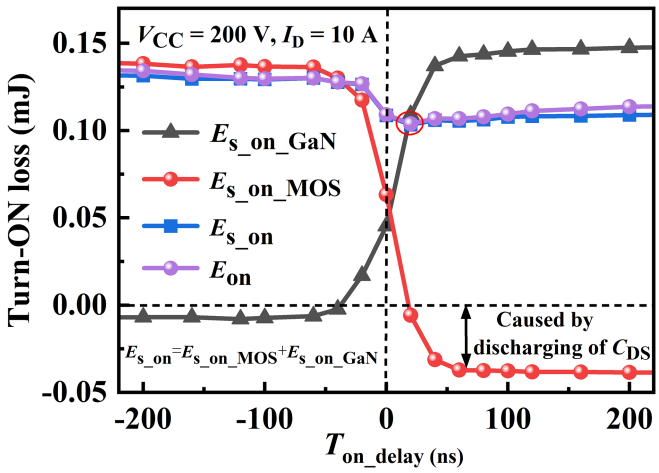


Fig. 15. Turn-ON loss as functions of $T_{\text{on\_delay}}$ for Hybrid-I. (Minimum at $T_{\text{on\_delay}} = 20$ ns).

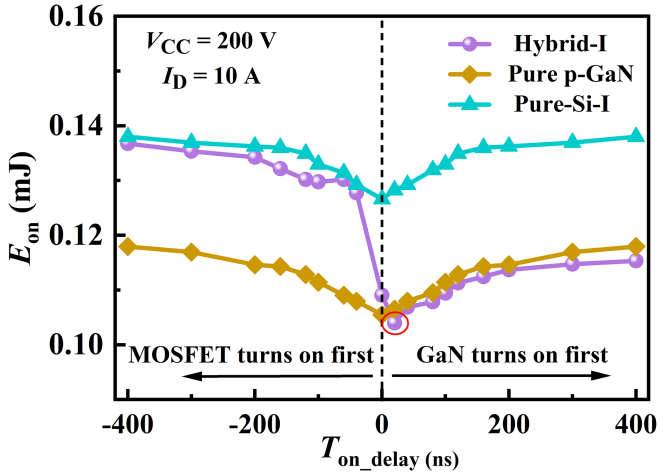


Fig. 17. Comparison of E_{on} for three switches. (Minimum at $T_{\text{on\_delay}} = 20$ ns for Hybrid-I).

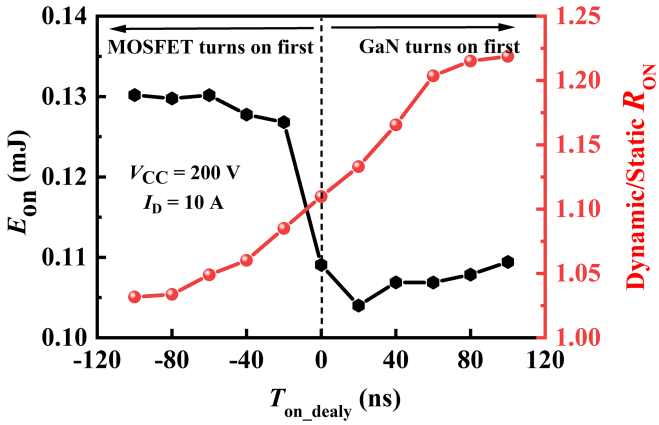


Fig. 16. Impact of $T_{\text{on\_delay}}$ on E_{on} and dynamic R_{ON} for Hybrid-I. Optimum $T_{\text{on\_delay}}$ for achieving a minimum overall loss depends on the switching frequency and duty cycle in the specific applications.

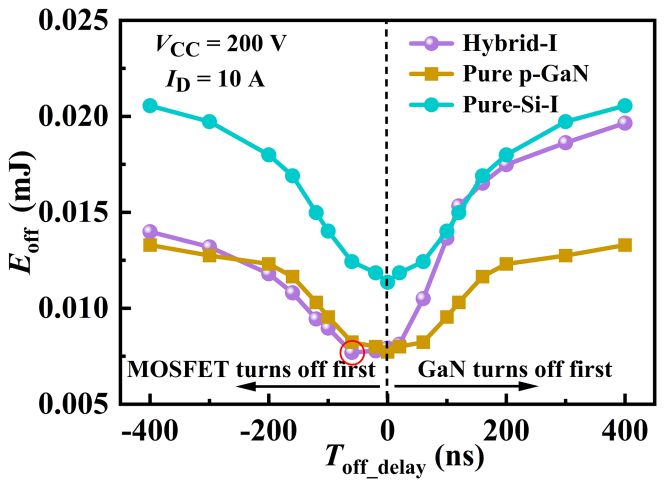


Fig. 18. Turn-OFF loss as functions of $T_{\text{off\_delay}}$ for Hybrid-I (Minimum at $T_{\text{off_delay}} = -60$ns), pure p-GaN and pure-Si-I switch.

depends on the switching frequency and duty cycle in the specific applications.

Fig. 17 compares the total turn-ON loss (E_{on}) for the hybrid switch, the pure p-GaN switch and the pure-Si-I switch. The pure p-GaN switch exhibits lower E_{on} than the pure-Si-I switch because of the smaller capacitance. When $T_{\text{on\_delay}} > 0$ ns, the hybrid switch shows almost the same E_{on} as the pure p-GaN switch. When $T_{\text{on\_delay}} < 0$ ns, the hybrid switch shows almost the same E_{on} as the pure-Si-I switch.

Fig. 18 compares the total turn-OFF loss (E_{off}) for the hybrid switch, the pure p-GaN switch and the pure-Si-I switch. The pure-Si-I switch has the highest E_{off} as expected. The hybrid switch shows almost the same E_{off} as the pure p-GaN switch when $T_{\text{off\_delay}} < 0$. This makes sense because the GaN HEMT experiences hard turn-OFF when $T_{\text{off\_delay}} < 0$. However, when $T_{\text{off\_delay}} > 0$, the E_{off} for the hybrid switch becomes higher than the pure p-GaN switch and is almost the same as the pure-Si-I switch. This makes sense because the MOSFET experiences hard turn-OFF when $T_{\text{off\_delay}} > 0$. This indicates that allowing the GaN HEMT to experience hard turn-OFF results in lower E_{off}, and it also does not induce degradation of the dynamic R_{ON}.

C. Hybrid-I in Buck Converters

The GaN/Si hybrid switch is tested in an asynchronous buck converter. The test circuit for the buck converter is shown in Fig. 19(a). D_{W} is a SiC diode (IDW40G120C5B) to handle freewheeling current. An inductor of 100 μH is selected as L_{F} and a capacitor of 44 μF is selected as C_{F}. The test system setup is shown in Fig. 19(b).

Fig. 20 shows the tested efficiencies for the 200-to-48 V converters using Hybrid-I switch. $T_{\text{on\_delay}}$ has a significant impact on the system's efficiency. For a given frequency, the efficiency first increases and then decreases when $T_{\text{on\_delay}}$ varies from 0 to –200 ns. The optimal $T_{\text{on\_delay}}$ that enables the highest efficiency differs for each switching frequency. The

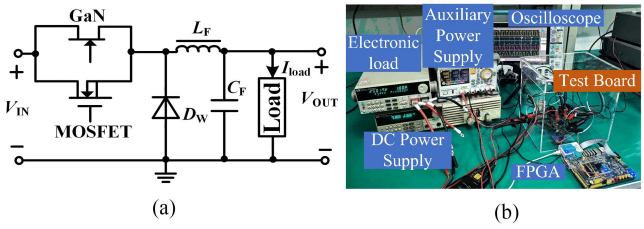


Fig. 19. (a) Test circuit for asynchronous buck converter using a hybrid switch. (b) Test setup for buck converter.

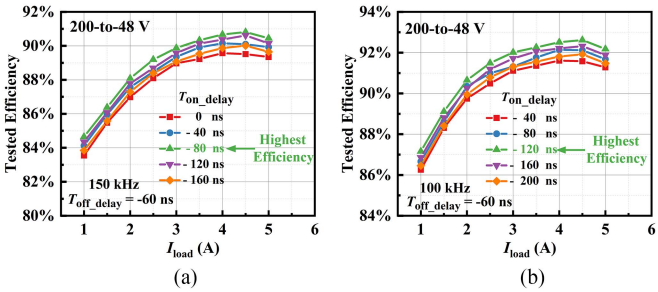


Fig. 20. Impact of $T_{\text{on\_delay}}$ on tested efficiency for 200-to-48 V buck converter using Hybrid-I switch operated at (a) 150 and (b) 100 kHz.

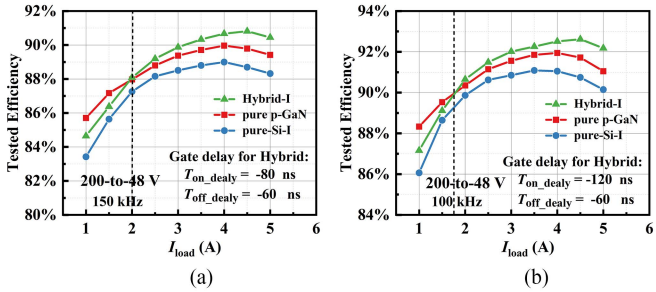


Fig. 21. Efficiency comparison for 200-to-48 V buck converters using three different switches operated at (a) 150 and (b) 100 kHz.

highest efficiencies at 150 and 100 kHz are obtained when $T_{\text{on\_delay}}$ is set to –80 and –120 ns, respectively. It indicates that the lower the switching frequency, the longer the turn-ON delay required in the GaN HEMT to realize the highest efficiency. This can be well explained by the tradeoff relationship between the dynamic ON-resistance and the turn-ON loss for a hybrid switch.

Fig. 21 compares the efficiency for the 200-to-48 V converters using different switches. The Hybrid-I switch operates with optimized $T_{\text{on\_delay}}$ and $T_{\text{off\_delay}}$. The pure p-GaN switch and the pure-Si-I switch operate with no gate delay between paralleled devices. The converter using pure p-GaN switch shows the highest efficiency only at very light load. This is because the dynamic R_{ON} degradation of the p-GaN HEMT at lower currents is not severe and the switching losses dominate the total losses. The hybrid switch, however, enables the highest efficiency over a wide current range. This is because the conduction losses become predominant as the current increases [39], [40]. The hybrid switches enable more effective dynamic R_{ON} suppression. Moreover, as the switching frequency decreases,

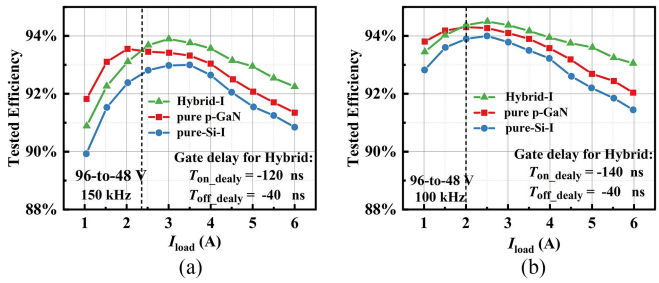


Fig. 22. Efficiency comparison for 96-to-48 V buck converters using three different switches operated at (a) 150 kHz and (b) 100 kHz.

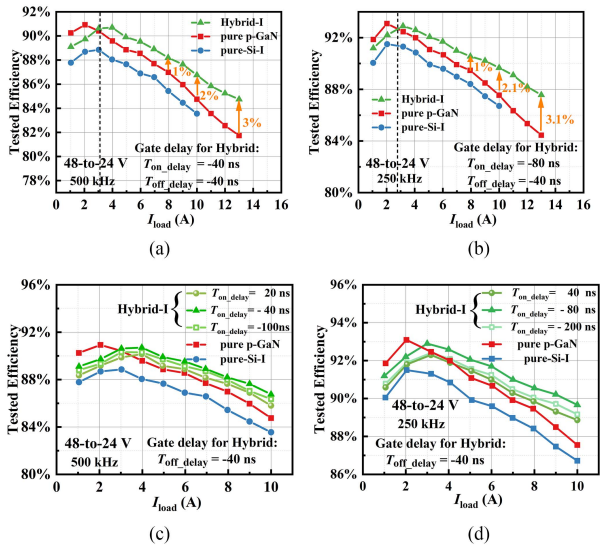


Fig. 23. Efficiency comparison for 48-to-24 V buck converters using three different switches operated at (a) 500, (b) 250, (c) 500, and (d) 250 kHz. $T_{\text{on\_delay}}$ is set within a wide range for hybrid switch in (c) and (d).

the intersection of the efficiency curves of the Hybrid switch and pure p-GaN switch shifts toward the left.

Fig. 22 compares the efficiency for the 96-to-48 V converters using different switches. The converter using pure p-GaN switch shows the highest efficiency only at very light load. The hybrid switch, however, enables the highest efficiency over a wide current range.

In order to further investigate the performance at higher frequencies and currents, the Hybrid-I switch is also tested at a frequency up to 500 kHz and a load current up to 13 A, as shown in Fig. 23. The converter using Hybrid-I switch has an efficiency improvement of 3% compared to converters using pure p-GaN switch, with output power of more than 300 W and switching frequency of 500 kHz. Similarly, as the switching frequency decreases, the intersection of the efficiency curves of the Hybrid switch and pure p-GaN switch shifts towards the left. Moreover, there is not very stringent requirement for precise control of $T_{\text{on\_delay}}$. As shown in Fig. 23(c) and (d), even when the $T_{\text{on\_delay}}$ is set within a wide range (e.g., –200 $< T_{\text{on\_delay}} <$ 40 ns at 250 kHz, and –100 $< T_{\text{on\_delay}} <$ 20 ns at 500 kHz), the hybrid solution still achieves higher efficiency compared to pure p-GaN switch.

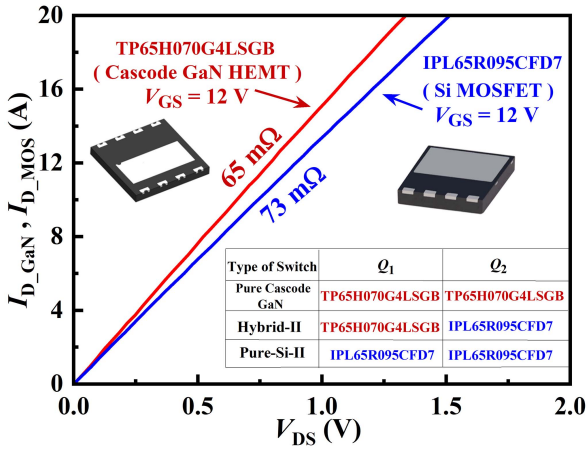


Fig. 24. Output characteristics for the DUTs measured by Keysight B1505A semiconductor parameter analyzer [41], [42].

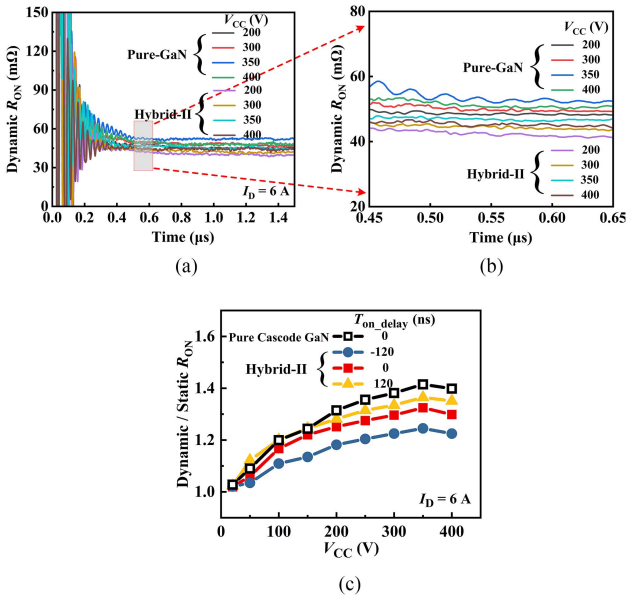


Fig. 25. Impact of OFF-state voltage on the dynamic R_{ON}. (a) Measured dynamic R_{ON} transients with different V_{CC}. (b) Enlarged view of (a). (c) Dynamic / static R_{ON} value as a function of V_{CC}.

The current ratio of the GaN HEMT and Si MOSFET used in this work is 1:1. Adopting devices with different die-sizing ratios may yield more optimal solutions.

IV. Hybrid-II

In this section, the Hybrid-II (Cascode GaN HEMT/Si MOSFET) switch is investigated.

The Cascode GaN HEMT consists of two individual dies (a normally OFF Si MOSFET and a normally-on HEMT) mounting in one package. It has the same threshold voltage and gate drive voltage as the SJ MOSFET. This makes the drive control of Hybrid-II more convenient since the two devices can use the same driver (SI8261BCC-C-ISR). The resistance extracted from curve tracer for the Cascode GaN HEMT (65 mΩ) is slightly

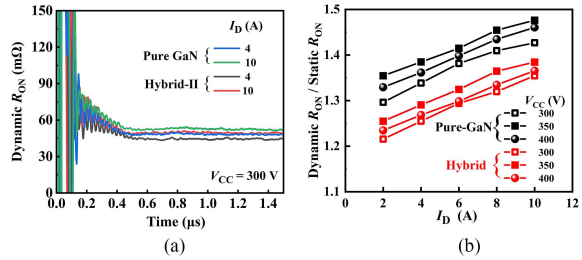


Fig. 26. (a) Measured dynamic R_{ON} transients for I_D = 4 and 10 A. (b) Dynamic / static R_{ON} value as a function of I_D.

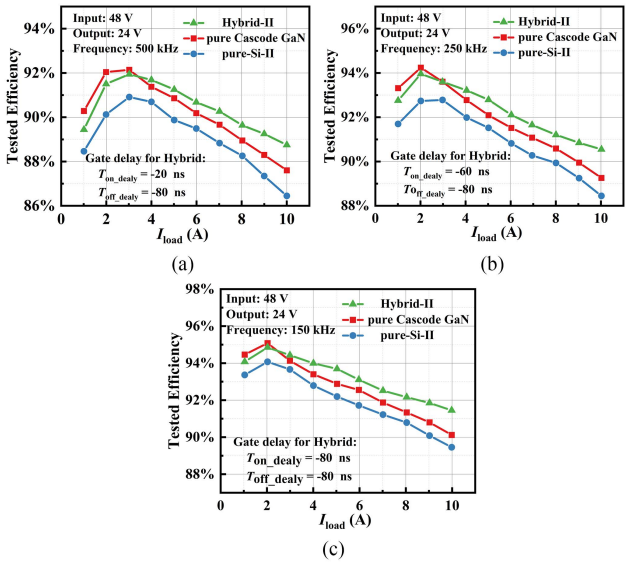


Fig. 27. Efficiency comparison for 48-to-24 V buck converters using three different switches operated at (a) 500, (b) 250, and (c) 150 kHz.

lower than that for the Si MOSFET (73 mΩ), as shown in Fig. 24. During the test, both devices are switched on with $V_{GS} = 12$ V, and switched OFF with $V_{GS} = 0$ V.

Fig. 25 shows the impact of OFF-state voltage (V_{CC}) on the dynamic R_{ON}. Hybrid-II switch shows lower dynamic R_{ON} than that of pure Cascode GaN switch under the same V_{CC}. A negative T_{on_delay} for Hybrid-II can further decrease the dynamic R_{ON}.

Dynamic R_{ON} transients switched from different ON-state currents (I_D) for the pure cascode GaN switch and Hybrid-II switch are measured. Fig. 26(a) shows the impact of I_D on the dynamic R_{ON} for the investigated switches. The dynamic R_{ON} increases with I_D. For a more intuitive comparison, the dynamic R_{ON} values extracted at 500 ns after switching are normalized in Fig. 26(b). The ratio of dynamic R_{ON} to static R_{ON} reaches its maximum value when V_{CC} is 350 V, and then drops as V_{CC} continues to increase. For all switches, the dynamic R_{ON} increases with I_D. Compared to the pure cascode GaN switch, the dynamic R_{ON} for the Hybrid-II switch is significantly suppressed over a wide range of I_D.

Hybrid-II and its counterparts are tested in a 48-to-24 V asynchronous buck converter. Fig. 27 compares the efficiency for converters using different switches. Hybrid-II operates with optimized T_{on_delay} and T_{off_delay}. The pure cascode GaN switch

TABLE II
EFFICIENCY IMPROVEMENT OF HYBRID SWITCHES OVER THE PURE-GAN SWITCHES AT AN OUTPUT POWER OF 240 W

Voltage \ Frequency		500kHz	250kHz	150kHz	100kHz
Hybrid-I	48-to-24 V	2.01%	2.12%		
	96-to-48 V			0.88%	0.92%
	200-to-48 V			1.10%	1.13%
Hybrid-II	48-to-24 V	1.15%	1.30%	1.33%	

and the pure-Si-II switch operate with no gate delay between parallelled devices. The converter using pure cascode GaN switch shows the highest efficiency only at very light load. The hybrid switch, however, enables the highest efficiency over a wide current range.

V. CONCLUSION

In this study, two types of GaN/Si hybrid switches (p-GaN gate HEMT/Si MOSFET and Cascode GaN HEMT/Si MOSFET) are demonstrated in hard-switching applications. Both device-level and system-level performances are investigated with extensive experiments and solid analysis. The conclusions are as follows:

1) The GaN/Si hybrid switches exhibit suppressed dynamic $R_{\rm ON}$ when compared with their pure-GaN counterparts. The dynamic $R_{\rm ON}$ can be further decreased when the GaN device turns ON lagged behind the Si device within the hybrid switch.
2) There exists a trade-OFF relationship between the turn-ON loss and the dynamic $R_{\rm ON}$ for a GaN/Si hybrid switch. A carefully engineered gate control pattern between GaN and Si devices within the hybrid switch can minimize the total loss, enabling higher power conversion efficiency in a dc–dc buck converter than the pure-GaN switch does. Table II listed the efficiency percentage improvement in various buck converters under different voltage conversion levels and switching frequencies. As the output power continues to increase, the advantages of the hybrid solution can be even more pronounced.
3) Hybrid switches configured with either a p-GaN gate HEMT or a Cascode GaN HEMT are promising in increasing the output power for GaN-based converters. The Cascode GaN HEMT has the same threshold voltage and gate voltage as the Si MOSFET, making the gate control more convenient.

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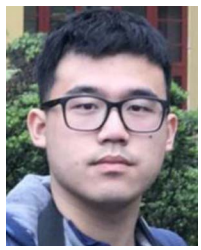

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