Discontinuous Pulse-Width Modulation With Balanced DC-Link Capacitor Voltages for Three-Phase Four-Level Inverters

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***Abstract*—Compared with three-level inverters, four-level inverters need more switching times to balance the dc-link capacitor voltages, lowering the efficiency. This article proposes a four-level discontinuous pulsewidth modulation (4L-DPWM) to reduce the switching loss of inverters by clamping the switching state of one phase, and the dc-link capacitor voltage balancing is achieved as well. First, the subsector division is optimized. In each subsector, the switching-state sequence consists of five basic vectors that clamp the phase with the highest current under the unity power factor condition. Then, voltage balancing equations are derived and considered when calculating the dwelling times of five basic vectors. As a result, the switching loss is reduced, and the dc-link capacitor voltage is balanced. Finally, A 6-kVA three-phase four-level inverter prototype is built to conduct experiments. Experimental results show that the proposed 4L-DPWM scheme can effectively balance the capacitor voltage and achieve higher efficiency.**

***Index Terms*—Capacitor voltage balancing, discontinuous pulsewidth modulation (DPWM), four-level inverter.**

I. Introduction

TO ACHIEVE higher capacity and lower conduction loss, the dc-link voltage of three-phase inverters is increased [1], [2], [3]. For example, 1500 V dc-link voltage has been gradually utilized by photovoltaic systems and microgrids in recent years [4], [5], raising an urgent need to reduce the voltage stress of switching devices in the topology [6], [7], [8], [9]. Four-level inverters feature lower voltage stress and better harmonic performance than three-level inverters. Fig. 1 shows the topology of the three-phase four-level tree-type active neutral-point clamped (TANPC) inverter, which requires the minimum switching devices among four-level topologies [10], [11]. To fabricate a 1500 V inverter, the four-level TANPC inverter only needs two 1200 V devices and four 650 V devices for each phase, while three-level inverters must utilize higher-voltage-rating devices [12].

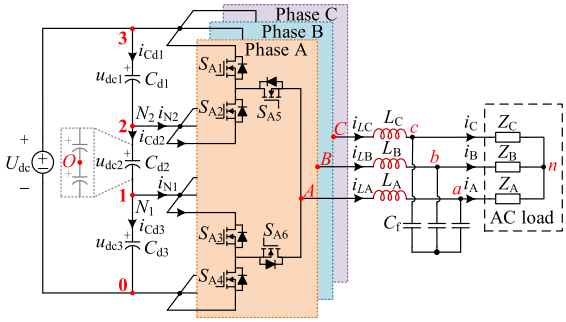

Fig. 1. Topology of the three-phase four-level TANPC Inverter.

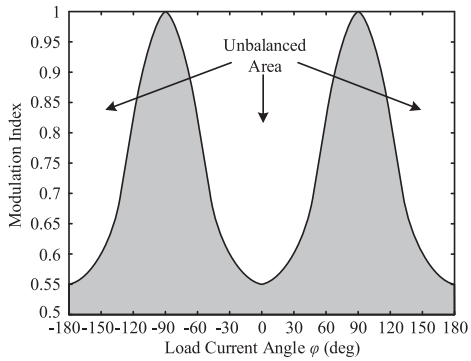

Fig. 2. Voltage balancing region of four-level inverter by using the conventional SVPWM with NTVs.

However, it is more difficult to balance the dc-link capacitor voltage in a four-level inverter compared with three-level inverters. The conventional space-vector pulsewidth modulation (SVPWM) strategy based on the nearest three vectors (NTVs) cannot achieve balanced capacitor voltage under high modulation indices [13], as illustrated in Fig. 2. The unbalanced dc-link capacitor voltage leads to alternating output current distortion and increased voltage stress on switching devices.

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Employing virtual space vectors is an effective method to balance the dc-link capacitor voltage. A virtual-vector pulsewidth modulation (VVPWM) for three-phase four-level inverters was introduced in [14], where basic vectors are linearly combined in fixed proportions to generate virtual vectors that have no impact on the dc-link capacitor voltages. The three nearest virtual vectors synthesize the reference voltage. As a result, the voltage balance of all dc-link capacitors can be achieved with all modulation indices and power factors (PFs) within one switching period [15], [16]. However, since virtual vectors are composed of up to five basic vectors, synthesizing the reference vector through virtual vectors significantly increases the switching times [17].

Utilizing additional phase output voltage levels within one switching period is another way to balance the dc-link capacitor voltage. In [18] and [19], a carrier overlapped pulsewidth modulation (COPWM) was proposed. Carrier signals with different amplitudes were overlapped to generate three voltage levels in each switching period, and the dwelling time of the intermediate voltage levels is equal. Thus, the total injected current of each capacitor is zero in a fundamental period, and dc-link capacitor voltages can be naturally balanced. In [20], by introducing a voltage level that is not adjacent to the target level, the redundant level modulation can control the charge/discharge status of the dc-link capacitors under full operating conditions, thereby achieving the voltage balance of dc-link capacitors. However, these methods generate four switching state transitions within one switching period, leading to a high switching loss.

Discontinuous pulsewidth modulations (DPWMs) can lower switching times by clamping the switching state of one phase during each switching period [21]. Recently, DPWM schemes have been widely adopted in two-level and three-level inverters [22]. However, its application in four-level inverters is still underexplored since the reduced switching times could cause an imbalance of capacitor voltages [23]. Therefore, the balance of dc-link capacitor voltages and the low switching loss have not yet been achieved simultaneously for three-phase four-level inverters with DPWM schemes.

This article proposes a four-level DPWM (4L-DPWM) scheme to achieve high efficiency and balanced dc-link capacitor voltage. In each subsector, the switching-state sequence consists of five basic vectors that clamp the phase with the highest current under the unity PF condition, and voltage balancing equations are derived and considered when calculating the dwelling times of the five basic vectors. As a result, both the dc-link capacitor voltage balance and the high efficiency are achieved.

The rest of this article is organized as follows. Section II presents the subsector division and switching-state sequences of the proposed 4L-DPWM scheme. Detailed power loss analysis and comparison analysis are given as well. In Section III, a 6-kVA TANPC inverter prototype was built to conduct experiments. Finally, Section IV concludes the article.

II. Proposed 4L-DPWM Scheme

In this section a 4L-DPWM with balanced dc-link capacitor voltage is proposed to lower the switching loss.

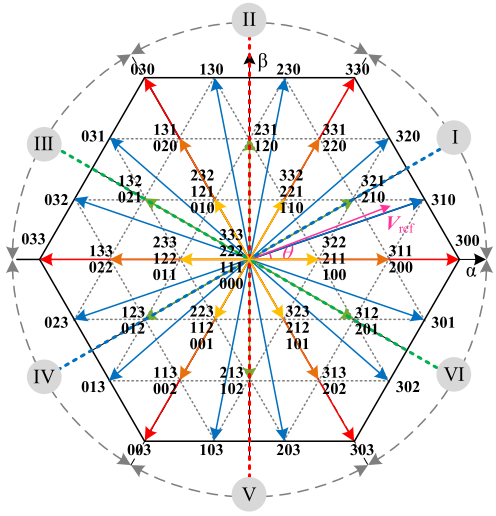

Fig. 3. Overall space-vector diagram of three-phase four-level inverter.

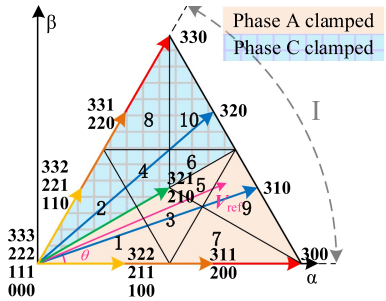

Fig. 4. Subsector division of the proposed 4L-DPWM in sector I.

A. Switching-State Sequence of the Proposed 4L-DPWM

Fig. 1 shows the topology of the three-phase four-level TANPC Inverter. As depicted in Fig. 1, the three-phase output terminals of the inverter are marked by A, B, and C. Terminal O represents the virtual neutral point of the dc-link. U_{dc} represents the dc-link voltage.

By controlling the switching devices, the voltage between terminal X (X = A, B, or C) and terminal O can achieve four levels ($U_{dc}/2$, $U_{dc}/6$, $-U_{dc}/6$, $-U_{dc}/2$), which are denoted as 3, 2, 1, and 0, respectively.

The space-vector diagram of the three-phase four-level inverter is shown in Fig. 3. Sector I is taken as an example for analysis. As depicted in Fig. 4, each sector is divided into ten subsectors. To minimize the switching losses, the switching state sequences of the proposed 4L-DPWM are designed to clamp the phase with the highest current under the unity PF condition, as given in Table I. It can be seen that, the phase-A switching state is clamped at three-level in subsectors 1, 3, 5, 7, and 9. The phase-C switching state is clamped at 0-level in subsectors 2, 4, 6, 8, and 10. Thus, the switching times can be reduced by 1/3.

B. DC-Link Capacitor Voltage Balancing Constraints for Dwelling Time Calculation

By using the five basic vectors shown in Table I to synthesize the reference vector, the switching state sequence is capable of

TABLE I
SWITCHING-STATE SEQUENCE OF 4L-DPWM AT BIG SECTOR I

Subsector	Switching-state sequence								
	V_{s1}	V_{s2}	V_{s3}	V_{s4}	V_{s5}	V_{s4}	V_{s3}	V_{s2}	V_{s1}
1	311	321	322	332	333	332	322	321	311
2	220	210	110	100	000	100	110	210	220
3	310	311	321	322	332	322	321	311	310
4	320	220	210	110	100	110	210	220	320
5	310	320	321	322	332	322	321	320	310
6	320	310	210	110	100	110	210	310	320
7	300	310	311	321	322	321	311	310	300
8	330	320	220	210	110	210	220	320	330
9	300	310	320	321	322	321	320	310	300
10	330	320	310	210	110	210	310	320	330

balancing the dc-link capacitor voltage. According to [20], the voltages of C_{d3} and C_{d1} can be self-balanced over a fundamental period when the voltage of C_{d2} is balanced. To keep the voltage of C_{d2} balanced during a switching period T_s, (1) should be satisfied as follows. i_{Cd2} is the current of C_{d2}

$$\int_{kT_s}^{(k+1)T_s} i_{Cd2}dt = 0. \tag{1}$$

Assuming that the dc-link voltage remains constant, (2) can be derived by using Kirchhoff law. i_{Cd1} and i_{Cd3} represent currents of C_{d1} and C_{d3}. i_{N1} and i_{N2} are currents flowing out from terminal N_1 and N_2 as shown in Fig. 1

$$\begin{cases} \int_{kT_s}^{(k+1)T_s} i_{Cd2}dt = \int_{kT_s}^{(k+1)T_s} (i_{Cd1} - i_{N2})\, dt \\ \int_{kT_s}^{(k+1)T_s} i_{Cd2}dt = \int_{kT_s}^{(k+1)T_s} (i_{Cd3} + i_{N1})\, dt \\ \int_{kT_s}^{(k+1)T_s} i_{Cd1}dt + \int_{kT_s}^{(k+1)T_s} i_{Cd2}\mathrm{d}t + \int_{kT_s}^{(k+1)T_s} i_{Cd3}dt = 0 \end{cases}. \tag{2}$$

Combining (2), (3) can be derived from (1), as follows:

$$\int_{kT_s}^{(k+1)T_s} i_{Cd2}\mathrm{d}t = \frac{1}{3}\left(\int_{kT_s}^{(k+1)T_s} i_{N1}\mathrm{d}t - \int_{kT_s}^{(k+1)T_s} i_{N2}dt\right) = 0. \tag{3}$$

The condition that the reference vector is located at subsector 7 of sector I is taken as an example for deriving the dc-link capacitor voltage balancing constraint. According to the switching-state sequence of subsector 7, (4) can be derived. T_{Vsx} represents the dwelling time of vector $\boldsymbol{V_{sx}}$, as listed in Table I ($x = 1, 2, 3, 4, 5$). Combining (3) and (4), it can be found that (5) should be satisfied to balance the capacitor voltage

$$\begin{cases} \int_{kT_s}^{(k+1)T_s} i_{N1}dt = (T_{Vs2} + T_{Vs3})\, i_{LB} + (T_{Vs3} + T_{Vs4})\, i_{\mathrm{LC}} \\ \int_{kT_s}^{(k+1)T_s} i_{N2}dt = (T_{Vs4} + T_{Vs5})\, i_{\mathrm{LB}} + T_{Vs5} i_{\mathrm{LC}} \end{cases} \tag{4}$$

$$\begin{cases} T_{Vs2} + T_{Vs3} - T_{Vs4} - T_{Vs5} = 0 \\ T_{Vs3} + T_{Vs4} - T_{Vs5} = 0 \end{cases}. \tag{5}$$

The dc-link capacitor voltage balancing equations when the reference vector is located at other subsectors can be similarly derived, as listed in Table II.

The normalized reference vector, $\boldsymbol{V_{\mathbf{ref}}}$, can be expressed as (6). θ represents the phase angle of the reference vector. $V_{\mathrm{ref\_}\alpha}$ and $V_{\mathrm{ref\_}\beta}$ represent the α- and β-axis components of the reference vector, respectively. MI represents the modulation index, which is calculated by (7). U_{ac} represents the RMS value of alternating output voltage

$$\boldsymbol{V_{\mathbf{ref}}} = \mathrm{MI} \cdot \boldsymbol{e}^{j\theta} = V_{\mathrm{ref\_}\alpha} + jV_{\mathrm{ref\_}\beta} \tag{6}$$

$$\mathrm{MI} = \sqrt{6}U_{\mathrm{ac}}/U_{\mathrm{dc}}. \tag{7}$$

To synthesize the reference vector, the dwelling time of each vector must meet the requirement of the volt-second balance principle. Combining dc-link capacitor voltage balancing equations, the dwelling time of each vector used by the proposed 4L-DPWM can be calculated by (8). V_{sx_α} and V_{sx_β} represent the α- and β-axis components of $\boldsymbol{V_{sx}}$ ($x = 1, 2, 3, 4, 5$), respectively. k_{sx} and j_{sx} represent the coefficients corresponding to functions of dc-link capacitor voltage balancing constraints, as analyzed above. ($x = 1, 2, 3, 4, 5$). d_{sx} is the dwelling duty

TABLE II
VOLTAGE BALANCING CONSTRAINTS OF 4L-DPWM AT SECTOR I

Subsector	Voltage balancing constraints
1	$\begin{cases} T_{Vs1} - T_{Vs2} - T_{Vs3} = 0 \\ T_{Vs1} + T_{Vs2} - T_{Vs3} - T_{Vs4} = 0 \end{cases}$
2	$\begin{cases} T_{Vs3} + T_{Vs4} - T_{Vs1} - T_{Vs2} = 0 \\ T_{Vs2} + T_{Vs3} - T_{Vs1} = 0 \end{cases}$
3	$\begin{cases} T_{Vs1} + T_{Vs2} - T_{Vs3} - T_{Vs4} = 0 \\ T_{Vs2} + T_{Vs3} - T_{Vs4} - T_{Vs5} = 0 \end{cases}$
4	$\begin{cases} T_{Vs4} + T_{Vs5} - T_{Vs2} - T_{Vs3} = 0 \\ T_{Vs3} + T_{Vs4} - T_{Vs1} - T_{Vs2} = 0 \end{cases}$
5	$\begin{cases} T_{Vs1} - T_{Vs2} - T_{Vs3} - T_{Vs4} = 0 \\ T_{Vs3} - T_{Vs4} - T_{Vs5} = 0 \end{cases}$
6	$\begin{cases} T_{Vs4} + T_{Vs5} - T_{Vs3} = 0 \\ T_{Vs2} + T_{Vs3} + T_{Vs4} - T_{Vs1} = 0 \end{cases}$
7	$\begin{cases} T_{Vs2} + T_{Vs3} - T_{Vs4} - T_{Vs5} = 0 \\ T_{Vs3} + T_{Vs4} - T_{Vs5} = 0 \end{cases}$
8	$\begin{cases} T_{Vs5} - T_{Vs3} - T_{Vs4} = 0 \\ T_{Vs4} + T_{Vs5} - T_{Vs2} - T_{Vs3} = 0 \end{cases}$
9	$\begin{cases} T_{Vs2} - T_{Vs3} - T_{Vs4} - T_{Vs5} = 0 \\ T_{Vs4} - T_{Vs5} = 0 \end{cases}$
10	$\begin{cases} T_{Vs5} - T_{Vs4} = 0 \\ T_{Vs3} + T_{Vs4} + T_{Vs5} - T_{Vs2} = 0 \end{cases}$

TABLE III
DWELLING DUTY OF EACH VECTOR BY USING THE PROPOSED 4L-DPWM AT SECTOR I

Subsector	d_{s1}	d_{s2}	d_{s3}	d_{s4}	d_{s5}
1	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}\right)$	$V_{\text{ref\_}\beta}$	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-3V_{\text{ref\_}\beta}\right)$	$2V_{\text{ref\_}\beta}$	$-\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}+1$
2	$V_{\text{ref\_}\beta}$	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}\right)$	$0.5\left(-\sqrt{3}V_{\text{ref\_}\alpha}+3V_{\text{ref\_}\beta}\right)$	$\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}$	$-\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}+1$
3	$\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}-1$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+3V_{\text{ref\_}\beta}\right)$	$V_{\text{ref\_}\beta}$	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-3V_{\text{ref\_}\beta}\right)$	$-\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}+1$
4	$\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}-1$	$-\sqrt{3}V_{\text{ref\_}\alpha}+1$	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}\right)$	$0.5\left(-\sqrt{3}V_{\text{ref\_}\alpha}+3V_{\text{ref\_}\beta}\right)$	$-2V_{\text{ref\_}\beta}+1$
5	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}\right)$	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+3V_{\text{ref\_}\beta}\right)-1$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}\right)$	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-3V_{\text{ref\_}\beta}\right)$	$-\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}+1$
6	$V_{\text{ref\_}\beta}$	$\sqrt{3}V_{\text{ref\_}\alpha}-1$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}\right)$	$0.5\left(-\sqrt{3}V_{\text{ref\_}\alpha}+3V_{\text{ref\_}\beta}\right)$	$-2V_{\text{ref\_}\beta}+1$
7	$\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}-1$	$2V_{\text{ref\_}\beta}$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+3V_{\text{ref\_}\beta}\right)$	$V_{\text{ref\_}\beta}$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}\right)$
8	$2V_{\text{ref\_}\beta}-1$	$\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}$	$-\sqrt{3}V_{\text{ref\_}\alpha}+1$	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}\right)$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}\right)$
9	$\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}-1$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}-V_{\text{ref\_}\beta}\right)$	$0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+3V_{\text{ref\_}\beta}\right)-1$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}\right)$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}\right)$
10	$2V_{\text{ref\_}\beta}-1$	$-V_{\text{ref\_}\beta}+1$	$\sqrt{3}V_{\text{ref\_}\alpha}-1$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}\right)$	$1-0.5\left(\sqrt{3}V_{\text{ref\_}\alpha}+V_{\text{ref\_}\beta}\right)$

of $\boldsymbol{V_{sx}}$, representing the ratio of T_{Vsx} to T_s ($x = 1, 2, 3, 4, 5$), as expressed by (9)

$$\begin{bmatrix} V_{s1\_\alpha} & V_{s2\_\alpha} & V_{s3\_\alpha} & V_{s4\_\alpha} & V_{s5\_\alpha} \\ V_{s1\_\beta} & V_{s2\_\beta} & V_{s3\_\beta} & V_{s4\_\beta} & V_{s5\_\beta} \\ 1 & 1 & 1 & 1 & 1 \\ k_{s1} & k_{s2} & k_{s3} & k_{s4} & k_{s5} \\ j_{s1} & j_{s2} & j_{s3} & j_{s4} & j_{s5} \end{bmatrix} \begin{bmatrix} T_{Vs1} \\ T_{Vs2} \\ T_{Vs3} \\ T_{Vs4} \\ T_{Vs5} \end{bmatrix} = \begin{bmatrix} V_{\text{ref\_}\alpha} \\ V_{\text{ref\_}\beta} \\ 1 \\ 0 \\ 0 \end{bmatrix} T_s \tag{8}$$

$$d_{s1} = \frac{T_{Vsx}}{T_s}\,(x = 1, 2, 3, 4, 5)\,. \tag{9}$$

Combining (8) and Table II, the dwelling duty of each vector by using the proposed 4L-DPWM scheme at sector I is given in Table III. The voltage balancing equations used in the dwelling duty calculation are independent of the phase currents. Thus, the balance of the capacitor voltages is not affected by the PF.

C. Implementation of the Proposed 4L-DPWM

This section presents the implementation of the proposed 4L-DPWM scheme. Firstly, the phase angle of the reference vector can easily identify the big sector. Then, the subsector should be identified. The condition that the reference vector is located at subsector 5 of sector I is analyzed as an example. The inscribed circle radius of the space-vector diagram is set at 1. Boundary lines of subsector 5 are depicted in Fig. 5. Thus, (10) should be followed when the reference vector is located at subsector 5. The boundary of other subsectors can be similarly derived. Then, the subsector identification method when the reference vector is located at sector I is given in Table IV

$$\begin{cases} V_{\text{ref\_}\beta} \geqslant -V_{\text{ref\_}\alpha}/\sqrt{3} + 2/3 \\ V_{\text{ref\_}\beta} \leqslant V_{\text{ref\_}\alpha}/\sqrt{3} \\ V_{\text{ref\_}\beta} \geqslant \sqrt{3}V_{\text{ref\_}\alpha} - 1 \end{cases}. \tag{10}$$

After identifying the subsector, the dwelling time of each vector can be calculated according to Table III. Then, the modulation signals should be derived. The proposed 4L-DPWM scheme has four types of switching-state sequence, as shown in Fig. 6. m_{Xn} represents the nth modulation signal of phase-X ($n = 1, 2, 3$). u_c represents the carrier signal, whose peak value

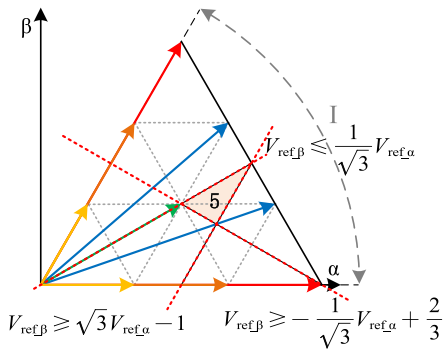

Fig. 5. Linear programming of subsector 5 in sector I.

TABLE IV
SUBSECTOR DIVISION OF 4L-DPWM AT SECTOR I

Sub-sector	Criteria for subsector judgement $\left(X=\sqrt{3}V_{\text{ref\_}\alpha}-1,\ Y=V_{\text{ref\_}\alpha}/\sqrt{3},\ Z=-V_{\text{ref\_}\alpha}/\sqrt{3}+2/3\right)$
1	$\left(V_{\text{ref\_}\beta}\leqslant -X\right)\&\left(V_{\text{ref\_}\beta}\leqslant Y\right)$
2	$\left(V_{\text{ref\_}\beta}\leqslant -X\right)\&\left(V_{\text{ref\_}\beta}\geqslant Y\right)$
3	$\left(V_{\text{ref\_}\beta}\geqslant -X\right)\&\left(V_{\text{ref\_}\beta}\geqslant X\right)\&\left(V_{\text{ref\_}\beta}\leqslant Y\right)\&\left(V_{\text{ref\_}\beta}\leqslant Z\right)$
4	$\left(V_{\text{ref\_}\beta}\geqslant -X\right)\&\left(V_{\text{ref\_}\beta}\geqslant Y\right)\&\left(V_{\text{ref\_}\beta}\leqslant 0.5\right)\&\left(V_{\text{ref\_}\alpha}\leqslant 1/\sqrt{3}\right)$
5	$\left(V_{\text{ref\_}\beta}\geqslant X\right)\&\left(V_{\text{ref\_}\beta}\leqslant Y\right)\&\left(V_{\text{ref\_}\beta}\geqslant Z\right)$
6	$\left(V_{\text{ref\_}\beta}\geqslant Y\right)\&\left(V_{\text{ref\_}\beta}\leqslant 0.5\right)\&\left(V_{\text{ref\_}\beta}\geqslant 1/\sqrt{3}\right)$
7	$\left(V_{\text{ref\_}\beta}\leqslant X\right)\&\left(V_{\text{ref\_}\beta}\leqslant Z\right)$
8	$\left(V_{\text{ref\_}\beta}\geqslant 0.5\right)\&\left(V_{\text{ref\_}\alpha}\leqslant 1/\sqrt{3}\right)$
9	$\left(V_{\text{ref\_}\beta}\leqslant X\right)\&\left(V_{\text{ref\_}\beta}\geqslant Z\right)$
10	$\left(V_{\text{ref\_}\beta}\geqslant 0.5\right)\&\left(V_{\text{ref\_}\alpha}\geqslant 1/\sqrt{3}\right)$

is H. The relationship between the modulation signal, m_{Xn}, and the type of switching- state sequence can be derived from Fig. 6, expressed as (11). d_{X1} and d_{X2} represent the dwelling duty of one-level and two-level to switching period in phase-X bridge-leg voltage (X = A, B, C), respectively. By using (11),

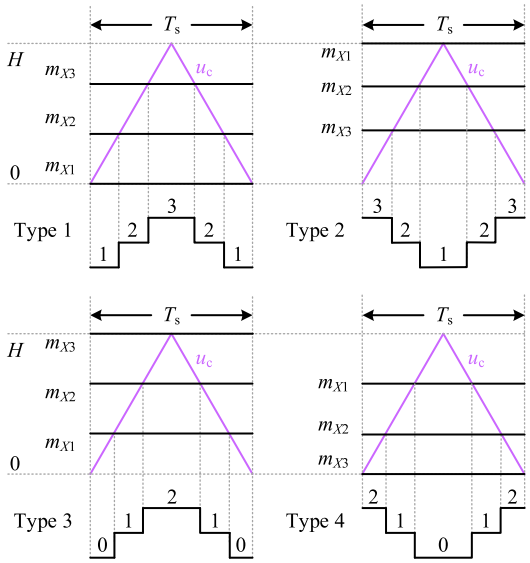

Fig. 6. Four types of switching-state sequences with the 4L-DPWM scheme.

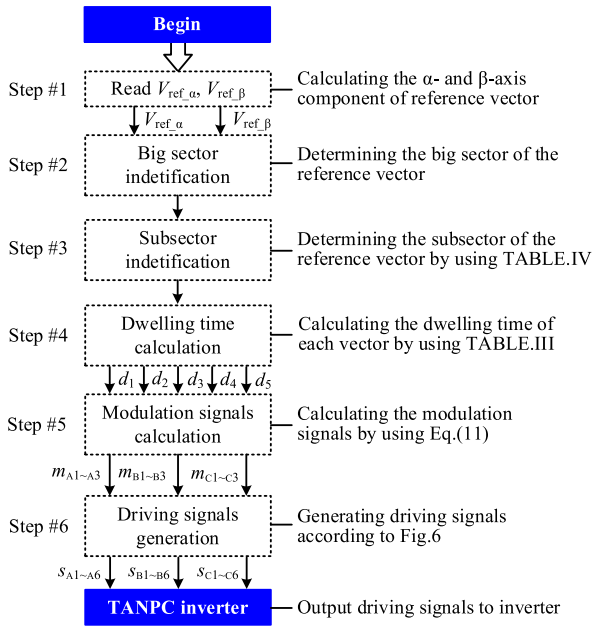

Fig. 7. Implementation of the proposed 4L-DPWM scheme.

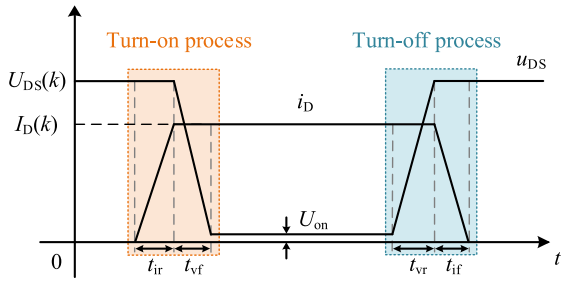

Fig. 8. Switching process of SiC MOSFET.

the three modulation signals for the clamped phase are set at H or 0 simultaneously to clamp the switching state at three-state or zero-state, respectively.

When the reference vector is located at sector I, combining (11) with Tables I, III, and IV, modulation signals corresponding with switching-state sequences can be derived. Then, actual driving signals are generated based on the modulation signal. These two different types of switching-state sequences in Fig. 6 can be easily realized by a digital signal processor (DSP) with an enhanced pulsewidth modulator. The modulation signal is loaded into the counter-compare register, and the time-base counter provides the carrier signal for comparison. The same modulation process can be conducted when the reference vector is located at other big sectors

$$\text{Type1},\begin{cases} m_{X3}=H\left(d_{X1}+d_{X2}\right)\\ m_{X2}=Hd_{X1}\\ m_{X1}=0 \end{cases}$$

$$\text{Type2},\begin{cases} m_{X3}=H\left(1-d_{X1}-d_{X2}\right)\\ m_{X2}=H\left(1-d_{X1}\right)\\ m_{X1}=H \end{cases}$$

$$\text{Type3},\begin{cases} m_{X3}=H\\ m_{X2}=H\left(1-d_{X2}\right)\\ m_{X1}=H\left(1-d_{X1}-d_{X2}\right) \end{cases}$$

$$\text{Type4},\begin{cases} m_{X3}=0\\ m_{X2}=Hd_{X2}\\ m_{X1}=H\left(d_{X1}+d_{X2}\right) \end{cases} \tag{11}$$

The overall implementation process of the proposed 4L-DPWM scheme is depicted in Fig. 7. First, the α- and β-axis components of the reference vector are calculated by using inverse Park transformation. Step #2 and Step #3 identify the big sector and subsector. The big sector can be identified according to the phase angle of the reference vector, and Table IV is used to identify the subsector. In step #4, following the capacitor voltage balance equations, the dwelling time of each vector is calculated, as given in Table III. Then, modulation signals are computed in step #5 by using (11). Finally, step #6 generates the driving signals according to the comparing logic shown in Fig. 6, and outputs the driving signals to the four-level inverter.

D. Power Loss Analysis

A piecewise linear switching process model of MOSFET, as shown in Fig. 8, was built to conduct the switching loss analysis of the proposed 4L-DPWM scheme and existing schemes. t_{ir} and t_{if} represent the rise and fall time of the drain current of MOSFET. t_{vr} and t_{vf} represent the rise and fall time of the drain-source voltage of MOSFET. The switching loss and conduction loss of MOSFET S_{mn} (m = A, B, C; n = 1, 2, 3, 4, 5, 6), as shown in Fig. 1, during k-th switching period can be calculated by (12) and (13). $U_{\mathrm{DS}}^{mn}(k)$ and $I_D^{mn}(k)$ represent the drain-source voltage and drain current of MOSFET S_{mn}, respectively. $R_{\mathrm{ds(on)}}$ represents the ON-state resistance of MOSFET. $d_{\mathrm{on}}^{mn}(k)$ is the duty cycle of MOSFET S_{mn} in kth switching period. T_{s} and T_1

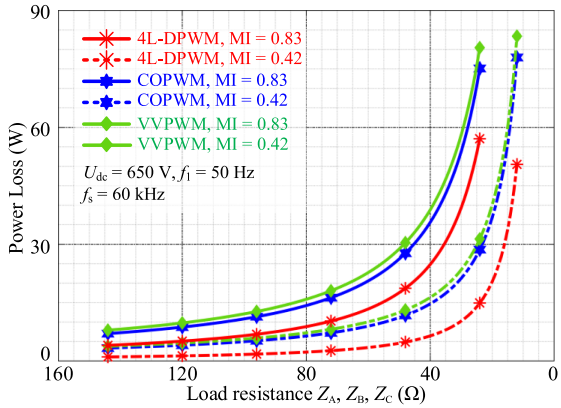

Fig. 9. Calculated total power loss of three-phase four-level inverter with different modulation schemes.

TABLE V
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value
Rated output power	6 kW
Rated DC-link voltage U_{dc}	650 V
DC-link capacitor C_{d1}, C_{d2}, C_{d3}	1560 μF
Switching frequency f_s	60 kHz
Fundamental frequency f_1	50 Hz
Filter inductor L_A, L_B, L_C	450 μH
Filter capacitor C_f	4.7 μF
SiC MOSFET (S_{mn}; m=A, B, C; n=1, 2, 3, 4, 5, 6)	IV1Q12080T3

denote the switching period and fundamental period, respectively. Then, the total switching loss and total conduction loss of the three-phase four-level inverter, as depicted in Fig. 1, can be calculated as (14). N_f is the ratio of switching frequency f_s to fundamental frequency f_1 (f_s/f_1). Therefore, the total loss P_{loss} can be expressed as (15).

$$E_{\text{sw}}^{mn}(k) = \begin{cases} \frac{U_{\text{DS}}^{mn}(k) I_D^{mn}(k)}{2T_s}\left(t_{ir}+t_{if}+t_{vr}+t_{vf}\right), & \text{not clamped} \\ 0, & \text{switching state is clamped} \end{cases} \tag{12}$$

$$E_{\text{con}}^{mn}(k) = [I_D^{mn}(k)]^2 R_{\text{ds(on)}} \cdot d_{\text{on}}^{mn}(k)\, T_s \tag{13}$$

$$\begin{cases} P_{\text{sw}} = \frac{1}{T_1}\sum_{k=1}^{N_f}\left(\sum_{m=A,B,C}\sum_{n=1}^{6} E_{\text{sw}}^{mn}(k)\right) \\ P_{\text{con}} = \frac{1}{T_1}\sum_{k=1}^{N_f}\left(\sum_{m=A,B,C}\sum_{n=1}^{6} E_{\text{con}}^{mn}(k)\right) \end{cases} \tag{14}$$

$$P_{\text{loss}} = P_{\text{sw}} + P_{\text{con}} \tag{15}$$

The calculated power loss of the three-phase four-level TANPC inverter with different schemes is depicted in Fig. 9. The operation conditions and output filter configuration are in accordance with experiments, as listed in Table V. Three-phase loads are set at 24 Ω. IV1Q12080T3 produced by INVENTCHIP is used as the SiC MOSFET. t_{ir}, t_{if}, t_{vr}, and t_{vf} can be obtained

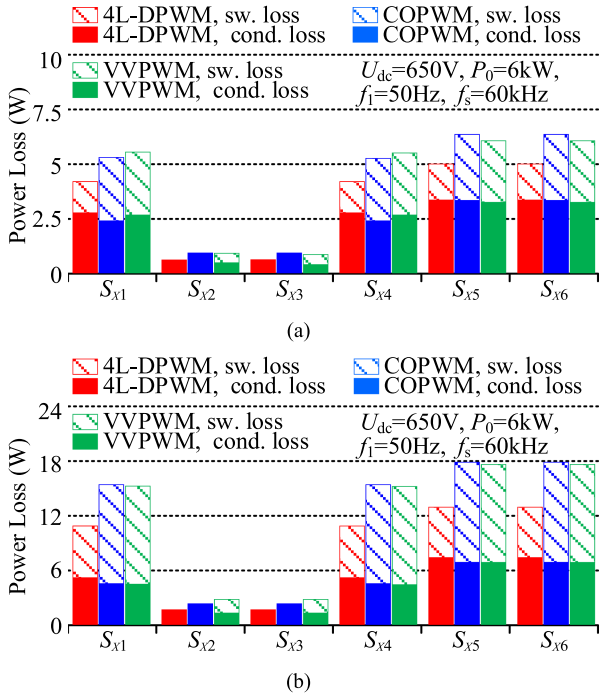

Fig. 10. Loss distribution analysis of different modulation schemes at rated operation conditions with different devices. (a) SiC MOSFET. (b) Si IGBT.

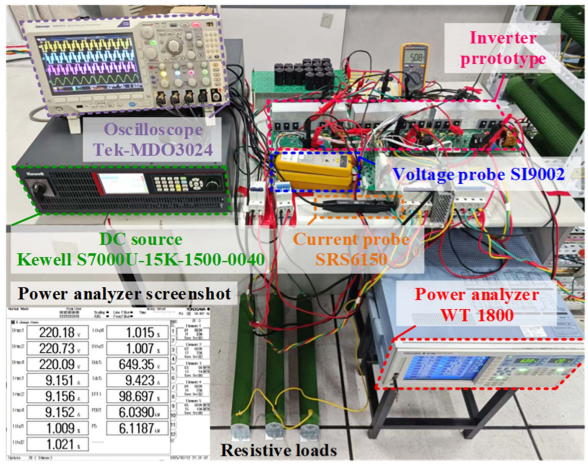

Fig. 11. Photograph of the platform and experimental setup.

from its datasheet. When the modulation is set at 0.83, the inverter operates with a rated output voltage, 220 V. From Fig. 9, it can be seen that, due to the reduction of switching times, the proposed 4L-DPWM scheme reduces the switching loss significantly compared with the VVPWM scheme and COPWM scheme. Therefore, the proposed 4L-DPWM can achieve higher efficiency.

Fig. 10 presents the power loss distribution by using different modulation schemes. The MI is set at 0.83 (rated condition). The output power is set at 6-kW. SiC devices and Si devices are both considered. IKW25N120T2 produced by INFINEON is used as Si IGBTs, and IV1Q12080T3 is still used as SiC MOSFET. It is noted that the power loss calculation of Si IGBT is different

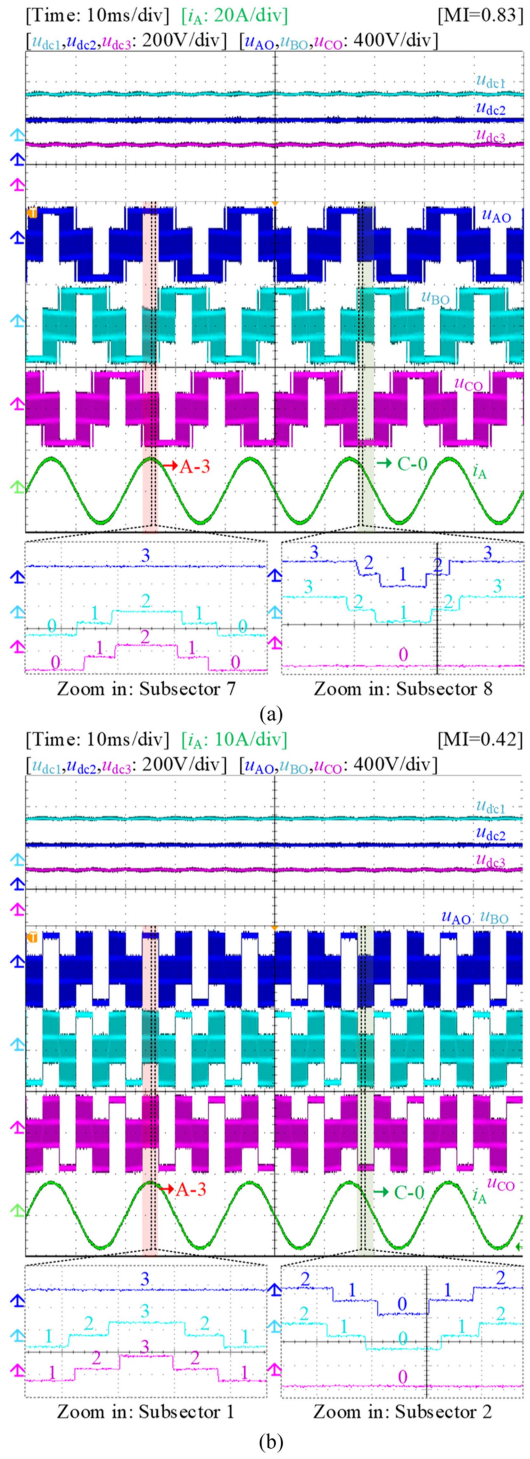

Fig. 12. Steady-state waveforms of the proposed 4L-DPWM scheme. (a) MI = 0.83. (b) MI = 0.42.

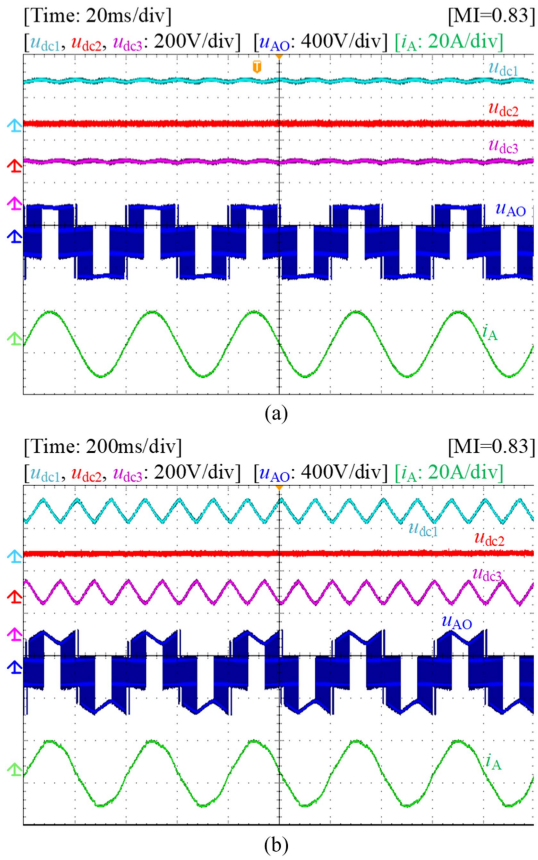

Fig. 13. Steady-state waveforms of the proposed 4L-DPWM scheme with lower fundamental frequency at rated MI. (a) $f_1 = 25$ Hz. (b) $f_1 = 2.5$ Hz.

from that of SiC MOSFET. Since the power loss model of Si IGBT can be found in [24], the detailed power loss calculation process of Si IGBT is not presented here. From Fig. 10, it can be seen that, compared with COPWM and VVPWM, the proposed 4L-DPWM scheme reduced the switching loss by about 50%, and thus featuring the lowest total power loss as shown in Fig. 9. Besides, although the switching loss and conduction loss are increased significantly when Si IGBTs are employed, the proposed 4L-DPWM scheme is still effective in reducing switching loss. The power loss distribution among S_{x1} to S_{x6} can also be seen in Fig. 10. Under the unit PF, the devices S_{x2} and S_{x3} have the lowest power loss, while S_{x5} and S_{x6} have the highest power loss. Since the proposed 4L-DPWM reduces the switching loss of S_{x5} and S_{x6}, the power loss difference between each device is also reduced compared with the existing COPWM and VVPWM schemes.

III. Experimental Results

A 6-kW SiC-based three-phase four-level TANPC inverter prototype is developed to verify the effectiveness of the proposed 4L-DPWM scheme. The specifications of the prototype are listed in Table V. The prototype is controlled by a DSP TMS320F28379D and a field programmable gate array EF2L45GL144B. Fig. 11 shows the photograph of the platform and experimental setup. The TANPC inverter is powered by a dc source, Kewell S7000U-15K, and its output is connected with three-phase loads. The efficiencies and total harmonic distortion (THD) are measured by a six-channel power analyzer WT1800E. Experimental waveforms are captured by an oscilloscope Tektronix MDO-3024. Voltage waveforms are measured by a voltage probe (SI9002), and current waveforms are measured by a current probe (SRS6150) with 50 MHz bandwidth.

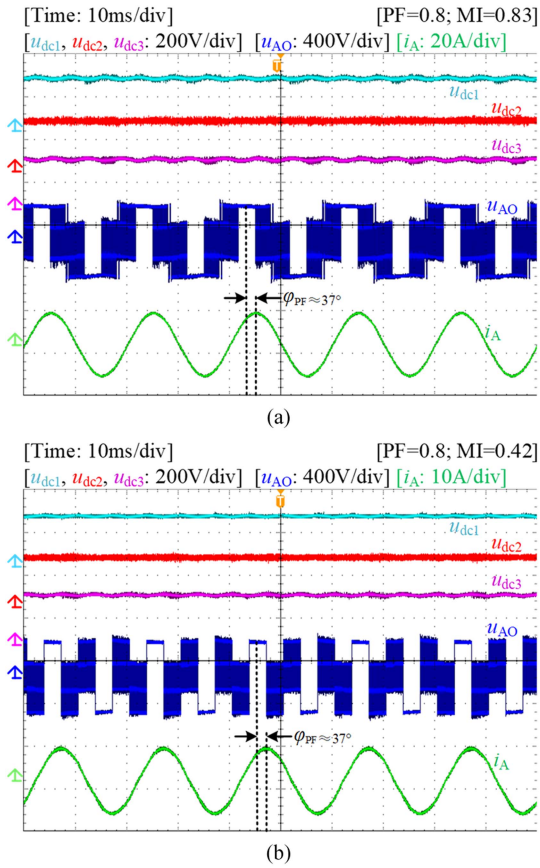

Fig. 14. Steady-state waveforms of the proposed 4L-DPWM scheme with nonunit power factor. (a) MI = 0.83. (b) MI = 0.42.

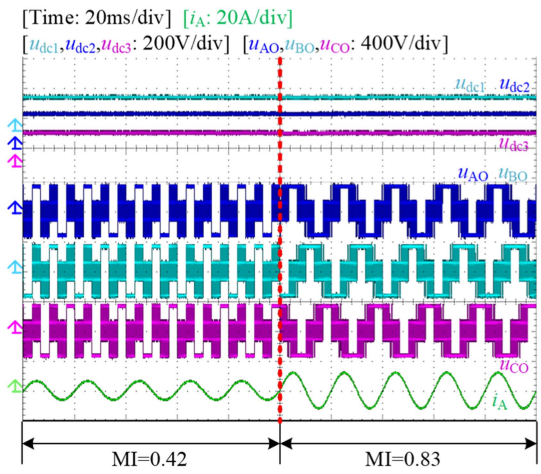

Fig. 15. Dynamic waveforms of the proposed 4L-DPWM scheme when MI is step-changed from 0.42 to 0.83.

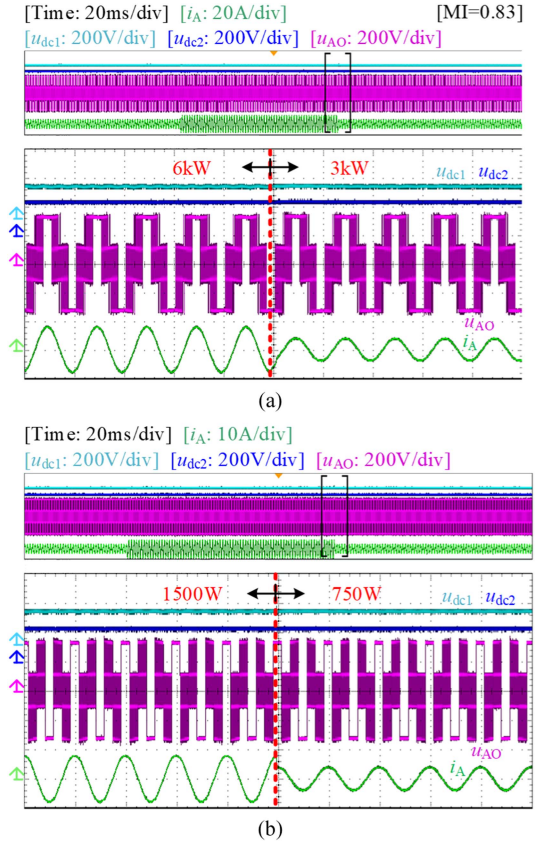

Fig. 16. Dynamic waveforms of the proposed 4L-DPWM scheme with step-changed output power. (a) MI = 0.83. (b) MI = 0.42.

A. *Verification of the Proposed 4L-DPWM Scheme*

Steady-state waveforms of the proposed 4L-DPWM scheme with MI of 0.83 and 0.42 are presented in Fig. 12. $u_{\mathrm{dc1}}, u_{\mathrm{dc2}}, u_{\mathrm{dc3}}$ denote the voltages across the dc-link capacitors C_{d1}, C_{d2}, and C_{d3}, respectively. u_{XO} represents the bridge-leg voltage of phase X ($X = A$, B, or C) between terminal X and terminal O, as shown in Fig. 1. i_A is the alternating output current of phase A. Fig. 12 indicates that the proposed 4L-DPWM scheme can balance the dc-link capacitor voltage with different modulation indices. u_{dc2}, the middle capacitor voltage, is always equal to $U_{\mathrm{dc}}/3$. u_{dc1} and u_{dc3} also achieve dynamic balance over a fundamental period. Besides, it can be seen that the bridge-leg voltage is clamped near the peak value point of the phase voltage with different modulation indices, indicating that the switching state of one phase is clamped and switching times are reduced as well.

Steady-state waveforms by using the proposed 4L-DPWM with lower fundamental frequencies are shown in Fig. 13. The MI is set at 0.83, and the output power is 6 kW. The charging and discharging time for the upper and lower capacitors increases with lower fundamental frequencies. Thus, since the dc-link capacitance is not changed, the oscillation of the upper and lower capacitor voltages increases. But they can also achieve dynamic balance within a fundamental period. Since u_{dc2} is actively balanced by using (5) within a switching period, it will not be affected by the fundamental frequencies.

Steady-state waveforms under the nonunit PF are shown in Fig. 14. φ_{PF} represents the PF angle by which the output voltage leads the output current. The three- phase loads are set at $20+j15\ \Omega$ with a PF of about 0.8. It can be seen that, the proposed 4L-DPWM scheme can still achieve dc-link capacitor balance with nonunit PFs.

Fig. 15 shows the dynamic waveforms of the proposed 4L-DPWM scheme when the MI is step-changed from 0.42 to 0.83. From Fig. 15, it can be seen that the proposed 4L-DPWM

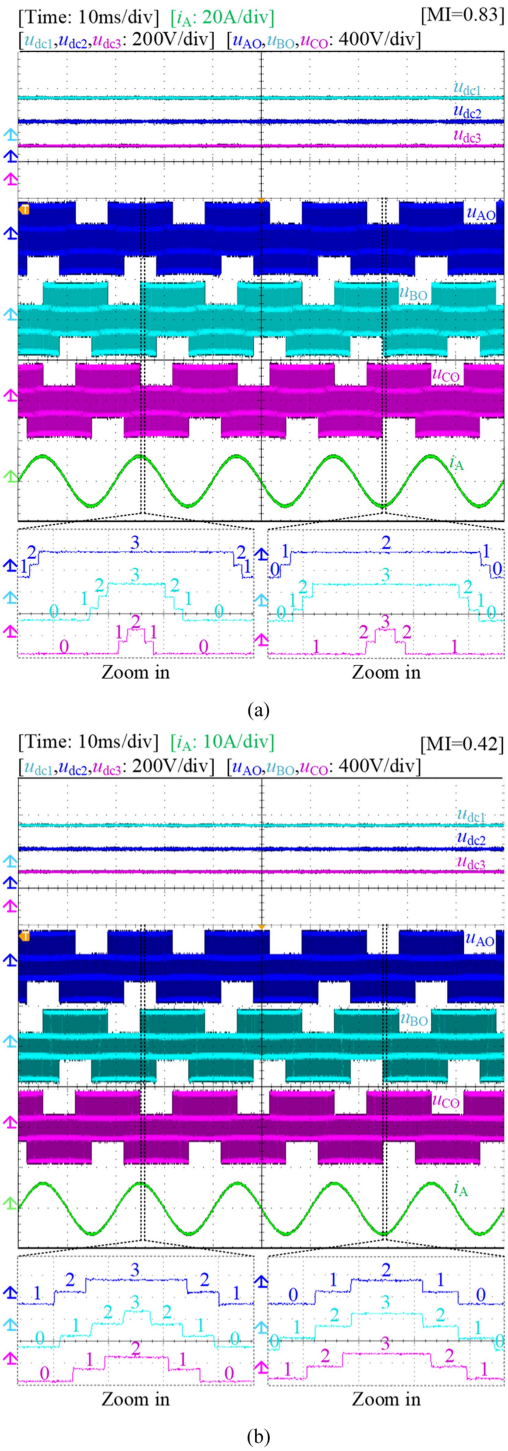

Fig. 17. Steady-state waveforms of the VVPWM scheme. (a) MI = 0.83. (b) MI = 0.42.

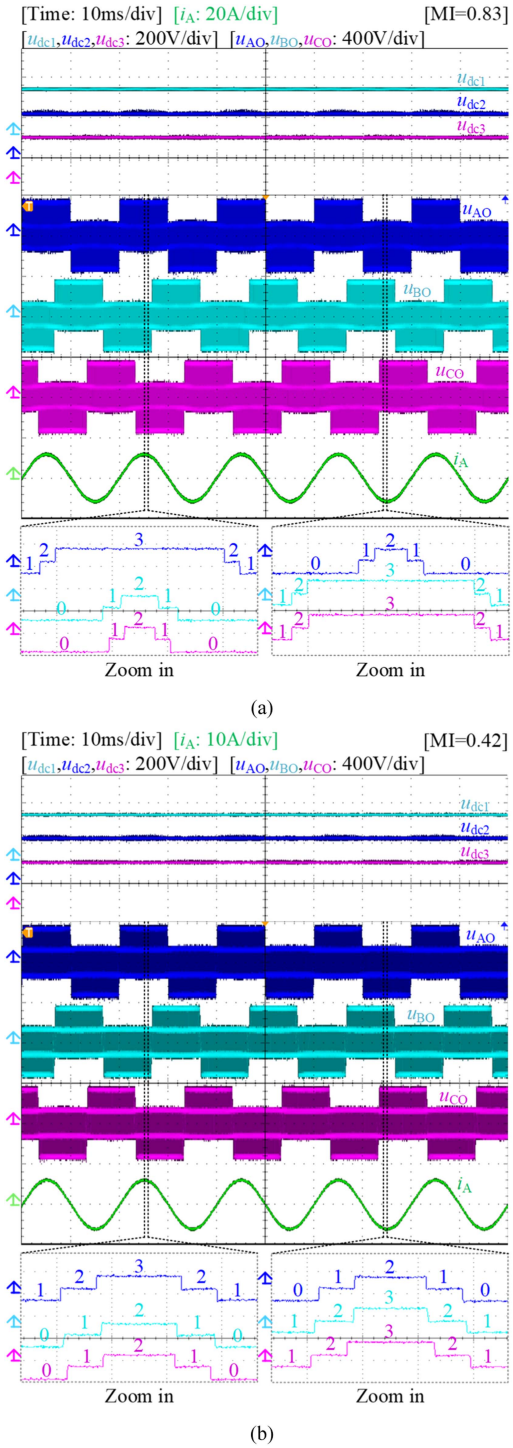

Fig. 18. Steady-state waveforms of the COPWM scheme. (a) MI = 0.83. (b) MI = 0.42.

does not generate severe alternating output current distortion under step-changed MI conditions, and the dc-link capacitor voltages are well balanced. Dynamic waveforms of the proposed 4L-DPWM scheme with step-changed output power are presented in Fig. 16. It indicates that the proposed 4L-DPWM still exhibits a good balance of dc-link capacitor voltage with the output power is step-changed.

B. Comparison Analysis

The proposed 4L-DPWM scheme is compared with the VVPWM scheme proposed in [14] and the COPWM scheme proposed in [18] and [19]. Steady-state waveforms of the VVPWM scheme and COPWM are illustrated in Figs. 17 and 18, respectively. It can be seen that these two schemes

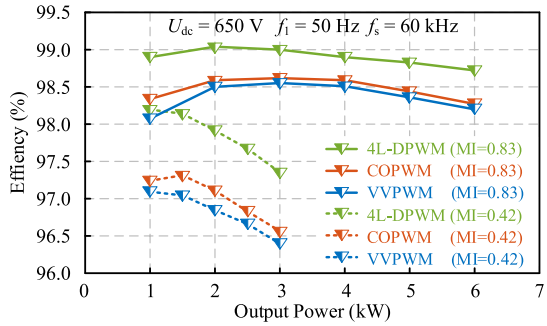

Fig. 19. Measured efficiencies under different output power and MIs by using different schemes.

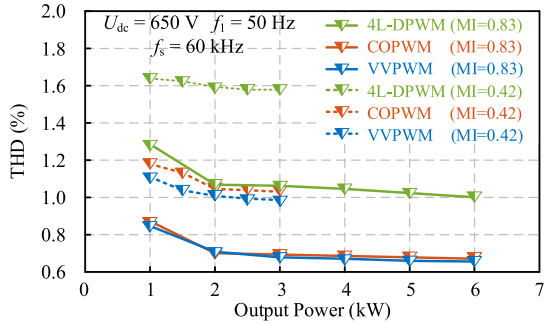

Fig. 20. Measured phase current THDs under different output power and MIs by using different schemes.

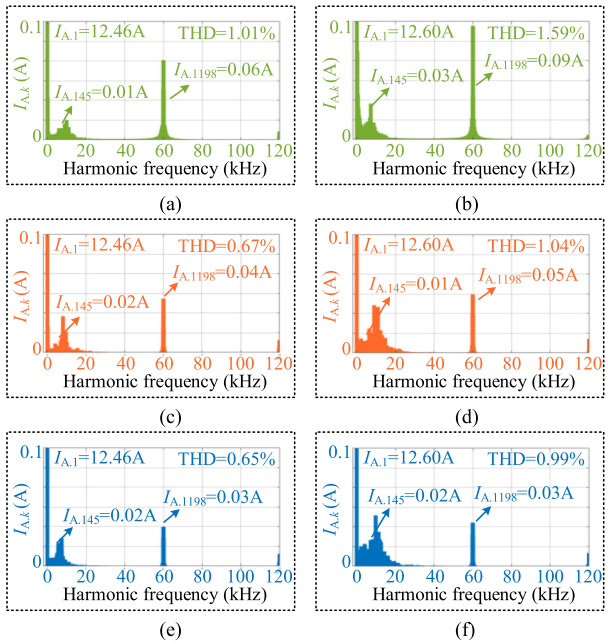

Fig. 21. FFT analysis of alternating output current with different schemes. (a) 4L-DPWM (MI = 0.83, P_o = 6 kW). (b) 4L-DPWM (MI = 0.42, P_o = 3 kW). (c) COPWM (MI = 0.83, P_o = 6 kW). (d) COPWM (MI = 0.42, P_o = 3 kW). (e) VVPWM (MI = 0.83, P_o = 6 kW). (f) VVPWM (MI = 0.42, P_o = 3 kW).

can also balance dc-link capacitor voltage, but employ more switching times. In Fig. 17, all phase-legs operate at switching frequency, with one phase-leg using four voltage levels to synthesize the reference vector. In Fig. 18, all three phase-legs have three voltage levels, resulting in more switching times as well. Thus, these existing modulation schemes could generate higher switching loss than the proposed 4L-DPWM scheme.

Fig. 19 shows the measured efficiencies under different output power and MIs by using different schemes. It can be seen that, by using the proposed 4L-DPWM scheme, the efficiency performance is improved over the full operating power range. Compared with the VVPWM scheme, the proposed 4L-DPWM achieves an efficiency improvement of over 0.5% at various output power. Compared with the COPWM scheme, the proposed 4L-DPWM scheme improves efficiency by approximately 0.4% at the rated power.

Fig. 20 shows the measured current THDs under different output power and MIs. From the FFT analysis and the curves of current THD, it can be seen that, since the switching times are reduced, the THDs of the proposed 4L-DPWM scheme are slightly higher than those of the VVPWM scheme and the COPWM scheme. However, the THDs of the proposed 4L-DPWM are still lower than 3%, featuring good harmonic performance. Fig. 21 shows spectrums of alternating output current by using different modulation schemes with a three-phase 24 Ω load resistance. The spectrums are calculated by the FFT tools in MATLAB, and the current data is recorded by the oscilloscope MDO-3024. $I_{A.k}$ represents the amplitude of k-th harmonics of the phase-A output current. It can be seen that, the proposed 4L-DPWM increases the harmonics near the switching frequency, leading to higher current THD.

Therefore, the proposed 4L-DPWM achieves both the self-balance of dc-link capacitor voltage and higher efficiency, compared with existing schemes. Satisfied harmonics performance is also achieved.

IV. Conclusion

In this article, a 4L-DPWM scheme is proposed to achieve high efficiency and self-balance dc-link capacitor voltage simultaneously. Analysis and experimental results demonstrate the following advantages.

1) The proposed 4L-DPWM scheme achieves the self-balance of dc-link capacitor voltages by considering the voltage balancing equations while calculating the vector dwelling time. Besides, the switching time is reduced by 1/3 by clamping the phase with the highest current under the unity PF during each switching period, leading to high efficiencies.
2) Compared with existing schemes that balance dc-link capacitor voltages, the proposed 4L-DPWM scheme significantly reduces switching loss by about 50%. Thus, compared with the VVPWM scheme proposed in [14], the proposed 4L-DPWM scheme achieves an efficiency improvement of over 0.5% at various output power. Compared with the COPWM scheme proposed in [18], the proposed 4L-DPWM scheme improves efficiency by nearly 0.4% at the rated power.

Therefore, the proposed 4L-DPWM scheme can be utilized by high-switching-frequency three-phase four-level inverters.

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