Direct Synthesis Based Centralized PI Controller Design for Single Inductor Multioutput (SIMO) Buck Converter to Alleviate Cross Regulation

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***Abstract*—The main control challenge in the single inductor multioutput buck converter (SIMOBC) is the cross-regulation in the output voltages. To alleviate this cross-regulation, a centralized frequency domain PI controller design methodology based on direct synthesis for SIMOBC is presented. In this method, the controller parameter is evaluated by comparing the closed loop transfer function (CLTF) matrix of the SIMOBC model with the desired CLTF matrix. The desired CLTF is considered as a diagonal matrix to achieve no cross-regulation in the output voltages. The diagonal element of the desired CLTF matrix is selected to have the desired closed-loop dynamics of the individual output of the SIMOBC. The controller is further approximated as a PI controller by frequency response matching at low frequency point. To validate the proposal, two cases are considered, i.e., single inductor dual output and single inductor three output buck converter. The performance of the proposed scheme is investigated using both MATLAB simulations and hardware experiments involving both the converters. Results verify the effectiveness of the proposed control scheme.**

***Index Terms*—Direct synthesis scheme, PI controller, single inductor multioutput converter, state-space small signal modeling.**

I. Introduction

NOWADAYS, the necessity of multiport dc supply with different voltage levels is increasing. It is broadly used in battery-operated devices such as personal digital assistants, mobile phones, computers, electric vehicles, hybrid electric vehicles, and bias supplies [1], [2], [3]. The single-inductor multiple-output (SIMO) converters are attracting the researchers to fulfil the requirement of a multiport dc source as it is smaller in size and cost-effective. However, the main issues with the SIMO converters are ripple in output voltage, cross-regulation in different loops and power conversion efficiency [4], [5], [6], [7], [8], [9], [10], [11], [12]. The single inductor multioutput buck converter (SIMOBC) is a multi-input multioutput (MIMO) system with n inputs (duty cycle of n switches) and n outputs (output voltages across capacitors). The main control issue in the MIMO system is the interacting nature of different loops.

Single inductor dual output buck converter (SIDOBC) is a class of MIMO converters [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29] and several control schemes have been presented in the literature to minimize the cross-regulation issue. The study reported in [23] has controlled SIDOBC using nonlinear gain compensation technique in the digital control domain. The effect of cross regulation still persists in the differential mode loop, which is further improved in [9] using digital predictive control technique. State-space averaging technique-based model of SIDOBC has been utilized in [21] and compensators have been designed in continuous time domain to achieve desired loop gains with specified phase-margin and bandwidth requirement. The performance of SIDOBC is further improved in [24] with the use of an inductor current ripple based model and cross-derivative state feedback controller. Their method involves the pole-zero cancellation between self-loop and cross-loop, which makes the overall system sensitive to input voltage variation as well as components of converter. The robust performance of SIDOBC is further improved in [19], where a centralized controller is designed with the concept of open-loop shaping of the MIMO system by convex minimization of the second norm of error between the desired and actual open loop transfer function matrix. They have considered a number of operating point and circuit parameter variations along with input voltage to show the desired output voltages. However, the topology configuration of their converter poses a limitation that the output voltage of one channel is always less than the other. This shortcoming is eliminated in [25], where they have used an additional switch in the SIDOBC and the output voltage is regulated with the model predictive control technique.

Qian et al. [28] proposed a control strategy for three port dc–dc converter, which is based on decoupling network to manage cross-coupled control loops. In [26], a digital controller was developed for the single inductor MIMO converter with different voltage sources based on model predictive control, power

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sharing, and time-multiplexing to reduce the cross regulation. Here, the total power from multiple sources is shared to the multiple loads through the single inductor based on priority decided by the time-multiplex controller. Wang et al. [17] explored the effect of SIDOBC circuit parameters on the stability by developing a discrete iterative model in peak control mode based on inductor currents border lines. Improved performance in terms of cross-regulation suppression and stability margin has been obtained by Wang et al. [27], where they have used capacitor current ripple control technique in place of inductor current as capacitor current reflects the variation in load more quickly than inductor peak current. However, capacitor ripple current based technique has limited stable operating load range due to incomplete operation state and single switching path. This is eliminated in [10] with the use of capacitor ripple voltage control in addition to the capacitor ripple current control. In [29], a dead-beat based control technique is presented, which is capable of achieving output voltage regulation and also inductor current regulation. Following conclusions can be drawn from the aforementioned discussion:

1) Existing methods to reduce the cross regulation in SIMOBCs are complex.
2) Existing literature primarily focuses on SIDOBC while the extension to multioutput converter has not received the attention that it deserves.
3) Literature on centralized controller design for SIMOBC is scarce.
4) There is need for designing unified control strategy which suites MIMO converters of different orders.

In this regard, a centralized PI controller design (without decoupling network) based on direct synthesis approach (in frequency domain) is presented for different types of SIMOBCs. In the direct synthesis approach, the closed-loop transfer function matrix (output voltage to reference voltage) is equated with the desired closed loop transfer function matrix [30]. The obtained controller expression is further approximated to PI controller by frequency response matching at low frequency point. To eliminate the cross regulation in multioutput, the desired transfer function matrix is selected as a diagonal matrix, which avoids unnecessary interaction between various outputs thereby enhancing the performance of this design. The proposed method is experimentally validated using two benchmark MIMO converters adopted from literature [i.e., SIDOBC and single inductor three output buck converter (SITOBC)]. The salient features of this work are outlined as follows:

1) Unified control scheme, which is applicable for dc–dc MIMO converters of different order.
2) Centralized control scheme, which does not require a decoupling mechanism for the control of MIMO converters. This results in enhanced system performance by coordinating all inputs and outputs simultaneously thereby reducing interference and hardware redundancy.
3) The efficacy of this scheme is validated experimentally using two MIMO converters (i.e., SIDOBC and SITOBC) by considering various practical scenarios.

The rest of this article is organized as follows. Section II describes the basic operation and state-space modeling of SIMOBC. Section III represents the centralized PI controller design methodology for SIMOBC. The MATLAB simulation and hardware results of the proposed control scheme are discussed in Sections IV. Finally, Section V concludes this article.

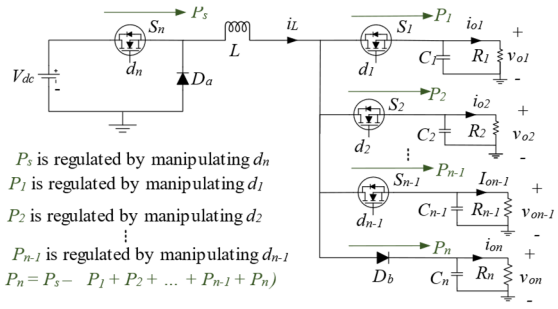

Fig. 1. Circuit diagram of SIMOBC.

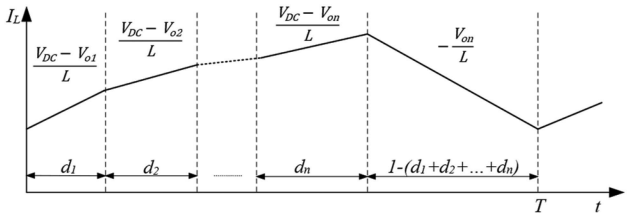

Fig. 2. Switching characteristics of SIMOBC.

II. Transfer Function Model of the SIMOBC

The circuit diagram of SIMOBC is shown in Fig. 1. A single inductor (L) is used to obtain different output voltages v_{o1}, v_{o2}, $\ldots v_{on}$ (where v_{o1}, v_{o2}, $\ldots$, $v_{on-1} < v_{on}$) from single supply voltage (V_{dc}). C_1, C_2, $\ldots$, and C_n are capacitors across the outputs, which is used to maintain the output voltages constant. The control objective is to regulate the output voltages v_{o1}, v_{o2}, $\ldots$ v_{on} to a prespecified reference voltage V_{o1_ref}, V_{o2_ref}, $\ldots V_{on\_ref}$, respectively. These output voltages can be regulated by the control of the duty cycles $d_1, d_2, \ldots . d_n$ for corresponding switches S_1, S_2, $\ldots .$ S_n and two diodes (D_a and D_b). The duty cycle $d_{\rm n}$ regulates the input power (P_s) by controlling the inductor current whereas the output power (P_1) is controlled by duty cycle d_1, output power (P_2) is controlled by duty cycle d_2, $\ldots$ and output power ($P_{\rm n}$) is controlled by duty cycle $d_{\rm n}$, which ultimately controls the output voltages. The loads of the converter are R_1, R_2, $\ldots .$ R_n. The switching characteristics of inductor current with respect duty cycle of corresponding switches is shown in Fig. 2. The positive slop of inductor current shows the charging and negative slop indicates the discharging inductor current. The characteristics shown in Fig. 2 further used to derive the transfer function of SIMOBC using state-space averaging technique.

The averaged state-space model of SIMOBC [14], [27] in obtained as

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \tag{1}$$

where unnumbered equation shown at the bottom of next pagethe

steady state dynamics of SIMOBC, i.e., $V_{oi}(s)/V_{dc}(s)$ (where i is output port number), can be determined by solving the equations obtained from (1) by putting matrices A, B, and C and assuming all switches and diodes are ideal and neglecting the perturbation in state and control variables. The input–output relation of the SIMOBC is obtained through the gain transfer function matrix as given by

$$\begin{bmatrix} v_{o1} \\ v_{o2} \\ \vdots \\ v_{on} \end{bmatrix} = \begin{bmatrix} G_{11}(s) & G_{12}(s) & \dots & G_{1n}(s) \\ G_{21}(s) & G_{22}(s) & \dots & G_{2n}(s) \\ \vdots & \vdots & \ddots & \vdots \\ G_{n1}(s) & G_{n2}(s) & \dots & G_{nn}(s) \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ d_n \end{bmatrix} \quad (2)$$

where

$$\begin{bmatrix} G_{11}(s) & G_{12}(s) & \dots & G_{1n}(s) \\ G_{21}(s) & G_{22}(s) & \dots & G_{2n}(s) \\ \vdots & \vdots & \ddots & \vdots \\ G_{n1}(s) & G_{n2}(s) & \dots & G_{nn}(s) \end{bmatrix} = G(s).$$

$G(s)$ is the open loop transfer function matrix of SIMOBC, which is derived from the $[sI - A]^{-1}B$, where I is the identity matrix. It is evident from (2) that the outputs of SIMOBC are depending on the duty cycles (d_1, d_2 … and d_n), which make the control of outputs very difficult due to cross coupling.

III. Controller Design Methodology

In this work, centralized controllers have been considered for the control of SIMOBC. This scheme does not have the requirements of a decoupler matrix and it results in a simplified control structure [17], [27]. The centralized control scheme for the SIMOBC is shown in Fig. 3. Here, $C(s)$ is controller matrix and $G(s)$ is the transfer function matrix of the SIMOBC. The

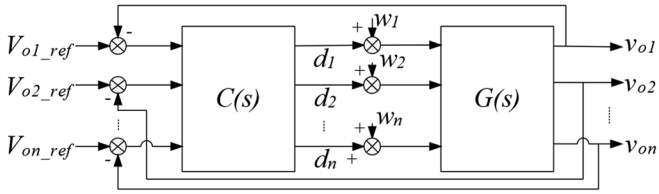

Fig. 3. Block diagram of SIMO system with controller.

controller manipulates the duty cycles (d_1,d_2 … and d_n) to maintain output voltages (v_{o1}, v_{o2} … and v_{on}) of the system at reference voltages (V_{o1_ref}, V_{o2_ref} … and V_{on_ref}). w_1, w_2 … and w_n represents the disturbances (change in supply voltage, load and duty cycle) in the control loop.

The centralized PI controller $C(s)$ has been considered for the voltage regulation of SIMOBC as

$$C(s) = \begin{bmatrix} C_{11}(s) & C_{12}(s) & \dots & C_{1n}(s) \\ C_{21}(s) & C_{22}(s) & \dots & C_{2n}(s) \\ \vdots & \vdots & \ddots & \vdots \\ C_{n1}(s) & C_{n2}(s) & \dots & C_{nn}(s) \end{bmatrix}. \quad (3)$$

From Fig. 2, the closed-loop transfer function ($G_{CL}(s)$) of the system without disturbances can be written as

$$G_{CL}(s) = \frac{v_o}{v_{ref}} = (I + G(s)C(s))^{-1} G(s)C(s). \quad (4)$$

To minimize the cross-coupling, the controller $C(s)$ should be designed in such a way as to reduce the interaction between *i*th input and to *k*th output. This is achieved by selecting a centralized controller, which minimizes the OFF-diagonal element in (4) to zero. Here, the controller is designed through a direct synthesis

$$x = [i_L \quad v_{c1} \quad v_{c2} \quad \dots \quad v_{cn}]^T$$

$$u = [cv_{dc} \quad d_1 \quad d_2 \quad \dots \quad d_n]^T$$

$$y = [v_{o1} \quad v_{o2} \quad \dots \quad v_{on}]^T$$

$$A = \begin{bmatrix} 0 & \frac{-d_2}{L} & \frac{-d_2}{L} & & \frac{-d_{n-1}}{L} & \frac{-(1-d_1-d_2\dots-d_{n-1})}{L} \\ \frac{d_1}{C_1} & -\frac{1}{R_1C_1} & 0 & \cdots & 0 & 0 \\ \frac{d_2}{C_2} & 0 & -\frac{1}{R_2C_2} & & 0 & 0 \\ & \vdots & & \ddots & \vdots & \\ \frac{d_{n-1}}{C_{n-1}} & 0 & 0 & & -\frac{1}{R_{n-1}C_{n-1}} & 0 \\ \frac{1-d_1-d_2\dots-d_{n-1}}{C_n} & 0 & 0 & \cdots & 0 & -\frac{1}{R_nC_n} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{d_1+d_2\dots+d_n}{L} & \frac{V_{dc}+V_{on}-V_{o1}}{L} & \frac{V_{dc}+V_{on}-V_{o2}}{L} & & \frac{V_{dc}+V_{on}-V_{on-1}}{L} & \frac{V_{dc}}{L} \\ 0 & \frac{I_L}{C_1} & 0 & \cdots & 0 & 0 \\ 0 & 0 & \frac{I_L}{C_2} & & 0 & 0 \\ & \vdots & & \ddots & \vdots & \\ 0 & 0 & 0 & & \frac{I_L}{C_{n-1}} & 0 \\ 0 & \frac{-I_L}{C_n} & \frac{-I_L}{C_n} & \cdots & \frac{-I_L}{C_n} & \frac{-I_L}{C_n} \end{bmatrix}$$

$$C = [0 \quad 1 \quad 1 \quad \dots \quad 1].$$

(DS) scheme. In the DS scheme, the desired closed loop dynamics are decided first afterwards the controller is derived, which gives the desired dynamics. The desired closed-loop transfer function matrix (M_{des}) with OFF-diagonal elements zero has been considered for the SIMOBC as

$$M_{des}(s) = \begin{bmatrix} m_{11}(s) & m_{12}(s) & \dots & m_{1n}(s) \\ m_{21}(s) & m_{22}(s) & \dots & m_{2n}(s) \\ \vdots & \vdots & \ddots & \vdots \\ m_{n1}(s) & m_{n2}(s) & \dots & m_{nn}(s) \end{bmatrix} \tag{5}$$

where

$$m_{ii}(s) = \frac{v_{o_i}(s)}{v_{ref_i}(s)} = \frac{1}{(\tau_{ii}s+1)^n}\ ;\ m_{ki} = 0$$

subscript "ii" represents the equal row and column.

The $\tau_{ii}(s)$ is the desired time constant of the ith forward path and n is the order of the reference model. Controllers for the SIMOBC are designed in such a way to have closed-loop system dynamics of (4) and the desired transfer function in (5) should be same and it can be written as

$$M_{des}(s) \cong (I + G(s)C(s))^{-1} G(s)C(s). \tag{6}$$

In (6), $M_{des}(s)$ and $G(s)$ are the matrices of order n×n and matrix of order n×n can be written as

$$C(s) = G^{-1}(s)M_{des}(s)(I - M_{des}(s))^{-1}. \tag{7}$$

To obtain the elements of controller *C(s)* in (7), the inverse of $G(s)$ and $(I - M_{des}(s))$ is required and it yields a complex expression, which necessarily not be in physically realizable or simple PI controller form. A suitable approximation technique is required to obtain the controller in PI controller form as

$$C_{PI}(s) = K_P + \frac{K_I}{s} \tag{8}$$

where K_P is a proportional gain matrix and K_I is an integral gain matrix. Here, the controller $C_{PI}(s)$ is obtained from $C(s)$ by applying an approximate frequency response matching technique reported in [30] and [31]. The approximation technique is based on following concept.

Suppose a real valued function $\varphi(x)$ is approximated to another real valued function $\varphi_{apprx.}(x)$. Consider that the $\varphi^{(i)}(x)$, $i \in [1, m]$ are the derivatives of the function $\varphi(x)$ in the region the point $x = x_0$. Let the function $\varphi(x)$ is having given distinct value for the real numbers x_i; where $x_i = x_0 + pi$, with $p > 0$. Considering the notation of calculus of divided difference $\varphi[x_0] = \varphi(x_0)$ we may define divided differences of arguments 2 to $m+1$

$$\begin{aligned} \varphi[x_0x_1] &= (\varphi[x_0] - \varphi[x_1])/(x_0 - x_1) \\ \varphi[x_0x_1x_2] &= (\varphi[x_0x_1] - \varphi[x_1x_2])/(x_0 - x_2) \\ &\vdots \\ .\varphi[x_0x_1 \dots .x_k] &= (\varphi[x_0x_1 \dots x_{k-1}] \\ &\quad - \varphi[x_1x_2 \dots .x_k])/(x_0 - x_k) \\ &\quad k \in [1, n]. \end{aligned} \tag{9}$$

Assume that the maximum and minimum value of $x_0, x_1, \dots .x_m$ are bounded by the interval (a, b), function $\varphi(x)$, and its $(n-1)$ derivatives are continuous and finite and also there exist $\varphi^n(x)$. It can be easily shown that [30]

$$\varphi[x_0x_1x_2 \dots x_m] = h^{-m} \sum_{i=0}^{m} \frac{(-1)^{m-i}}{i!\,(k-i)!} \varphi(x_i) = \frac{1}{m!}\varphi^{(m)}(\varepsilon) \tag{10}$$

where ε lies in the interval $x_0 \le \varepsilon \le x_0 + mh$.

Now consider $\emptyset(x)$ another function with its derivative $\emptyset^{(i)}(x)$ around a point $x = x_0$ with

$$\phi(x_i) = \varphi(x_i), \qquad i \in [0, m]. \tag{11}$$

From (11), $\emptyset^{(m)}(\varepsilon) = \varphi^{(m)}(\xi)$ where ε lies in the interval $x_0 \le \varepsilon \le x_0 + mh$. For very small positive number h,

$$\varphi^{(i)}(x) = \phi^{(i)}(x), \qquad i \in [0, m]. \tag{12}$$

So, using (11) for a small value of h, another function $\emptyset(x)$ for a real valued function $\varphi(x)$ can be selected always which satisfy the approximate relation in (12). Thus, matching two differential functions at very small value will yield an approximate linear function. The above concept is used in the controller design section for approximation.

To obtain the PI controllers for the SIMOBC, the two relations in (7) and (8) are equated, which is mathematically written as

$$C(s)|_{s=j\omega} \cong C_{PI}(s)|_{s=j\omega} \tag{13}$$

Or

$$C_r(\omega) + jC_i(\omega) \cong C_{r,pi}(\omega) + jC_{i,pi}(\omega) \tag{14}$$

where, $C(s)|_{s=j\omega} = C_r(\omega) + jC_i(\omega)$ and $C_{PI}(s)|_{s=j\omega} = C_{r,pi}(\omega) + jC_{i,pi}(\omega)$.

Equation (14) yields two relations by equating real and imaginary parts as

$$C_r(\omega) = C_{r,pi}(\omega) \text{ and } C_i(\omega) = C_{i,pi}(\omega). \tag{15}$$

The Taylor series expansions around $\omega = 0$ in (15) are further matched and it gives following relations:

$$\frac{d^r}{d\omega^r} C_{r,pi}(\omega)|_{\omega=0} = \frac{d^r}{d\omega^r} C_r(\omega)|_{\omega=0}$$

and

$$\begin{aligned} &\frac{d^r}{d\omega^r} C_{i,pi}(\omega)|_{\omega=0} = \frac{d^r}{d\omega^r} C_i(\omega)|_{\omega=0} \\ &\text{where}, r \in [0, m-1]. \end{aligned} \tag{16}$$

Using (9)–(12), the differential relation (16) will be approximated to linear relation as given by

$$C_{r,pi}(\omega)|_{\omega=\omega_r} = C_r(\omega)|_{\omega=\omega_r}\ ;\ r \in [0, m-1]$$

and

$$C_{i,pi}(\omega)|_{\omega=\omega_r} = C_i(\omega)|_{\omega=\omega_r}\ ;\ r \in [0, m-1]. \tag{17}$$

The low frequency point for $\omega = \omega_o$ is selected as 1% of the bandwidth of the diagonal element of the desired closed-loop transfer function matrix. With one frequency point (17) will give two equations by separating the real and imaginary part and its

TABLE I
CIRCUIT PARAMETER OF SIMOBC

Description	Symbol	SIDOBC	SITOBC
Dc voltage source	V_{dc}	12 V	12 V
Output voltages	V_{o1} V_{o2} V_{o3}	5 V, 8 V, --	5 V, 6 V, 8 V
Inductor	L	1 mH	1 mH
Capacitor	C_1 C_2 C_3	100 µF 100 µF --	100 µF 100 µF 220 µF
Output resisters	R_1, R_2 R_3	10 Ω 15 Ω --	10 Ω 15 Ω 20 Ω
Switching frequency	f_{sw}	50 kHz	50 kHz

solution gives the parameter of the individual PI controller. Thus, the controller parameter is obtained by following the steps given below:

- *Step-1:* Develop the closed-loop transfer-function matrix of the SIMOBC by state-space averaging technique (1), (2).
- *Step-2:* Select the desired CLTF matrix with the desired time constants as the diagonal matrix (5).
- *Step-3:* Determine the controller matrix ($C(s)$) as in (7).
- *Step-4:* Approximate the controller determined in step 3 as a PI controller at low frequency (i.e., $s = j\omega_o$) which follows (17).
- *Step-5:* Check the performance of the controller developed in step 4 for SIMOBC in simulation.
- *Step-6:* If performance in step 5 is not satisfactory, then repeat steps 2–5 with different desired time constants until results are satisfactory.
- *Step-7:* The controller parameter for which simulation results are satisfactory will be selected.

IV. RESULTS AND DISCUSSION

This section evaluates the steady state and transient performances of suggested controller design strategy using benchmark SIMOBC circuits (SIDOBC and SITOBC). Additionally, the robust stability under variations in the circuit parameters is analyzed. Practical feasibility of this design is studied through various case studies using SIDOBC and SITOBC circuit parameters given in Table I. The suggested scheme is further compared with that of [28] in terms of transient behavior (rise, time, and settling time) and steady state dynamics [Figure of merit (FOM)] for evaluating the cross-regulation.

FOM is used to measure the cross-regulation effect in SIMO converters. It serves as a standard in comparing different control strategies and circuit topologies in terms of their ability to minimize cross-regulation. It provides a clear numerical representation of how well a particular design maintains independent control over multiple outputs. FOM (self and cross) [14], [29]

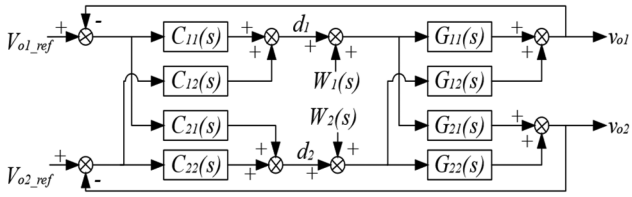

Fig. 4. Block diagram of control system for SIDOBC converter.

is expressed as follows:

$$\text{FOM (self)} = \frac{\Delta V_i}{V_i} * \frac{I_i}{\Delta I_i}$$
$$\text{FOM (cross)} = \frac{\Delta V_j}{V_j} * \frac{I_i}{\Delta I_i} \tag{18}$$

where ΔV_i and ΔV_j are the average deviations in output voltages, ΔI_i is the change in output current applied in channel i and j represents the other channel.

A. Single Inductor Dual Output Buck Converter

The schematic block diagram of the centralized control scheme for SIDOBC is shown in Fig. 4. In a SIDOBC, the system dynamics are governed by three state variables (i_L, v_{o1}, and v_{o2}) along with two independent control inputs (d_1 and d_2). Effective regulation is achieved by strategically utilizing feedback from both direct and cross-coupled outputs to control the system. In a SIDOBC, a sudden load variation in one of the outputs (e.g., v_{o1}) prompts the corresponding output capacitor to either supply or absorb current to maintain voltage stability. This causes a shift in the duty cycle of the switching element associated with that output. Consequently, the second output's capacitor must compensate for this adjustment, leading to fluctuations in v_{o2}, thereby highlighting the cross-regulation effect. This ensures that load variations in one output are dynamically counteracted by appropriate adjustments in the control inputs, significantly reducing cross-regulation and improving overall system stability.

To facilitate controller design using the proposed method, transfer function of SIDOBC ($G(s)$) using (2) is derived as

$$G_{11}(s) = \frac{10333s^2 + 7.946 \times 10^7 s + 1.017 \times 10^{11}}{s^3 + 1667s^2 + 5.672 \times 10^6 s + 4.225 \times 10^9}$$
$$G_{12}(s) = \frac{-10333s^2 + 6.708 \times 10^7 s + 2.742 \times 10^{10}}{s^3 + 1667s^2 + 5.667 \times 10^6 s + 4.225 \times 10^9}$$
$$G_{21}(s) = \frac{5.806 \times 10^7 s + 3.87 \times 10^{10}}{s^3 + 1667s^2 + 5.672 \times 10^6 s + 4.225 \times 10^9}$$
$$G_{22}(s) = \frac{6.194 \times 10^7 \text{s} + 6.194 \times 10^{10}}{s^3 + 1667s^2 + 5.672 \times 10^6 s + 4.225 \times 10^9}. \tag{19}$$

The desired transfer function matrix given in (5) is selected with $\tau_{11} = 0.0008 - 0.01\ s$ and $\tau_{22} = 0.0008 - 0.01\ s$. As the order of SIDOBC is 3, $m = 3$ is chosen in (5). By considering the frequency point for matching as $\omega = 0.001$ *rad/s* and following the controller design step discussed in the previous section,

TABLE II
CONTROLLER PARAMETER AND TRANSIENT PERFORMANCE PARAMETERS FOR SIDOBC WITH VARIOUS DESIRED TIME CONSTANTS

S. N.	τ_1	τ_2	$C_{11}(s)$		$C_{12}(s)$		$C_{21}(s)$		$C_{22}(s)$		V_{o1}			V_{o2}		
			K_{P11}	K_{I11}	K_{P12}	K_{I12}	K_{P21}	K_{I21}	K_{P22}	K_{I22}	t_r (ms)	t_s (ms)	$\%M_p$	t_r (ms)	t_s (ms)	$\%M_p$
1.	0.0008	0.0008	0.004	20.81	−0.015	−9.213	−0.009	−13.007	−6.4e-4	34.18	4	14	2.8	0.76	10	1.37
2.	0.0005	0.0005	0.016	33.298	−0.028	−14.741	−0.020	−20.811	0.0153	54.688	2.1	19	3.4	0.7	10	1.06
3.	0.0005	0.001	0.016	33.298	−0.010	−7.37	−0.020	−20.811	−0.0059	27.344	1.9	20	7.4	0.78	15	1.87
4.	0.001	0.001	5e-7	16.649	−0.010	−7.37	−0.005	−10.405	−0.0059	27.344	4.8	20	2.4	2.23	20	1.5
5.	0.001	0.0005	5e-7	16.649	−0.028	−14.741	−0.005	−10.405	0.0153	54.688	5.3	20	1.2	0.42	10	1
6.	0.003	0.003	−0.011	5.55	0.001	−2.45	0.005	−3.468	−0.02	9.114	14.6	55	0.8	6.4	7	2.9
7.	0.005	0.001	−0.013	3.329	−0.010	−7.37	0.007	−2.081	−0.0059	27.344	40	60	0	3.8	20	0.62
8.	0.005	0.005	−0.013	3.329	0.0037	−1.474	0.007	−2.081	−0.023	5.468	25.85	70	0.6	10	60	1.75
9.	0.005	0.01	−0.013	3.329	0.005	−0.737	0.007	−2.081	−0.025	2.734	27.85	120	2.4	14.7	90	2.25
10.	0.008	0.008	−0.014	2.08	0.005	−0.92	0.008	−1.3	−0.024	3.41	50	120	0.5	15.35	100	1.75
11.	0.01	0.005	−0.014	1.664	0.0037	−1.474	0.008	−1.040	−0.023	5.468	60	120	0	12.19	70	1.12
12.	0.01	0.01	−0.014	1.664	0.005	−0.737	0.008	−1.040	−0.025	2.734	60	60	0.4	20	120	1.75

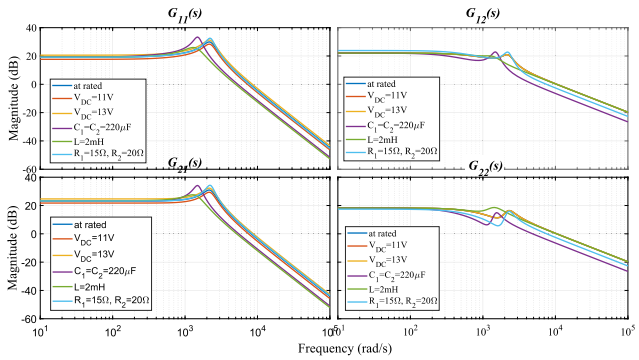

Fig. 5. Bode plot of open-loop transfer function of SIDOBC.

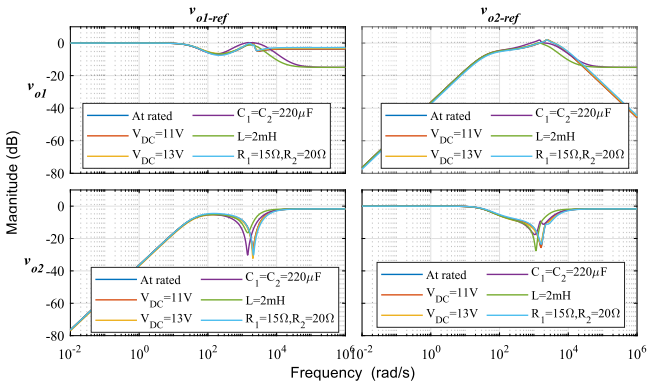

Fig. 6. Bode plot of closed-loop transfer function of SIDOBC.

the controller parameters are obtained, as given in Table II. All these controller parameters are tested on SIDOBC with a set point tracking command of $V_{o1\_ref} = 5\ V$ and $V_{o2\_ref} = 8V$. The corresponding rise time (t_r), settling time (t_s), and percent overshoot ($\%M_p$) for outputs (v_{o1} and v_{o2}) are given in Table II. From this table, it is evident that satisfactory responses are achieved for a wide range of tuning parameters. It is also seen from the table that increase in desired time constants (τ_1 and τ_2) results in slower response with lesser overshoot and vice versa.

To comprehensively evaluate the robustness of the proposed control strategy, a frequency-domain analysis of the controller is performed for $\tau_{11} = 0.005\ s$ and $\tau_{22} = 0.005\ s$. The open-loop Bode plots of the SIDOBC models for different parameter settings are shown in Fig. 5, where the significant gain in the OFF-diagonal elements at low frequencies indicates the presence of cross-regulation effects among multiple input–output pairs. To demonstrate the capability of the proposed controller design in suppressing these effects, the closed-loop Bode plot with the controller parameters (designed using nominal model) is presented in Fig. 6. The results vindicate that the desired steady-state performance is achieved while effectively minimizing cross-regulation, as evident from the reduced OFF-diagonal gains. Moreover, the controller designed based on the nominal model, maintains stable and satisfactory performance even under perturbed circuit conditions, ensuring robust control behavior across varying operating scenarios.

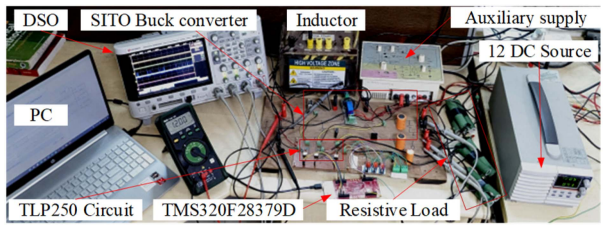

Fig. 7. Hardware set-up for SIDOBC and SITOBC.

The performance of the proposed control scheme is further validated through hardware experiments. A dedicated hardware prototype of SIDOBC is developed, as shown in Fig. 7. The output voltages of SIDOBC are sensed with a voltage sensor (LV25-P) and compared with corresponding reference commands. The controller manipulates the duty cycles (d_1 and d_2) to minimize the error. Microcontroller (TMS320F28379D) is used as an interfacing element. MOSFET (IRF640) is used as a switching device and current sensor (LA55-P) is used to record the inductor current.

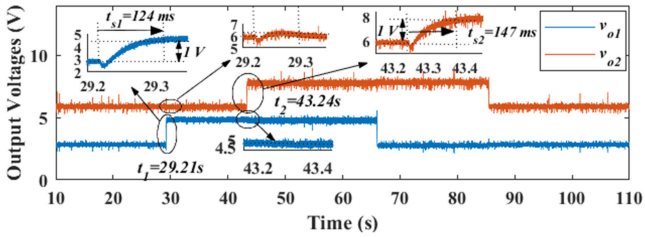

Fig. 8. Response of SIDOBC for setpoint change command.

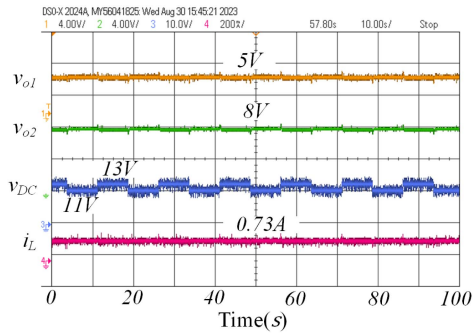

Fig. 9. Steady state response for ±1 V periodic change in supply voltage ($V_{dc} = 12\,V$).

Experiments are performed to verify the effectiveness of proposed controller for SIDOBC in following the following cases:

1) *Case-1 (Set-point response):* Step change in reference voltage (V_{o1_ref} and V_{o2_ref})
2) *Case-2:* Disturbance response due to change in supply voltage.
3) *Case-3:* Disturbance response due to change in the load (R_1 and R_2).
4) *Case-4:* Comparison of simulation and experimental responses.
5) *Case-5:* Effect of tuning parameter (i.e., τ_{11} and τ_{22}) in transient performance.
6) *Case-6:* The effect of circuit parameter change.

1) Case-1: Step Change in Reference Voltages (V_{o1_ref} and V_{o2_ref}): The SIDOBC is operated with reference command of $V_{o1\_ref} = 3\,V$ and $V_{o2\_ref} = 6\,V$. The reference command V_{o1_ref} has been changed from 3 V to 5 V and again to 3 V at time $t_1 = 29.21$ s and $t_3 = 65.98$ s, respectively. Whereas, V_{o2_ref} has been changed from 6 V to 8 V at t = 43.24 s and 8 V to 6 V at t = 85.47 s. The responses of v_{o1} and $v_{o2}$are shown in Fig. 8.

The controller manipulates the duty cycles in response to the changing reference commands and the output voltages (v_{o1} and v_{o2}) follow the corresponding reference commands (V_{o1_ref} and V_{o2_ref}Thus, better tracking performances has been observed.

2) Case-2: Effect of Supply Voltage Change on Output Voltage: To investigate the load disturbance rejection performance, a change in supply voltage is considered as a disturbance, then performance of the nominal controller is analyzed. A ±1 V periodic change in 12 V supply is intentionally introduced while operating the SIDOBC with setpoint command of $V_{o1\_ref} = 5\,V$ and $V_{o2\_ref} = 8\,V$. The corresponding responses of the output voltages along with supply voltage are shown in Figs. 9 and 10. From the response it can be seen that the output voltages track the setpoint command in the presence of periodic disturbance in supply voltages.

3) Case-3 Step Change in Load Resistance (R_1 and R_2): The proposed SIDOBC control scheme is further evaluated by changing the loading conditions. A 5 Ω resistance has been increased in R_1 at time $t_2 = 24.781$ s and in R_2 at $t_2 = 38.858$ s. the corresponding response is shown in Fig. 11. A slight deviation during transient is observed, however, converter is maintaining their reference set-point command. Thus, the load disturbance rejection is achieved successfully.

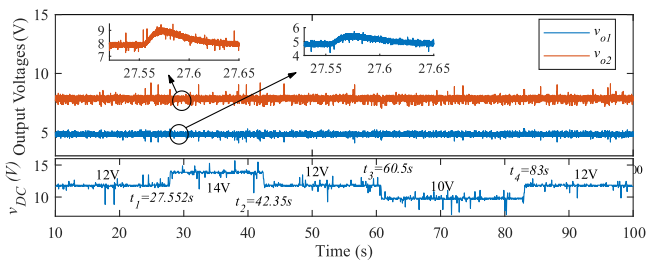

Fig. 10. Steady state output voltage response of supply voltage change.

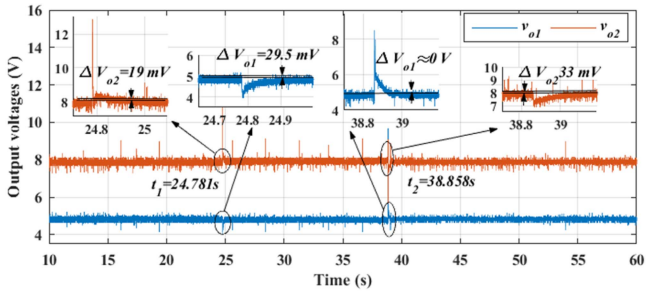

Fig. 11. Steady-state response for load resistance change.

The effectiveness of the proposed SIDOBC control scheme under varying load conditions is further analyzed by introducing step changes in the load resistances. Specifically, at $t_1 = 24.781$ s, the load resistance R_1 is increased by 5 Ω, reducing the corresponding load current I_{o1} from 500 mA to 333 mA. This results in a voltage deviation of $\Delta\, v_{o1} = 29.5\,mV$ and $\Delta\, v_{o2} = 19\,mV$. Similarly, at $t_2 = 38.858$ s, the load resistance R_2 is increased by 5 Ω, causing a reduction in $I_{o2}$from 530 mA to 400 mA, leading to a voltage deviation of $\Delta v_{o1} \approx 0\,mV$ and $\Delta\, v_{o2} = 33\,mV$. The transient responses, as illustrated in Fig. 11, indicate minor deviations during the transition phase; however, the converter effectively maintains its reference set-point. Furthermore, the cross-regulation effect is quantitatively assessed, yielding FOM (cross) = 0.007 and FOM (self) = 0.018, demonstrating excellent disturbance rejection and minimal cross-coupling interference. These results validate the robustness of the proposed control strategy in ensuring stable and precise output voltage regulation under dynamic load variations.

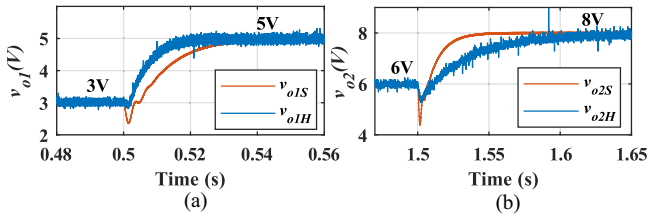

Fig. 12. Transient responses obtained from hardware and simulation with change in set-point (a) V_{o1_ref} and (b) V_{o2_ref}.

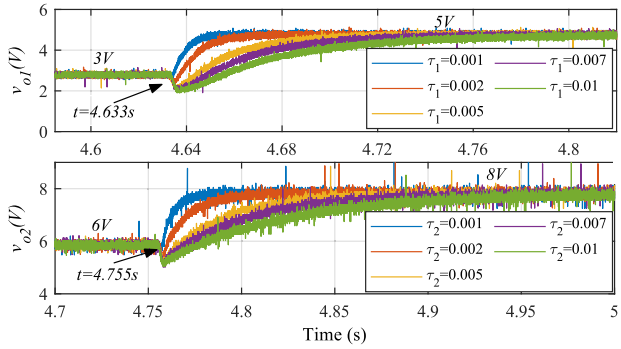

Fig. 13. Transient responses of output voltage with various desired time constants.

4) Case-4 Comparison of Simulation and Experimental Responses: Since some assumptions and approximations are taken while modeling and designing the proposed SIDOBC controller, it is required to compare the results of the simulation with the experimental results. Also, since the MATLAB simulation runs in virtual time, it will be valuable to validate the results in real time through hardware setup. The hardware and simulation results for 2 V step change in V_{o1_ref} and V_{o2_ref} at time 0.5 s and 1.5 s, respectively, are observed in output voltages (v_{o1H}, v_{o1S}, v_{o2H}, and v_{o2S}) are shown in Fig. 12. Here, the subscripts "H" and "S" represent the hardware and simulation results, respectively. It is evident from the figures that the characteristics of the hardware results perfectly match the characteristics of the simulation results. Moreover, Fig. 12 demonstrates the robustness of the proposed method in dealing with parasitic resistances.

5) Case-5 Effect of Tuning Parameter (τ_{11} and τ_{22}) in Transient Performance: The transient performance of hardware results with various desired time constants is observed in this section. In Table II, detailed information regarding the controller and transient parameters is listed corresponding to the various desired time constants using MATLAB simulation. It is observed from the table that settling time for the output of SIDOBC improves as the τ_{11} and τ_{22} is decreased. Out of these sets of time constants from the table, five-time constants are selected for hardware implementation of SIDOBC to verify the simulation results. Using hardware set-up, the corresponding output voltages obtained for a 2 V set-point change in V_{o1_ref} and $V_{o2_ref}$is displayed in Fig. 13. It is evident from the figure that the hardware with different desired time constant is satisfactory in terms of transient response.

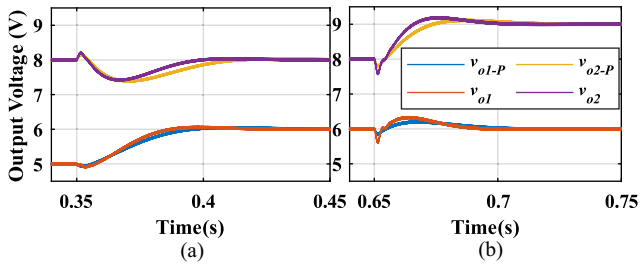

Fig. 14. Comparison of SIDOBC controller performance with and without parasitic parameter change for 1 V change in (a) V_{o1_ref} and (b) V_{o2_ref}.

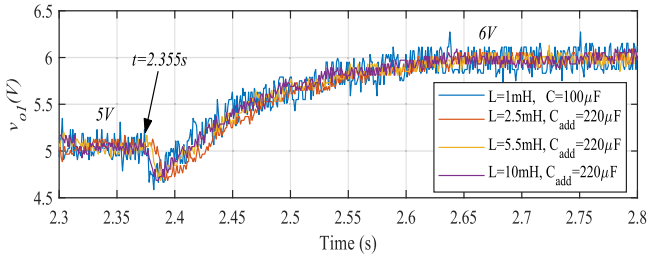

Fig. 15. Experimental comparison of transient response of voltage changes in V_{o1_ref} of SIDOBC with set of perturbed circuit parameter.

6) Case-6 Robustness Analysis of the Proposed Scheme: The robustness evaluation of the proposed controller for the SIDOBC is conducted through two distinct scenarios: 1) variations in parasitic parameters and 2) deviations in circuit parameters.

a) Parasitic parameter change: To show the impact of change in parasitic parameters of SIDOBC on the performance of proposed control scheme, the parasitic parameter values of the converter are considered as per the datasheet of individual elements. The performance comparison with and without these parasitic parameters are shown in Fig. 14. This figure illustrates the variations in output voltage under two different scenarios: 1) all converter components are considered ideal and 2) parasitic parameter values obtained from the datasheets of the respective components are incorporated to account for practical nonidealities. The voltage variation is analyzed by modifying the reference voltage to evaluate the impact of these parasitic effects on system performance. Specifically, Fig. 14(a) represents the case where the reference voltage V_{o1_ref} is varied from 5 V to 6 V, while Fig. 14(b) depicts the scenario where the reference voltage V_{o2_ref} is adjusted from 8 V to 9 V. Suffix "p" represents performance with parasitic parameter. From the figure, it is observed that controller performance with parasitic parameter change is satisfactory.

b) Circuit parameter change: To change the inductance value of circuit, the nominal inductor is replaced by another one. For changing the capacitance value, the additional capacitor (C_{add}) is connected in parallel with output capacitors (C_1 and C_2). The comparison of transient responses for output V_{01} with different set of inductance and capacitance are shown in Fig. 15. It is clear from the figure that only the ripples in output voltage are different whereas the transient response remains intact (in terms of settling time and overshoot) for all the aforementioned changes. Similar behaviour is observed for V_{02}; however, for

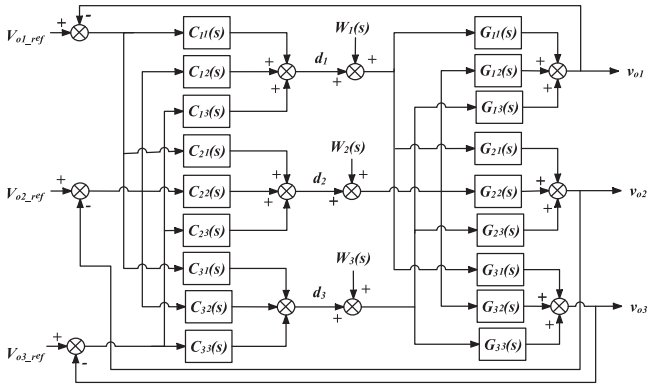

Fig. 16. Control scheme for SITOBC.

brevity, only the variation in V_{01} is shown. Thus, the proposed control scheme shows robust performance in the persistence of parametric uncertainty.

B. Single Inductor Three Output Buck Converter (SITO-BC)

To show the effectiveness of the proposed scheme a MIMO converter namely SITO-BC has been considered. This converter is a three input three output system and the control become more challenging in elimination cross regulation issue. The circuit parameter is given in Table I and control structure is shown in Fig. 16. The transfer function model $G(s)$ of this converter is obtained as

$$G_{11}=\frac{13000s^3+7.286e07s^2+1.116e11s+4.385e13}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}$$

$$G_{12}=\frac{4.615e07\,s^2+6.614e10\,s+2.769e13}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}$$

$$G_{13}=\frac{-13000\,s^3+2.448e07\,s^2+2.133e10\,s-4.615e12}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}$$

$$G_{21}=\frac{5.385e07\,s^2+6.284e10\,s+2.052e13}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}$$

$$G_{22}=\frac{13000\,s^3+6.258e07s^2+1.15e11\,s+5.577e13}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}$$

$$G_{23}=\frac{-13000\,s^3+2.141e07s^2+1.928e10\,s-8.716e12}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}$$

$$G_{31}=\frac{4.615e07s^2+5.385e10\,s+1.539e13}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}$$

$$G_{32}=\frac{3.692e07s^2+5.538e10\,s+1.846e13}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}$$

$$G_{33}=\frac{3.692e07s^2+6.154e10\,s+2.462e13}{s^4+2167s^3+4.872e06s^2+5.056e09s+1.597e12}. \quad (20)$$

The proposed controller design method has implemented and controller parameter have been evaluated for wide range of desired reference model. The desired time constants for all the control loops are selected as $\tau_{11}=\tau_{22}=\tau_{33}=0.0005\,s$. The

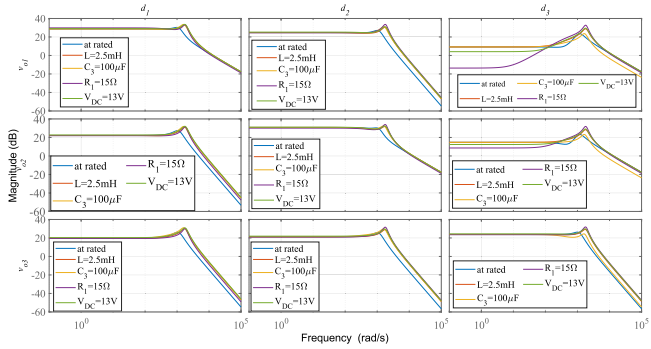

Fig. 17. Bode plot of open loop transfer function of SITO converter with various parameter change.

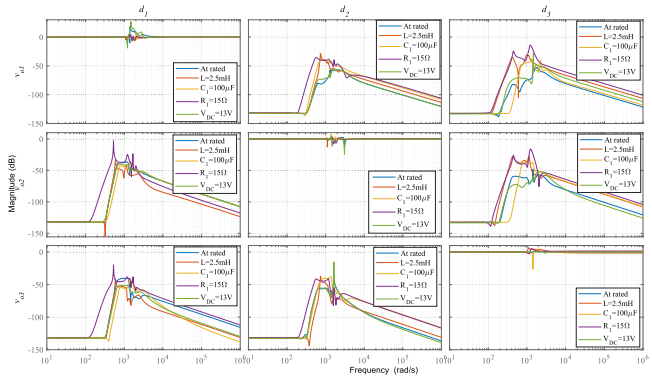

Fig. 18. Bode plot of closed-loop transfer function of SITO converter with various parameter change.

controllers are obtained as

$$\begin{aligned}
C_{11}&=-1.3973\times10^{-4}+\frac{17.7777}{s} & C_{23}&=-0.01004+\frac{5.7778}{s}\\
C_{12}&=8.3842\times10^{-5}+\frac{-10.6667}{s} & C_{31}&=-0.01507+\frac{-4.4444}{s}\\
C_{13}&=-0.00778+\frac{1.33333}{s} & C_{32}&=-0.01809+\frac{-5.33333}{s}\\
C_{21}&=6.9868\times10^{-5}+\frac{-8.8888}{s} & C_{33}&=0.03266+\frac{20.6667}{s}.\\
C_{22}&=-1.25764\times10^{-4}+\frac{16}{s}
\end{aligned} \quad (21)$$

The Bode plot of nominal converter model along with perturbed parameters are shown Fig. 17. From the figure it is observed that strong cross regulation is present and it make control of very much challenging. Due to this any disturbance or parametric changes affect other controlled variables. The Bode plot of converter model along with the controller is shown in Fig. 18. From this figure desired steady state performance with negligible cross regulation is observed. The performance of the suggested scheme is further evaluated in hardware experiment. A dedicated circuit of SITO BC with circuit parameter given in Table I has been developed, as shown in Fig. 7.

1) Case-1 Step Change in Reference for the Output Voltages (v_{o1}, v_{o2}, and v_{o3}): The converter is operated with nominal condition and change of 1 V is introduced at $t_1=13.77$ s in v_{o1}. The output voltage response is shown Fig. 19 and it can be seen that the output voltage v_{o1} tracks the reference command whereas other outputs (v_{o2} and v_{o3}) are unchanged. Similarly, change in reference command to v_{o2} and v_{o3} are given at different instant

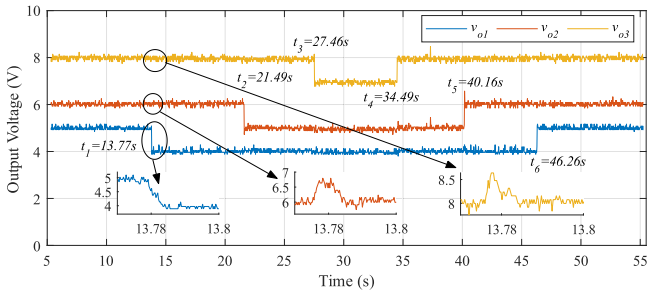

Fig. 19. Output voltage response with step change in set-point voltage.

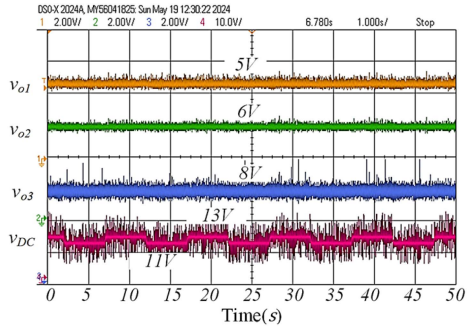

Fig. 20. Output voltage response with periodic change in supply voltage.

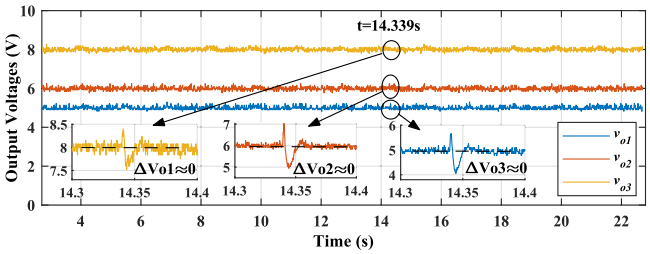

Fig. 21. Output voltage response of SITOBC with change in load.

of time. From the responses satisfactory performances has been observed.

2) Case-2 Periodic Change in Supply Voltages (v_{dc}): The enhanced load-disturbance rejection performance of the suggested scheme has been evaluated by introducing periodic change in the supply voltage while converter is operated with nominal setpoint command. A supply voltage is changed periodically between 11 V to 13 V and corresponding responses of output voltages are shown in Fig. 20. From this figure it is evident that output voltages are intact at nominal value in spite of periodic fluctuation in the supply voltage.

3) Case-3 Change in Load Resistances (R_1 and R_2): The load disturbance rejection capability of the proposed control scheme is evaluated by varying the load resistance while maintaining the converter at its nominal operating point. Specifically, at t = 14.339 s, the load R_2 is reduced from 20 Ω to 10 Ω, and the corresponding output voltage responses are depicted in Fig. 21. The results indicate that the converter effectively regulates the output voltages to their predefined steady-state values, exhibiting minimal transient deviations. The percentage overshoot observed in v_{o1}, v_{o2}, and v_{o3} is 16%, 16.67%, and

TABLE III
COMPARISON TABLE OF PROPOSED CONTROL TECHNIQUE WITH EXISTING LITERATURE

	Patra et al. [24]	Dasika et al. [19]	This work	
Converter	SIDOBC	SIDOBC	SIDOBC	SITOBC
Process	Discrete component	FPGA	TMS320F28379D	
Input voltage	4.8 V	5 V	12 V	12 V
Output voltages	3.3, 1.2 V	1, 1.5 V	5, 8 V	5, 6, 8V
Switching frequency	100 kHz	500 kHz	50 kHz	50 kHz
Inductor	10 μH	5 μH	1 mH	1 mH
Capacitors	10 μF	10,10 μF	100,100 μF	100, 100, 220 μF
FOM self	0.030	0.02 0.03	0.018 0.02	00
FOM cross	0.008	0.02 0.01	0.007 ~00	00 00

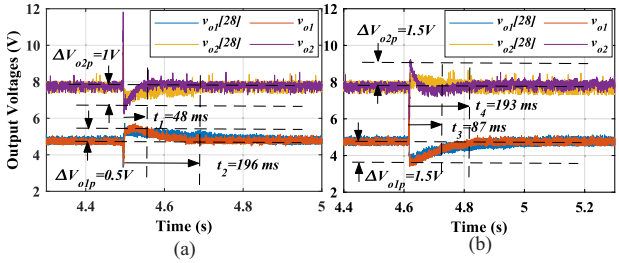

Fig. 22. Load disturbance rejection of proposed method and [28] amid (a) 5 Ω change in R_1 and (b) 5 Ω change in R_2.

5%, respectively, with all outputs achieving steady-state within a settling time of less than 15 ms. These findings confirm the robustness of the proposed controller in mitigating load-induced perturbations while ensuring stable and rapid voltage regulation.

C. Comparison With the Existing Methods

The performance of the proposed controller design technique has been compared with the existing work in the literature [19], [24] The circuit parameter, design specification and the performance index to quantify the cross-regulation effect are given in Table III. From the table it is observed that the performance index FOM self as well as FOM cross are lower in comparison with [19], [24]. Thus, better performance is achieved. It is also to note that the work of [19], [24] are suggested for SIDOBC only, however, the proposed scheme is deal with a generalized controller design technique, which can be applied to different size of converters.

To further validate the performance of the proposed control strategy, setpoint tracking, and disturbance rejection capabilities are compared with the method of [28] using the SIDOBC in a distinct manner, as depicted in Figs. 22 and 23 . It is evident that the proposed controller achieves a significantly faster settling time, ensuring quicker stabilization of output voltages after a load change (48 ms for the former and 196 ms for the latter amid

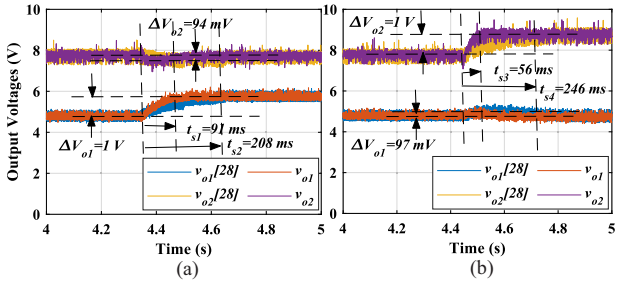

Fig. 23. Setpoint tracking of proposed method and [28] amid 1 V (a) change in V_{o1-ref} and change in V_{o2-ref}.

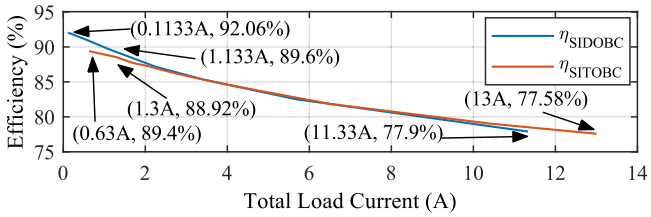

Fig. 24. Efficiency versus load current plot of SIDOBC and SITOBC controllers.

changes in R_1; 87 ms for the former and 193 ms for the latter amid changes in R_2). Also, the changes in setpoint are tracked by the proposed method faster than that of [28] (91 ms for the former and 94 ms for the latter change in V_{o1_ref}; 56 ms for the former and 246 ms change in V_{o2_ref}). While peak overshoot of the proposed method during disturbance rejection is slightly higher than that of [28], the deviation of the former is minimal and well within acceptable limits compared to the latter. This minor increase in overshoot does not compromise overall stability or performance, as the system swiftly recovers and achieves the desired steady-state value. Therefore, the proposed controller proves to be more effective in maintaining stability and achieving rapid transient response compared to the method used in [28].

D. Efficiency

The converter efficiency is obtained through simulation in PLECS by considering datasheets of diodes and MOSFETs used in SIDOBC and SITOBC. The total load current is calculated by adding individual load currents through each load (i.e., $i_{\text{total}} = i_{o1} + i_{o2} + i_{o3} + \ldots$), ranging from 0.133 A to 11.33 A for SIDOBC and 0.63 A to 13 A for SITOBC. The efficiency [25] is calculated as the ratio of the sum of all power consumed by individual loads to the input power, i.e.,

$$\eta = \frac{V_{o1}I_{o1} + V_{o2}I_{o2} + V_{o3}I_{o3} + \ldots}{V_{dc}I_{dc}}.$$

The plot of efficiency of the converters (SIDOBC and SITOBC) against load current is shown in Fig. 24. It has been found that the efficiency of converter decreases with the increase in total load current and the maximum efficiency of SIDOBC is 92.06% and SITOBC is 89.4% . The efficiency is also calculated at nominal points for both the converters and found to be 89.6% for SIDOBC and 88.92% for SITOBC.

V. Conclusion

This article presents the centralized PI controller design for SIMOBC, based on the model matching technique at low frequency points. The cross-regulation in the outputs of the SIMOBC has been minimized by considering the desired transfer function matrix as diagonal matrix. The mathematical modeling of the SIMOBC is done by using the state-space average technique and the PI controller parameters are tuned to obtain the desired result by varying the time constants. The proposed control scheme is simulated in the MATLAB/SIMULINK environment and verified with the laboratory experimental setup of the SIDOBC and SITOBC. The results obtained from the proposed method for SIDOBC and SITOBC are found to be satisfactory in terms of good set-point tracking and load disturbance rejection for nominal as well as perturbed systems. Furthermore, the cross-regulation in output voltages is satisfactorily minimized.

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