Current Ripple Reduction and ZVS Realization With Optimized DCM Modulation Based on Off-Time Discrete Control for Grid-Tied Inverters

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***Abstract*—This article proposes a modulation strategy for single-phase full-bridge grid-tied inverters operated with discontinuous current mode (DCM). Zero-voltage switching (ZVS) for turn-ON can be achieved by discretely adjusting the length of zero current period, in which the voltage across the devices is oscillating in the DCM-operated inverter. However, the conventional bipolar modulation for DCM leads to a high current ripple flowing into the semiconductor devices and inverter-side inductors. In addition to that, a non-negligible reverse current flows at the end of device conduction due to charge and discharge the parasitic capacitance of the semiconductor devices especially for the designs with high switching frequency. This article proposes an advanced trapezium-like current modulation to reduce the current ripple, including the reverse current. In the proposed modulation, the current ripple is quantitatively analyzed by considering the impact of the device parasitic capacitance and reduced to the minimum value at which ZVS can be maintained. The effect of the current ripple reduction on conduction losses in semiconductor devices is analyzed using various design considerations, including chip size and operating switching frequency. The loss reduction by the proposed strategy was verified in experiments using a 400-W prototype with GaN-HEMT devices operating with the switching frequency of 1 MHz.**

***Index Terms*—Current ripple reduction, discontinuous current mode (DCM), grid-tied inverter, zero-voltage switching (ZVS).**

I. Introduction

SINGLE-PHASE inverters with full-bridge topology are widely adopted for low power dc–ac conversion in various applications including microinverters for photovoltaic (PV) systems [1], [2]. With the rapid development of the PV market, there is a growing demand for improvements in efficiency and power density for microinverters [3]. The adoption of gallium nitride high electron mobility transistors (GaN-HEMTs) has enabled higher switching frequency, which can further enhance power density by reducing the size of passive components [4], [5]. However, despite these advantages, GaN-based inverters under hard-switching operation can still suffer from excessive switching losses, limiting system efficiency [6]. Therefore, achieving zero-voltage switching (ZVS) is particularly important for GaN-based converters, as it enables extremely low switching losses. This is because, in GaN devices, the turn-ON loss is eliminated by ZVS, and the energy stored in their parasitic capacitance, which is typically the dominant contributor to the turn-OFF loss, is not dissipated [7], [8], [9], [10], [11].

One way to achieve ZVS is to operate the inverter in a boundary conduction mode (BCM). In the BCM, a reverse direction current is provided for the switches to be turned-ON to discharge the output capacitance; therefore, it can achieve full ZVS operation in every switching cycle. However, BCM introduces a varying switching frequency, which can fluctuate excessively depending on the modulation strategy, particularly as the ac line voltage approaches zero. An excessively high switching frequency leads to increased switching losses, while a frequency too low—well below the cut-off frequency of the filter to attenuate the current ripple—can cause a significant output current distortion [12], [13], [14]. Besides, the state-of-the-art BCM often requires an accurate zero-crossing detection circuit. From the hardware point of view, detection circuit delays can be challenges for achieving ZVS in MHz operations [15], [16]. The overall cost and size can also be increased due to the auxiliary circuit.

As an alternative approach, a discontinuous current mode (DCM) enables flexible switching frequency control owing to the presence of a zero-current period. Hybrid control schemes combining DCM and BCM have recently attracted growing interest, as they help retain the ZVS capability of BCM while narrowing the switching frequency range [17], [18]. However, when the DCM is used partially in the line phase, ZVS is not always guaranteed, as it depends on the control strategy [13]. On the other hand, the zero-current period in DCM facilitates sensor-less current control by inherently resetting accumulated current errors each cycle [19]. This feature allows a simple average current control method, without conventional feedback, to be effectively used for regulating sinusoidal output current in the inverters fully operated in DCM.

To achieve ZVS operation in the DCM inverters, the authors have proposed an off-time discrete control [20], [21]. This method utilizes an oscillation caused by the parasitic capacitance of power semiconductor devices and the filter inductor during the zero-current period of the DCM modulation, and can achieve ZVS by discretely adjusting the length of the zero-current period so that all the turn-ON are performed at the bottom of

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the oscillating device voltage. On the other hand, the parasitic capacitance causes a small reverse current at the end of device conduction, and it lead to an increase in peak currents for a given output current, especially for the design with very high switching frequency [22]. This makes a drawback of DCM worse, which is the higher peak current compared to that in BCM.

Apart from the conduction mode (BCM or DCM), single-phase full-bridge inverters have bipolar and unipolar modulations. The unipolar modulation is advantageous for DCM because it has lower current ripple for the same average current; therefore, it can reduce conduction losses at the semiconductor devices and inductor [23]. The off-time discrete control can be applied to both the bipolar and unipolar modulations of the DCM. It can achieve ZVS in all the line phase with the bipolar modulation; however, it can lose ZVS with the unipolar modulation for almost half of the line phase. Similar phenomena are well studied in PFC circuits [24], [25]. The main reason originates from the difference in resonance loops between two modulations. It is also reported that DCM with the unipolar modulation has a much lower magnitude of the reverse current mentioned above than that with the bipolar modulation due to an incomplete discharge of the parasitic capacitance [26].

In previous work, the authors have proposed a hybrid control strategy that switches the modulation mode between the unipolar and bipolar modulations as function of the line phase [27]. The demonstration results showed that the ZVS operation can be extended in comparison to that with the conventional unipolar modulation at the expense of increased current ripple by introducing the bipolar modulation. However, the higher current ripple with the bipolar modulation can still be a limitation when the conduction loss is a target of optimization. It can be considered that there is a tradeoff relationship between the current ripple and the achievement of ZVS.

In recent studies, a trapezium current mode (TPCM) has emerged as a new modulation method that uses a three-level voltage applied to the inductor and creates a trapezium shape in the current waveform [28], [29], [30], [31]. The works presented in [30] and [31] demonstrated ZVS operations with the TPCM based on BCM and DCM, respectively. It has been reported that the current ripple can be reduced by introducing a low current slope section. However, quantitative analyses on the peak current reduction and the ZVS capability are not performed in the above works.

With the increased control degree-of-freedom, the TPCM can be used to bridge the gap between the bipolar and unipolar modulations, since the TPCM has intermediate characteristics between them. The current shape can be controlled to be closer to that with the unipolar modulation; in that case, the current ripple can be reduced. Alternatively, the ZVS can be guaranteed by adjusting the current shape to be closer to that with the bipolar modulation. This article proposes a method to minimize the current ripple of TPCM while maintaining ZVS capability. It can also contribute to suppress the reverse current at the end of device conduction; therefore, further reduction in peak-to-peak current can be possible.

The basic concept of the proposed control was presented in the preliminary work of this research [32]. Although Huang et al. [32] included basic experimental investigations, it lacked proper control implementation and quantitative analyzes on the technical merit, similar to other studies employing TPCM. To clarify the significance of the proposed approach, this article presents a substantially extended and distinct study. Specifically, this article focuses on the following three aspects. First, it theoretically clarifies why model-based current control alone can ensure system stability, even with an *LCL* filter, in DCM-operated inverters. Second, it derives a practical implementation of control to achieve the minimum switching current required to achieve ZVS, that was presented in [32], in cooperate with developing analytical current model. Third, it investigates the effectiveness of the proposed operation in terms of power loss reduction in detail. The loss reduction by the current ripple reduction with ensuring the ZVS are analyzed for a 1 MHz operated 400 W single-phase full-bridge inverter using GaN devices. It is based on the developed analytical current model in this article, and including inductor losses, which was not separately discussed in [32], in addition to the device conduction losses.

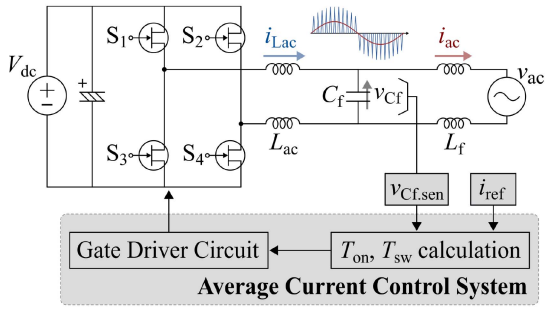

Fig. 1. Single-phase full-bridge grid-tied inverter for the operation in DCM.

II. Overview of Conventional DCM Modulations

A. Average Current Control of DCM-Operated Inverter

The schematic circuit diagram of a single-phase grid-tied inverter that can operate with DCM is shown in Fig. 1. The basic concept of the control system is to predict switching duty ratio to achieve a desired average value of the bridge-output current, i_{Lac}, in the next switching cycle. It is worth noting that i_{Lac} is being filtered and delivered to the ac-side, and thus, the average value, $\overline{i_{\mathrm{Lac}}}$, is indeed the output current. As a result, the output current of the inverter, i_{ac}, aligns its reference value, i_{ref}. For converters operating in DCM, the inductor current always starts at zero in each switching cycle, and it makes a simple feed-forward current control approach fully sufficient.

Fig. 2(a) shows the schematic inductor current waveform of the DCM inverter during one switching cycle. With a bipolar modulation, both the diagonal devices, S_1 and S_4, are turned-ON/OFF simultaneously. During the on-state period, T_{on}, the voltage across the inverter-side inductor, L_{ac}, is $V_{\mathrm{dc}} - v_{\mathrm{ac}}$, where V_{dc} is the dc-link voltage and v_{ac} is the grid voltage. The inductor current is actually governed by the filter capacitor voltage, v_{Cf}; however, it can be assumed to be equal to v_{ac}. In

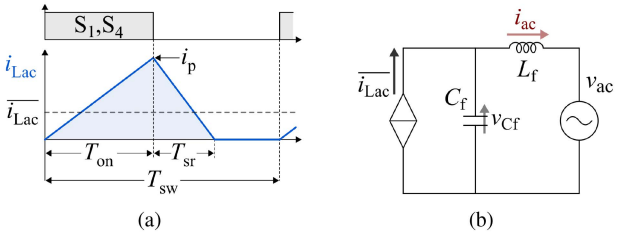

Fig. 2. DCM operation with the bipolar modulation. (a) Schematic waveform of inductor current. (b) Equivalent circuit model.

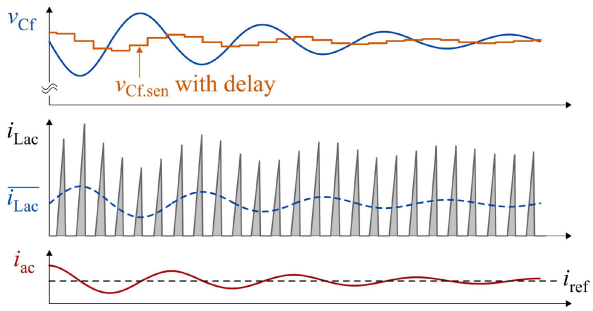

Fig. 3. Damping of CL filter resonance due to inherent feedback of DCM-inverter, caused by delays in the capacitor voltage sensor.

the second interval, $T_{\rm sr}$, the voltage becomes $-V_{\rm dc}-v_{\rm ac}$, which makes $i_{\rm Lac}$ decrease from its peak to zero. The inductor current peak, $i_{\rm p}$, can be expressed as

$$i_{\rm p}=\left(\frac{V_{\rm dc}-v_{\rm ac}}{L_{\rm ac}}\right)T_{\rm on}=\left(\frac{V_{\rm dc}+v_{\rm ac}}{L_{\rm ac}}\right)T_{\rm sr}. \tag{1}$$

Then, the relationship between $\overline{i_{\rm Lac}}$ and control parameters, $T_{\rm on}$ and the switching period, $T_{\rm sw}$, can be expressed as

$$\overline{i_{\rm Lac}}=\frac{i_{\rm p}(T_{\rm on}+T_{\rm sr})}{2T_{\rm sw}}=\frac{V_{\rm dc}(V_{\rm dc}-v_{\rm ac}){T_{\rm on}}^2}{L_{\rm ac}(V_{\rm dc}+v_{\rm ac})T_{\rm sw}}. \tag{2}$$

As shown in Fig. 2(b), the equivalent circuit of the DCM inverter with the average current control can be considered as a controlled current source with a CL filter. $T_{\rm on}$ and $T_{\rm sw}$ are determined to make the controlled current source, $\overline{i_{\rm Lac}}$, equal to $i_{\rm ref}$.

LCL filters are known to introduce resonance issues into the system in conventional feedback control scheme. Even though the average current control for the DCM inverter is not based on the feedback scheme and the current at $L_{\rm ac}$ is considered as a controlled current source, $C_{\rm f}$ and $L_{\rm f}$ can still cause a resonance. However, it is known that DCM operations with the average current control are stable in practice as the authors experimentally demonstrated in [20], [21], and [22].

Here, a small-signal disturbance in the capacitor voltage, generated by the resonance between $L_{\rm f}$ and $C_{\rm f}$, is considered. This disturbance causes a deviation between $v_{\rm Cf}$ and its sampled voltage, $v_{\rm Cf.sen}$, as shown in Fig. 3 due to delays in sensing and sampling. This deviation affects the actual current waveform of $i_{\rm Lac}$, therefore, its average, $\overline{i_{\rm Lac}}$, as the switching operations are performed based on $v_{\rm Cf.sen}$ regardless of the deviation of $v_{\rm Cf}$.

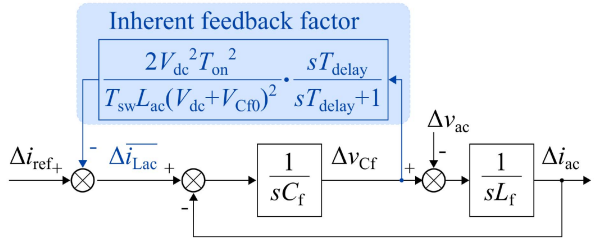

Fig. 4. Block diagram of the DCM-inverter with LCL filter that illustrating how the variation in $\Delta v_{\rm Cf}$ influences $\Delta\overline{i_{\rm Lac}}$ and, affects the perturbation of grid-side current, $\Delta i_{\rm ac}$.

It has been observed that the oscillating component in $\overline{i_{\rm Lac}}$ has a phase opposite to that of $v_{\rm Cf}$, which acts as a natural feedback mechanism to suppress further oscillation of $v_{\rm Cf}$.

In order to investigate the damping mechanism further, a linearized control block or model that represents the DCM inverter operation is required, as the nonlinear factor involved in the duty ratio calculation in (2) can complicate time-domain stability analysis. To achieve this, a small-signal model can be used to approximate the relationship among the small-signal variations in control inputs, such as $i_{\rm ref}$ and $T_{\rm on}$, and their effects on various circuit quantities, including $\overline{i_{\rm Lac}}$, $v_{\rm Cf}$, $v_{\rm ac}$, and $i_{\rm ac}$. Here, $\Delta i_{\rm ref}$, $\Delta T_{\rm on}$, $\Delta\overline{i_{\rm Lac}}$, $\Delta v_{\rm Cf}$, $\Delta v_{\rm ac}$, and $\Delta i_{\rm ac}$ represent the small-signal perturbations of the corresponding variables around their steady-state values. In contrast, $T_{\rm on0}$ and $V_{\rm Cf0}$ denote the operating points of the on-state time and capacitor voltage, respectively. While the detailed derivation is presented in the Appendix, the resulting fully linearized small-signal model from $\Delta v_{\rm Cf}$ to $\Delta\overline{i_{\rm Lac}}$ can be derived and expressed as

$$\Delta i_{\rm ref}-\frac{2{V_{\rm dc}}^2{T_{\rm on0}}^2}{T_{\rm sw}L_{\rm ac}(V_{\rm dc}+V_{\rm Cf0})^2}\cdot\left(1-\frac{1}{1+sT_{\rm delay}}\right)\cdot\Delta v_{\rm Cf}=\Delta\overline{i_{\rm Lac}} \tag{3}$$

where s is a complex variable. To derive the above model, the sampling process of the capacitor voltage is assumed as a first-order delay whose total delay time is $T_{\rm delay}$.

The block diagram of the linearized small-signal model of the DCM-operated inverter with the average current control can be depicted as Fig. 4. As can be seen from the block diagram, the relationship between $\Delta v_{\rm Cf}$ and $\Delta\overline{i_{\rm Lac}}$ works as a negative feedback; therefore, has a damping effect for the perturbation. Moreover, it is evident that the delay time, $T_{\rm delay}$, influences the damping factor. When $T_{\rm delay}=0$, the damping factor disappears, whereas for $T_{\rm delay}\to\infty$, the damping factor can be approximated as

$$\frac{2{V_{\rm dc}}^2{T_{\rm on}}^2}{T_{\rm sw}L_{\rm ac}(V_{\rm dc}+V_{\rm Cf0})^2}=A \tag{4}$$

where A is defined as a positive constant coefficient.

For instance, a disturbance in the grid voltage, $\Delta v_{\rm ac}$, and the resulting perturbation in the grid-side current, $\Delta i_{\rm ac}$, are assumed here. When the damping effect by the natural feedback is disabled, which can be considered by giving $T_{\rm delay}=0$, the relationship between $\Delta i_{\rm ac}$ and $\Delta v_{\rm ac}$ for $\Delta\overline{i_{\rm Lac}}=0$ can be

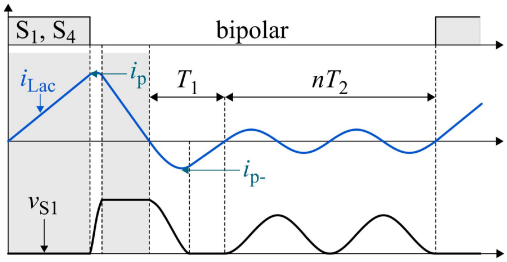

Fig. 5. Schematic waveform of bipolar DCM operation in one switching cycle with the off-time discrete control. It considers the oscillation caused by the drain-source parasitic capacitance of the switching device, $C_{\rm ds}$, and $L_{\rm ac}$.

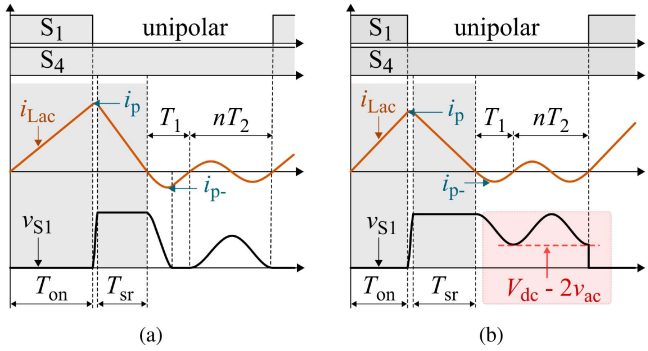

Fig. 6. Switching cycle behavior of the off-time discrete control with the unipolar modulation (a) when $2v_{\rm ac} \geq V_{\rm dc}$. (b) When $2v_{\rm ac} < V_{\rm dc}$.

expressed as

$$\frac{\Delta i_{\rm ac}}{\Delta v_{\rm ac}} = \frac{-sC_{\rm f}}{s^2 L_{\rm f} C_{\rm f} + 1} \tag{5}$$

which indicates that the poles exist on imaginary axis; therefore, possible oscillation at the frequency determined by $L_{\rm f}$ and $C_{\rm f}$ does not decay theoretically. Conversely, by incorporating the feedback loop described in (4) by giving $T_{\rm delay} \to \infty$, the relationship between $\Delta i_{\rm ac}$ and $\Delta v_{\rm ac}$ can be modified as

$$\frac{\Delta i_{\rm ac}}{\Delta v_{\rm ac}} = \frac{-sC_{\rm f} - A}{s^2 L_{\rm f} C_{\rm f} + sL_{\rm f} A + 1}. \tag{6}$$

The transfer function (6) has all the two poles in the left half plane, indicating system stability.

It can be concluded that the inherent mechanism of the DCM-operated inverter with the delayed capacitor voltage information creates a natural feedback loop; therefore, the system can ensure stability for the natural resonance caused by $L_{\rm f}$ and $C_{\rm f}$.

B. Off-Time Discrete Control for DCM

The fundamental operating principles of the DCM inverter have thus far been discussed using the conventional bipolar modulation. In this section, a key aspect of this work, ZVS operation for the DCM inverter, is introduced. This can be realized by extending the average current model to account for the parasitic capacitance of the switching devices. Furthermore, the peak inductor current values in the feed-forward control scheme have been reconsidered to accommodate necessary modifications to the average current model. In addition, an unipolar modulation, which is another modulation widely employed for DCM inverters, is briefly introduced and compared with the bipolar modulation.

As shown in Fig. 5, in actual DCM-operated converters, there is an oscillation during the zero current period, which is caused by the drain-source parasitic capacitance of switching devices, $C_{\rm ds}$, and the inverter-side inductors, $L_{\rm ac}$. The oscillation period can be divided into two parts. The first part is referred to as T_1, in which a large negative current can be observed in the current flowing into the inductor, $i_{\rm Lac}$. After $i_{\rm Lac}$ increases to zero, the second part of the oscillation starts. Its cycle is referred to as T_2, and the resonance can be assumed to be a pure LC resonance. The total period of the second part of the oscillation is defined as nT_2. It has been reported that ZVS can be achieved in the DCM-operated inverter with an off-time discrete control, which was proposed by the authors in [20] and [21]. The main concept of the off-time discrete control is to select an integer number for n to make the switches always turn-ON at zero voltage.

Although the ZVS operation can improve the performance of DCM inverters, the large negative current during T_1 is still a problem for further high switching frequency operations. In [22], the main peak, $i_{\rm p}$, and the negative peak during T_1, $i_{\rm p-}$, in the bipolar modulation are derived by considering the oscillation period and are expressed as

$$i_{\rm p} = \sqrt{\frac{(V_{\rm dc} + v_{\rm ac})\left[(V_{\rm dc} - v_{\rm ac}) i_{\rm ref} T_{\rm sw} + 2C_{\rm ds} V_{\rm dc} v_{\rm ac}\right]}{L_{\rm ac} V_{\rm dc}}}$$

$$i_{\rm p-} = -\sqrt{\frac{C_{\rm ds}}{L_{\rm ac}}} \cdot (V_{\rm dc} + v_{\rm ac}) \quad \text{(bipolar)}. \tag{7}$$

Equation (7) indicates that both $i_{\rm p}$ and $|i_{\rm p-}|$ becomes high with increase in $C_{\rm ds}$ and decrease in $L_{\rm ac}$. It should be mentioned that $L_{\rm ac}$ must be low for the designs with higher switching frequency; therefore, this phenomenon causes non-negligible problems in the DCM-operated inverters designed with extremely high switching frequencies.

As a promising solution, the unipolar modulation can be applied to achieve lower current ripple compared to the bipolar modulation for the same current reference, $i_{\rm ref}$, under the same converter design. Fig. 6 illustrates the schematic waveforms with the unipolar modulation. In contrast to the bipolar modulation, one of the diagonal devices of the full-bridge is operated at line frequency, resulting in reduced number of switching operations. In addition, during the second interval, $T_{\rm sr}$, the voltage across the inductor becomes $-v_{\rm ac}$, which influences the inductor current waveform. The main and negative peak of $i_{\rm Lac}$ for the unipolar modulation can be expressed as

$$i_{\rm p} = \sqrt{\frac{2v_{\rm ac}\left[(V_{\rm dc} - v_{\rm ac}) i_{\rm ref} T_{\rm sw} + 2C_{\rm ds} V_{\rm dc}(2v_{\rm ac} - V_{\rm dc})\right]}{L_{\rm ac} V_{\rm dc}}}$$

$$i_{\rm p-} = -\sqrt{\frac{2C_{\rm ds}}{L_{\rm ac}}} \cdot v_{\rm ac} \quad \text{(unipolar)} \tag{8}$$

which can be derived in the same way as for the bipolar modulation. Equations (7) and (8) indicate that both the main and the

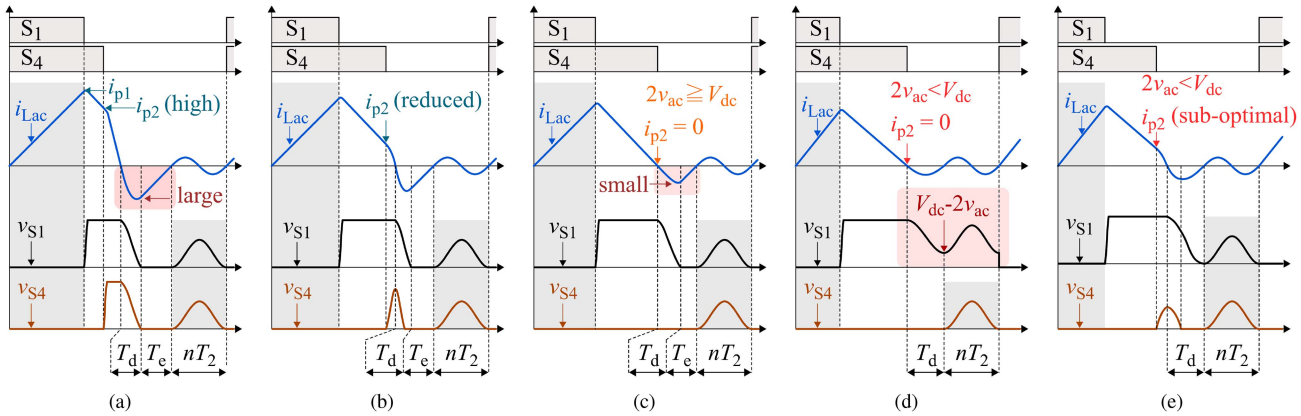

Fig. 7. Key waveforms of the trapezium-like current modulation in one switching cycle with turn-OFF current, i_{p2} that is (a) high value, (b) relatively small value, (c) equal to zero when $2v_{ac} \geq V_{dc}$, (d) equal to zero when $2v_{ac} < V_{dc}$, and (e) suboptimal value when $2v_{ac} < V_{dc}$.

negative peak current can be lower with the unipolar modulation in comparison to that with the bipolar modulation for the same current reference and switching frequency.

However, the unipolar modulation still has some disadvantages in comparison to the bipolar modulation. The amplitude and offset of the oscillation are different from those with the bipolar modulation. These phenomena can make the unipolar modulation lose the ZVS operation when $2v_{ac} < V_{dc}$, as shown in Fig. 6(b). Under this condition, the device voltage, v_{S1}, can not touch zero during nT_2; therefore, only a valley switching can be achieved with the off-time discrete control. The minimum turn-ON voltage that can be achieved is $V_{dc} - 2v_{ac}$. This can be considered as the main disadvantage of the unipolar modulation for the off-time discrete control.

To overcome the drawback of losing ZVS in the unipolar modulation, the authors have proposed a hybrid modulation strategy that combines the bipolar and unipolar modulations [27]. The hybrid modulation uses the unipolar modulation for high ac voltage phase and the bipolar modulation for the phase around voltage zero crossing. ZVS can be achieved in the entire phase and power range by the hybrid modulation; however, relatively high current ripples during the phase in which the converter operates with the bipolar modulation can still be a limitation to improve the efficiency further.

III. Proposed ZVS Modulation Strategy With Reduced Current Ripple

In order to reduce the current stress on the devices while achieving ZVS in all the line phase, an improved trapezium-like current modulation is proposed in this section. It is worth mentioning that the proposed modulation primarily focuses on the condition $2v_{ac} < V_{dc}$. This section also considers unity power factor operation, which reflects the typical operating condition of PV inverters [33]. The improved modulation follows the general concept of a TPCM strategy, which has three-level current slope. By inserting an additional interval with a lower current slope, the waveform of i_{Lac} becomes a trapezium shape; therefore, the proposed modulation can achieve a lower peak current than that with the bipolar modulation for the same output current. As shown in Fig. 7, a pair of diagonal devices, S_1, S_4, are turned-ON at the same instant; however, they have different on-state times to regulate the inductor current. The diagonal devices are turned-OFF at different inductor currents, i_{p1} and i_{p2}, respectively. In the following discussion, S_1 is turned-OFF at first and S_4 is turned-OFF later; however, the order can be switched.

Although i_{p1} and i_{p2} can individually be selected in the TPCM strategy, $|i_{p1}| \geq |i_{p2}|$ holds for all switching cycles and current reference when the inverter operates at unity power factor. When i_{p2} becomes smaller, TPCM is closer to the unipolar modulation. In contrast, i_{p2} increases, TPCM is closer to the bipolar modulation. Therefore, i_{p2} should be reduced as much as possible to reduce i_{p1}. In this case, the TPCM can be assumed to be almost the same as unipolar modulation, so a reduction in large valley areas can also be expected.

Generally, the turn-OFF operation of devices is accompanied by charging and discharging of the parasitic capacitance which are performed by i_{Lac}. When i_{Lac} is high enough at a turn-OFF instant, the parasitic capacitance of the device is fully charged after the turn-OFF operation, then another linear current-slope state starts. However, when i_{Lac} is not enough, the charging process is not completed by the time that i_{Lac} reaches zero and a different operation happens after that. With the TPCM, the turn-OFF current of the first switching, i_{p1} is always higher than that of the second switching, i_{p2}. Therefore, the transient after the turn-OFF of S_4 should be analyzed and discussed with the magnitude of i_{p2}, as the key parameter. The transient operation can be classified into the following cases.

1) Enough High i_{p2}: Under this condition, i_{p2} is large enough to fully charge the parasitic capacitance of S_4 just after its turn-OFF. As it is shown in Fig. 7(a), there is a period that the voltages across S_1 and S_4, v_{S1} and v_{S4} respectively, are equal to V_{dc} and those of the opposite devices become zero. During this period, i_{Lac} decreases linearly by the reverse conduction of the opposite devices. After i_{Lac} is crossing zero, there is a valley part in i_{Lac}, which can be divided into two parts, T_d and T_e. During the time period T_d, both the parasitic capacitance of S_1 and S_4

are discharged by negative i_{Lac}. When the parasitic capacitance is fully discharged, an extra reverse conduction time period, T_{e}, starts where inductor current increases linearly to zero by the reverse conduction of S_1 and S_4.

The process after the turn-OFF of S_4 is the same as that in the bipolar modulation. Therefore, during T_{d}, a large negative inductor current flows in i_{Lac} whose value is the same as that of the bipolar modulation. Although the main peak of the inductor current can be reduced by introducing the lower current slope period by the TPCM, the large negative current makes the average of i_{Lac} low and results in the increase of the peak inductor current for the same output current reference.

After T_{e}, the second resonance period, nT_2 starts. Since the initial values of v_{S1} and v_{S4} under this condition are zero, they can touch zero during the resonance period, which means ZVS with the off-time discrete control can be achieved. It should be noted that the cycle of the second oscillation becomes equal to that with the bipolar modulation because of the same equivalent circuit of the resonance loop.

2) Reduced i_{p2}: When i_{p2} is relatively low, the parasitic capacitance of S_4 can not fully be charged after the device is turned-OFF, as shown in Fig. 7(b). Under this condition, i_{Lac} decreases nonlinearly to zero while charging the parasitic capacitance of S_4. Therefore, the third linear current slope state disappears, and the entire waveform of i_{Lac} is no longer a perfect trapezium shape.

During the time period T_{d}, the device voltages v_{S1} and v_{S4} start to decrease to zero individually with different initial voltages. After both v_{S1} and v_{S4} reach zero, i_{Lac} is lineally increased to zero through the reverse conduction of S_1 and S_4 during the time period T_{e}. It can be found that the valley part of i_{Lac} becomes lower than that observed in Fig. 7(a) owing to the partial charge and discharge of the parasitic capacitance of S_4 with this relatively low i_{p2}. It should also be mentioned that the valley value of v_{S1} and v_{S4}, during the oscillation period nT_2 can still be zero; therefore, ZVS can be achieved by applying the off-time discrete control under a certain voltage condition discussed later.

3) $i_{\mathrm{p2}} = 0$: According to the above discussion, it can be considered that reducing i_{p2} to zero is the best solution for TPCM since minimum negative inductor current; therefore, minimum current ripple can be achieved under this condition as shown in Fig. 7(c). However, it can lose ZVS for $i_{\mathrm{p2}} = 0$ under the condition of $2v_{\mathrm{ac}} < V_{\mathrm{dc}}$.

Due to the insufficient initial energy from the inductor and the ac voltage source, v_{S1} cannot be discharged to zero during T_{d}. Since the device can not fully be discharged and reverse conducted, T_{e} does not exist under this condition. Therefore the initial voltage for the following resonance period, nT_2 becomes not zero as shown in Fig. 7(d).

It should be noted that the operation under $i_{\mathrm{p2}} = 0$ is almost the same as that with the unipolar operation except for the oscillation cycle T_2 due to the different equivalent circuit for resonance. Therefore, the operation has the same advantage with the unipolar modulation, that is the reduced peak current, and conversely the same disadvantage, that is losing ZVS under $2v_{\mathrm{ac}} < V_{\mathrm{dc}}$. On the other hand, operations under high i_{p2} become closer to the bipolar modulation and have a large valley part of i_{Lac}. It can be said that controlling i_{p2} can offer optimization of the operation between the bipolar and unipolar modulations.

4) Suboptimal i_{p2} for $2v_{\mathrm{ac}} < V_{\mathrm{dc}}$: The operation with $i_{\mathrm{p2}} = 0$ can achieve the minimum negative inductor current; however, it can not achieve ZVS when $2v_{\mathrm{ac}} < V_{\mathrm{dc}}$. It is considered that for the above voltage condition, there is a suboptimal nonzero i_{p2} to achieve a minimum negative inductor current with keeping the ZVS by the off-time discrete control.

In the suboptimal condition, i_{Lac} reaches zero when v_{S1} reaches zero as shown in Fig. 7(e). This is the operation with the minimum i_{p2} for keeping ZVS under the voltage condition of $2v_{\mathrm{ac}} < V_{\mathrm{dc}}$. In comparison to the case with high i_{p2} as shown in Fig. 7(a), there is no extra reverse conduction period, T_{e}, and the operation directly transfers to the second oscillation period nT_2; therefore, the negative inductor current can be reduced. At the same time, the initial voltage for nT_2 is still zero; therefore, ZVS can be achieved.

The suboptimal i_{p2} can be calculated by considering the energy conservation for the period between the turn-OFF of S_4 and the beginning of nT_2 as

$$i_{\mathrm{p2}} = \sqrt{\frac{2C_{\mathrm{ds}}}{L_{\mathrm{ac}}}{V_0}^2 + \frac{4C_{\mathrm{ds}}}{L_{\mathrm{ac}}}v_{\mathrm{ac}}V_0} \tag{9}$$

where V_0 is the first peak of v_{S4} that is achieved when $i_{\mathrm{Lac}} = 0$, and can be given as

$$V_0 = \sqrt{V_{\mathrm{dc}}\left(V_{\mathrm{dc}} - 2v_{\mathrm{ac}}\right)}. \tag{10}$$

Although the TPCM with $i_{\mathrm{p2}} = 0$ is a promising solution for $2v_{\mathrm{ac}} \geq V_{\mathrm{dc}}$, both the diagonal devices are operated at a high frequency. Alternatively, the unipolar modulation can also provide the same current waveforms except for the oscillation period, T_2, with almost half of the number of switching, and its ZVS capability under $2v_{\mathrm{ac}} \geq V_{\mathrm{dc}}$ is same as that of the TPCM with $i_{\mathrm{p2}} = 0$; therefore, this article proposes to apply the trapezium-like current modulation for $2v_{\mathrm{ac}} \leq V_{\mathrm{dc}}$ and the conventional unipolar modulation for $2v_{\mathrm{ac}} \geq V_{\mathrm{dc}}$.

IV. Detailed Inductor Current Model and Comparison of Peak Current Values

A. Analytical Model for Proposed Modulation

In order to implement and realize the proposed trapezium-like current modulation and to discuss its advantage analytically, the detailed analytical current model is presented in this section. Fig. 8 depicts the inductor current and device voltages with the proposed ZVS modulation and the suboptimal value for i_{p2}. It should be mentioned that the discussion for the trapezium-like current modulation is for the case of $2v_{\mathrm{ac}} < V_{\mathrm{dc}}$.

During the on-state period, T_{on}, inductor current i_{Lac} increases linearly to its first peak value, i_{p1}, and the area surrounded by i_{Lac} can be expressed as

$$Q_{\mathrm{on}} = \frac{1}{2}i_{\mathrm{p1}}T_{\mathrm{on}} = \frac{(V_{\mathrm{dc}} - v_{\mathrm{ac}})}{2L_{\mathrm{ac}}}{T_{\mathrm{on}}}^2. \tag{11}$$

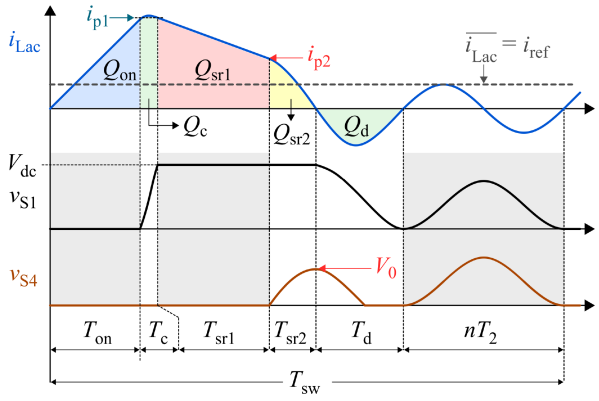

Fig. 8. Detailed behaviors of the proposed trapezium-like current modulation in one switching cycle with the suboptimal value for i_{p2}.

After device S_1 turned-OFF, there is a time interval T_c, where the parasitic capacitance of S_1 is charged from 0 to V_{dc} and that of the opposite device S_3 is discharged to 0. Then, the area surrounded by i_{Lac} can be expressed as

$$Q_c = \int_0^{T_c} i_{Lac} dt = 2V_{dc}C_{ds} \tag{12}$$

which is equal to the transferred charge of the parasitic capacitance for both S_1 and S_3. This article assumes that Q_c can be approximated as a rectangle area and i_{Lac} is constant during T_c. With this assumption, T_c can be expressed as

$$T_c = \frac{2V_{dc}C_{ds}}{i_{p1}} = \frac{2V_{dc}C_{ds}L_{ac}}{(V_{dc} - v_{ac})T_{on}}. \tag{13}$$

In addition, during the next time period, T_{sr1}, the inductor current can be assumed to be decreased from i_{p1} to the second current peak, i_{p2}. Then, T_{sr1} can simply be derived as

$$T_{sr1} = \frac{L_{ac}}{v_{ac}} (i_{p1} - i_{p2}) \tag{14}$$

and the current area Q_{sr1} can be expressed as

$$Q_{sr1} = \frac{L_{ac}}{2v_{ac}} \left({i_{p1}}^2 - {i_{p2}}^2 \right). \tag{15}$$

The time interval after S_4 turns OFF and the inductor current decreases to zero is referred to as T_{sr2}. The behavior during T_{sr2} can be considered as a pure LC resonance. As it is mentioned in Section III, the parasitic capacitance of S_4 is charged from 0 to V_0 and that of the opposite device S_2 is discharged to 0. The total transferred charge flowing through the inductor can be obtained by integrating i_{Lac} and expressed as

$$Q_{sr2} = \int_0^{T_{sr2}} i_{Lac} dt = 2V_0 C_{ds}. \tag{16}$$

Its time periods, T_{sr2}, can be expressed as

$$T_{sr2} = \sqrt{2L_{ac}C_{ds}} \arccos \left(\sqrt{\frac{2C_{ds}{v_{ac}}^2}{L_{ac}{i_{p2}}^2 + 2C_{ds}{v_{ac}}^2}} \right). \tag{17}$$

During the next time period, T_d, the parasitic capacitance of S_1 and S_4 are discharged to 0 and those of the opposite device, S_3 and S_2, are charged. Although the number of parasitic capacitance involved in LC resonance loop changes during T_d when v_{S4} reaches zero, i_{Lac} during this period represents the charge transferred from S_1 and to S_3 as

$$i_{Lac} = C_{ds} \left(\frac{dv_{ds(S_1)} + dv_{ds(S_3)}}{dt} \right) \tag{18}$$

where $v_{ds(S_1)}$ and $v_{ds(S_3)}$ represent the drain-source voltages of the upper and lower devices, respectively. Therefore, the area surrounded by i_{Lac} can be expressed as

$$Q_d = \int_0^{T_d} i_{Lac} dt = 2V_{dc}C_{ds}. \tag{19}$$

The resulting equation indicates that the contribution from Q_d to the total area in the switching cycle is canceled by that from Q_c. On the other hand, its time periods, T_d, can be expressed as

$$T_d = \sqrt{L_{ac}C_{ds}} \arcsin \left(\frac{2\sqrt{v_{ac}V_0}}{v_{ac} + V_0} \right) + \sqrt{2L_{ac}C_{ds}} \arccos \left(\frac{V_0 - v_{ac}}{\sqrt{{v_{ac}}^2 + {V_0}^2}} \right). \tag{20}$$

The cycle of the second resonance can be derived by considering the equivalent circuit for the oscillation, and can be expressed as

$$T_2 = 2\pi\sqrt{L_{ac}C_{ds}}. \tag{21}$$

The area surrounded by i_{Lac} during this period becomes zero when the off-time discrete control successfully achieves turn-ON at zero current instants.

According to the time duration of the periods obtained from the above equations, the switching cycle, T_{sw}, can be expressed as

$$T_{sw} = T_{on} + T_c + T_{sr1} + T_{sr2} + T_d + nT_2. \tag{22}$$

On the other hand, the average current of i_{Lac} for the current control, $\overline{i_{Lac}}$, can be expressed as

$$\overline{i_{Lac}} = \frac{Q_{on} + Q_{sr1} + Q_{sr2} + Q_c - Q_d}{T_{sw}} = \frac{4L_{ac}C_{ds}V_0v_{ac} - {L_{ac}}^2{i_{p2}}^2 + V_{dc}(V_{dc} - v_{ac}){T_{on}}^2}{2L_{ac}v_{ac}T_{sw}}. \tag{23}$$

In order to implement the proposed trapezium-like current modulation, T_{on} and T_{sw} must be solved from (22) and (23). The flowchart of the proposed step-by-step calculation method for T_{on} and T_{sw} is shown in Fig. 9. For the first step, T_{sr2}, T_d, T_2, and i_{p2} in (22) and (23) in each switching cycle should be calculated. These variables are independent of T_{on} and only change with the ac line voltage, v_{ac}. Since the switching frequency is much higher than the line frequency, the above parameters can be considered as constant values in one switching cycle.

As mentioned in Section II-B, the main concept of the off-time discrete control is to select an integer number for n in (22) to achieve ZVS. It is worth noting that n can independently be selected; however, a large number for n results in a higher

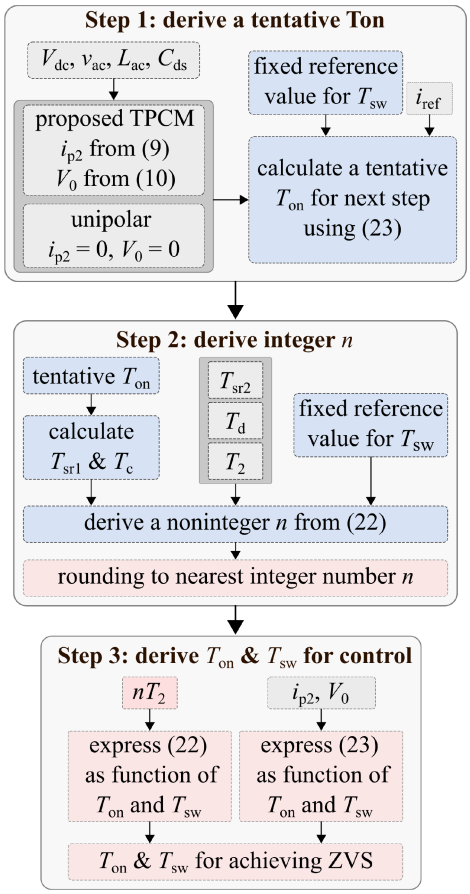

Fig. 9. Flowchart for calculation T_{on} and T_{sw} when using the proposed trapezium-like current modulation.

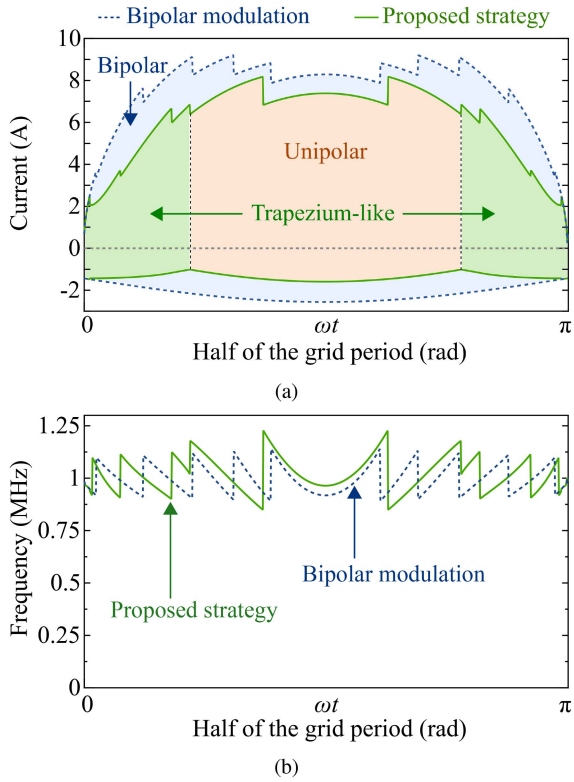

Fig. 10. Examples of resulting variables with the bipolar modulation and the proposed strategy. (a) Main peak and negative peak values of i_{Lac}. (b) Switching frequency f_{sw}.

peak current, and a small number for n results in an increased switching frequency. This article follows a method for selecting preferred n, in which both the switching frequency and peak current are suppressed [21]. The detailed calculation method for n can be divided into two steps, as shown in Fig. 9. In Step 1, a fixed value for T_{sw}, which is a set-point of the median of the fluctuating switching frequency, is tentatively considered and T_{on} for given reference current $\overline{i_{\mathrm{Lac}}}$ is calculated from (23). In Step 2, the tentative value, T_{on} and the fixed value, T_{sw} are used to calculate a noninteger value for n, which is then rounded to the nearest integer. In Step 3, T_{on} and T_{sw} for given $\overline{i_{\mathrm{Lac}}}$ and the integer number for n is derived again from (22) and (23).

On the other hand, the unipolar modulation is utilized for $2v_{\mathrm{ac}} \geq V_{\mathrm{dc}}$ in the proposed modulation. The unipolar modulation can be considered as a special case of the trapezium-like current modulation where $i_{\mathrm{p2}} = 0$ is assumed. T_{sr2} does not exist in the unipolar modulation; moreover, T_{d} can be different from (20) as

$$T_{\mathrm{d}} = \sqrt{2L_{\mathrm{ac}}C_{\mathrm{ds}}}\arccos\left(\frac{v_{\mathrm{ac}} - V_{\mathrm{dc}}}{v_{\mathrm{ac}}}\right) + \frac{\sqrt{2L_{\mathrm{ac}}C_{\mathrm{ds}}V_{\mathrm{dc}}(2v_{\mathrm{ac}} - V_{\mathrm{dc}})}}{V_{\mathrm{dc}} - v_{\mathrm{ac}}} \tag{24}$$

due to the different equivalent circuit for the resonance [27]. Q_{d} does not change. For the same reason, the oscillation cycle, T_2, can also be different from that with the trapezium-like modulation as

$$T_2 = 2\pi\sqrt{2L_{\mathrm{ac}}C_{\mathrm{ds}}}. \tag{25}$$

Since the modified time period and the areas surrounded by i_{Lac} are still independent of T_{on}, the unipolar modulation can also be implemented in the same manner as the trapezium-like current modulation.

B. Current Ripple Profile of Proposed Strategy

In order to investigate the performance of the current ripple reduction, peak values with the bipolar modulation and the proposed strategy, which combines the trapezium-like current modulation and the unipolar modulation were calculated and discussed in this section. Fig. 10 plots the calculated peak values of i_{Lac} and the switching frequencies of S_1 as function of the line phase at the rated current operation of an inverter. The values were calculated using the current model and the modulation strategy described in the previous section, and the circuit parameters listed in Table I.

The positive peak currents and the negative peak currents are separately shown in Fig. 10(a). It is demonstrated that both peak values are significantly reduced when the proposed strategy is applied. It can be observed that the negative peak reduction by the proposed strategy was not negligible in this design. The

TABLE I
CIRCUIT PARAMETERS

DC voltage	$V_{\rm dc}$	360 V
AC voltage (rms)	$V_{\rm ac}$	200 V
Line frequency	$f_{\rm grid}$	50 Hz
Rated current (rms)	$I_{\rm ac.rated}$	2 A
Switching frequency	$f_{\rm sw}$	1 MHz
Drain-source capacitance	$C_{\rm ds}$	0.11 nF
Inverter-side inductance	$L_{\rm ac}$	6.8 μH
Percentage impedance	$\%X_{\rm Lac}$	0.0021%
Grid-side inductance	$L_{\rm f}$	5.0 μH
Percentage impedance	$\%X_{\rm Lf}$	0.0016%
Filter capacitance	$C_{\rm f}$	0.22 μF

positive peak could be reduced owing to the inherent advantage of the trapezium-like current shape and the reduction in the contribution of the negative area to the average. The reduced peak currents result in a decrease in the rms value of the current flowing through the devices and inductors for the same output current. Consequently, the device conduction loss and inductor loss are expected to be reduced.

On the other hand, the bipolar modulation and proposed strategy have similar characteristics of the switching frequency as shown in Fig 10(b). The switching frequencies are varying around 1 MHz, and they change in step because of the discretely controlled oscillation period by the off-time discrete control. However, it should be noted that the proposed strategy has reduced number of switching by introducing the unipolar modulation for $2v_{\rm ac} > V_{\rm dc}$. Therefore, remaining switching losses that are not eliminated by the ZVS operations can also be reduced. Its impact depends on the characteristics of the switching device, and its operating condition.

C. Evaluation of Semiconductor Conduction Loss

In the following discussion, effects of the current ripple reduction on the conduction loss of semiconductor devices are analyzed. As mentioned in Section II-B, the negative peak of the inductor current can significantly increase with the reduced inductance. In addition, the main current peak must be increased to keep the same average current in one switching cycle, which is equal to the output current of the grid-tied inverter. On the other hand, the high current ripple increases the need for devices with large chip areas and low on-resistance to reduce its conduction loss. However, the large chip area of semiconductor devices means an increase in parasitic capacitance, which finally leads to an increase in the negative and main current peak values.

In order to evaluate the contribution of the proposed strategy to the improvement of this tradeoff, the conduction loss of semiconductor devices with different chip areas is estimated under a set of converter specifications as 400 W of rated power, $V_{\rm dc} = 360$ V and $V_{\rm ac} = 200$ V. The results are shown in Fig. 11. It should be mentioned that the relative chip area, α, is defined based on a specific GaN-HEMT device, that is GS66504B from GaN Systems with 650V/15A ratings. The output parasitic capacitance is assumed to be the same as that shown in Table I, and its on-state resistance is assumed to be 258 mΩ. In addition, it is regarded that the on-state resistance is inversely proportional to α, and the parasitic capacitance value is proportional to α. In

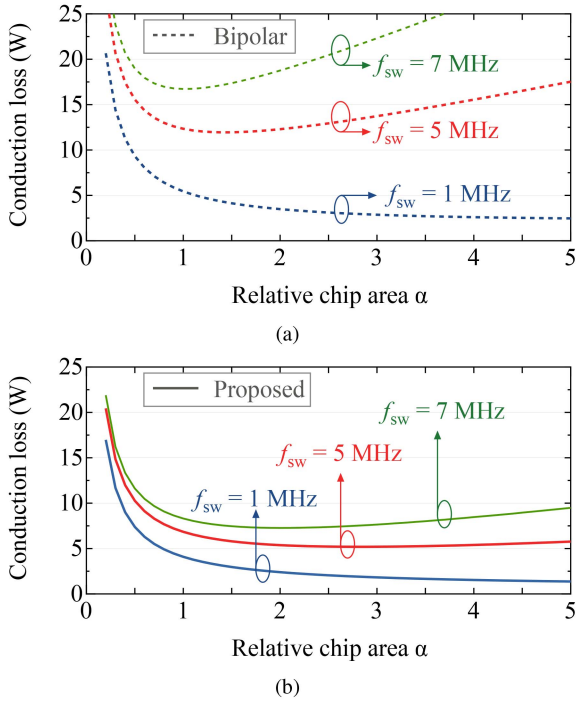

Fig. 11. Estimated conduction loss of a 400 W rated DCM-inverter in dependence of the relative chip area α and for three considered switching frequencies, $f_{\rm sw}$. (a) With bipolar modulation. (b) With proposed modulation strategy.

order to evaluate the effect of operating frequency, the losses as function of α with three switching frequencies: 1 MHz, 5 MHz, and 7 MHz, were estimated.

Although using semiconductor devices with larger chip area can reduce the conduction loss in the DCM-operated inverter, the increased parasitic capacitance can cause problems at a certain point. As shown in Fig. 11(a), the conduction loss continuously decreases as the relative chip area increases when the switching frequency is set at 1 MHz. This is expected since the on-resistance is reduced and the conduction loss is correspondingly reduced. However, the conduction loss increases when the switching frequency is set at 5 MHz, even though the on-resistance decreases. The dramatic increase in peak-to-peak current ripple is the cause of this phenomenon. It can be observed that the problems mentioned above become more severe as the switching frequency increases. It is demonstrated that further high-frequency operations of DCM-operated inverters have limitations due to the continuously increasing current ripple even with ZVS.

On the other hand, as shown in Fig. 11(b), it can be observed that with the proposed strategy, a significant loss reduction for each switching frequency can be observed. Especially for 7 MHz, the loss is less than half that of the bipolar modulation. Moreover, the trends of increasing conduction loss with the proposed strategy, both in terms of frequency and chip area, are slower than those of the bipolar modulation. It can be concluded that the proposed modulation strategy is more suitable for DCM grid-tied inverters because it can significantly reduce conduction losses compared to that with the bipolar modulation

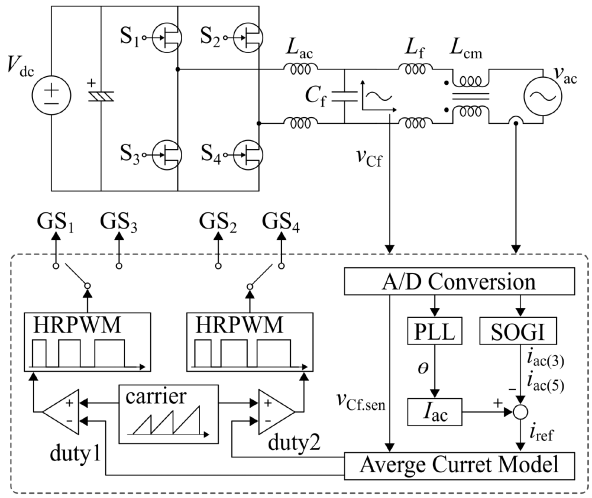

Fig. 12. Simplified system structure of the experimental prototype of the single-phase grid-tied inverter.

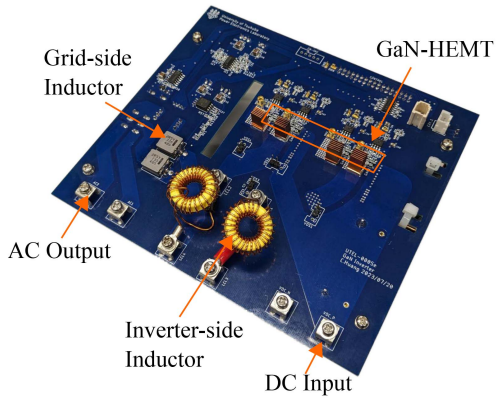

Fig. 13. Overview of the fabricated single-phase inverter.

especially for the designs with very high switching frequency and/or reduced on-resistance of semiconductor devices.

In general, the turn-OFF operation of semiconductor devices is accompanied by the charging and discharging of parasitic capacitance, and the charge is transferred by the current flowing through the inductor; therefore, it increases the peak currents in DCM operations. The bipolar modulation makes the parasitic capacitance of all semiconductor devices be fully charged and discharged, resulting in the highest current ripple. On the other hand, the proposed modulation strategy can modify the number of device involved in the LC resonance loop and also control the state of charging and discharging to decrease the impact of the parasitic capacitance on the peak current. The estimation results reveal the effectiveness of the proposed modulation strategy in controlling the charging and discharging of the parasitic capacitance, and confirm that it can be a key technique to achieve further high frequency operations with this approach.

V. Experimental Verification

A. Experimental Setup

To verify the proposed ZVS modulation strategy for MHz-operated GaN inverters, a 400-W prototype was fabricated and implemented. The system structure of the experimental prototype of the single-phase grid-tied inverter operated in the DCM is shown in Fig. 12. For the control, a DSP based microcontroller (TMS320F28335) was used. To achieve an enough accuracy of the turn-ON time and switching cycle for MHz-operations, high-resolution PWM modules in the microcontroller were used. Two reference signals representing turn-ON duration were compared with a common single-edge carrier to generate gate signals for the trapezium-like current modulation, then the signals were allocated to two devices in accordance with the line phase. A reference current synchronized in phase with the grid voltage through a phase locked loop was given. All the calculations run every 50 μs by a 20 kHz timer interrupt, to ensure enough calculation resources. It is important to note that this implementation of the calculation cycle, which is that the sampling frequency is lower than the switching frequency, brings a delay of the capacitor voltage used for the calculation, $v_{\mathrm{Cf.sen}}$. As discussed in Section II-A, the delay ensures the stability of the DCM inverter operated with the feedforward control based on the average current model.

Although the main current control was based on the feedforward control, a current sensor was connected to the grid-side inductor to perform a low-order harmonic compensation. Huang et al. [22] reported that the output current of DCM-operated power inverters can still be distorted even with enough accurate model considering the time required for charging and discharging and nonlinearity of the parasitic capacitance due to remaining errors. One such error is caused by the misalignment and nonlinearity of inductor parameters. Another possible reason is the time delay of the gate signals. It has been reported that the distortion becomes significant when the inverters are operated at very low instantaneous power, such as zero-crossing of the ac line voltage, and is mainly composed by low-order harmonics, such as third- and fifth-order harmonics [31].

In the following experiments, a supplemental feedback control was applied to compensate for the remaining distortion in addition to the use of precise average current model proposed in [22]. The second-order generalized integrators (SOGIs) [34] were used to extract third- and fifth-order harmonic components, $i_{\mathrm{ac}(3)}$ and $i_{\mathrm{ac}(5)}$, in the current, and those are subtracted from the original current reference. It should be mentioned that the use of SOGI is intended to compensate for steady-state current distortions; therefore, it can be achieved with a low gain. Consequently, SOGI is not a concern when conducting stability analysis for the current control of DCM inverters.

The main circuit parameters are the same with those listed in Table I. GaN-HEMT devices (GaNSystems GS66504B, 650 V, 15 A) were selected for the prototype. The overview of the fabricated prototype is shown in Fig. 13. The inverter-side inductors were made of a toroidal type core, whose parameters are listed in Table II. In addition, an EMI filter was connected to the ac side of the inverter to suppress common mode EMI in the experiment. This was especially needed for the unipolar and the proposed modulation strategy.

TABLE II
TOROIDAL INDUCTOR PARAMETERS

Core material	-	Mix-06 (Micrometals)
Core type	-	T80
Cross section area	A_e	0.231 cm^2
Core volume	V_e	1.19 cm^3
Relative permeability	μ_i	8.5
Inductance factor	A_L	4.5 nH/N^2
Number of turns	N	25
Total inductance	L_{ac}	3.4 μH×2
Steinmetz parameters	α, β, k_i	1.0, 2.1, 0.24

TABLE III
THREE MODULATION STRATEGIES

Modulation strategies	$2v_{ac} < V_{dc}$	$2v_{ac} \geq V_{dc}$
Bipolar	bipolar	bipolar
Hybrid	bipolar	unipolar
Proposed	trapezium-like current	unipolar

B. Performance Evaluation of Current Ripple Reduction and ZVS Achievement

The experiments were conducted to evaluate three modulation strategies including the bipolar, hybrid proposed in [27], and the proposed strategy as listed in Table III. The experiments aimed at to verify the advantage of the proposed strategy in comparison to the bipolar modulation. In addition to that, results with the hybrid modulation and the proposed strategy were compared with each other in order to highlight the loss reduction of the proposed trapezium-like current modulation applied in low ac voltage phase.

The experimentally measured waveforms with the bipolar modulation, hybrid modulation, and proposed modulation strategy at the rated current operation are shown in Fig. 14. It can be observed that the peak values of i_{Lac} with the proposed method were lower than those with the bipolar modulation and hybrid modulation in entire ac line phase angle. A significant current ripple reduction with the proposed strategy was achieved especially in the low ac voltage phase. This clearly indicates the advantage of the proposed strategy. It was also confirmed that the experimental results were in good agreement with the calculation results shown in Fig. 10(a).

To evaluate the ZVS performance of the discussed modulations including the proposed strategy, the drain-source voltage of one device, v_{S1}, and the inverter-side inductor current, i_{Lac}, were measured. The measured voltage and current waveforms with the proposed strategy under the rated current operation are shown in Fig. 15. When the ac line phase was close to 90°, the inverter was operated with the unipolar modulation. It was observed from Fig. 15(a) that the oscillation of v_{S1} reached almost zero and the ZVS operation was achieved. On the other hand, Fig. 15(b) shows those of the phase near to 30°, where the inverter was operated with the trapezium-like current modulation. The current shape became a trapezium waveform, and the oscillation of v_{S1} could also reach almost zero. It could also be observed that the oscillation cycles were different between two modulations.

The waveforms of v_{S1} and i_{Lac} were also measured when the DCM-inverter operated at a light load condition (50 W) with

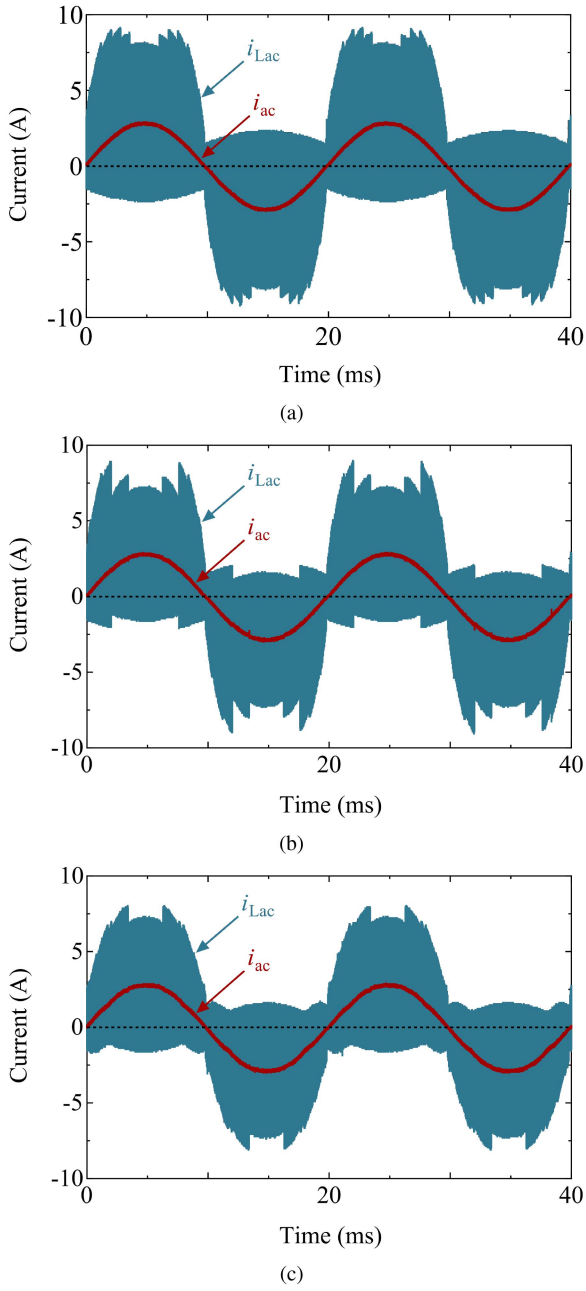

Fig. 14. Experimental waveforms of i_{Lac} and i_{ac} at the rated current in line cycle view with (a) bipolar modulation, (b) hybrid modulation, and (c) proposed strategy.

the proposed strategy. The inverter has longer oscillation period for the light load condition; therefore, this condition can clarify the ZVS performance among modulations. Fig. 16(a) shows the measured waveforms when the ac line phase was close to 45°, where the inverter was operated with the unipolar modulation. On the other hand, Fig. 16(b) shows those of the phase near to 30°, where the inverter was operated with the trapezium-like current modulation. Oscillations of v_{S1} and switchings performed at the bottom of the oscillation, which is referred to as valley switching, could be observed in both modulations; however, the oscillation was slightly damped with the unipolar modulation;

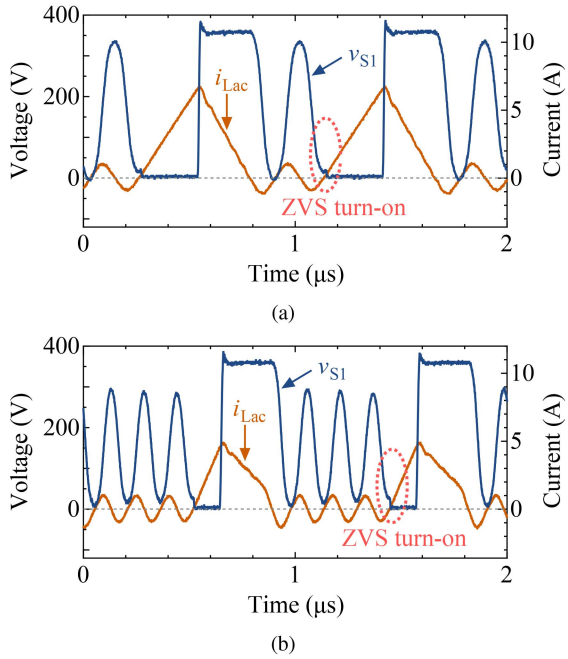

Fig. 15. Measured drain-source voltage of one device, v_{S1}, and inverter-side inductor current, i_{Lac}, when the inverter operated at the rated power (400 W) with the proposed strategy (a) when AC line phase was close to 90° and (b) when AC line phase was close to 30°.

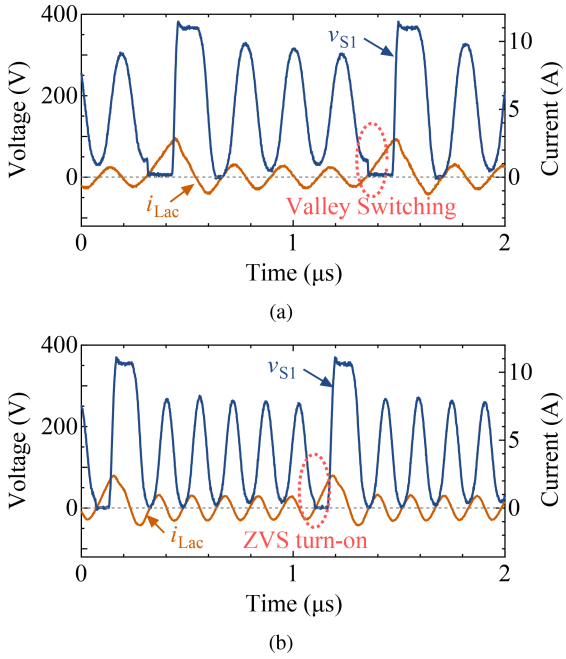

Fig. 16. Measured drain-source voltage of one device, v_{S1}, and inverter-side inductor current, i_{Lac}, when the inverter operated at a light load condition (50 W) with the proposed strategy (a) when AC line phase was close to 45° and (b) when AC line phase was close to 30°.

on the other hand, the oscillation with the trapezium-like current modulation can last for long time. This is caused by the difference in resonance loop. The dc-side capacitor is involved into the resonance with the unipolar modulation [27]; therefore, parasitic resistance on the resonance circuit can be increased.

For further evaluation of the overall ZVS performance of the three modulation strategies, the turn-ON voltages of the device in all the switching cycles under the light load condition (50 W) were extracted from the measured waveforms over half of an ac line cycle. The results are shown in Fig. 17. It can be observed that the turn-ON voltages of the device with all three methods were sufficiently low in comparison to the dc supply voltage. Especially for the bipolar modulation, the turn-ON voltages were extremely close to zero for all the ac line phase. On the other hand, the turn-ON voltages became slightly higher around 45° of the ac voltage phase, where the modulation was changed to the unipolar modulation in the hybrid modulation and the proposed strategy. The reason can be thought as the stronger damping of the oscillation in the unipolar modulation and longer oscillation period introduced for the line phase far from 90°. It can also be observed that the turn-ON voltages during the phase with the bipolar modulation were still close to zero even with the hybrid modulation. The trapezium-like current modulation in the proposed strategy could also achieve nearly perfect ZVS operations. This is because it has the same resonance loop as that of the bipolar modulation.

The energy loss due to the nonperfect ZVS operations is evaluated by the function, E_{oss}, which can be expressed as

$$E_{oss} = \int_0^{V_{ds}} v C_{oss}(v) dv. \tag{26}$$

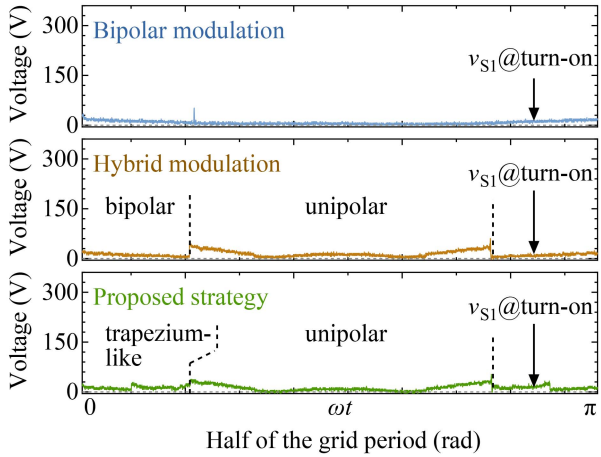

Fig. 17. Extracted instantaneous turn-ON voltages from measured waveforms of the device voltages with the bipolar modulation, hybrid modulation, and proposed strategy.

It defines the energy stored in the parasitic capacitance of the switching devices when its charged voltage is V_{ds}. It dissipates at turn-ON instant; therefore, it can represent the energy loss due to the nonperfect ZVS by giving the turn-ON voltages as V_{ds}. It can be calculated from the voltage-dependent characteristics of C_{oss}, which can be measured or are provided by manufacturers. The power loss can be derived by integrating E_{oss} for all the turn-ON instants with the measured turn-ON voltages shown in Fig. 17.

The power loss caused by the nonperfect ZVS operations with the bipolar, hybrid, and proposed modulations were estimated

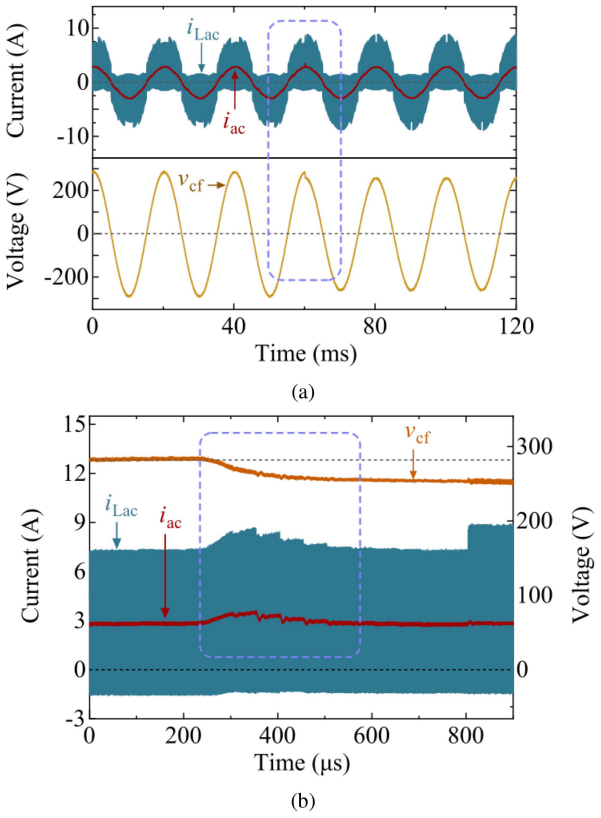

Fig. 18. Transient response for a step-down change of the gird voltage from 100% to 90%, shown in (a) line cycle view and (b) switching cycle view.

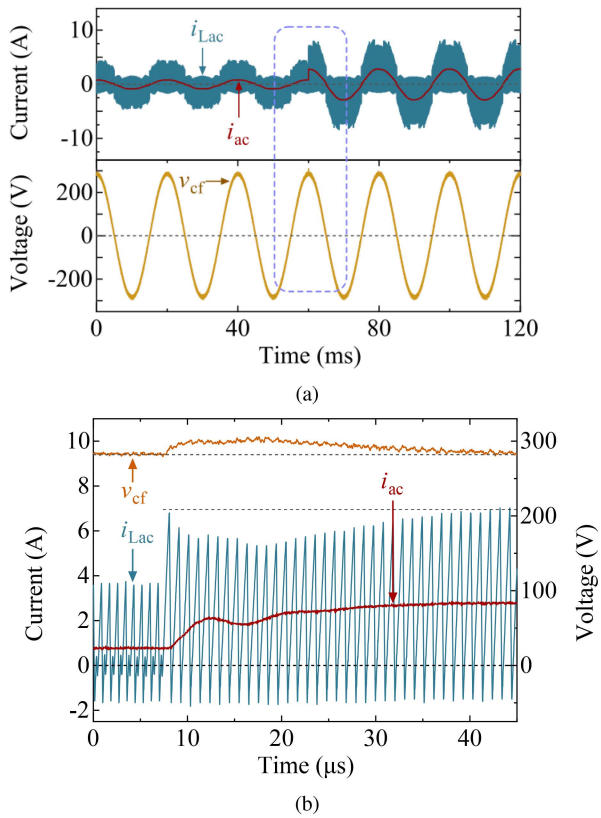

Fig. 19. Transient response for a step-up change of the current reference from 25% to 100% in (a) line cycle view and (b) switching cycle view.

to be 0.03 W, 0.07 W, and 0.08 W, respectively. These losses can be considered to be negligible when they are compared to $E_{\rm oss}$ under the full hard switching, in which the turn-ON voltage is equal to $V_{\rm dc}$, that is approximately 6 W. It makes sense since $E_{\rm oss}$ is roughly linear to the square of the voltage. Consequently, the damping of the oscillation is not an important issue from the point of conversion efficiency.

C. Dynamic Performance Tests

Previous experimental investigations have shown that the proposed modulation strategy can properly operate under steady-state and reduce the current ripple in comparison with the other modulations. This section discusses the transient response of the proposed control scheme to give a clear view of the control capability.

Fig. 18 shows the transient response for 10% step change in the grid voltage, $v_{\rm ac}$, with the proposed modulation strategy. Note that the step change was intentionally set to occur at the peak of $v_{\rm ac}$ to evaluate under the worst case. After the step change, variations in the filter capacitor voltage, $v_{\rm Cf}$, and grid-side current, $i_{\rm ac}$, were observed; however, no significant transient oscillations occurred. This result indicates system stability.

Fig. 19 shows the transient response for a step change in the current reference from 0.25 A (0.125 p.u.) to 2.0 A (1.0 p.u.) with the proposed modulation strategy. It can clearly be observed that the grid current $i_{\rm ac}$ can keep its stability after the step change. It could be observed that $i_{\rm Lac}$ could follow the step change immediately; however, $i_{\rm ac}$ could not respond as fast as $i_{\rm Lac}$. It is reasonable because the response of $i_{\rm ac}$ is limited by the CL filter consisting of $L_{\rm f}$ and $C_{\rm f}$. At the same time, a natural resonance at the frequency determined by the CL filter was observed. As explained in Section II-A, the resonance was quickly decayed in a few oscillation cycles due to the inherent feedback mechanism. The above experimental results confirmed the damping effect by the inherent feedback loop.

D. Inductor Loss Estimation for DCM

The inductor current ripple is directly related to the power loss at the inductor and the conduction loss of the GaN-HEMT devices. The conduction loss can easily be calculated by the current flowing through the device and the on-state resistance of the device, $R_{\rm on}$, which is provided by the manufacturer. However, the inductor loss is difficult to predict especially for the high frequency operated DCM inverters [35].

In order to investigate the effect of the current ripple reduction on inductor losses, the core and winding losses were estimated for the DCM-operated inverters. Assuming that the inductor is designed to operate in the linear region, an improved generalized Steinmetz equation (iGSE) can be used to estimate the inductor core loss as

$$P_{\rm v} = \frac{1}{T}\int_0^T k_{\rm i} \cdot \left|\frac{dB}{dt}\right|^{\alpha} \cdot |\Delta B|^{\beta-\alpha} dt \qquad (27)$$

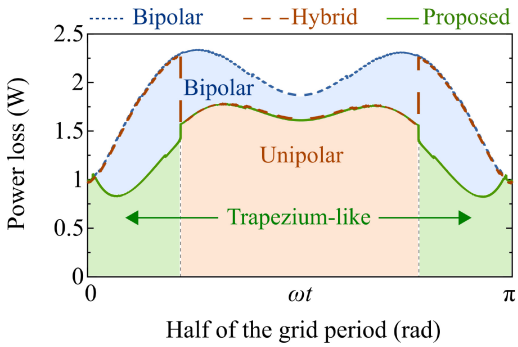

Fig. 20. Estimated power losses of inductor core with the bipolar modulation, hybrid modulation, and the proposed strategy.

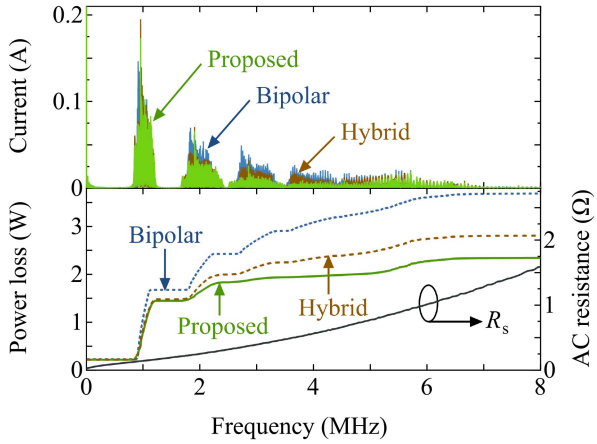

Fig. 21. Spectra of the harmonic components of i_{Lac}, measured ac resistance of the inductor winding, R_{s}, and the calculated winding losses with three modulations. The losses indicate those generated by the harmonic current components the frequency of which is lower than the frequency indicated by the x-axis.

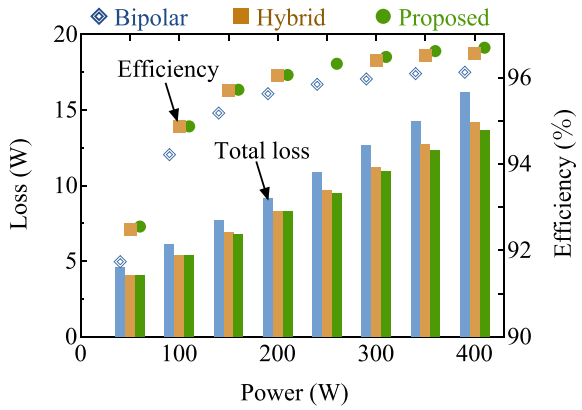

Fig. 22. Measured efficiencies and total losses with the bipolar modulation, hybrid modulation, and proposed strategy.

where α, β, and k_{i} are the Steinmetz parameters of the inductor, and P_{v} is the power loss per volume. The basic principle of the iGSE is to divide the inductor core losses based on different excitation conditions and calculate them individually. The analytical current models provided in Section IV-A can be used to calculate the core losses with the DCM-operated inverters. The power loss generated during each section of the inductor current was calculated piecewise, and the losses from all sections were summed up and averaged over one switching cycle.

Fig. 20 shows the estimated core losses under the rated current operation as function of the line phase with the bipolar modulation, hybrid modulation, and the proposed strategy. The calculated values are based on the specifications of the fabricated converter for experiments, which are listed in Table I. Core material and its Steinmetz parameters used for the calculation are listed in Table II. As shown in Fig. 20, it can be observed that the proposed strategy can achieve lower core loss than the bipolar modulation owing to the lower current ripple. In addition, it achieves lower core loss than the hybrid modulation owing to the loss reduction in the trapezium-like current modulation part.

The average values of the core losses over a half line cycles with the bipolar modulation, hybrid modulation, and the proposed strategy were 1.93 W, 1.72 W, and 1.40 W, respectively. The hybrid modulation and the proposed strategy can reduce the overall core loss by 11% and 28%, respectively, in this case.

In contrast to the core loss, the winding loss is considered to be linear to the rms values of the inductor current; therefore, it can be calculated by measured ac resistance as function of frequency and harmonic components of the current. The ac resistance of the fabricated inductor was measured using an impedance analyzer (Keysight Technologies E4990 A), and the results are shown in Fig. 21. Based on the ac resistance, the winding loss with three different modulations were calculated.

Fig. 21 shows the calculated winding losses. The upper part of the graphs shows the spectra of the inductor current, i_{Lac}, from 0 to 8 MHz. To clarify the contribution of frequency components of the current to winding loss, the losses shown in Fig. 21 indicates those generated by the harmonic current components the frequency of which is lower than the frequency indicated by the x-axis. It can be observed that the contribution of the current components around 1 MHz to the winding losses were almost the same among the three modulations; however, the proposed strategy has lower winding loss than the others owing to the reduced contribution of the frequency components between 1.5 and 6 MHz. It is owing to the relatively not sharp current shapes by the unipolar and trapezium-like modulations in comparison to that by the bipolar modulation. Consequently, the overall winding loss with considering up to 8 MHz could significantly be reduced by 35% in this case.

E. Efficiency Comparison and Loss Analysis

In order to evaluate the efficiency improvement of the DCM-operated inverter by the proposed strategy, the input and output power were measured by a power analyzer (HIOKI PW8001). The measured efficiencies and the total losses of the fabricated inverter are shown in Fig. 22. It can be observed that significant loss reductions were achieved by the hybrid modulation and the proposed strategy in comparison to the bipolar modulation. The total loss was reduced by 2.0 W with the hybrid modulation, and its efficiency at the rated power operation was 96.5%. The proposed strategy achieved further loss reduction, which was

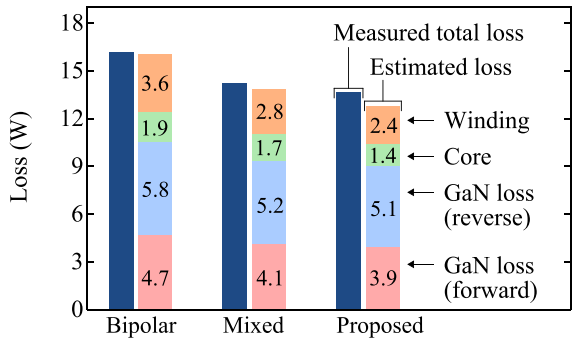

Fig. 23. Measured total losses and estimated loss distribution with the bipolar modulation, the hybrid modulation, and the proposed strategy.

2.6 W in comparison to the bipolar modulation. The efficiency was 96.7%, which was the highest efficiency among the discussed modulations.

To confirm the reason for the loss reduction, the power losses at the rated current operation were analyzed. Fig. 23 shows the estimated loss break-downs in comparison with the measured total losses. The estimated results obtained in Section V-D were used for this discussion regarding the inverter-side inductor losses. In contrast, the loss generated at the grid-side inductors was assumed to be negligible because the current flowing through them had continuous sinusoidal waveform without high current ripples. To estimate the losses generated at semiconductor devices, the current flowing into the devices is needed to know; however, it is very difficult to measure the current flowing into GaN-HEMT devices directly in such a high-frequency operation; therefore, the conduction losses of the devices were calculated from the waveforms obtained by a time-domain simulation. It was assumed that the turn-ON loss can be neglected owing to the ZVS operations by the off-time discrete control, as mentioned in Section V-B. In addition, the energy loss generated by the parasitic capacitance, which is included in the turn-OFF loss, does not dissipate with the ZVS turn-ON. It has been reported that the energy loss generated by the parasitic capacitance dominates the turn-OFF energy loss in the GaN-HEMT devices that were used in this experiment [7], [8]; therefore, it was assumed that the turn-OFF loss can also be neglected.

Based on the above assumptions, the sum of the estimated losses at semiconductors and the inductor was reduced by 2.2 W and 3.3 W with the hybrid modulation and the proposed strategy, respectively. The reductions in the measured total loss roughly agreed with the reductions in the estimated losses. The differences between the estimated and measured losses, which are the unspecified power losses, were extremely low; therefore, it can be confirmed that the loss estimation and its break-downs are reliable. In particular, it proves that the switching loss can actually be negligible when the ZVS by the off-time discrete control is applied.

It should be mentioned that the loss difference between the hybrid modulation and the proposed strategy was 0.6 W. This may be thought to be minor; however, it is about 25% of the total loss reduction. It can be considered that the loss reduction represents the advantage of the current ripple reduction by the trapezium-like current modulation well despite being used for a relatively small portion in the total switching cycles.

VI. Conclusion

This article proposed an improved trapezium-like current modulation for the DCM-operated single-phase full-bridge inverter to achieve ZVS with low current ripple. The minimum turn-OFF current that can realize ZVS was analyzed and implemented to the proposed strategy. The experimental results with the proposed strategy and conventional modulations were compared with each other to demonstrate the effectiveness of the inductor current ripple mitigation. The proposed strategy demonstrated its effectiveness as the efficiency improvement in the fabricated inverter. The estimation of the loss reduction agreed well to the experimentally measured loss reduction; therefore, it is possible to estimate the advantages of the proposed strategy for other designs, for example, those with much higher switching frequency, and much higher power capacity with different GaN-HEMT devices.

In general, there is an unavoidable tradeoff relationship between the current ripple and ZVS capability in DCM-operated inverters with conventional modulations. A thorough understanding of the charging and discharging behavior of the device parasitic capacitance has enabled a way to improve the tradeoff relationship, i.e., ZVS operation at low current ripple. The method proposed in this article is considered to be significant progress in developing a more efficient ZVS realization by resolving the tradeoff.

Appendix

To simplify the analysis, the total delay time is denoted as $T_{\rm delay}$, and the sampling process is modeled as a first-order delay, where $v_{\rm Cf.sen}$ can be expressed as

$$v_{\rm Cf.sen} = \frac{v_{\rm Cf}}{1 + sT_{\rm delay}} \tag{28}$$

where s is a complex variable, and $v_{\rm Cf.sen}$ and $v_{\rm Cf}$ are expressed in s-domain.

Here, $I_{\rm ref0}$, $T_{\rm on0}$, and $V_{\rm Cf.sen0}$ denote the operating points of the reference current, on-state time, and sampled capacitor voltage, respectively. In contrast, $\Delta v_{\rm Cf.sen}$, $\Delta i_{\rm ref}$, and $\Delta T_{\rm on}$ represent their small-signal perturbations, then (2) can be expressed as

$$(I_{\rm ref0} + \Delta i_{\rm ref}) \cdot \frac{V_{\rm dc} + V_{\rm Cf.sen0} + \Delta v_{\rm Cf.sen}}{V_{\rm dc} - V_{\rm Cf.sen0} - \Delta v_{\rm Cf.sen}} \cdot \frac{T_{\rm sw} L_{\rm ac}}{V_{\rm dc}} = (T_{\rm on0} + \Delta T_{\rm on})^2. \tag{29}$$

By subtracting the steady-state equation from the perturbed equation, a small-signal model that relates $\Delta i_{\rm ref}$ and $\Delta v_{\rm Cf.sen}$ to $\Delta T_{\rm on}$ can be obtained, as expressed by

$$\frac{2V_{\rm dc} I_{\rm ref0}}{(V_{\rm dc} - V_{\rm Cf.sen0})^2} \cdot \Delta v_{\rm Cf.sen} + \frac{V_{\rm dc} + V_{\rm Cf.sen0}}{V_{\rm dc} - V_{\rm Cf.sen0}} \cdot \Delta i_{\rm ref} = \frac{V_{\rm dc}}{T_{\rm sw} L_{\rm ac}} \cdot 2T_{\rm on0} \cdot \Delta T_{\rm on}. \tag{30}$$

Consequently, the nonlinear part in the calculation of $T_{\rm on}$ from the sampled voltage $v_{\rm Cf.sen}$ is linearized for further analysis.

In the same manner, the relationship between the small-signal variations in $T_{\rm on}$ and $\overline{i_{\rm Lac}}$ can be derived. Here, $V_{\rm Cf0}$ and $\overline{I_{\rm Lac0}}$ denote the operating points of the capacitor voltage and average current of the inductor current, respectively. In contrast, $\Delta v_{\rm Cf}$ and $\Delta\overline{i_{\rm Lac}}$ represent their small-signal perturbations. By rewriting (2) to include these perturbations and subtracting the steady-state equation, a small-signal model relating $\Delta T_{\rm on}$ to $\Delta\overline{i_{\rm Lac}}$ can be obtained, which can be expressed as

$$\frac{-2V_{\rm dc}{T_{\rm on0}}^2}{(V_{\rm dc}+V_{\rm Cf})^2}\cdot\Delta v_{\rm cf}+\frac{V_{\rm dc}-V_{\rm Cf0}}{V_{\rm dc}+V_{\rm cf0}}\cdot 2T_{\rm on0}\cdot\Delta T_{\rm on}=\frac{T_{\rm sw}L_{\rm ac}}{V_{\rm dc}}\cdot\Delta\overline{i_{\rm Lac}}. \tag{31}$$

By substituting (31) into (30) and applying the relationship described in (28), a fully linearized small-signal model from $\Delta v_{\rm Cf}$ to $\Delta\overline{i_{\rm Lac}}$ can be derived and expressed as

$$\Delta i_{\rm ref}-\frac{2{V_{\rm dc}}^2{T_{\rm on0}}^2}{T_{\rm sw}L_{\rm ac}(V_{\rm dc}+V_{\rm Cf0})^2}\cdot\left(1-\frac{1}{1+sT_{\rm delay}}\right)\cdot\Delta v_{\rm Cf}=\Delta\overline{i_{\rm Lac}}. \tag{32}$$

Note that the operating point $V_{\rm Cf.sen0}=V_{\rm Cf0}$ was assumed in deriving the above equation.

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