Bang-Bang Pulse Magnitude Modulation and Binary Search Tree-Based Voltage Balancing Method of Multilevel Inverter for Wireless Power Transfer

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***Abstract*—The delta-sigma pulse magnitude modulated multilevel inverter-based wireless power transfer systems are suitable for high-power applications to realize zero voltage switching (ZVS) and continuous output, but the resolution is fixed, and the heavy computational burden of the voltage balancing algorithm is a concerning issue. To solve the above problems, first of all, a bang-bang pulse magnitude modulation (BBPMM) method is proposed for the multilevel inverter-based wireless power transfer (WPT) system. The resolution of the proposed BBPMM is continuously adjustable, which is more flexible than the delta-sigma pulse magnitude modulation (PMM). Moreover, it is found that the BBPMM WPT system can decrease the ripple and total harmonic distortion of the inverter current in a wide range by adjusting the resolution compared with the delta-sigma PMM WPT system. Second, this article proposes a binary search tree-based capacitor voltage balancing method for the flying capacitor multilevel inverter in the WPT system. It combines the online and offline processes of the capacitor voltage balancing method to simplify the algorithm online in a control cycle. Furthermore, theoretical analysis, computer simulation, and a 1.5-kW seven-level flying capacitor inverter-based hardware experimentation are given to verify the effectiveness of the proposed BBPMM flying capacitor multilevel inverter-based WPT system.**

***Index Terms*—Bang-bang pulse magnitude modulation (BBPMM), capacitor voltage balance, multilevel inverter, wireless power transfer (WPT), zero voltage switching.**

I. Introduction

WIRELESS power transfer (WPT) technology, dating back to the pioneering work of Nikola Tesla over a century ago, has seen widespread adoption across various industries, spanning power levels from milliwatts to megawatts [1], [2], [3]. Its applications range from charging micro-robots and electric toothbrushes to powering electric vehicles [4] and high-speed trains [5]. The key advantages of this technology, such as the capability of providing electrical isolation, enhanced safety, convenience, and a great user experience, are among the main factors that increase its popularity. The WPT has attracted many academic researchers and engineers to actively explore its vast potential.

In recent years, the multilevel inverter-based WPT system has garnered increasing interest due to the advantage of a large operating range [6], [7] and breaking voltage limitations [8], [9]. These systems have been extensively researched for various applications. For example, it has been studied for low-voltage EV charging whose loading conditions can vary up to 450% [6], [7]. Besides, a medium-voltage dc distribution network (ranging from 1.5 to 50 kV) is commonly utilized for high-power applications to reduce the dc-bus current [10], such as submarine, data center, and fast EV charging. By integrating multilevel inverter-based WPT systems into medium-voltage dc-power networks, the voltage stress on individual semiconductor components can be minimized [12]. Furthermore, multilevel inverter-based multichannel WPT systems can simplify system configurations and eliminate coupling transformers [13].

However, the modulation and capacitor voltage balancing methods in multilevel inverter-based WPT systems are important issues. Further research is required to delve deeper into these critical issues and improve the system performance.

In recent developments, various modulation schemes for two-level inverter-based WPT systems have been thoroughly investigated. These schemes encompass pulsewidth modulation (PWM), ON-OFF keying modulation, hybrid modulation, pulse density modulation (PDM), pulse frequency modulation (PFM), and step density modulation (SDM). Among these, regarded as a PWM with adjustable angles, phase-shift control [14], [15], [16] is commonly used in the WPT system. However, it is plagued by hard switching issues. ON-OFF modulation regulates the output power of the WPT system by using low-frequency duty ratios, but it introduces significant output ripples. Hybrid modulation [17], which combines PFM and ON-OFF modulation, faces similar challenges. In contrast, PDM [18], [19], [20], [21], [22] and PFM are generally investigated in the WPT systems for their ability to overcome these limitations. To address these challenges, a low-subharmonic, full-range, and rapid PDM strategy [20] has been proposed for WPT systems based on full-bridge

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converters. In addition, the PFM is proposed in [23], [24], [25], and [26] for WPT systems to regulate the output power through higher-order harmonics of the square wave at specific frequencies, among which, the Σ-Δ PFM is proposed in [24] to reduce output ripples of the dc-side voltage. More recently, the SDM [27] has shown promise in regulating the output power of the WPT systems by adjusting the step density, which combines both strengths of PDM and PFM.

Compared with the modulation methods of two-level converters for the WPT systems, the modulation methods of the multilevel converter for the WPT system are more flexible due to adding the freedom of magnitude. Multiple PWM waves of different frequencies are superimposed and used for the multilevel inverter-based multichannel WPT systems [13], but the modulation method has the problem of hard switching. The zero voltage switching (ZVS) modulation method of the MMC-based inductive power transfer system is proposed in [7]. It changes the number of submodules connected to the circuit to adjust the pulse magnitude of the MMC, but the output voltage of the MMC by using this modulation method can only be discrete. To solve this problem, our previous work proposes the Σ-Δ pulse magnitude modulation method and the token rotation-based capacitor voltage balancing method of the flying-capacitor multilevel inverter (FCMLI)-based WPT system [28], the output voltage can be continuously adjusted. However, first of all, the resolution of the Δ-Σ pulse magnitude modulation (PMM) is not adjustable, which could lead to a very long modulation period under some working conditions. Second, the algorithm needs to be completed in a very high-speed control cycle, which is half of the resonant cycle of the WPT system, but the algorithm of the token rotation-based capacitor voltage balancing method is complex, the computational burden is large, and the program operation takes up a long time, which limits the control frequency of the WPT system.

To further solve the above problems, this article proposed a novel implementation method of pulse magnitude modulation and a binary search tree (BST)-based capacitor voltage balancing method of the multilevel inverter for the WPT system, and the main contribution of this article is listed as follows:

1) The specially designed iterative functions, as shown in (4) and (5), are proposed, which can converge in each amplitude interval of PMM, and can fit and approximate the actual normalized voltage ratio of the output voltage of the multilevel inverter. Based on the iterative functions, a Bang Bang pulse magnitude modulation (BBPMM) of the multilevel inverter for the WPT system is proposed. The resolution of the proposed BBPMM for the FCMLI-based WPT systems can be adjustable, which is more flexible than the Δ-Σ PMM.
2) It is found that the BBPMM can reduce the THD and current ripple of the transmitter current in a wide range by adjusting the resolution, compared with the Δ-Σ PMM.
3) The BST-based capacitor voltage balancing method of the FCMLI for the WPT system is proposed to reduce the computational burden in the control cycle, which is more than two times faster than the conventional token rotation-based capacitor voltage balancing method.

The rest of this article is organized as follows. Section II presents the proposed BBPMM method of the FCMLI-based WPT system and its basic principle. Section III presents the switching state analysis of the FCMLI and the proposed BST-based capacitor voltage balancing method of the FCMLI for the WPT system. Section IV presents the experimental verification. Section V concludes this article.

II. Bang-Bang Pulse Magnitude Modulated Multilevel Inverter-Based WPT System

A. Description of the FCMLI-Based WPT System

Fig. 1 shows an n-level FCMLI-based WPT system, where $C_{\rm dc}$ are the dc-side capacitors; u_1, u_2, u_3, …, and u_{n-2} are the voltages of the flying capacitors C_{f1}, C_{f2}, C_{f3}, …, and C_{fn-2}; L_t and L_r are the inductances of the transmitter and receiver coils; R_t and R_r are the equivalent series resistances of the transmitter and receiver parts; M denotes the mutual inductance between the primary coil and the secondary coil; C_t and C_r are the capacitances of series compensated capacitors, respectively; $R_{\rm dc}$ and $C_{\rm dc1}$ are the dc-link load and capacitor of the diode rectifier. The FCMLI is fed by a dc input voltage $V_{\rm dc}$ and drives a series-series resonant tank.

The proposed control of the multilevel inverter consists of two parts: the proposed BBPMM and the flying-capacitor voltage balancing method. The voltages of the flying capacitors u_1, u_2, u_3, …, and u_{n-2} are sampled for capacitor voltage balancing. The proposed control of the FCMLI-based WPT system will be discussed in Sections II-B and III in detail. The resonant frequencies of the resonators on the two sides are as

$$f_r = \frac{1}{2\pi\sqrt{L_tC_t}} = \frac{1}{2\pi\sqrt{L_rC_r}}. \tag{1}$$

To equalize the voltage of each switch, the voltages of the zth flying capacitor $C_{\rm fm}$ of the FCMLI should be controlled as

$$V_c(z) = \frac{(n-1-z)\,V_{\rm dc}}{n-1} \tag{2}$$

where $z = 1, 2, \ldots, n-2$.

B. Proposed BBPMM Method

Fig. 2 shows the proposed BBPMM in one control cycle, which is half of the resonant cycle of the WPT system, where $m = n - 1$. First, the root mean square (rms) value of the fundamental component of the output voltage of a multilevel inverter can be defined as follows:

$$U_{1\_\rm BBPM} = \delta\frac{2V_{\rm dc}}{\pi} \tag{3}$$

where δ is defined as the normalized voltage ratio; $V_{\rm dc}$ is the dc-side voltage of the multilevel inverter.

Variable A in Fig. 2 is used to ensure that a 0 level is output for every other control cycle. It is noticed that the normalized voltage ratio δ defined in BBPMM is similar to the duty ratio defined in the PWM. The δ^* is the command value of the normalized voltage ratio for the BBPMM, ranging in [0, 1]. For the n-level multilevel inverter, there are n kinds of basic voltage pulses,

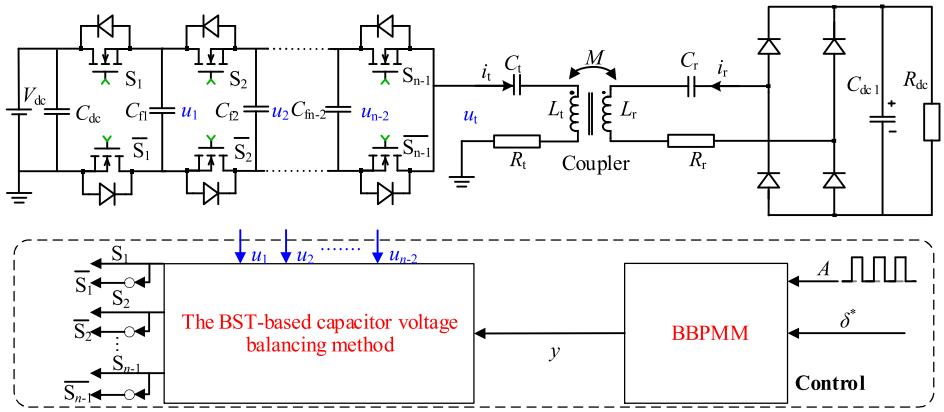

Fig. 1. BBPMM FCMLI-based WPT system.

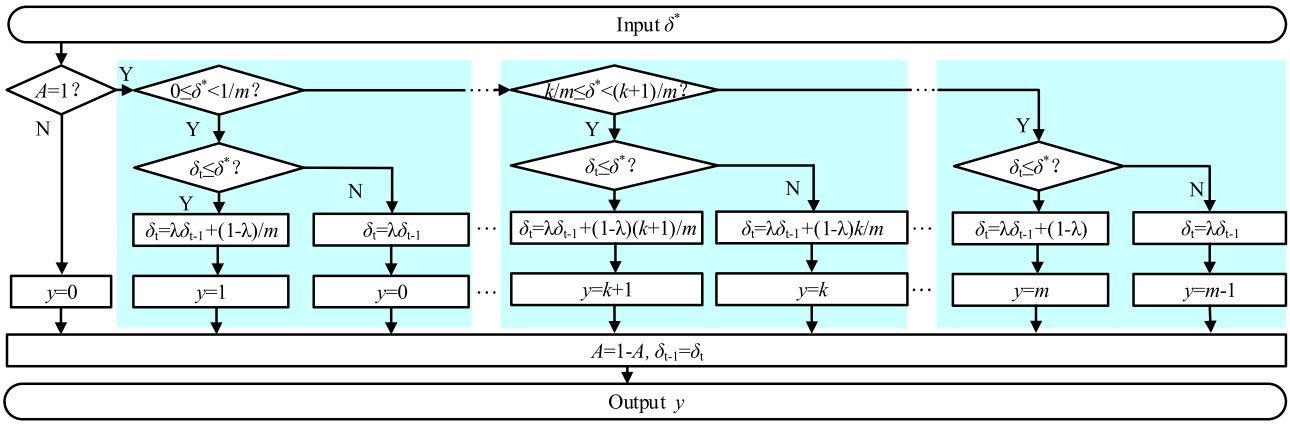

Fig. 2. Proposed BBPMM in one control cycle.

which can be expressed as "$\delta = 0,\ 1/m,\ 2/m,\ 3/m,\ \ldots,\ k/m,\ (k+1)/m,\ \ldots,$ and 1", and $m = n - 1$. The PMM uses the whole-wave voltage pulse with adjacent voltage magnitudes to construct the desired output voltage pulse. Thus, δ^* is divided into $n-1$ intervals: $[0, 1/m), [1, 2/m), \ldots, [k/m, (k+1)/m) \ldots, [1-1/m, 1]$. When $k/m \le \delta^* < (k+1)/m$, the output voltage consists of the voltage pulses with $\delta = k/m$ and $(k+1)/m$. When $k/m \le \delta^* < (k+1)/m$ and $\delta_t > \delta^*$, the normalized voltage ratio δ_t is calculated as

$$\delta_t = \lambda\delta_{t-1} + (1-\lambda)\, k/m \tag{4}$$

where δ_{t-1} is the normalized voltage ratio in the previous control cycle, and λ is defined as an attenuation factor ranging in (0, 1). In this case, the number of levels of the output voltage of the multilevel inverter is equal to k, denoted as $y = k$ in Fig. 2.

When $k/m \le \delta^* < (k+1)/m$ and $\delta^* \ge \delta_t$, the normalized voltage ratio δ_k is further calculated as follows:

$$\delta_t = \lambda\delta_{t-1} + (1-\lambda)\,(k+1)\,/m. \tag{5}$$

In this case, the number of voltage levels of the output voltage of the multilevel inverter is equal to $k+1$, denoted as $y = k+1$ in Fig. 2. It is noticed that δ_0 has to belong to (0, 1) to ensure the proper functioning of the proposed modulation method.

Furthermore, the basic principle of the proposed BBPMM will be explained clearly. In particular, it needs to be clarified how δ^* in BBPMM is proportional to the rms value of the fundamental component of the voltage output of the multilevel inverters. According to (4) and (5), while $0 < \delta^* < 1$, δ_t gradually increases or decreases to δ^*, then it remains in an interval. When $k/m \le \delta^* < (k+1)/m$, δ_t in the steady state is derived as

$$\lambda\delta^* + (1-\lambda)\, k/m \le \delta_t \le \lambda\delta^* + (1-\lambda)\,(k+1)\,/m. \tag{6}$$

First of all, as shown in Fig. 3, m_1 is defined as the difference between the maximum value of δ_t and the command value δ^*, and m_2 is defined as the difference between δ^* and the minimum value of δ_t. When $k/m \le \delta^* < (k+1)/m$, m_1 and m_2 can be calculated as follows:

$$m_1 = (1-\lambda)\,((k+1)\,/m - \delta^*) \tag{7}$$

$$m_2 = (1-\lambda)\,(\delta^* - k/m)\,. \tag{8}$$

According to (7) and (8), the width of the interval can be expressed as follows:

$$m_r = m_1 + m_2 = \frac{1-\lambda}{m}. \tag{9}$$

It can be found from (9) that λ determines the width of the interval, and a bigger λ will lead to a narrower width of the

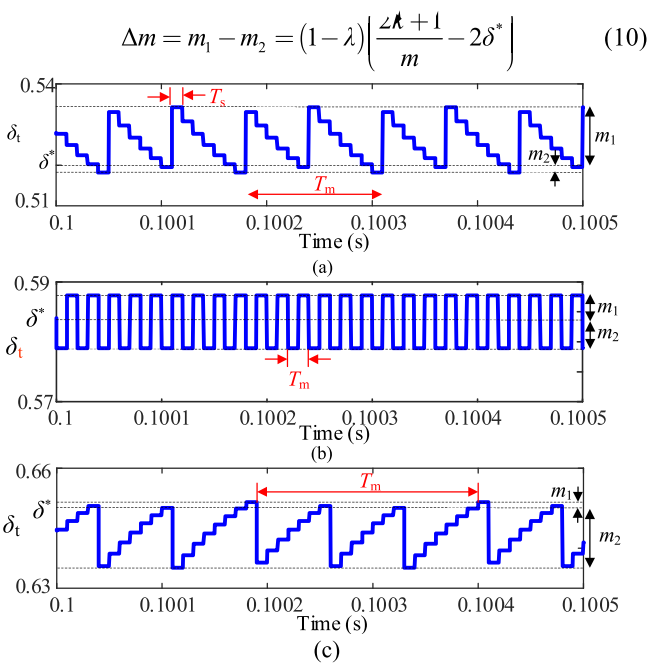

Fig. 3. Time-domain wave of δ_t for different δ^* when $\lambda = 0.9$. (a) $\delta^* = 0.55$. (b) $\delta^* = 7/12$. (c) $\delta^* = 0.65$.

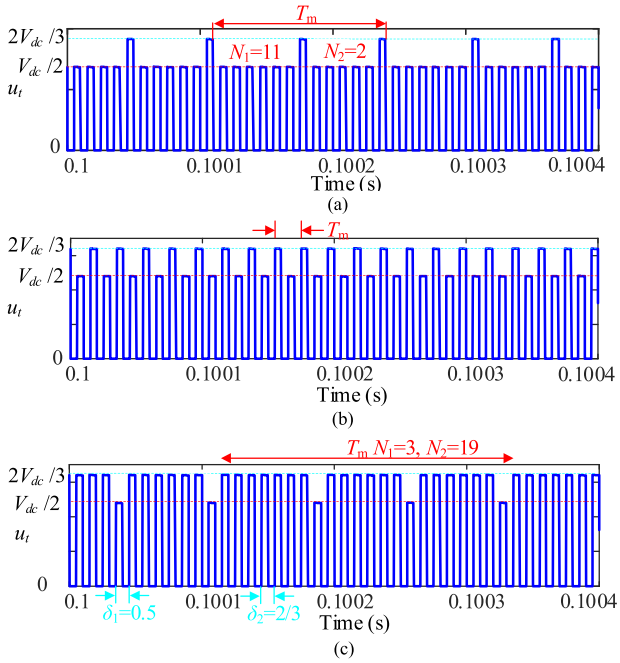

Fig. 4. Time-domain wave of u_t for the seven-level inverter-based WPT system when $\lambda = 0.9$. (a) $\delta^* = 0.52$. (b) $\delta^* = 7/12$. (c) $\delta^* = 0.65$.

interval. The control object of the proposed BBPMM is the difference between m_1 and m_2, which is defined as the weight factor of the voltage pulse with the adjacent magnitudes of the output voltage of the multilevel inverter:

$$\Delta m = m_1 - m_2 = (1-\lambda)\left(\frac{2k+1}{m} - 2\delta^*\right). \tag{10}$$

In the range of $[k/m, (k+1)/m)$, when $\delta^* = (2k+1)/(2m)$, $\Delta m = 0$, $m_1 = m_2$. In this case, the number of voltage pulses of different magnitudes is the same. For example, Fig. 3(b) shows the time-domain waveform of δ_k when $\delta^* = 7/12$ for the seven-level inverter-based WPT system, and Fig. 4(b) shows the corresponding output voltage of the multilevel inverter. When $k/m < \delta^* < (2k+1)/(2m)$, $\Delta m < 0$, $m_1 < m_2$. In this case, the density of voltage pulses with smaller amplitude is greater, as shown in Figs. 3(a) and 4(a). When $(2k+1)/(2m) < \delta^* < (k+1)/m$, $\Delta m > 0$, $m_1 > m_2$. In this case, the density of voltage pulses with greater amplitude is greater, as shown in Figs. 3(c) and 4(c). The weight factor Δm can proportionally change the density of voltage pulses with different magnitudes, which further affects the fundamental component of the output voltage of the FCMLI.

As shown in Fig. 3, the time between two adjacent maximum values or two adjacent minimum values of δ_k is the modulation period T_m. Correspondingly, as shown in Fig. 4, the output voltage consists of voltage pulses with two kinds of magnitudes. Thus, the normalized voltage ratio can be calculated as follows:

$$\delta_{\mathrm{PMM}} = \frac{N_1\delta_1 + N_2\delta_2}{N_1 + N_2} \tag{11}$$

where the N_1 and N_2 mean the numbers of the whole-wave voltage pulse with $\delta = \delta_1$ and $\delta = \delta_2$, respectively; $\delta_1 = 0.5$ and $\delta_2 = 2/3$ in Fig. 4.

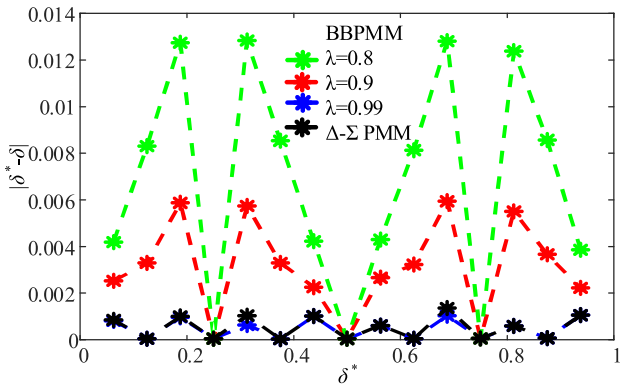

Fig. 5. Resolution of the BBPMM related to λ.

When N_1 and N_2 are coprime, the modulation period is the minimum solution. The modulation period of the BBPMM methods can be expressed as

$$T_M = (N_1 + N_2)\, T_S \tag{12}$$

where $T_s = 1/f_\tau$.

According to (11), it can be calculated that δ_{PMM} can be calculated as 0.5256, 7/12, and 0.6439. There is a deviation between the command value and the actual value. Furthermore, λ is a key variable that determines the resolution of the proposed BBPMM, meanwhile influencing the resolution of the output voltage. As shown in Fig. 5, the deviation is reduced when increasing λ, and the closer λ is to 1, the higher the resolution of the proposed modulation method. When $\lambda = 0.99$, the resolution of BBPMM is slightly higher than that of the Δ-Σ PMM. Both the proposed BBPMM and Δ-Σ PMM can reach the resolution of 0.0001.

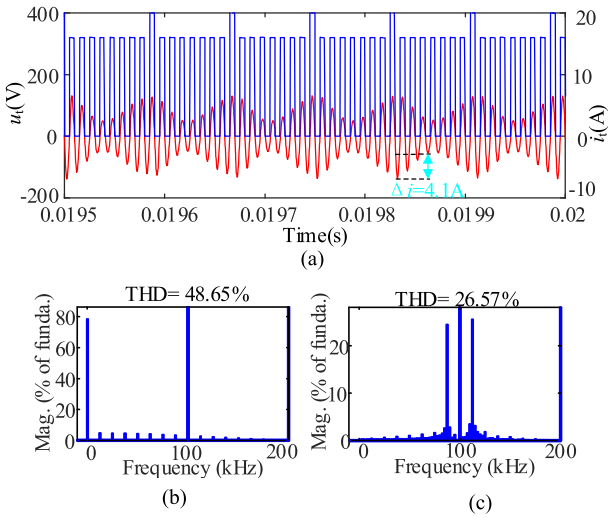

Fig. 6. Time-domain waves and DFT of u_t and i_t of the Δ-Σ PMM WPT system. (a) Time-domain waves. (b) DFT of u_t. (c) DFT of i_t.

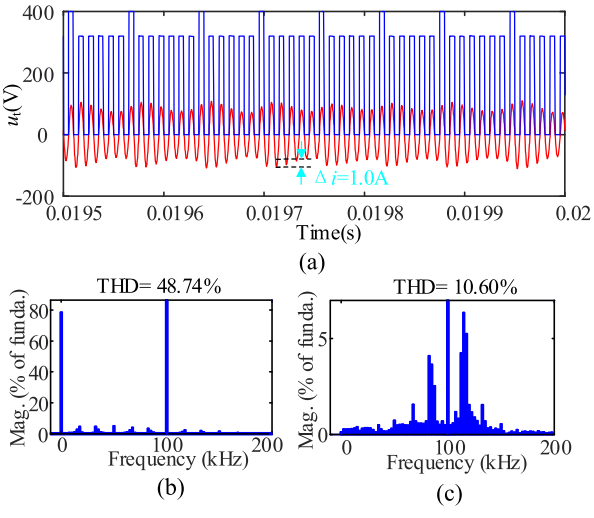

Fig. 7. Time-domain waves and DFT of u_t and i_t of the BBPMM WPT system when λ = 0.9. (a) Time-domain waves. (b) DFT of u_t. (c) DFT of i_t.

C. Harmonic Analysis of BBPMM and Δ-Σ PMM

The output voltage of the multilevel inverter can be represented by a Fourier series of

$$u_t(t) = \sum_{-\infty}^{\infty} k_n e^{2in\pi f_0 t} \tag{13}$$

where f_0 is called the fundamental frequency, and k_n is the Fourier coefficient at the nth harmonic. The harmonic frequency can be derived as follows:

$$f_h = \left(1 \pm \frac{h}{N_t}\right)(2n-1) f_0, h = 0, 1, 2, \ldots, N_t - 1. \tag{14}$$

Due to the fact that a complete modulation period T_m includes several resonant cycles, the spectrum of u_t contains both sub-harmonics and interharmonics. The main difference between BBPMM and Δ-Σ PMM is the interharmonics of the output voltage. Due to the impedance characteristic, the WPT system is sensitive to the interharmonics of the voltage near the resonant frequency. The frequency of interharmonics can be seen in (14), which depends on the modulation period. The magnitude of interharmonics is related to the voltage pulse sequence, which is difficult to derive, but the discrete Fourier transform (DFT) could be applied. Figs. 6 and 7 compare the time-domain waveforms and DFT analysis of the u_t, i_t of the WPT system by using BBPMM and Δ-Σ PMM. It is found that the THD of the transmit current of the BBPMM WPT system is much smaller than that of the Δ-Σ PMM WPT system. It is because adjusting the resolution of BBPMM leads to a short modulation period, leading to different interharmonics near the resonant frequency, as shown in Figs. 6 and 7.

In addition, Fig. 8 compares the simulation results of THD and current ripple of the transmitter current of the WPT system by using the BBPMM and Δ-Σ PMM when the interval of δ^* is 0.03215. The system parameter is shown in Table II. It can be found that when $\delta^* = 0.25$, 0.5, and 0.75, the current ripples and THD of Δ-Σ PMM and BBPMM WPT systems are the same

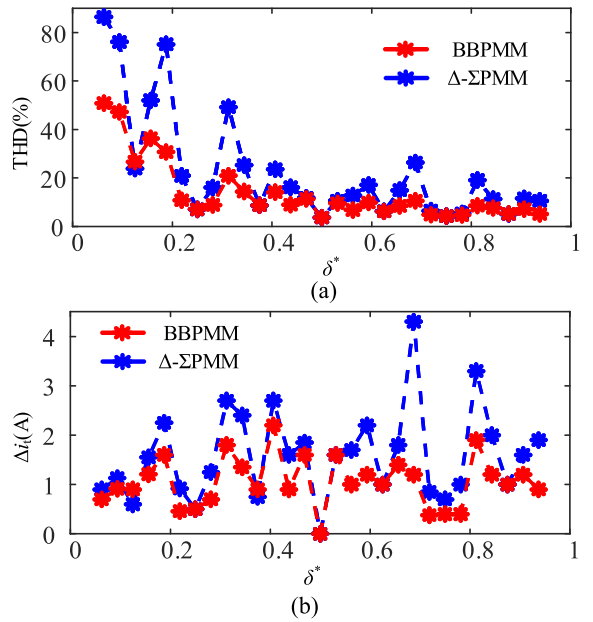

Fig. 8. Simulation results of THD and current ripple of transmitter current of BBPMM and Σ-Δ PMM when λ = 0.9. (a) THD. (b) Current ripple.

because they have the same output voltage. When $\delta^* = 0.6825$, the maximum current ripple of the Δ-Σ PMM WPT system is 4.1 A, but the current ripple of the BBPMM WPT system is 1.0 A, and the ripple minimization accounts for 75.6%. In the wide range of δ^*, Fig. 8 shows that the THD and current ripple of the BBPMM WPT system are close to or smaller than those of the Δ-Σ PMM WPT system.

III. BST-Based Voltage Balancing Method of Multilevel Inverter for the WPT System

A. Switching State Analysis

The way the flying capacitor is connected to the circuit and the direction of the transmitter current determine how the

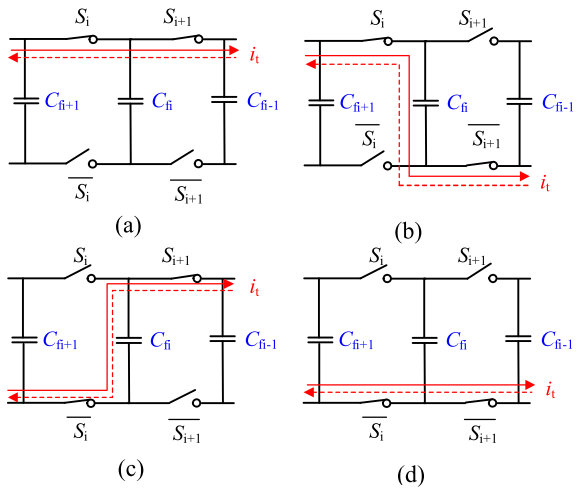

Fig. 9. Current flow of the subcircuit of the FCMLI in different switch states of "S_iS_{i+1}". (a) 11. (b) 10. (c) 01. (d) 00.

flying capacitor is charged. As shown in Fig. 9, the switching state "S_iS_{i+1}" determines whether C_i is charged. As shown in Fig. 9(a) and (d), when "S_iS_{i+1}" is selected as "11" and "00", C_i is bypassed, and the transmitter current flows on the upper and lower branches, respectively. As shown in Fig. 9(b) and (c), when "S_iS_{i+1}" is selected as "10" and "01", C_i is charged and discharged by the transmitter current, respectively. According to Fig. 9, it can be summarized as follows:

1) The output voltage of the multilevel inverter depends on the number of turn-ON states of "$S_1S_2S_3$ ... S_{n-1}", which can be derived as

$$u_t = \frac{V_{\mathrm{dc}}}{n-1}\sum_{i=1}^{n-1} S_i. \tag{15}$$

2) The charging or discharging pattern of the flying capacitors C_{f1}, C_{f2}, C_{f3}, ..., and C_{fn-2} depends on the switching states of "S_1S_2", "S_2S_3", "S_3S_4", ..., and $S_{n-2}S_{n-1}$, and the direction of transmitter current.

B. BST-Based Offline Design of Table

The algorithm of the capacitor voltage balancing needs to be completed in a very high-speed control cycle, which is half of the resonant cycle of the WPT system, but the computational burden of the conventional method is large, which limits the control frequency of the WPT system. To solve this problem, a BST-based capacitor voltage balancing method is proposed, consisting of an offline table generation method and a simplified online voltage balancing method.

Three key factors determine the preset switching state of the multilevel inverter, including the output voltage of the multilevel inverter, the voltage priority of the flying capacitors, and the flying-capacitor voltages [28]. Three variables related to the three factors can be defined as B_i, B_j, and B_k, respectively.

The variable B_i belongs to [0, 1, 2, 3,... $n-1$], and "$B_i = z$" means that the output voltage of the multilevel inverter is $zV_{\mathrm{dc}}/(n-1)$. Besides, according to (15), the output voltage of the multilevel inverter depends on the switch-ON number of the switching states "$S_1S_2S_3$, ...S_{n-1}". Thus, B_i can also be calculated as

$$B_i = \sum_{j=1}^{n-1} S_j. \tag{16}$$

The variable B_j belongs to [0, 1, 2, 3, ..., $n-3$], and "$B_j = i$" means that the charging priority of the $(i+1)$th flying capacitors is the highest. Furthermore, the charging priority can be expressed as "$C_{fi+1} > C_{fi+2} > \ldots C_{fn-2} > C_{f1} > C_{f2} > \ldots > C_{fi-1}$".

By judging whether the flying capacitor voltage is bigger than the reference value, the voltage state of every flying capacitor is encoded as 1 and 0, respectively. Furthermore, a_i is defined as the voltage state of ith flying capacitor, and a_i can be expressed as follows:

$$\begin{cases} a_i = 1, u_i > V_{\mathrm{dc}} - \frac{i}{n-1}V_{\mathrm{dc}} \\ a_i = 0, u_i \le V_{\mathrm{dc}} - \frac{i}{n-1}V_{\mathrm{dc}} \end{cases} \tag{17}$$

where i ranges in [1, 2, ...$n-2$].

The variable B_k can be expressed as follows:

$$B_k = 2^{n-2}a_1 + 2^{n-3}a_2 + \cdots + 2^{n-m}a_m + \cdots + 2a_{n-2} + a_{n-1}. \tag{18}$$

Thus, the voltage states of the flying capacitors denoted as B_k can be summarized as 2^{n-2} types, ranging in [0, 1, 2, 3, ..., $2^{n-2}-1$]. Fig. 10 shows the method to produce the three-dimensional array consisting of the preset switching states, and four key steps as shown in Fig. 10 will be explained in details as below.

Step 1: The main body of the flowchart in Fig. 10 consists of a typical nested for loop. It will produce a three-dimensional $(n)\times(n-2)\times(2^{n-2})$ array. An arbitrary output voltage of the FCMLI, arbitrary priority, and arbitrary voltage state can correspondingly produce a preset switching state. The array consists of these preset switching states. This array is produced offline and can be used for capacitor voltage balancing method online.

Step 2: Based on the voltage sample state (B_k) and an algorithm that converts decimal to binary, a corresponding voltage sample state of every flying capacitor can be obtained, denoted as $\mathbf{A}_n = [a_1, a_2, a_3, \ldots, a_{n-2}]$. Taking a seven-level inverter as an example, when $B_k = 15$, "$a_1a_2a_3$, ..., a_{n-2}" can be calculated as "01111", thus, $\mathbf{A}_n = [0, 1, 1, 1, 1]$.

Step 3: As shown in Fig. 11, step 3 is divided into two parts. In part 1, setting the charging priority of the first flying capacitor to the highest ($C_{f1} > C_{f2} > \ldots C_{fi} > \ldots > C_{fn-2}$), thus, $b_1 =$ 1-a_1 to make sure the first capacitor is charged or discharged in a correct way. The charging state of a_i is determined by "b_ib_{i+1}". When $a_i = 1$, the voltage of the ith flying capacitor is bigger than the reference value, thus, "b_ib_{i+1}" is supposed to be "01" to discharge the ith flying capacitor. However, even if $b_i = 1$, in this case, b_{i+1} is also supposed to be 1 to keep the capacitor voltage. When $a_i = 0$, the voltage of the ith flying capacitor is less than the reference value, thus, "b_ib_{i+1}" is supposed to be "10" to charge the ith flying capacitor. However, even if b_i is 0, b_{i+1} also needs to be 0 to keep the capacitor voltage. As discussed above, it can be concluded that $b_{i+1} = a_i$. Thus, in part 2, setting (B_j

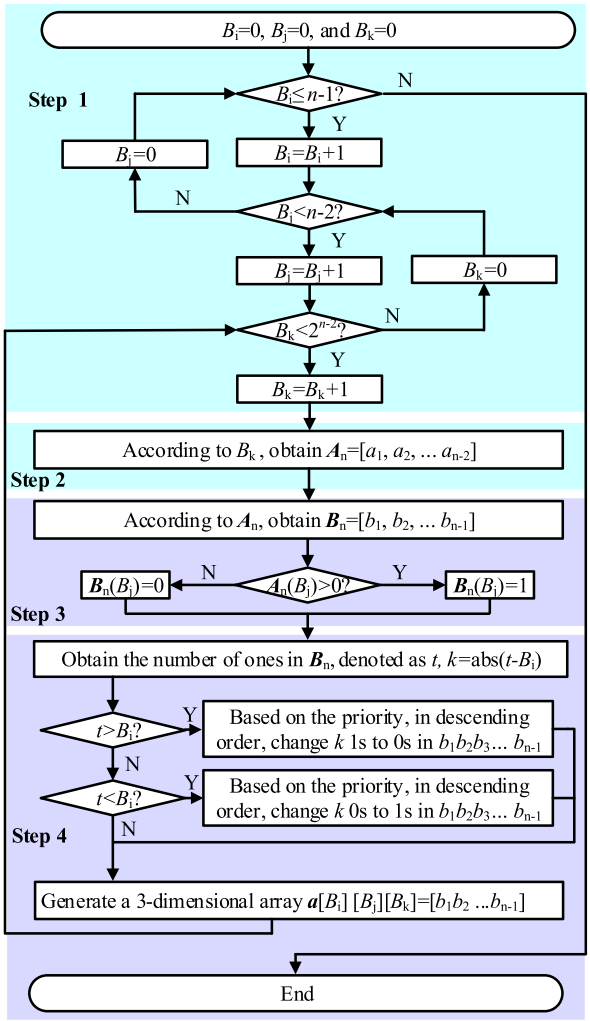

Fig. 10. Flowchart to create the three-dimensional offline table.

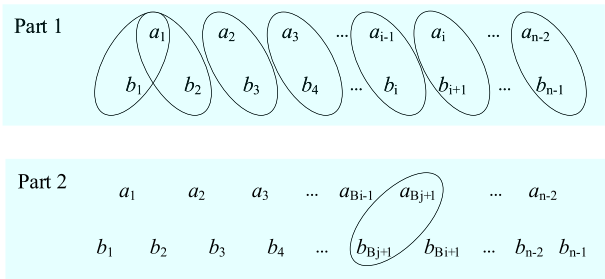

Fig. 11. Method to produce the desired switching state according to the capacitor-voltage state in step 3.

+ 1)th flying capacitor has the highest priority, thus, b_{Bj+1} = 1-a_{Bj+1}. According to the two parts discussed above, as shown in Fig. 10, a preset switching state ($\mathbf{B}_n$) related to the voltage state ($\mathbf{A}_n$) can be obtained. For example, if $B_j = 0$ and $\mathbf{A}_n$ = [0, 1, 1, 1, 1], $\mathbf{B}_n$ will be [1,0, 1, 1, 1, 1] after part 1 in step 3, and $\mathbf{B}_n$ will be [1,0, 1, 1, 1, 1] after part 2 in step 3.

Step 4: Finally, the number of ones in $\mathbf{B}_n$ is supposed to be B_k. Thus, according to the priority, change "1" to "0" or "0" to "1" in descending order to make sure that the number of one in $\mathbf{B}_n$ equals B_i. For example, when $B_j = 0$ and $B_i = 2$, $\mathbf{B}_n$ after step 3 is [1, 0, 1, 1, 1, 1], then, change "1" to "0" from the order of $b_6 - b_5 - b_4 - b_3 - b_2 - b_1$, until $b_6 + b_5 + b_4 + b_3 + b_2 + b_1 = B_i$. Thus, the final switch states "S_1 S_2 S_3 S_4 S_5 S_6", equaling to "b_1 b_2 b_3 b_4 b_5 b_6", will be "101000" after above operation.

TABLE I
$S_1S_2S_3S_4S_5S_6$ OF SEVEN-LEVEL INVERTER WHEN $B_j = 0$

B_k \ B_i	0	1	2	3	4	5	6
0	000000	100000	100001	100011	100111	101111	111111
1	000000	100000	100001	100011	100111	101111	111111
2	000000	100000	100010	100011	100010	101111	111111
3	000000	100000	100010	100011	100111	101111	111111
4	000000	100000	100100	100101	100111	101111	111111
5	000000	100000	100100	100101	100111	101111	111111
6	000000	100000	101000	101001	101011	101111	111111
7	000000	100000	101000	101001	101011	101111	111111
8	000000	100000	101000	101010	101011	101111	111111
9	000000	100000	101000	101010	101011	101111	111111
10	000000	100000	101000	101100	101101	101111	111111
11	000000	100000	101000	101100	101101	101111	111111
12	000000	100000	101000	101100	101101	101111	111111
13	000000	100000	101000	101100	101101	101111	111111
14	000000	100000	101000	101110	010110	101111	111111
15	000000	100000	101000	101100	101110	101111	111111
16	000000	010000	010010	010011	010111	011111	111111
17	000000	010000	010010	010011	010111	011111	111111
18	000000	010000	010010	010011	010111	011111	111111
19	000000	010000	010010	010011	010111	011111	111111
20	000000	010000	010100	010101	010111	011111	111111
21	000000	010000	010100	010101	010111	011111	111111
22	000000	010000	010100	010110	010111	011111	111111
23	000000	010000	010100	010110	010111	011111	111111
24	000000	010000	011000	011001	011011	011111	111111
25	000000	010000	011000	011001	011011	011111	111111
26	000000	010000	011000	011010	011011	011111	111111
27	000000	010000	011000	011010	011011	011111	111111
28	000000	010000	011000	011100	011101	011111	111111
29	000000	010000	011000	011100	011101	011111	111111
30	000000	010000	011000	011100	011101	011111	111111
31	000000	010000	011000	011100	011101	011111	111111

Taking a seven-level half-bridge flying-capacitor inverter as an example, Table I shows the offline table only when $B_j = 0$, by using the proposed method in Fig. 10. It can be found that only when $B_i = 0$ or 6, there is only one kind of switching state. When $B_i \neq 0$ or 6, there are redundant switching states. For a seven-level half-bridge flying-capacitor inverter, there are six tables, such as Table I.

C. Look-Up Table-Based Capacitor Voltage Balancing

Then, the capacitor voltage balancing method based on the look-up table method can be used to simplify the process online to break the limitation of the switching frequency. Fig. 12 shows the look-up table-based capacitor voltage balancing method in one control cycle, and the input of the proposed method contains the output of the proposed BBPMM y and the sampled voltage of the flying capacitors. First of all, according to the sampled voltages u_1 u_2 …u_{n-2}, (17), and (18), the array index B_k related to the voltage state of the flying capacitors can be obtained. Then, when $0 < y < n - 1$, $B_j = B_j - 1$; if $B_j < 0$, $B_j = n - 2$. The array index B_j is related to the charging priority of the flying capacitor. This operation can make sure that the priority of capacitor charging is changed in turn. The output of

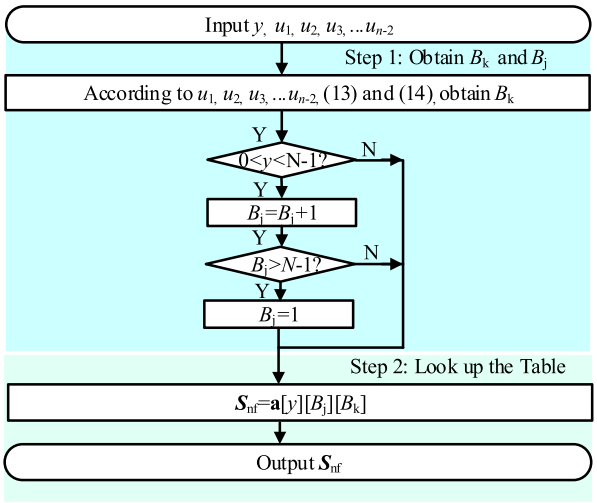

Fig. 12. Look-up table-based capacitor voltage balancing method.

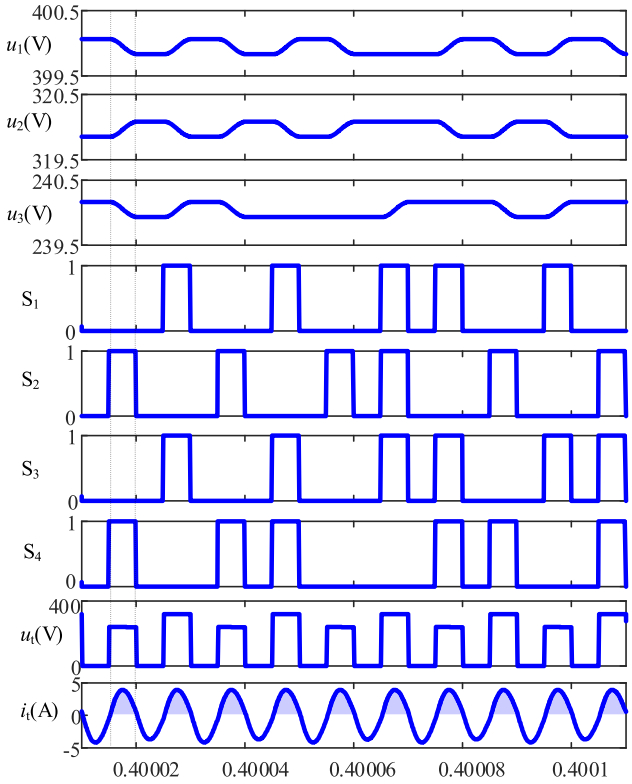

Fig. 13. Time-domain wave of the BBPMM multilevel inverter-based WPT system when $\delta^* = 7/12$.

the BBPMM y is also the array index related to the voltage level. Finally, according to y, B_j, and B_k, the switching state can be obtained by the array produced offline as shown in Fig. 10.

To further explain the charging/discharging process of the proposed BST-based capacitor voltage balancing method, Fig. 13 shows an example of the flying capacitor charging/discharging of the seven-level inverter-based WPT system when $\delta^* = 7/12$. As shown in Fig. 13, the transmitter current is used for charging or discharging. The amount of charge and discharge of the flying capacitor is proportional to the integral of the transmitter

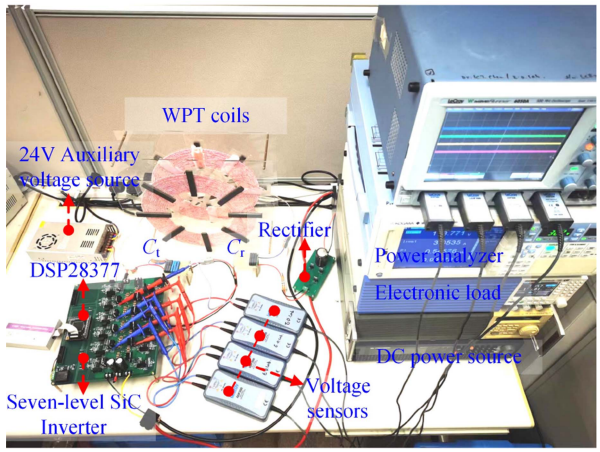

Fig. 14. Experimental platform.

current of the WPT system in one control cycle. The execution frequency of the balancing algorithm is twice the switching frequency. Ignoring the influence of harmonic current, during a control cycle, the voltage variation of ith flying capacitor can be expressed as

$$\Delta u_i = \frac{1}{C_{fi}} \int_0^{T_s/2} i_t(t)\, dt = \frac{I_t T_s}{\pi C_{fi}} \le \frac{P_r T_s}{C_{fi} V_{\rm dc}} \tag{19}$$

where I_t is the peak value of the transmitter current; P_r is the rated power of the WPT system.

Furthermore, the voltage ripple of the flying capacitor during the modulation period can be derived as follows:

$$\Delta u_{ci} = N \Delta u_i \tag{20}$$

where $1 \le N < n-2$.

IV. Simulation and Experimental Verification

A. Hardware Implementation

Fig. 14 shows the prototype of the seven-level flying capacitor inverter-based WPT system by using the proposed BBPMM. When $R_{\rm dc} = 88\,\Omega$, the input power is 1.5 kW. The system consists of a dc power source (MR50040), a power analyzer (WT5000), a silicon-carbide-based seven-level flying capacitor inverter with drivers, a WPT circuit, a full-bridge rectifier, an electronic load (PLZ1003WH), a 24-V auxiliary voltage source, and a DSP TMS320F28377 board. The transmitter and receiver coils are made of Litz wire. The 24 V voltage source is used to feed the auxiliary circuit. The power analyzer measures the input and output power. All flying capacitors have the same capacitance and rated voltage for convenience and lower voltage ripple. The system parameters are listed in Table II.

The differential circuits based on the isolated amplifiers (AMC1311DWVR) are used to sample flying capacitor voltages and input voltage. The voltage sampling calibration is achieved by linear fitting in Microsoft Excel. This experiment was run at room temperature. To speed up the algorithm, the BBPMM algorithm, the BST-based capacitor voltage balancing algorithm, the Σ-Δ PMM algorithm, and the conventional token rotation-based voltage balancing algorithm are all written in the RAM

TABLE II
SYSTEM PARAMETERS OF THE WPT SYSTEM

Items	Value
DC-link voltage (U_{dc})	480 V
Primary (Secondary) capacitance (C_t, C_r)	(8.6, 8.44) nF
Primary (Secondary) coil inductance (L_t, L_r)	(297.2, 297.1) μH
Primary (Secondary) series resistance (R_t, R_r)	(0.3, 0.3) Ω
Coils diameter (d_1, d_2)	(30, 30) cm
Distance between two coils (d)	10 cm
Mutual inductance (M)	72.96 μH
Resonant frequency (f_r)	100 kHz
Output capacitance (C_o)	220 μF
DC capacitors (C_{dc1}, C_{dc2})	(100, 100) μF
Load resistance (R_{dc})	55.31 Ω
Dead time (T_d)	100 ns
Digital signal processor	TMS320F28377
SiC MOSFET	SCT3080AL
Diode	STPSC40G12WL
Driver	UCC21710
Voltage sample	AMC1311DWVR

of DSP TMS320F28377. When executing the algorithms on the 200 MIPS single-core processor of the DSP TMS320F28377, the proposed BST-based voltage balancing method only needs 85 clock cycles, while the conventional token rotation-based capacitor voltage balancing method [28] needs 179 clock cycles. Thus, compared with the traditional method, the proposed voltage balancing method can obviously decrease the computational burden online and is 2.1059 times faster than that in [28].

B. Flying Capacitor Voltage Balance Analysis

Besides, Fig. 15 shows the flying capacitor voltages and dc-side output voltage of the FCMLI-based WPT system with step and ramp responses. When δ^* steps from 3/16 to 11/16 or from 11/16 to 3/16, the output voltage steps from 43.0 to 160 V or from 160 to 43.0 V within 0.04 s, but all the flying capacitor voltages u_3, u_4, and u_5 have insignificant changes as shown in Fig. 15(a) and (b). When the load steps from 57.86 to 28.93 Ω or from 28.93 to 57.86 Ω, the output voltage steps from 160 to 80.0 V or steps from 80.0 to 160.0 V within 0.02 s, and all the flying capacitor voltages u_3, u_4, and u_5 have insignificant changes as shown in Fig. 15(c) and (b). As shown in Fig. 15(e) and (f), when δ^* is ramped up from 0.1 to 0.9 or ramped down from 0.9 to 0.1, the output voltage ramps from 23.2 to 209.3 V or from 209.3 to 23.2 V, and all the flying capacitor voltages u_3, u_4, and u_5 have insignificant changes.

In addition, Fig. 15(g)–(i) shows the flying capacitor voltage and the output voltage when there is a large disturbance of the input voltage. Fig. 15(g) shows that when the input voltage changes from 320 to 480 V and $\lambda = 0.9$, u_3, u_4, and u_5 decrease to the new reference values within 0.125 s, and u_{dc} increases from 136.0 to 204.0 V within 0.04 s. Fig. 15(j) shows that when the input voltage changes from 480 to 320 V and $\lambda = 0.9$, u_3, u_4, and u_5 decrease to the new reference values within 0.125 s, and u_{dc} decreases from 204 to 136.0 V within 0.04 s. Comparing Fig. 15(g) and (i), it can be found that a changing λ from 0.9 to 0.95 leads to insignificant changes in the dynamic response of u_3, u_4, u_5, and u_{dc} when the input voltage step increases from 320 to 480 V. Fig. 15(j) shows that when δ^* is a 50-Hz

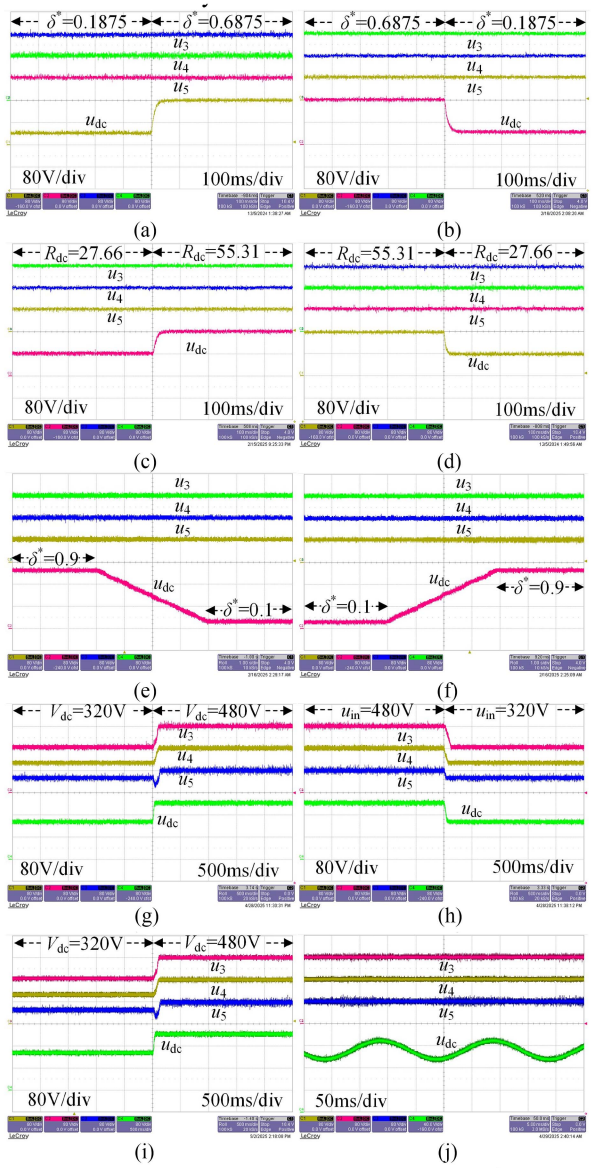

Fig. 15. DC-side Output voltage and capacitor voltages of the FCMLI-based WPT system. (a) Step increasing δ^*. (b) Step decreasing δ^*. (c) Step increasing R_{dc}. (d) Step increasing R_{dc}. (e) Increasing δ^* in a ramp. (f) Decreasing δ^* in a ramp. (g) $\lambda = 0.9$, step increasing V_{dc}. (h) $\lambda = 0.9$, Step decreasing V_{dc}. (i) $\lambda = 0.95$, step increasing V_{dc}. (j) Sine command of 50 Hz for δ^*.

sinusoidal signal, the output voltage is sinusoidal, and all the flying capacitor voltages u_3, u_4, and u_5 can be kept constant at the reference value. The experimental results in Fig. 15 show the stability and effectiveness of the proposed voltage balancing method of the FCMLI-based WPT system.

C. Characteristic Analysis

With different δ^*, Fig. 16 compares the experimental waveforms of the output voltage u_t and the transmitter current i_t of the seven-level inverter by using the proposed BBPMM and Σ-Δ PMM. Comparing Fig. 16(a) and (b), when $\delta^* = 3/16$, the Δi and THD of BBPMM with $\lambda = 0.9$ are 1.2 A and 28.57%, and the Δi and THD of the Σ-Δ PMM are 2 A and 46.18%. When δ^*

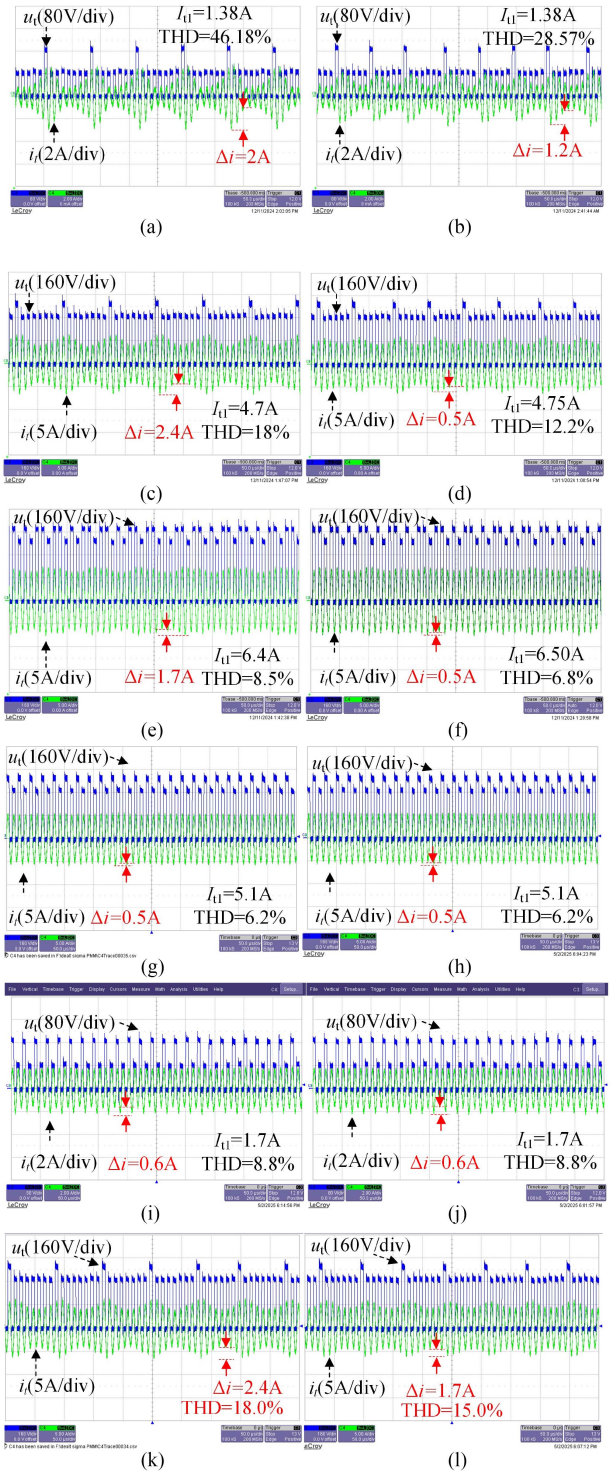

Fig. 16. Inverter output voltages and currents. (a) Σ-Δ PMM, $\delta^* = 3/16$. (b) BBPMM, $\delta^* = 3/16$, $\lambda = 0.9$. (c) Σ-Δ PMM, $\delta^* = 11/16$. (d) BBPMM, $\delta^* = 11/16$, $\lambda = 0.9$. (e) Σ-Δ PMM, $\delta^* = 15/16$. (f) BBPMM, $\delta^* = 0.75$, $\lambda = 0.9$. (g) Σ-Δ PMM, $\delta^* = 0.25$. (h) BBPMM, $\delta^* = 0.25$, $\lambda = 0.9$. (i) Σ-Δ PMM, $\delta^* = 0.75$. (j) BBPMM, $\delta^* = 0.75$, $\lambda = 0.9$. (k) BBPMM, $\delta^* = 11/16$, $\lambda = 0.99$. (l) BBPMM, $\delta^* = 11/16$ $\lambda = 0.95$.

$= 3/16$, compared with the Σ-Δ PMM, the current ripple Δi and the THD of BBPMM with $\lambda = 0.9$ reduce by 40% and 38.1%, respectively. Comparing Fig. 16(c) and (d), when $\delta^* = 11/16$, the Δi and THD of BBPMM with $\lambda = 0.9$ are 0.5 A and 12.2%,

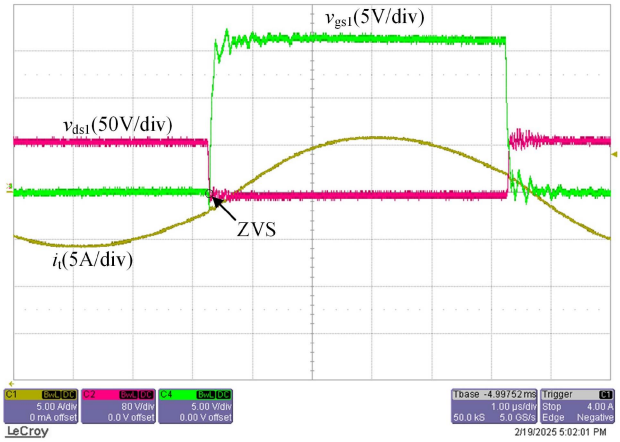

Fig. 17. Experimental waves of v_{ds1}, v_{gs1}, and it when $\delta* = 0.9375$.

and the Δi and THD of the Σ-Δ PMM are 2.4 A and 18%. When $\delta^* = 11/16$, compared with the Σ-Δ PMM, the current ripple Δi and the THD of BBPMM with $\lambda = 0.9$ reduce by 79.5% and 33%, respectively. Comparing Fig. 16(e) and (f), when $\delta^* = 15/16$, the Δi and THD of BBPMM with $\lambda = 0.9$ are 0.5 A and 6.8%, and the Δi and THD of the Σ-Δ PMM are 1.7 A and 8.5%. When $\delta^* = 11/16$, compared with the Σ-Δ PMM, the current ripple Δi and the THD of BBPMM with $\lambda = 0.9$ reduce by 70.6% and 20%, respectively. Comparing Fig. 16(c) and (k), it is found that when $\delta^* = 3/16$, the BBPMM with $\lambda = 0.99$ and Σ-Δ PMM have the same voltage and current waveforms. Furthermore, comparing Fig. 16(d), (k), and (l), when λ is 0.99, 0.95, and 0.9, the THD of BBPMM is 18.0%, 15.0%, and 12.2%, and the current fluctuations are 2.4, 1.7, and 0.5 A, respectively. It can be found that when $\delta^* = 11/16$, a decrease in λ can decrease the THD and the current ripple. Some work conditions exist where the ripple and the THD of the transmitter current of the Σ-Δ PMM are high. In these cases, compared with Σ-Δ PMM, the THD and current ripple of the transmitter current can be further reduced by regulating λ of the BBPMM. Comparing (g) and (h) or (i) and (j), it is found that when $\delta^* = 0.25$ and 0.75, the BBPMM with $\lambda = 0.9$ and Σ-Δ PMM have the same voltage and current waveforms, which is consistent with the simulation results as shown in Section II-C.

Fig. 16 shows that the slopes of the output voltage of the multilevel inverter reach their final value just slightly before the zero-crossing points of the transmitter current for both BBPMM and Σ-Δ PMM. It means that both the proposed BBPMM and the Σ-Δ PMM can realize the ZVS. Furthermore, Fig. 17 shows the switching waveforms of the BBPMM-WPT system while $\delta^* = 0.9375$, where v_{ds1} and v_{gs1} are the drain-source voltage and gate-source voltage of the switch S_1, respectively. Fig. 17 shows that v_{gs1} becomes a high-level voltage after v_{ds1} becomes zero, indicating that S_1 can realize reliable ZVS for the BBPMM-WPT system.

Furthermore, Fig. 18 compares the system efficiency and output voltage of the multilevel inverter-based WPT system by using BBPMM and Σ-Δ PMM. Due to the realization of the ZVS, the system efficiency is high during a wide range of

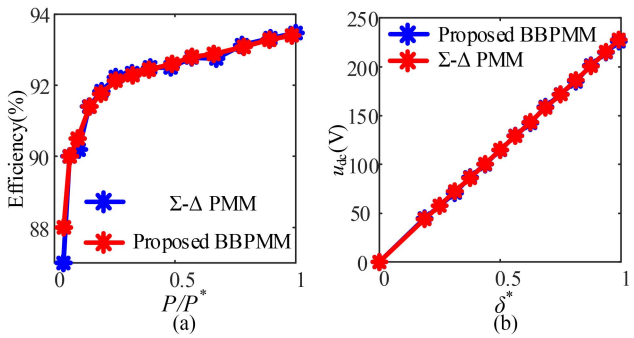

Fig. 18. Relation between the system efficiency, output power, and output voltage by changing δ^*. (a) System efficiency and output power by changing δ^*. (b) Output voltage by changing δ^*.

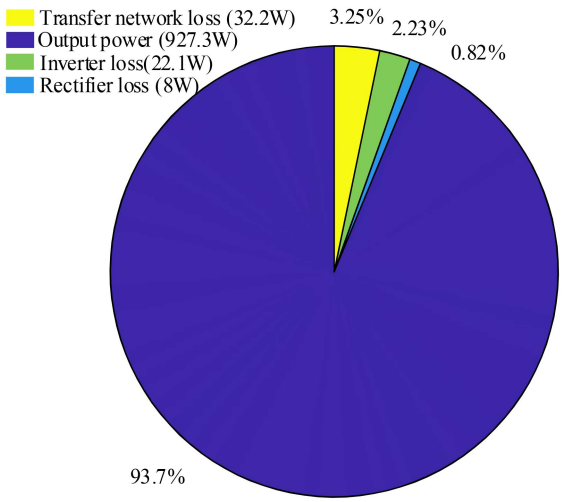

Fig. 19. Output power and power losses when $\delta^* = 0.99$, $R_{dc} = 55.31$.

output power for both BBPMM and Σ-Δ PMM. As shown in Fig. 18(a), the slope of the system efficiency of the BBPMM and Σ-Δ PMM is similar, both of them are kept above 90% in a wide output power range (10%–100% P_r), and the efficiency is measured by WT5000. Fig. 18(b) shows that the dc-side output voltage is proportional to δ^* for both BBPMM and Σ-Δ PMM, which verifies the theoretical analysis in Section II-B.

In addition, the input and output powers of the seven-level inverter and the diode rectifier are measured by WT5000, and then, the percentage of loss components with respect to the input power can be calculated. Fig. 19 shows the output power and power loss distribution of the BBPMM seven-level half-bridge inverter-based WPT system when $\delta^* = 0.99$ and $R_{dc} = 55.31$, where the input power is 989.6 W and the system efficiency is 93.7%. The transfer network loss accounts for 3.25%, which is maximal. The power loss of the seven-level inverter accounts for 2.23%, and the power loss of the diode rectifier accounts for 0.82%.

D. Comparison Between the Proposed Method and the Conventional Methods

First of all, compared with the Σ-Δ PDM [18] or Σ-Δ PFM [24] for the two-level inverter or the Σ-Δ SVPFM three-level inverter-based WPT system, the Σ-Δ PMM for the multilevel inverter has a lower harmonic current on the transmitter side and a lower dc-side voltage ripple in a wide range [28]. Moreover, the Σ-Δ PMM for the multilevel inverter can be connected to a higher dc voltage bus. The BBPMM has the above advantage as the Σ-Δ PMM. Besides, the resolution of the above modulation method based on the Σ-Δ modulator is not adjustable, but BBPMM has a continuously adjustable resolution, which is also a unique advantage. The BBPMM can furthermore reduce the THD and current ripple of the Σ-Δ PMM by adjusting the resolution. Meanwhile, BBPMM has the same disadvantage as the Σ-Δ PMM. When the voltage level n of the multilevel inverter increases by 1, two additional MOSFETs, an additional set of flying capacitors, and an additional set of voltage sampling circuits are required, leading to an increase in the cost. The voltage self-balancing method of the multilevel inverter for the WPT system needs to be further investigated to reduce the cost in the future. One of the potential applications of the proposed system is wireless charging of electric vehicles, providing efficient power transmission and reliable operation. Second, multilevel inverter-based WPT systems can be used for high-power applications connected to the dc medium voltage, such as the underwater data center and large electric boats.

V. Conclusion

The BBPMM and BST-based capacitor voltage balance methods of the multilevel inverter for WPT systems have been proposed and implemented. Some conclusive remarks are summarized below:

1) The BBPMM of multilevel inverters for WPT systems has been proposed and verified in this article. It is based on specially designed iterative functions to fit and approximate the actual normalized voltage ratio of the output voltage of the multilevel inverter. It has the significant advantage of adjustable resolution, which is more flexible than the Σ-Δ PMM.
2) Furthermore, it is found that the BBPMM multilevel inverter-based WPT systems can decrease the ripple and THD of the transmitter current in a wide range by adjusting the resolution, compared with the Σ-Δ PMM multilevel inverter-based WPT system.
3) Besides, the BST-based capacitor voltage balancing method of the FCMLI for the WPT system has been proposed. It combines the online and offline processes of the capacitor voltage balance method to simplify the algorithm in a control period of the BBPMM multilevel inverter-based WPT system. The technique can make the flying capacitor voltages of the multilevel inverter with arbitrary voltage levels balanced at the reference values, and it requires a low online computational burden, which increases the potential for higher switching frequency of the PMM multilevel inverter-based WPT system.

Finally, experimental verification was given to verify the feasibility of the proposed modulation method and the BST-based capacitor voltage balancing method.

REFERENCES

[1] S. Thomas, "Connecting with wireless power transfer," *Nat. Electron.*, vol. 6, Feb. 2023, Art. no. 106.

[2] Z. Zhang and K. T. Chau, "Homogeneous wireless power transfer for move-and-charge," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6213–6220, Nov. 2015.

[3] W. Han, K. T. Chau, C. Jiang, W. Liu, and W. H. Lam, "Design and analysis of quasi-omnidirectional dynamic wireless power transfer for fly-and-charge," *IEEE Trans. Magn*, vol. 55, no. 7, Jul. 2019, Art. no. 8001709.

[4] Q. Deng, W. Liu, J. Lu, C. C. Mi, and K. T. Chau, "Integrated sensorless wireless charging using symmetric high-order network for multistorey car parks," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 10568–10581, Aug. 2024.

[5] J. H. Kim et al., "Development of 1-MW inductive power transfer system for a high-speed train," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6242–6250, Oct. 2015.

[6] W. V. Wang, D. J. Thrimawithana, and M. Neuburger, "An Si MOSFET-based high-power wireless EV charger with a wide ZVS operating range," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11163–11173, Oct. 2021.

[7] W. V. Wang, D. J. Thrimawithana, F. Lin, and G. A. Covic, "An MMC-based IPT system with integrated magnetics and ZVS operations," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2425–2436, Feb. 2022.

[8] X.-J. Ge, Y. Sun, Z.-H. Wang, and C.-S. Tang, "A single-source switched capacitor multilevel inverter for magnetic coupling wireless power transfer systems," *Elect. Eng.*, vol. 101, no. 4, pp. 1083–1094, 2019.

[9] J.-Y. Lee, C.-Y. Liao, S.-Y. Yin, and K.-Y. Lo, "A multilevel inverter for contactless power transfer system," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 1, pp. 401–405, Jan. 2021.

[10] R. Guan et al., "A power self-balanced high step-down medium voltage DC converter with expandable soft-switching range," *IEEE Trans. Ind. Electron.*, vol. 71, no. 1, pp. 398–408, Jan. 2024.

[11] G. Kampitsis, E. I. Batzelis, A. Kolokasis, E. Matioli, and B. C. Pal, "A generalized phase-shift PWM extension for improved natural and active balancing of flying capacitor multilevel inverters," *IEEE Open J. Power Electron.*, vol. 3, pp. 621–634, 2022.

[12] J. Chevinly et al., "Gallium nitride (GaN) based high-power multilevel H-bridge inverter for wireless power transfer of electric vehicles," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2024, pp. 1–5.

[13] Y. Liu, C. Liu, X. Gao, and S. Liu, "Design and control of a decoupled multichannel wireless power transfer system based on multilevel inverters," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 10045–10060, Aug. 2022.

[14] A. Berger, M. Agostinelli, S. Vesti, J. A. Oliver, J. A. Cobos, and M. Huemer, "A wireless charging system applying phase-shift and amplitude control to maximize efficiency and extractable power," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6338–6348, Nov. 2015.

[15] Y. Jiang, L. Wang, Y. Wang, J. Liu, X. Li, and G. Ning, "Analysis, design, and implementation of accurate ZVS angle control for EV battery charging in wireless high-power transfer," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 4075–4085, May 2019.

[16] C. Jiang, K. T. Chau, T. W. Ching, C. Liu, and W. Han, "Time-division multiplexing wireless power transfer for separately excited DC motor drives," *IEEE Trans. Magn.*, vol. 53, no. 11, Nov. 2017, Art. no. 8205405.

[17] Z. Hua, K. T. Chau, W. Han, W. Liu, and T. W. Ching, "Output-controllable efficiency-optimized wireless power transfer using hybrid modulation," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4627–4636, May 2022.

[18] H. Li, S. Chen, J. Fang, Y. Tang, and M. A. de Rooij, "A low-subharmonic, full-range, and rapid pulse density modulation strategy for ZVS full-bridge converters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8871–8881, Sep. 2019.

[19] M. Fan, L. Shi, Z. Yin, L. Jiang, and F. Zhang, "Improved pulse density modulation for semi-bridgeless active rectifier in inductive power transfer system," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5893–5902, Jun. 2019.

[20] V. Yenil and S. Cetin, "An improved pulse density modulation control for secondary side controlled wireless power transfer system using LCC-S compensation," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12762–12772, Dec. 2022.

[21] J. Zhou, G. Guidi, S. Chen, Y. Tang, and J. A. Suul, "Conditional pulse density modulation for inductive power transfer systems," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 88–93, Jan. 2024.

[22] F. John, P. R. G. Komarasamy, N. Rajamanickam, L. Vavra, J. Petrov, and V. Kral, "Performance improvement of wireless power transfer system for sustainable EV charging using dead-time integrated pulse density modulation approach," *Sustainability*, vol. 16, no. 16, 2024, Art. no. 7045.

[23] R. Shinoda, K. Tomita, Y. Hasegawa, and H. Ishikuro, "Voltage-boosting wireless power delivery system with fast load tracker by $\Delta\Sigma$-modulated sub-harmonic resonant switching," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 288–289.

[24] X. Li, Y.-P. Li, C.-Y. Tsui, and W.-H. Ki, "Wireless power transfer system with $\Sigma\Delta$-modulated transmission power and fast load response for implantable medical devices," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 3, pp. 279–283, Mar. 2017.

[25] W. Liu, K. T. Chau, C. H. T. Lee, W. Han, X. Tian, and W. H. Lam, "Full-range soft-switching pulse frequency modulated wireless power transfer," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6533–6547, Jun. 2020.

[26] Z. Hua, K. T. Chau, W. Liu, X. Tian, and H. Pang, "Autonomous pulse frequency modulation for wireless battery charging with zero-voltage switching," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 8959–8969, Sep. 2023.

[27] J. Tang, T. Na, and Q. Zhang, "A novel full-bridge step density modulation for wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 41–45, Jan. 2023.

[28] J. Guo, K. T. Chau, W. Liu, Y. Hou, and W. L. Chan, "Pulse magnitude modulation and token rotation-based voltage balancing method of multi-level inverter for wireless power transfer," *IEEE Trans. Power Electron.*, vol. 40, no. 3, pp. 4652–4663, Mar. 2025.

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