An Optimal Burst Mode Control Method for CLLC Converter Based on Time Domain Model

Ting Luo, Jia Li, Yangfan Chen, Yipeng Yan, Jianglin Xiong, Guolin Lai, and Quanming Luo, *Member, IEEE*

***Abstract*—The CLLC resonant converters are drawing more and more attention due to their superiority in high efficiency, high power density, and low electromagnetic interference. However, CLLC converter still suffers the problems of unsatisfactory voltage regulation and low efficiency under light-load conditions. To address this issue, a burst mode control method with dual active modulation for CLLC converter is proposed in this article. With the aid of time-domain model and offline particle swarm optimization (PSO) algorithm, the proposed method optimizes the switching sequences of the pulse packets to achieve the minimum current root mean square (RMS) with the same transmitted energy and requires only sampling of the input and output voltages. Comparative experiments were conducted on a 1-kW prototype and the results show that the light load efficiency can be improved by applying the proposed burst mode control. Peak efficiency of 97.4% is achieved at 10% rated load, which is an improvement of more than 2% compared to the previous burst mode approaches.**

***Index Terms*—Burst mode, CLLC resonant converter, optimization, root mean square (RMS) current, time domain model.**

NOMENCLATURE

$\mathbf{C}$	Vector of constants in the general solution of v_{Cr2}.
C_2	Secondary bus capacitance.
C_{r1}	Primary resonant capacitance.
C_{r2}	Secondary resonant capacitance.
$\mathbf{D}$	Vector of derivatives of v_{Cr2}.
D_0	Phase shift of drive signals between the primary and secondary H-bridge.
D_1	Phase shift of drive signals between the two primary side half-bridge.
D_2	Phase shift of drive signals between the two secondary side half-bridge.
DA	Dual active.
$\mathbf{I}$	Identity matrix.
L_m	Magnetizing inductance.
L_{r1}	Primary resonant inductance.
L_{r2}	Secondary resonant inductance.
R_L	Load resistance.
R_{sample}	Voltage sampling resistance.
$\mathbf{S}$	Vector of bridge arm voltages.
SA	Single active.
$\mathbf{S}_k$	Vector of bridge arm voltages in the kth stage.
T_s	Switching cycle.
V_1	DC voltage of primary side.
V_2	DC voltage of secondary side($\bar{v}_{C2}$).
e_{bur}	Transmitted energy of one burst pulse packet.
f_{bur}	Fundamental burst frequency.
f_n	Normalized switching frequency.
f_r	Resonant frequency.
f_s	Switching frequency.
i_{Lm}	Magnetizing current.
i_{Lm_k}	Magnetizing current in the kth stage.
i_{Lr1}	Primary resonant inductor current.
i_{Lr1_k}	Primary resonant inductor current in the kth stage.
i_{Lr2}	Secondary resonant inductor current.
i_{Lr2_k}	Secondary resonant inductor current in the kth stage.
$i_{Q_k_\text{off}}$	Switching OFF current of Q_k.
$i_{S_k_\text{off}}$	Switching OFF current of S_k.
m	Normalized voltage gain ($m = nV_2/V_1$).
n	Turn ratio of transformer.
t_{bur}	Burst cycle.
t_{dead}	Dead time.
t_k	End moment of the kth stage since zero state.
v_{Cr1}	Primary resonant capacitor voltage.
v_{Cr1_k}	Primary resonant capacitor voltage in the kth stage.
v_{Cr2}	Secondary resonant capacitor voltage.
v_{Cr2_k}	Secondary resonant capacitor voltage in the kth stage.
v_{ab}	H-bridge voltage of primary side.
v_{cd}	H-bridge voltage of secondary side.
$\mathbf{x}$	Vector of state variables.

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I. INTRODUCTION

WITH the rapid development and promotion of distributed energy sources, electric vehicles, microgrids, and energy storage technologies, isolated bidirectional dc–dc converters (IBDCs) have received wide attention and application as the key component of energy conversion in the above fields [1], [2], [3], [4]. The CLLC resonant converter, as shown in Fig. 1, is often considered a bidirectional version of the LLC resonant converter. Like the LLC converter, the CLLC converter has

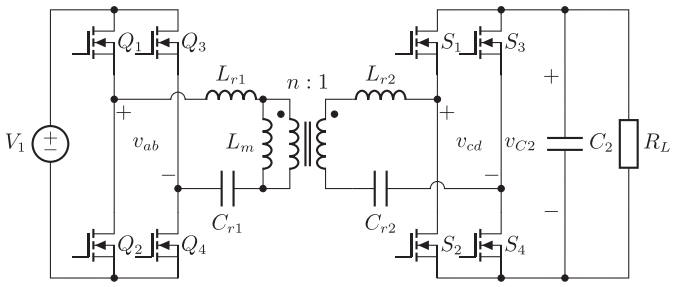

Fig. 1. Diagram of CLLC converter.

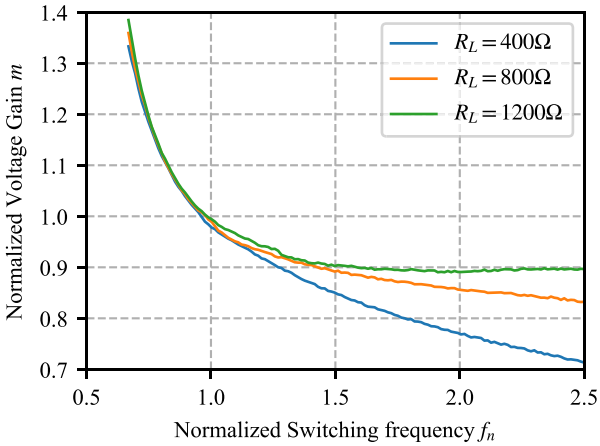

Fig. 2. Voltage gain curve of CLLC converter with PFM control (obtained by sweeping frequency experiment on the CLLC converter prototype).

excellent soft switching characteristics, achieving low switching losses, high efficiency, and high-power density. Therefore, the CLLC converter is also considered as the most promising IBDC converter topology [5], [6].

The pulse frequency modulation (PFM) is the most utilized modulation method for both LLC and CLLC converters [7], [8], [9], [10], [11]. By changing the switching frequency f_s, the PFM varies the ac impedance of the resonant tank, which in turn regulates the voltage gain m. As shown in Fig. 2, where

$$f_n = \frac{f_s}{f_r} \tag{1}$$

and for symmetrical CLLC, there is

$$f_r = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}} = \frac{1}{2\pi\sqrt{L_{r2}C_{r2}}}. \tag{2}$$

The voltage gain curve of PFM is load-dependent, especially in buck mode ($m < 1$). And the output voltage becomes difficult to regulate with PFM when lightly loaded.

Compared with PFM, the phase shift modulation (PSM) [12], [13] introduces a phase shift D_1 between the drive signals of the two half-bridges on the primary side, which in turn reduces the ac fundamental component of the v_{ab} and realizes further regulation of the output voltage in buck mode. However, when D_1 is large, the RMS value of resonant currents increases significantly and some switches lose zero voltage switching (ZVS) operation, resulting in a decrease in efficiency.

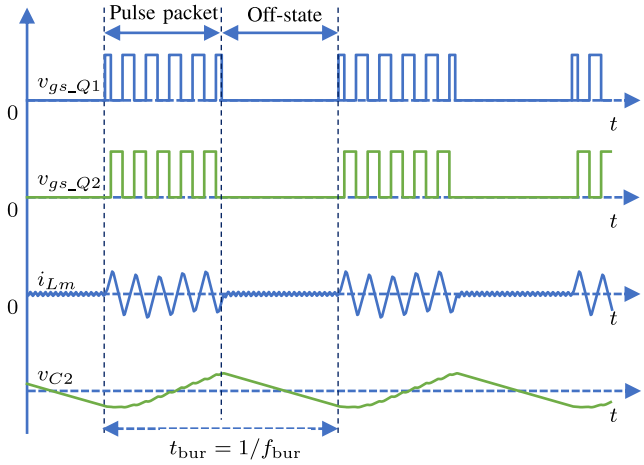

Fig. 3. Waveforms of the SA burst mode control.

Owing to the active H-bridges on both sides, the modulation methods of CLLC converters can be categorized into single active (SA) and dual active (DA), depending on whether the H-bridge secondary side operates like a full-bridge rectifier or not. Both the PFM and PSM described earlier are SA. The DA modulation methods control all eight switches of the CLLC converter and therefore have a higher degree of control freedom compared to SA methods.

In DA modulation method such as extended phase shift (EPS) [5], [14] and triple phase shift (TPS) [15], more phase shift variables (D_0, D_2) are introduced to further improve the efficiency in buck mode. However, the light load efficiency is still unsatisfactory due to the increasing share of switching loss and transformer core loss [6].

Burst mode is the most effective way to improve the light load efficiency of converter and has proven to be successful on LLC converters [16], [17]. The operating waveform of CLLC converter in conventional SA burst mode is shown in Fig. 3, where the controller sends out a pulse packet every t_{bur}, and there is no driving signals in the OFF-state phase.

An optimal SA burst mode control for CLLC converter was proposed in [18], which contains two pulses in each pulse packet and controls the output by adjusting t_{bur}. Another SA burst mode control method for CLLC converter based on trajectory control is proposed in [19]. However, the need for sampling the high-frequency signal v_{cr1} in the resonant tank makes it difficult to realize and only simulation results are provided. And due to the absence of drive signals in the OFF-state of SA burst mode, the interaction between parasitic capacitances and the resonant circuit elements leads to high frequency oscillation and produces high EMI noises [20].

In order to further improve the burst mode performance of the CLLC converter, a time domain based optimal DA burst mode control for CLLC converter is proposed in this article. With DA modulation, the waveforms of v_{ab} and v_{cd} can be controlled independently, thus providing more freedom in controlling the state variables.

As shown in Fig. 4, the proposed burst mode control contains four phases: Zero-state, start, quasi-steady-state, and stop. In the

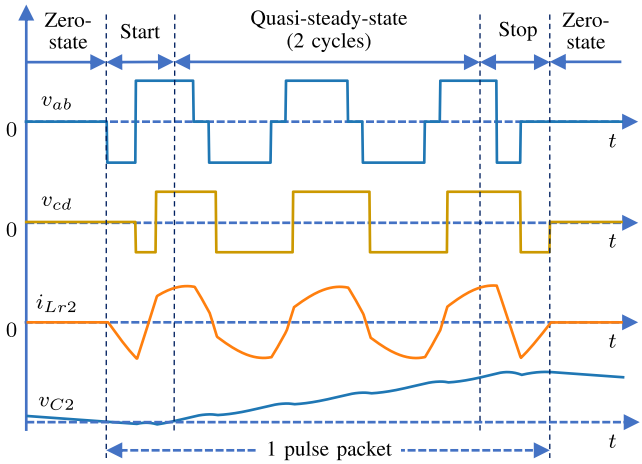

Fig. 4. Typical waveforms of the proposed burst mode control.

zero-state phase, different from the OFF-state phase in SA burst methods, the upper switches of all four half-bridges are kept turned on causing both v_{ab} and v_{cd} to be clamped to 0, and the drive signals in the stop phase is designed to ensure that all state variables reach 0 when entering the zero-state phase, eliminates high-frequency oscillations.

Since there is no power transfer nor loss in the zero-state phase, the average efficiency with the proposed burst mode equals to the efficiency during the pulse packet. And during the pulse packet is mainly the quasi-steady-state phase. In the quasi-steady-state phase, the CLLC converter can be regarded as operating in the normal mode since the output voltage variation is very small, therefore a normal mode optimized modulation method, i.e., current stress optimized-variable frequency-EPS (CSO-VF-EPS) is proposed in this article to further improve the efficiency.

The rest of this article is organized as follows. Section II provides the derivation of the time-domain analytical model of CLLC converter under DA modulation. In Section III, the time domain model based optimal burst mode control method is introduced. Experimental results are provided in Section IV. Finally, Section V concludes this article.

II. Time Domain Model of CLLC

The operating waveforms of CLLC converter with VF-EPS modulation are shown in Fig. 5. There is $D_2 = 0$ in buck mode, while $D_1 = 0$ in boost mode [14].

Compared with EPS, the switching frequency $f_s = 1/T_s$ is added as a new control variable in addition to D_0, D_1 and D_2, they together determine the switching moments (t_1, t_2 and t_3) of v_{ab} and v_{cd} between different voltage levels, and according to t_1, t_2, and t_3 the waveforms during the half switching cycle ($0 < t < T_s/2$) can be divided into three stages.

The equivalent circuit of a single stage is shown in Fig. 6, where v_{ab} and v_{cd} are considered as constants. In addition, there are four independent state variables as

$$\mathbf{x} = \begin{bmatrix} i_{Lr1} & i_{Lr2}/n & -v_{Cr1} & nv_{Cr2} \end{bmatrix}^T. \tag{3}$$

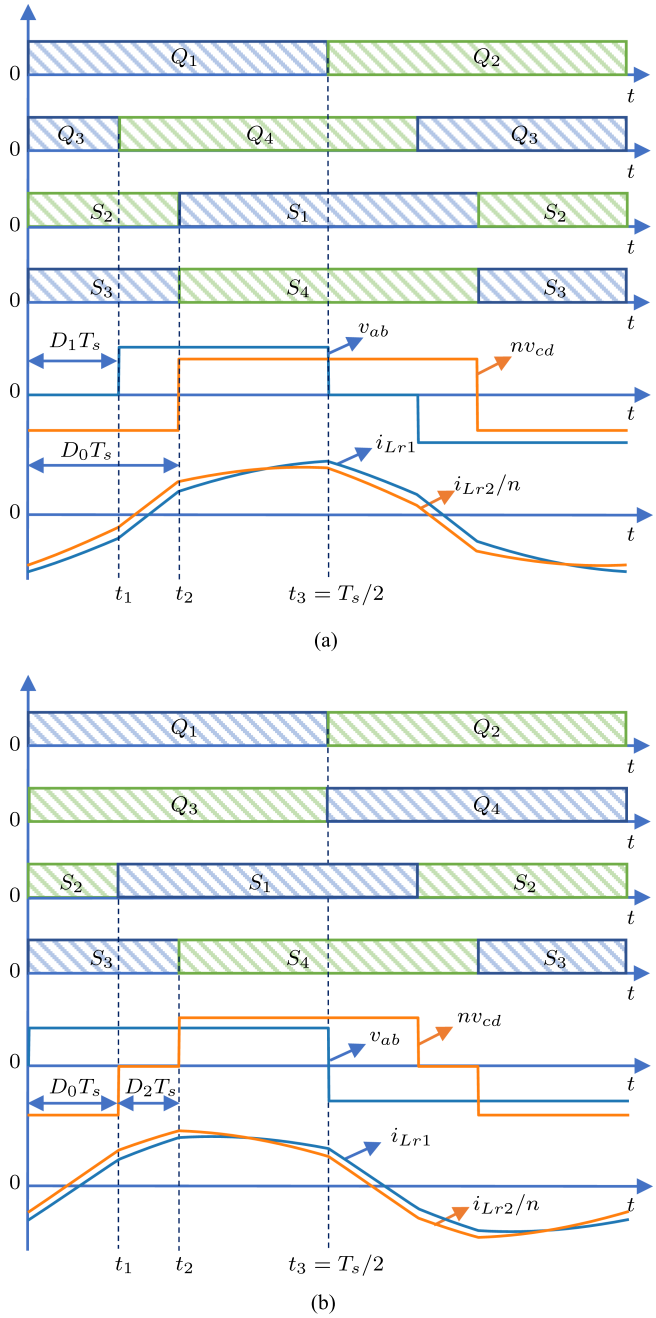

Fig. 5. Typical waveforms of CLLC converter with VF-EPS modulation. (a) Buck mode. (b) Boost mode.

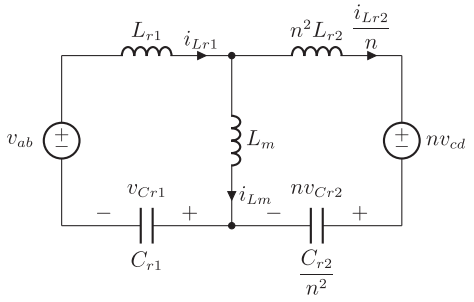

Fig. 6. Equivalent circuit of the CLLC resonant tank.

According to Kirchhoff's circuit laws, there is

$$\begin{cases} i_{Lr1} = i_{Cr1} \\ i_{Lr2} = i_{Cr2} \\ i_{Lm} = i_{Lr1} - i_{Lr2}/n \\ v_{Cr1} = v_{ab} - v_{Lr1} - v_{Lm} \\ nv_{Cr2} = v_{Lm} - nv_{Lr2} - nv_{cd} \end{cases} \tag{4}$$

and based on the differential equations for capacitors and inductors, there is

$$\begin{cases} v_{Lr1} = L_{r1} i'_{Lr1} \\ v_{Lr2} = L_{r2} i'_{Lr2} \\ v_{Lm} = L_m i'_m \\ i_{Cr1} = C_{r1} v'_{Cr1} \\ i_{Cr2} = C_{r2} v'_{Cr2} \end{cases}. \tag{5}$$

Combining (4) and (5) together and eliminating state variables other than nv_{Cr2} gives

$$anv^{(4)}_{Cr2} + bnv''_{Cr2} + n\left(v_{Cr2} + v_{cd}\right) = 0 \tag{6}$$

where

$$\begin{cases} a = (n^2 L_{r1} L_{r2} + L_{r1} L_m + n^2 L_{r2} L_m) C_{r1} C_{r2} / n^2 \\ b = (L_{r1} + L_m) C_{r1} + (n^2 L_{r2} + L_m) C_{r2} / n^2. \end{cases} \tag{7}$$

The characteristic equation of (6) has two pairs of conjugate imaginary roots, denoted $\pm\omega_1 i$ and $\pm\omega_2 i$, respectively, where

$$\omega_{1,2} = \sqrt{\left(b \pm \sqrt{b^2 - 4a}\right)/2a}. \tag{8}$$

Then the generalized solution for $n(v_{Cr2} + v_{cd})$ and its derivatives can be obtained as

$$\mathbf{D}(t) = \mathbf{M_C}(t)\mathbf{C} \tag{9}$$

where

$$\mathbf{M_C}(t) = \begin{bmatrix} \sin\omega_1 t & \cos\omega_1 t & \sin\omega_2 t & \cos\omega_2 t \\ \omega_1 \cos\omega_1 t & -\omega_1 \sin\omega_1 t & \omega_2 \cos\omega_2 t & -\omega_2 \sin\omega_2 t \\ -\omega_1^2 \sin\omega_1 t & -\omega_1^2 \cos\omega_1 t & -\omega_2^2 \sin\omega_2 t & -\omega_2^2 \cos\omega_2 t \\ -\omega_1^3 \cos\omega_1 t & \omega_1^3 \sin\omega_1 t & -\omega_2^3 \cos\omega_2 t & \omega_2^3 \sin\omega_2 t \end{bmatrix} \tag{10}$$

$$\mathbf{D}(t) = \begin{bmatrix} n(v_{Cr2} + v_{cd}) & nv'_{Cr2} & nv''_{Cr2} & nv'''_{Cr2} \end{bmatrix}^T \tag{11}$$

and

$$\mathbf{C} = \begin{bmatrix} c_1 & c_2 & c_3 & c_4 \end{bmatrix}^T. \tag{12}$$

Based on (4) and (5), there also is

$$\mathbf{D}(t) = \mathbf{M_V}\left(\mathbf{x}(t) + \mathbf{S}\right) \tag{13}$$

where

$$\mathbf{M_V} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & \frac{n^2}{C_{r2}} & 0 & 0 \\ 0 & 0 & \frac{n^2 L_{r2}}{a/C_{r1}} & -\frac{L_{r1} + n^2 L_{r2}}{a/C_{r1}} \\ -\frac{n^2 L_{r2}}{a} & -\frac{n^2 L_{r1} + n^4 L_{r2}}{a C_{r2}/C_{r1}} & 0 & 0 \end{bmatrix} \tag{14}$$

$$\mathbf{S} = \begin{bmatrix} 0 & 0 & v_{ab} & nv_{cd} \end{bmatrix}^T. \tag{15}$$

From (13) and (9), there is

$$\mathbf{C} = \mathbf{M_C}(0)^{-1}\mathbf{D}(0) = \mathbf{M_C}(0)^{-1}\mathbf{M_V}\left(\mathbf{x}(0) + \mathbf{S}\right) \tag{16}$$

and

$$\mathbf{x}(t) = \mathbf{M_V^{-1}}\mathbf{M_C}(t)\mathbf{M_C}(0)^{-1}\mathbf{M_V}\left(\mathbf{x}(0) + \mathbf{S}\right) - \mathbf{S}. \tag{17}$$

The variables on the right-hand side of (17) are all known except $\mathbf{x}(0)$, denote

$$\mathbf{A}(t) = \mathbf{M_V^{-1}}\mathbf{M_C}(t)\mathbf{M_C}(0)^{-1}\mathbf{M_V}. \tag{18}$$

Then, according to the symmetry of the state variables during the half switching cycle, the initial values of state variables in Fig. 5 can be expressed as (19).

Since the bridge arm voltages represented by $\mathbf{S}$ are not the same at different stages, $\mathbf{S}_k$ is used to represent the bridge arm voltages of the kth stage and its value can be found in Table I.

By morphing (19) and combine $\mathbf{x}(0)$ in the both side of equation together, the expression for $\mathbf{x}(0)$ can be obtained as (20), with which and (17), it is sufficient to solve for $\mathbf{x}(t)$ at any moment in the switching cycle.

$$\begin{aligned} -\mathbf{x}(0) = \mathbf{x}(t_3) &= \mathbf{A}(t_3 - t_2)\left(\mathbf{x}(t_2) + \mathbf{S}_3\right) - \mathbf{S}_3 \\ &= \mathbf{A}(t_3 - t_2)\left(\mathbf{A}(t_2 - t_1)\left(\mathbf{x}(t_1) + \mathbf{S}_2\right) - \mathbf{S}_2 + \mathbf{S}_3\right) - \mathbf{S}_3 \\ &= \mathbf{A}(t_3 - t_2)\left(\mathbf{A}(t_2 - t_1)\left(\mathbf{A}(t_1)\left(\mathbf{x}(0)\right.\right.\right. \\ &\quad \left.\left.\left. + \mathbf{S}_1\right) - \mathbf{S}_1 + \mathbf{S}_2\right) - \mathbf{S}_2 + \mathbf{S}_3\right) - \mathbf{S}_3 \end{aligned} \tag{19}$$

TABLE I
BRIDGE ARM VOLTAGES OF VF-EPS

Case	$\mathbf{S}_1$	$\mathbf{S}_2$	$\mathbf{S}_3$
$D_2 = 0, D_0 \geq D_1$	$\begin{bmatrix} 0 \\ 0 \\ 0 \\ -nV_2 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ -nV_2 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ nV_2 \end{bmatrix}$
$D_2 = 0, D_0 < D_1$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ -nV_2 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ 0 \\ nV_2 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ nV_2 \end{bmatrix}$
$D_1 = 0, D_0 \geq 0$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ -nV_2 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ nV_2 \end{bmatrix}$
$D_1 = 0, D_0 < 0$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ nV_2 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ V_1 \\ -nV_2 \end{bmatrix}$

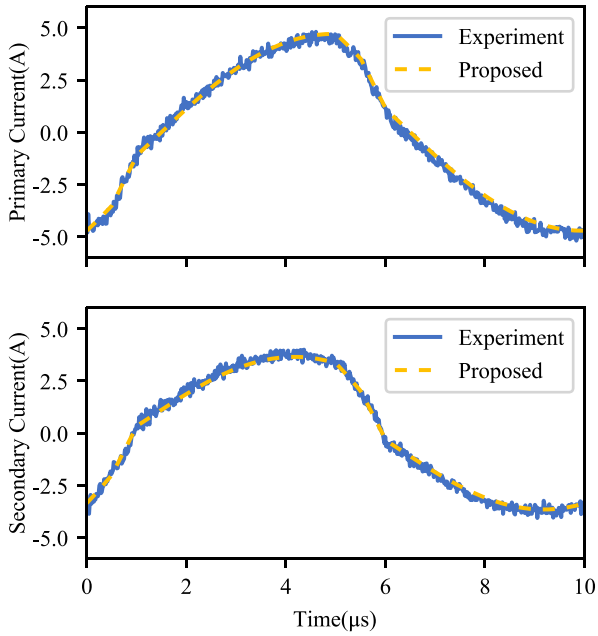

Fig. 7. Waveforms comparison between the proposed model and experiment when $D_0 = 0.1$, $D_1 = 0.05$, $f_s = 100$ kHz and $m = 0.75$.

$$\begin{aligned}\mathbf{x}(0) = & -\left(\mathbf{I} + \mathbf{A}(t_3 - t_2)\mathbf{A}(t_2 - t_1)\mathbf{A}(t_1)\right)^{-1} \\ & \left(\mathbf{A}(t_3 - t_2)\left(\mathbf{A}(t_2 - t_1)\left(\mathbf{A}(t_1)\mathbf{S}_1 - \mathbf{S}_1 + \mathbf{S}_2\right)\right.\right. \\ & \left.\left. -\mathbf{S}_2 + \mathbf{S}_3\right) - \mathbf{S}_3\right). \end{aligned} \tag{20}$$

For the CLLC converter with the parameters shown in Table IV, the comparison of the current waveforms between the measured values and the proposed model is shown in Fig. 7, indicating that the model is in accordance with the experiment.

III. Proposed Burst Mode Control Method

The waveforms of the proposed burst control during one burst cycle are shown in Fig. 4, which can be categorized into the zero-state phase and three phases in the pulse packet.

In the zero-state phase, there is no power flows through the CLLC resonant tank and all state variables remain zero while $Q_{1,3}$ and $S_{1,3}$ are held on to ensure $v_{ab} = v_{cd} = 0$. Since the duration of pulse packet is fixed, the $t_{\rm bur}$ is adjusted by varying the duration of the zero-state phase.

The other three phases in the pulse packet are described below, where the waveforms of the quasi-steady-state phase need to be determined first, as they are required to calculate the waveforms of the other two phases.

A. Quasi-Steady-State Phase

In the quasi-steady-state phase, the waveforms will repeat several switching cycles, and the energy transfer mainly occurs in this phase. Since there is only a small variation in v_{C2} within a single pulse packet, it can be assumed that the performance of the converter in the quasi-steady-state phase is the same as in normal mode. The number of switching cycles can be freely tuned, the larger the number of cycles, the closer the efficiency is to the peak efficiency in normal mode, but the output voltage ripple is also larger. In this article, the number of cycles is fixed to three.

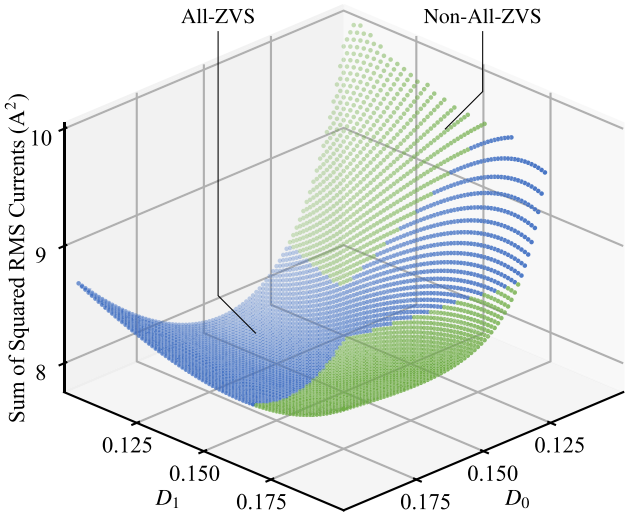

Fig. 8. Sum of squared RMS currents varying with modulation variables D_0 and D_1 when $m = 0.75$ and $p = 500$ W.

The modulation method in the quasi-steady-state phase can be selected and optimized in the same way as for normal mode. Furthermore, the transmission power in this phase is determined by the modulation variables and can be freely selected. In order to maximize the transmission efficiency in quasi-steady-state phase, a CSO-VF-EPS modulation for CLLC converter is proposed here.

As mentioned in the previous section, the VF-EPS modulation has three modulation variables i.e., D_0, D_1 and f_n in buck mode or D_0, D_2 and f_n in boost mode. For a given voltage gain $m = 0.75$, if f_n is adjusted to ensure $p = 500$ W, the current RMS then varies with D_0 and D_1 as shown in Fig. 8. Both the ZVS operation and the current RMS value are related to the combination of modulation variables.

The proposed CSO-VF-EPS modulation method ensures minimized RMS current and full ZVS operations by finding the optimal combination of modulation variables. And the optimization problem can be expressed as follows:

1) *Minimize:* $\sum_{k=1}^{2} i_{Lrk_\rm rms}(D_0, D_1, D_2, f_n)^2$
2) *Subject to:*
   a) *Power constraint:* The calculated power should be equal to its given value.
   b) *Voltage gain constraint:* $D_2 = 0$ when $m \le 1$ and $D_1 = 0$ when $m > 1$.
   c) *ZVS constraints 1:* $i_{Q_k_\rm off} t_{\rm dead} > 2V_1 C_{\rm oss}$
   d) *ZVS constraints 2:* $i_{S_k_\rm off} t_{\rm dead} > 2V_2 C_{\rm oss}$

Where $t_{\rm dead}$ is the dead time in driving signals, and the p in power constraint is taken to be 50% rated load, as this is highest efficiency point of CSO-VF-EPS according to the experimental results in Fig. 25. Then, the optimal results for different m are obtained as Fig. 9.

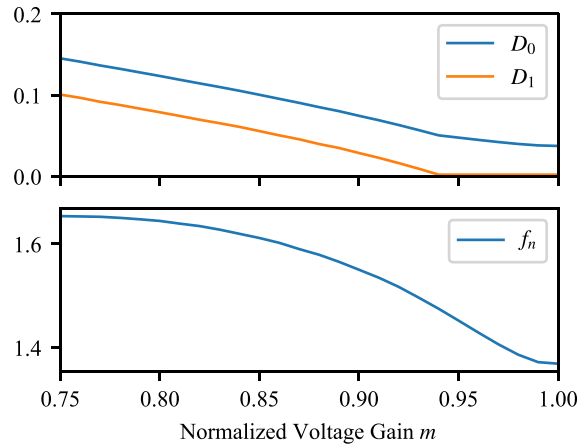

Fig. 9. Optimized modulation variables when $p = 500$ W.

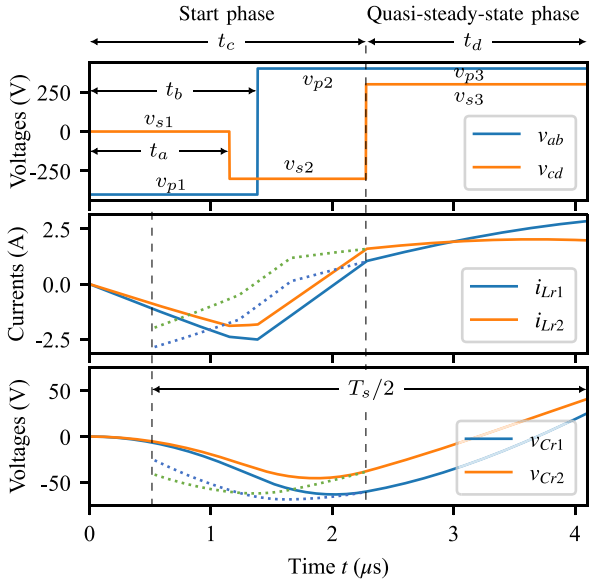

Fig. 10. Waveforms of start phase when $m = 0.75$.

B. Start Phase

The start phase can be regarded as an intermediate process in which the converter switches from zero-state to quasi-steady-state, and the main task of the start phase is to ensure a smooth switching.

The waveforms in the start phase are shown in Fig. 10, where the converter switching from the zero-state phase to the start phase at $t = 0$ and from the start phase to the quasi-steady-state phase at $t = t_c$. The dashed waveforms of the state variables when $t < t_c$ and the solid waveform when $t > t_c$ together constitute half of the quasi-steady-state switching cycle. Thus, t_d is introduced as an additional design degree of freedom so that the final state variables in the start phase can be optimized to be equal to the state variables at any moment in the quasi-steady-state phase.

As shown in Table II, there are a total of eight independent variables to control the waveforms of v_{ab} and v_{cd}, where v_{p3} and v_{s3} are excluded because they are part of the optimized CSO-VF-EPS waveforms for quasi-steady-state phase and determined by t_d.

TABLE II
VALUE RANGE OF VARIABLES IN START PHASE

Variable	Type	Value Range
t_a	Continues	$(0, t_c)$
t_b	Continues	$(0, t_c)$
t_c	Continues	$(0, T_s/2)$
t_d	Continues	$(0, T_s/2)$
v_{p1}	Discrete	$-V_1, 0, V_1$
v_{p2}	Discrete	$-V_1, 0, V_1$
v_{s1}	Discrete	$-V_2, 0, V_2$
v_{s2}	Discrete	$-V_2, 0, V_2$

TABLE III
NON-ZVS OPERATION CONDITIONS

Condition 1	Condition 2	Non-ZVS Count
$v_{p1} \neq 0$		1
$v_{p2} > v_{p1}$	$i_{Lr1}(t_b) > -2V_1C_{\text{oss}}/t_{\text{dead}}$	$(v_{p2} - v_{p1})/V_1$
$v_{p2} < v_{p1}$	$i_{Lr1}(t_b) < 2V_1C_{\text{oss}}/t_{\text{dead}}$	$(v_{p1} - v_{p2})/V_1$
$v_{p3} > v_{p2}$	$i_{Lr1}(t_c) > -2V_1C_{\text{oss}}/t_{\text{dead}}$	$(v_{p3} - v_{p2})/V_1$
$v_{p3} < v_{p2}$	$i_{Lr1}(t_c) < 2V_1C_{\text{oss}}/t_{\text{dead}}$	$(v_{p2} - v_{p3})/V_1$
$v_{s1} \neq 0$		1
$v_{s2} > v_{s1}$	$i_{Lr2}(t_a) < 2V_2C_{\text{oss}}/t_{\text{dead}}$	$(v_{s2} - v_{s1})/V_1$
$v_{s2} < v_{s1}$	$i_{Lr2}(t_a) > -2V_2C_{\text{oss}}/t_{\text{dead}}$	$(v_{s1} - v_{s2})/V_1$
$v_{s3} > v_{s2}$	$i_{Lr2}(t_c) < 2V_2C_{\text{oss}}/t_{\text{dead}}$	$(v_{s3} - v_{s2})/V_1$
$v_{s3} < v_{s2}$	$i_{Lr2}(t_c) > -2V_2C_{\text{oss}}/t_{\text{dead}}$	$(v_{s2} - v_{s3})/V_1$

Based on (17) and (18), the state variables in the start phase can be calculated as

$$\mathbf{x}(t_a) = \mathbf{A}(t_a)\begin{bmatrix}0\\0\\v_{p1}\\nv_{s1}\end{bmatrix} - \begin{bmatrix}0\\0\\v_{p1}\\nv_{s1}\end{bmatrix}, \tag{21}$$

$$\mathbf{x}(t_b) = \mathbf{A}(t_b - t_a)\left(\mathbf{x}(t_a) + \begin{bmatrix}0\\0\\v_{p1}\\nv_{s2}\end{bmatrix}\right) - \begin{bmatrix}0\\0\\v_{p1}\\nv_{s2}\end{bmatrix}, \tag{22}$$

$$\mathbf{x}(t_c) = \mathbf{A}(t_c - t_b)\left(\mathbf{x}(t_b) + \begin{bmatrix}0\\0\\v_{p2}\\nv_{s2}\end{bmatrix}\right) - \begin{bmatrix}0\\0\\v_{p2}\\nv_{s2}\end{bmatrix} \tag{23}$$

where $\mathbf{x}(t_c)$ is the final value of state variables in the start phase, and the previous calculation procedure is for $t_a \leq t_b$ conditions. But it is interesting to note that if one focuses only on $\mathbf{x}(t_c)$, according to the superposition theorem for circuits, it turns out that the previous procedure also applies for $t_a > t_b$.

Non-ZVS operations will significantly increase the switching losses, Table III summarizes all possible non-ZVS cases in the start phase. The total count of non-ZVS operations in the start phase is the sum of all rows that satisfy the conditions. This judgment is based on the turn-OFF current and the non-ZVS

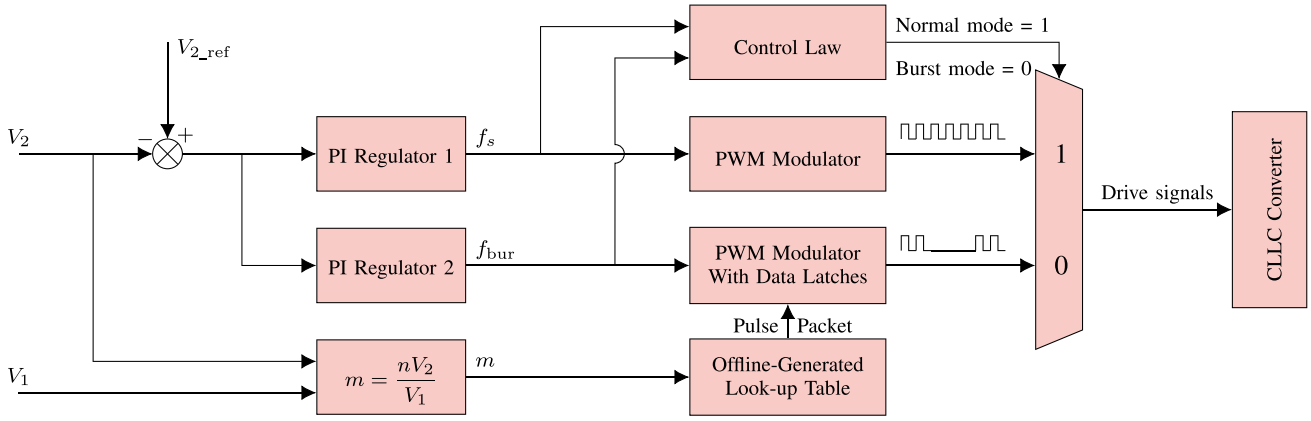

Fig. 11. Close-loop control block diagram of the CLLC converter with proposed burst mode control method.

count in each row may be one or two, depending on the number of switches turned ON during the voltage level change.

Since model errors accumulate over time, the duration of the start phase should be as short as possible. With this as the optimization objective and using the PSO algorithm again, the optimization problem for the variables in start phase can be expressed as

1) *Minimize:* t_c
2) *Subject to:*
   a) *Continues constraint:* $\mathbf{x}(t_c) = \mathbf{x}'(T_s/2 - t_d)$.
   b) *ZVS constraint:* Total count of non-ZVS operations equals one.

The $\mathbf{x}'(t)$ represents the state variables in the optimized CSO-VF-EPS waveforms used in quasi-steady-state, $\mathbf{x}'(T_s/2 - t_d)$ will then be the desired initial value of state variables in the quasi-steady-state. The number of non-ZVS operations is constrained to one, considering that the first switching is necessarily non-ZVS since $\mathbf{x}(0) = \mathbf{0}$.

Compared to the optimization in the quasi-steady-state phase, the PSO algorithm for the start phase contains more independent variables and therefore more likely to fall into local minima. However, since the time-domain model proposed provides analytical solutions, the computation of the fitness function for the PSO algorithm is very fast, and 50 iterations can be completed in 10 seconds with 10,000 particles (Based on Intel Core$^{\text{TM}}$i5-1240P CPU with single-threaded condition.). Thus, the local minima problem can be mitigated by increasing the number of particles and the number of repeated computations.

C. Stop Phase

Like the start phase, the stop phase can also be regarded as an intermediate process in which the converter switches from quasi-steady-state to zero-state. For the stop phase, the calculation of state variables requires an inversion of time, which means t_a, t_b and t_c will be negative, the rest is the same as the start phase and will not be repeated here.

D. Close-Loop Control

When the converter operates in burst mode, the frequency at which the modulator sends out a pulse packet is defined as the fundamental burst frequency f_{bur}, as shown in Fig. 3. The

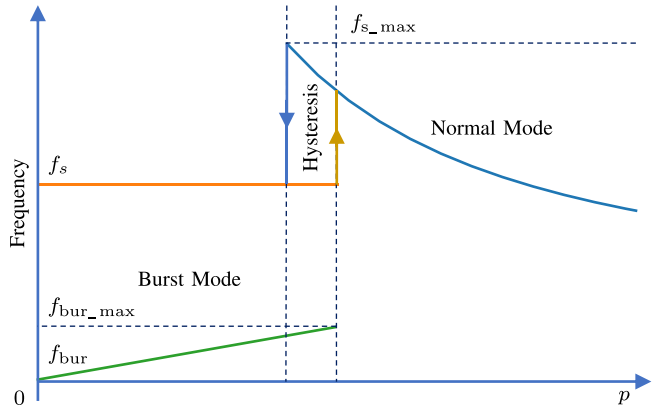

Fig. 12. Control law over entire load range.

waveforms and transmitted energy e_{bur} of each pulse packet are determined by the waveforms of v_{ab} and v_{cd}, independent of the output current. Thus, e_{bur} is essentially the same at the same m and drive signals. And the average transmission power in burst mode

$$p = f_{\text{bur}} e_{\text{bur}}. \tag{24}$$

The close-loop control diagram of the CLLC converter with proposed burst mode is shown in Fig. 11. The "PI Regulator 2" is used to adjust f_{bur} in order to keep the output voltage V_2 close to its reference value V_{2_ref}. A look-up table with pulse packets is required since the optimization results change with m as shown in Fig. 9.

As each pulse packet is about to start, the data latches inside the modulator will read and save the current pulse packet corresponding to m. The pulse packet is then sequentially converted into a train of drive signals to be input into the CLLC converter.

The control law over the entire load range is shown in Fig. 12. In burst mode, f_s represents the switching frequency in the quasi-steady-state phase. And it is independent of the power since the transmission power in quasi-steady-state is fixed at 500 W, while f_{bur} increases with power. When $f_{\text{bur}} \geq f_{\text{bur_max}}$, the converter will switch to normal mode.

In normal mode, the switching frequency f_s will decrease as p increases, and when p decreases, f_s will gradually increase until f_{s_max}, at which time the converter will switch to burst mode.

TABLE IV
MAIN PARAMETERS OF THE CLLC CONVERTER

Parameter	Value
Power	Input voltage $V_1 = 400$V Output voltage $V_2 = 300 - 400$V Transmitting power $p = 0 - 1000$W
Transformer	Material: PC95, bobbin: PQ5050 $L_m = 500\mu$H, $n = 1$ Pri.-28 strands of mylar wire (ϕ 0.1mm * 150, 45.7mΩ) Sec.-28 strands of mylar wire (ϕ 0.1mm * 150, 46.3mΩ)
Inductors	Material: PC44, bobbin: PQ4040 $L_{r1} = L_{r2} = 100\mu$H L_{r1}-20 strands of mylar wire (ϕ 0.1mm * 150, 23.6mΩ) L_{r2}-20 strands of mylar wire (ϕ 0.1mm * 150, 23.4mΩ)
Capacitors	Metallized polypropylene film capacitors (MKP) $C_{r1} = C_{r2} = 44$nF, $C_2 = 35\mu$F C_{r1}, C_{r2}-2 * B32672L8223J000(22nF, TDK) C_2-3D1U356KLMB0420450250EVT(35μF, STE)
Switches	SCT3060AL (ROHM) $R_{\mathrm{DS(on)}} = 80\mathrm{m}\Omega$, $C_{\mathrm{oss}} = 100$pF, $t_{\mathrm{dead}} = 200$ns
Controller	EP4CE10F17C8N

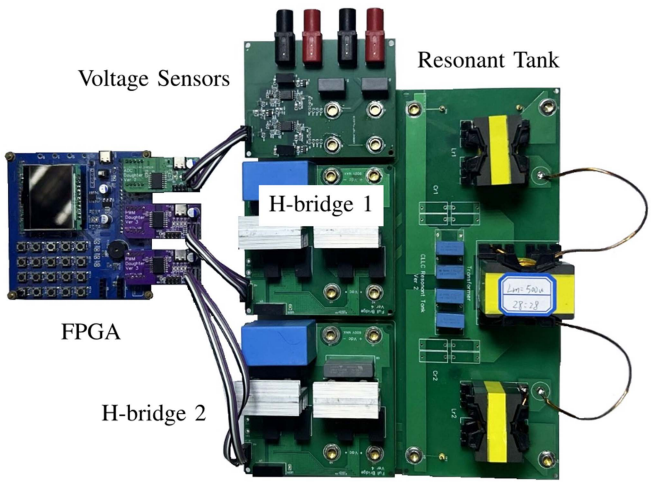

Fig. 13. CLLC prototype.

Since there is a gap in f_s between the two modes, a hysteresis loop is incorporated to improve the robustness of the system.

IV. EXPERIMENTS

A. Experiment Setup

A CLLC converter prototype with symmetrical parameters in Table IV was built to verify the proposed control method as shown in Fig. 13. Metalized polypropylene film capacitors are utilized as the resonant capacitors and filter capacitors due to their excellent high-frequency performance and low dielectric loss. In addition, the design of the parameters of the resonant tank is based on maximizing L_m while ensuring that the voltage gain range with PFM is met, and the results are rounded for ease of fabrication and memorization [8]. A self-made board based on the Intel Cyclone IV EP4CE10 FPGA is used as the controller.

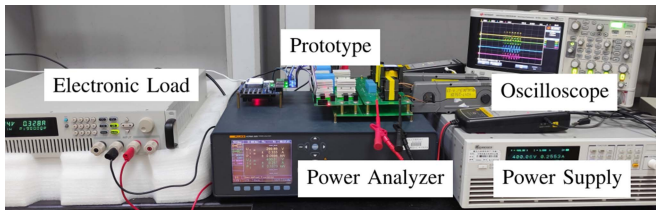

Fig. 14. Experimental test platform.

The corresponding experimental test platform is shown in Fig. 14, where the converter is operating at 100 W load and the four channels of the oscilloscope are measuring the bridge arm voltages and resonant currents respectively. The power analyzer is used to measure the efficiency of the prototype, with its measurement ports are directly connected to the input and output ports on the prototype.

B. Waveform Results

The operation waveforms of CLLC converter with normal mode control methods at 30% rated load are shown in Fig. 15. Since the CLLC converter operations in light load buck mode, the switching frequency of both PFM and CSO-VF-EPS is much higher than that of the quasi-steady-state phase in Fig. 16. The switching frequency of PSM is fixed at resonant frequency but the current RMS of PSM is significantly higher than other control methods.

The pulse packet waveforms at different m are shown in Fig. 16, the switching frequency f_s in the quasi-steady-state decreases with m, which is in accordance with the optimization results in Fig. 9. Benefiting from the ZVS constraints in optimizations of each phase, only the first and last switching in each pulse packet are non-ZVS, and the switching processes between zero-state and quasi-steady-state are smooth.

Since the circuit parameters of the experimental prototype are symmetrical, the operating characteristics after swapping the values of V_1 and V_2 are the same as in reverse operation. The operating waveforms in boost mode are shown in Fig. 17, where the waveforms of the v_{cd} are trilevel instead of the waveforms of v_{ab} in buck mode.

The proposed burst mode waveforms at different powers at $m = 0.75$ are shown in Fig. 18, and the waveforms of a single pulse packet at different powers are the same. The difference lies in the burst frequency f_{bur} and output voltage ripple $\widetilde{v}_{C2}$ where f_{bur} increases with power and $\widetilde{v}_{C2}$ decreases with power.

Methods proposed in [18] and [19] are denoted here as two-pulse SA burst method and three-pulse SA burst method, respectively. And the corresponding operating waveforms are shown in Figs. 19 and 20, respectively. Both SA burst methods suffer from bridge arm voltage oscillations.

As shown in Fig. 18, the proposed method contains multiple switching cycles in each pulse packet, which leads to the inclusion of switching ripple in the output voltage and further leads to an increase in the output voltage ripple. As shown in Fig. 21, the output voltage ripple of the proposed method is slightly higher than the other two SA methods. The peak-to-peak value of the

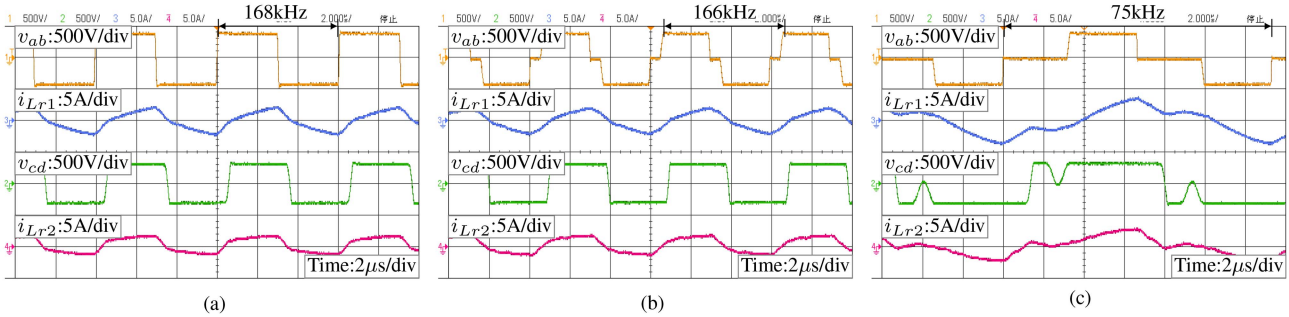

Fig. 15. Waveforms of CLLC converter under various normal mode control methods when $p = 300$ W, $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$. (a) PFM. (b) CSO-VF-EPS. (c) PSM.

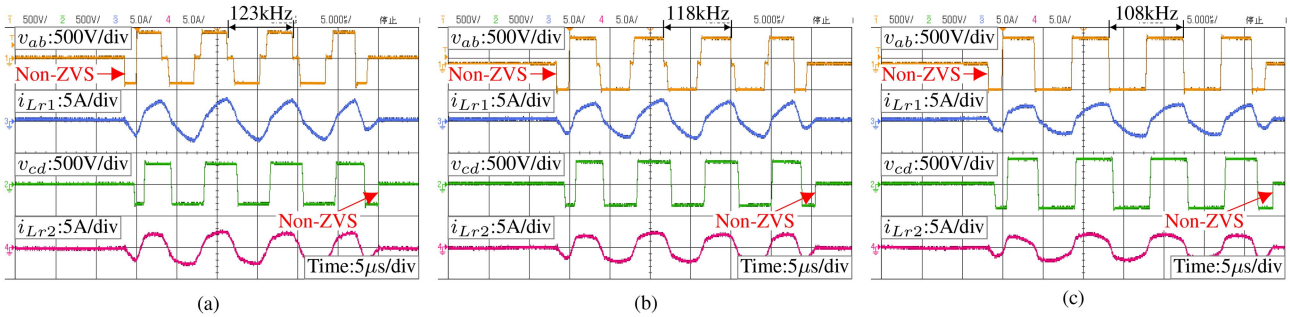

Fig. 16. Pulse packet waveforms of CLLC converter under the proposed burst mode control when $m < 1$. (a) $V_1 = 400$ V, $V_2 = 300$ V, $m = 0.75$. (b) $V_1 = 400$ V, $V_2 = 340$ V, $m = 0.85$. (c) $V_1 = 400$ V, $V_2 = 380$ V, $m = 0.95$.

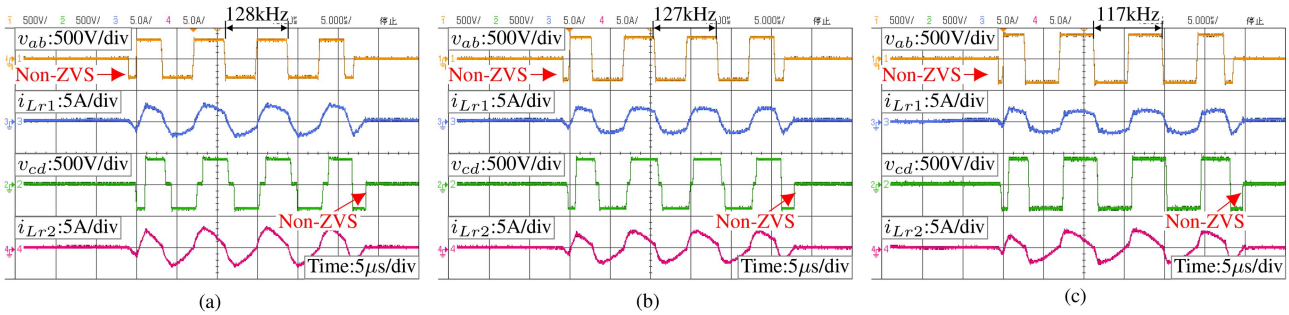

Fig. 17. Pulse packet waveforms of CLLC converter under the proposed burst mode control when $m > 1$. (a) $V_1 = 300$ V, $V_2 = 400$ V, $m = 1.333$. (b) $V_1 = 340$ V, $V_2 = 400$ V, $m = 1.176$. (c) $V_1 = 380$ V, $V_2 = 400$ V, $m = 1.053$.

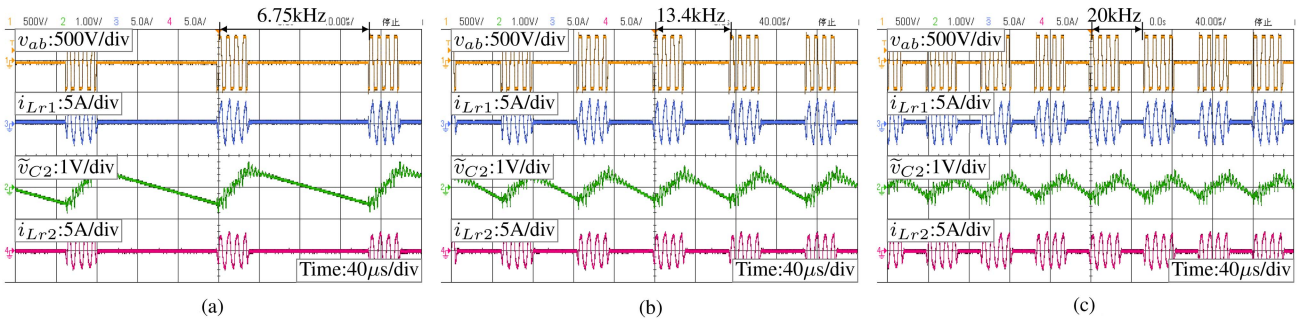

Fig. 18. Waveforms of CLLC converter under the proposed burst mode control when $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$.(a) $p = 100$ W. (b) $p = 200$ W. (c) $p = 300$ W.

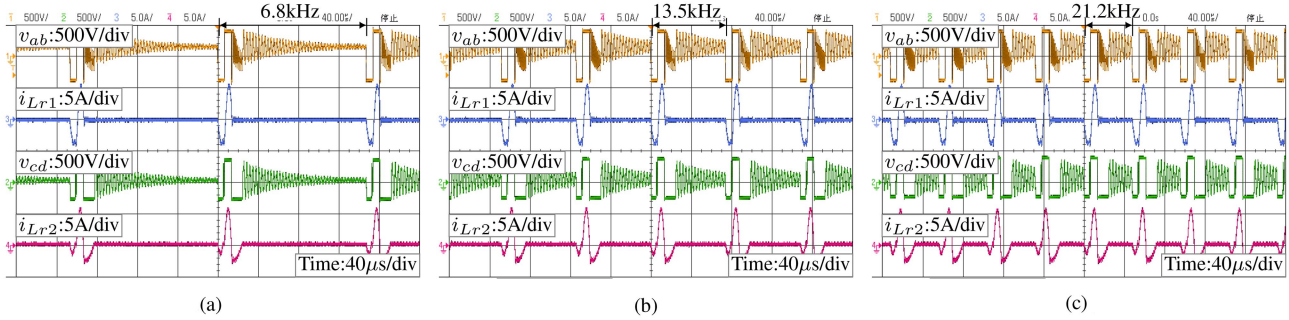

Fig. 19. Waveforms of CLLC converter under two-pulse SA burst mode control when $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$.(a) $p = 100$ W. (b) $p = 200$ W. (c) $p = 300$ W.

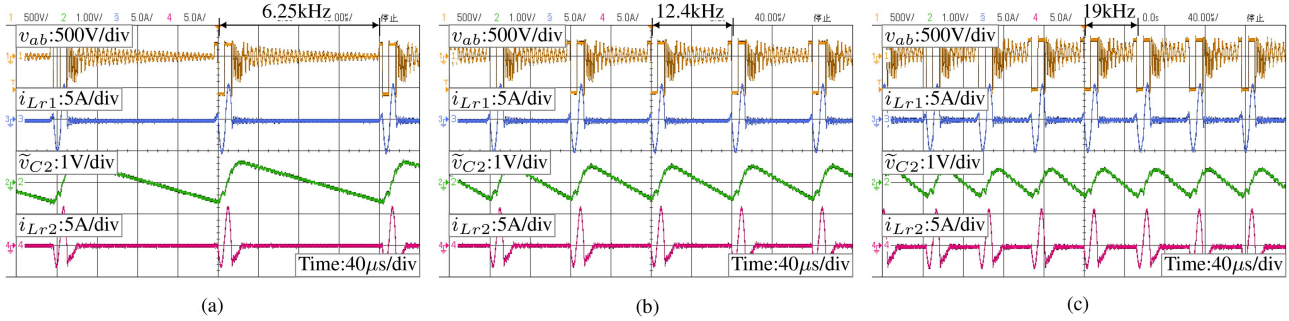

Fig. 20. Waveforms of CLLC converter under three-pulse SA burst mode control when $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$.(a) $p = 100$ W. (b) $p = 200$ W. (c) $p = 300$ W.

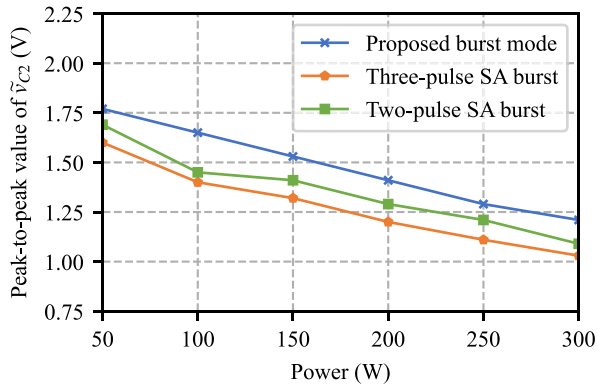

Fig. 21. Measured peak-to-peak value of output voltage ripples $\widetilde{v}_{C2}$ when $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$.

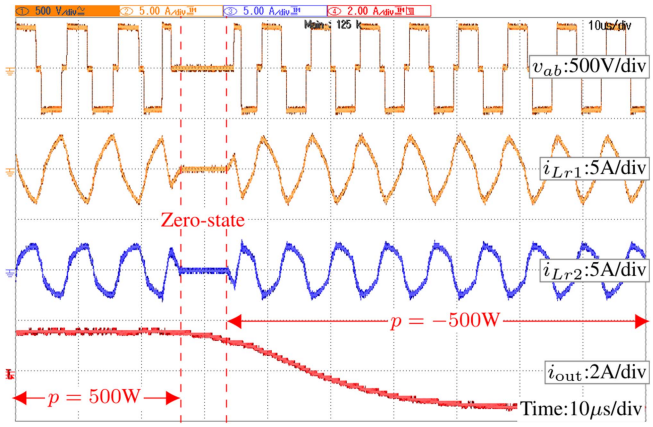

Fig. 22. Waveforms of power transfer direction switching of CLLC converter with the aid of start and stop phase when $V_1 = 400$ V and $V_2 = 300$ V.

output voltage ripple is maximum at $p = 50$ W, which is 0.58% of the output voltage.

With the aid of start and stop phase, fast and smooth switching of the power transfer direction is possible. Fig. 22 shows the open-loop waveforms of the power transfer direction switching with voltage sources connected on both sides. The converter passes sequentially through the stop, zero-state, and start phases and then enters the reverse power transfer state, where the delay in the output current is caused by the output filter capacitor C_2. The duration of the zero-state can be reduced to zero, so that the entire switching process can take only a few microseconds.

The step response dynamic waveforms of the converter for the output reference voltage V_{2_ref} are shown in Fig. 23. The dynamic process of the proposed burst mode control is smooth and able to complete within a few milliseconds.

The dynamic response waveforms of the converter during load jump are shown in Fig. 24. In Fig. 24(a), the load jumps from 10% to 100%, and the converter switches from burst mode to normal mode (CSO-VF-EPS). In Fig. 24(b), the load jumps back to 10%, while the converter switches from normal mode to burst mode.

In summary, the proposed burst mode control is capable of closed-loop operation within the full voltage gain, and the converter can switch operating modes according to the control

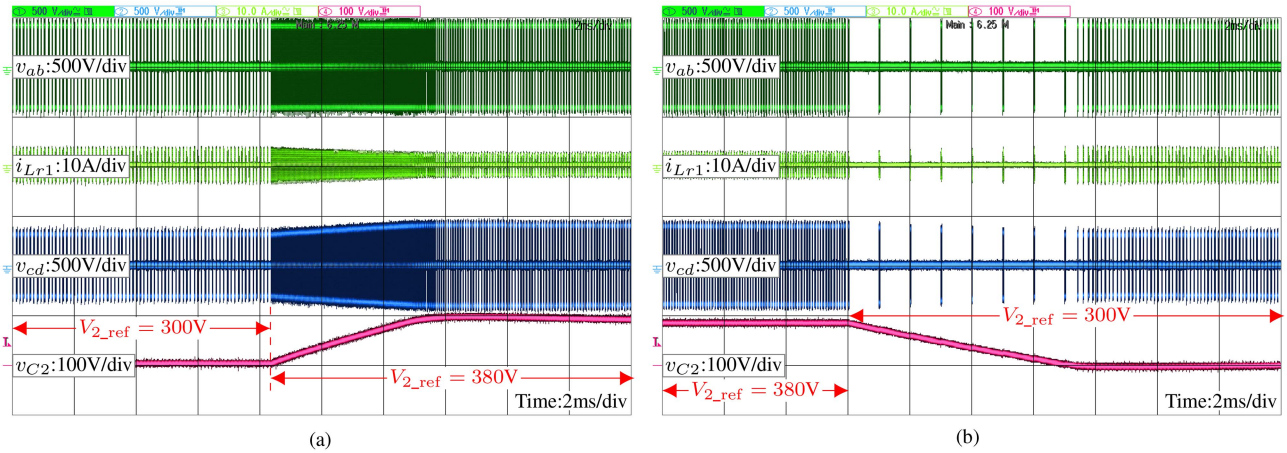

Fig. 23. Dynamic response under close-loop control when $R_L = 600\,\Omega$. (a) Reference output voltage V_{2_ref} step-up from 300 V to 380 V. (b) Reference output voltage V_{2_ref} step-down from 380 V to 300 V.

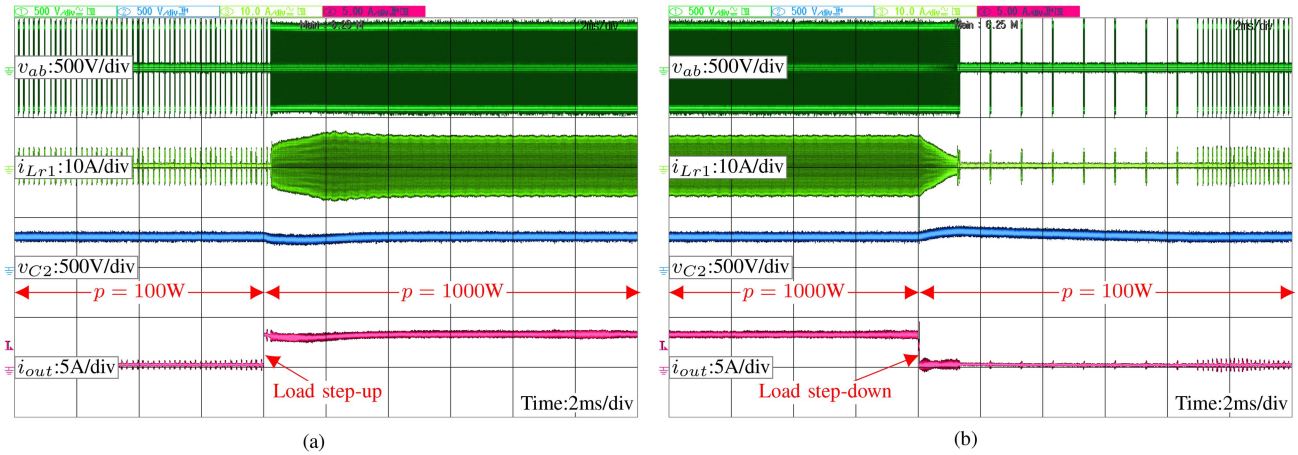

Fig. 24. Dynamic response under close-loop control when $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$. (a) Load step-up from 100 W to 1000 W. (b) Load step-down from 1000 W to 100 W.

law shown in Fig. 12 to achieve stable operation over the full power range.

C. Efficiency Results

The efficiency curves of the CLLC converter prototype with various control methods at $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$ are shown in Fig. 25, where the curve of PFM is incomplete due to unsatisfiable voltage gain. By applying the proposed burst mode control method, the efficiency at 10% rated load of the CLLC converter prototype can reach 97%, which is 1.6%, 1.8%, 3.2%, and 5.6% higher than the three-pulse SA burst, two-pulse SA burst, PSM, and CSO-VF-EPS, respectively.

The calculated power loss percentage of the proposed method at $m = 0.75$ are shown in Fig. 26 and the loss breakdown at $p = 100$ W are summarized as Table V, where the switching and conduction losses are calculated by methods in [7], and the core losses are calculated from [21]. In normal mode, the percentage of core loss remains essentially unchanged, while the percentage of conduction loss increases with load, leading to a decrease in efficiency at heavy loads.

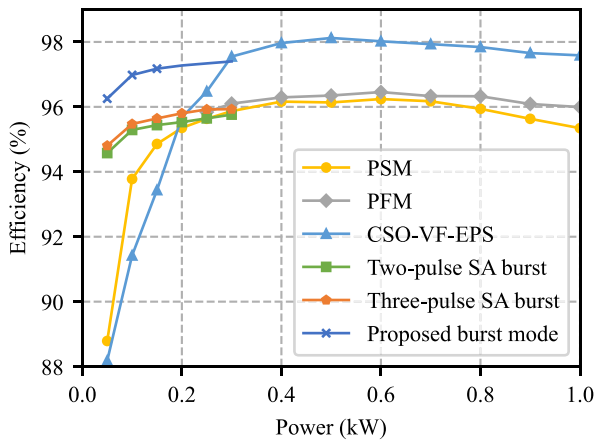

Fig. 25. Experimental efficiency curves of the CLLC converter prototype when $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$.

In burst mode the switching loss percentage increases significantly, which is caused by the two non-ZVS operations included in every pulse packet. If V_1 and V_2 stay constant, the burst

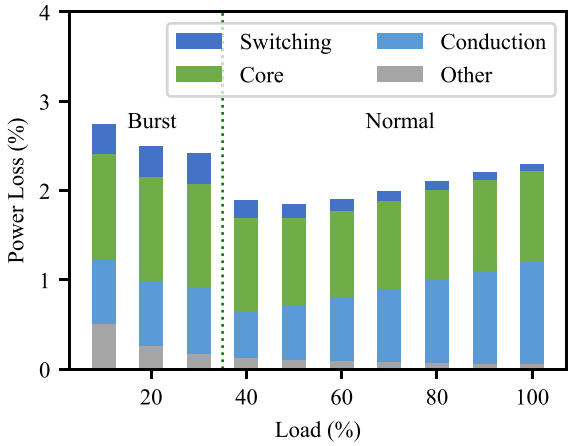

Fig. 26. Calculated power loss percentage under the proposed control method at different load when $V_1 = 400$ V, $V_2 = 300$ V and $m = 0.75$.

TABLE V
LOSS BREAKDOWN

Type	Component	(W)
Conduction	Transformer	0.135
	Primary resonant inductor	0.039
	Secondary resonant inductor	0.029
	Capacitors	0.062
	Primary switches	0.211
	Secondary switches	0.162
	PCB	0.094
Core	Transformer	0.452
	Primary resonant inductor	0.429
	Secondary resonant inductor	0.289
Switching	Primary switches	0.232
	Secondary switches	0.111
Other	Voltage sampling resistors	0.5
Sum(calculated)		2.75
Efficiency(measured)		97.0%

frequency f_{bur} of the proposed burst mode varies with transmitting power, while the operating waveforms and efficiency of each pulse packet should be the same. The other losses are mainly due to the sampling resistors, which equals to $(V_1^2 + V_2^2)/R_{\text{sample}}$ and therefore remains essentially unchanged with load, and the percentage increases as the load is reduced.

In Table V, the conduction losses and the inductor core losses are directly related to the magnitude of resonant currents, and together they account for 64.4% of all losses except for the fixed sampling resistor loss. Therefore, the rms currents is selected as the optimization objective.

Thermal images of the experimental prototype under different operating conditions are shown in Fig. 27. The highest point of temperature in both image is the voltage sampling resistors. In addition, the losses in the resonant tank are concentrated in the transformer and the two resonant inductors. As shown in Table V, the losses in the primary inductor are higher than the secondary, and therefore the temperature of the primary resonant inductor L_{r1} is higher than the secondary resonant inductor L_{r2}.

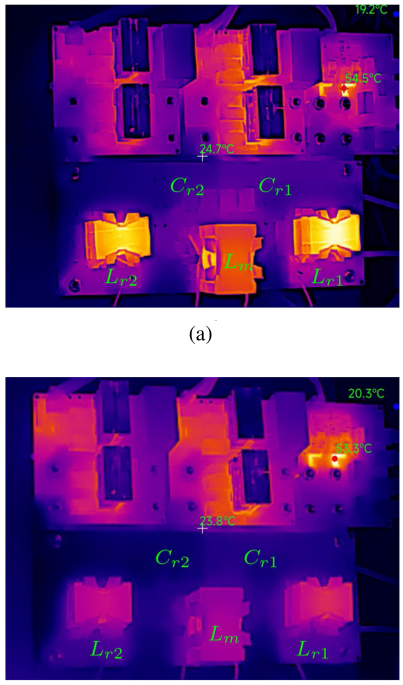

Fig. 27. Thermal images of the experimental prototype operating at $V_1 = 400$ V, $V_2 = 300$ V. (a) With CSO-VF-EPS, $p = 1000$ W. (b) With proposed burst mode, $p = 200$ W.

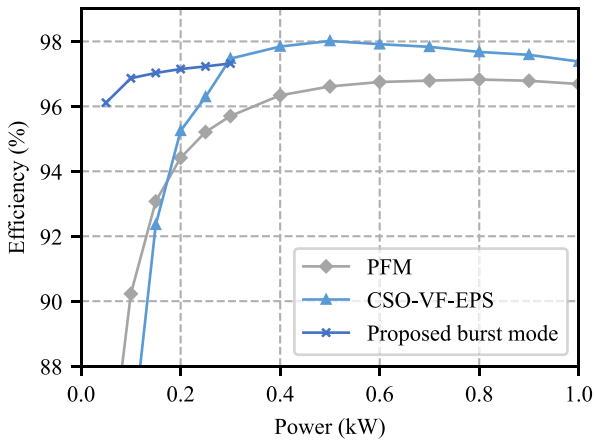

Fig. 28. Experimental efficiency curves of the CLLC converter prototype when $V_1 = 300$ V, $V_2 = 400$ V and $m = 1.33$.

The efficiency test results in boost mode are shown in Fig. 28, which excludes PSM and the other two SA burst modes since they are not capable for boost mode operation. And the efficiency of the proposed burst mode control in boost mode is almost the same as that in buck mode.

The efficiency curves with various control methods at $p = 100$ W are shown in Fig. 29, where there is no curve for PFM since the voltage gain cannot be satisfied with PFM control under such a light load. During mass fabrication, there are deviations in the circuit parameters (L_{r1}, L_{r2}, L_m, C_{r1} and C_{r2}) which in turn cause the operation waveforms to deviate from the optimized results and ultimately lead to a reduction in efficiency. Taking the maximum deviation as 5%, the error reaches its maximum

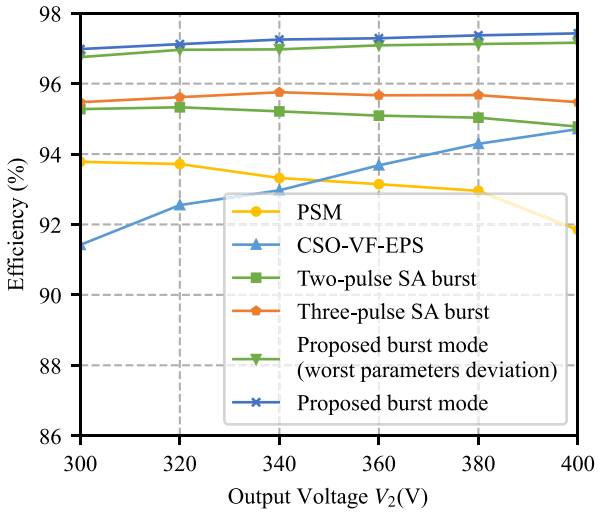

Fig. 29. Experimental efficiency curves of the CLLC converter prototype when $V_1 = 400$ V and $p = 100$ W.

when all the circuit parameters are 95% of their design values. As shown in Fig. 29, the average efficiency decreases by 0.24% in the worst parameter deviation condition compared to when there is no circuit parameter deviation.

For resonant converters, usually the closer m is to 1, the higher the efficiency. However, under light load conditions somewhat differently, the efficiency under PSM control decreases with the increase of m. This is mainly because the frequency of PSM is fixed and the core loss of transformer increases with the output voltage. For SA burst modes, on the other hand, the energy transmitted per pulse packet decreases as m increases, which leads to a decrease in efficiency.

To summarize, the efficiency test results show that the proposed burst mode control method can significantly improve the light load efficiency of the CLLC converter.

V. Conclusion

In this article, a burst mode control method with DA modulation for CLLC converter based on time-domain model is proposed. The look-up table computed based on the time-domain model and PSO optimization algorithm maximizes the use of the degrees of freedom in the DA modulation, and achieves the minimization of the current RMS for each pulse packet. Compared to the existing SA burst mode control methods, the proposed method has no high frequency oscillations. By modifying the circuit parameters in the CLLC resonant tank, the method proposed in this article can be directly applied to other types of IBDCs such as bidirectional LLC, bidirectional series resonant converter, and dual-active-bridge. Finally, a 1-kW CLLC converter prototype was built, and the proposed burst mode control method was fully verified by comparing it with other control methods, such as PFM, PSM, and SA burst modes. The experimental results show that the proposed method has the highest light load efficiency among these methods.

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