A Real-Time Simulation Model With Constant Admittance Matrix for Multiple Grid-Connected Converters System

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***Abstract*—Real-time simulation (RTS) is indispensable for validating multiple grid-connected converter systems that form the backbone of renewable energy stations. In this article, an RTS model for multiple grid-connected converters system is proposed by utilizing a half-step prediction-correction method. This model ensures a constant admittance matrix and facilitates delay-free decoupling of the converters. Furthermore, a hardware solution engine and implementation method using the field programmable gate array (FPGA) are developed for multiple converters system. Finally, the high accuracy and validity of the proposed model (PM) are validated through offline simulation, a physical prototype, and an FPGA-based RTS platform. The FPGA-based simulation results demonstrate that the PM can achieve RTS with 500-ns (minimum up to 80-ns) time-step for a radial multiconverter system comprising 130 converters (780 switching devices). For a trunk multiconverter system consisting of 11 converters (66 switching devices), the model can also achieve 500-ns (50 clock cycles) RTS. Compared with RT-LAB simulator, existing methods, and nodal analysis method, it exhibits certain advantages in terms of simulation scale, hardware resource usage and time-step.**

***Index Terms*—Delay-free decoupling, field programmable gate array (FPGA), half-step prediction-correction, multiple grid-connected converters system, real-time simulation (RTS).**

I. Introduction

THE rapid development of new type power system has led to a higher penetration of power electronic equipment in power system. Real-time simulation (RTS) plays a pivotal technical instrument for the online validation of the secure and reliable operation of multiconverter systems that constitute the foundation of renewable energy power stations [1], [2], [3], [4].

The utilization of decoupling techniques for RTS of multiple grid-connected converters system is an effective and prevalent methodology [5]. At the circuit solution level, the fundamental premise of decoupling is the partitioning of a complex circuit system into discrete, smaller subsystems that can be solved in parallel through the introduction of interface time-delay, thereby eliminating coupling at specific network connections. The subject of decoupling techniques has been the focus of extensive investigation within a substantial body of existing literature. The classical decoupling methods include the transmission line decoupling method [6], the multiregion Thevenin equivalent method [7], and the node tearing method [8]. These methods entail the programming of a large node admittance matrix into several smaller matrices, which serves to reduce the computational and storage pressure. These methods are primarily designed for utilization with ac systems. Nevertheless, the efficiency of these techniques needs to be improved when applied to multiconverter systems.

The latency insertion method (LIM), as proposed in [9] and [10], facilitates the decoupling of branch current and node voltage solutions by a half-step time-delay, thereby achieving fine-grained parallelism at the branch level. However, the inclusion of auxiliary inductors and capacitors can alter the dynamic characteristics of the system, thereby constraining the permissible simulation time-step and potentially limiting the overall efficiency [11]. In [12], a method for simulating microgrids that achieves submicrosecond simulation times and decouples distributed generation systems based on LIM is proposed. Moreover, Zheng et al. [13], a semi-implicit parallel shuffled frog leaping solver that employs a half-step sampling technique is proposed, which employs a similar solving process to LIM, further advancing the capabilities for RTS.

A solution framework based on the node voltage method has been designed in [14] to enhance the simulation efficiency of a multiconverter system. Kato et al. [15] present a hybrid method that combines explicit and implicit equations to achieve decoupling, thereby enabling multirate simulation of voltage source converters (VSCs). In [16], the power electronic transformer (PET) is decoupled using an approximate equivalence of the

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port voltage with one-step time-delay, on the basis that the dynamics of dc capacitors are much slower. Consequently, they are selected as the interfaces between the partitioned subcircuits in [17]. The solver introduced in [18] partitions the circuit with energy storage elements by using the higher order derivatives of the energy storage elements. The introduction of coupling variables during circuit division is a crucial aspect of the process. Nevertheless, the introduction of artificial time-delay is typically obligatory, yet it may potentially compromise the simulation accuracy and numerical stability in these methods.

In [19], a delay-free decoupling method is proposed and subsequently applied to RTS. However, the prediction step in this method requires consideration of two time-steps, which may potentially impact the precision of the resulting outcomes. In [20], state-space nodal (SSN) method is proposed by OPAL-RT, which utilizes the state-space method to model the subsystems and subsequently transforms them into the form of the nodal method. Subsequently, the method is converted into the form of the nodal method in order to solve the global solution, which is suitable for solving large-scale power electronic systems (PESs). Nevertheless, this approach is inherently constrained by the inability to parallelize the calculations of current and voltage at the node decomposition stage. The method proposed in [21] is equally efficacious in achieving decoupling, while maintaining a balance between accuracy and numerical stability. However, this method lacks the constant admittance feature. Besides, Sun et al. [22] propose a low resource consumption field programmable gate array (FPGA)-based RTS method for power electronic converters, which greatly reduces the dependence on multipliers through shift-addition operations, thus optimizing resource utilization and enhancing computational efficiency.

A parameterized average value model is proposed in [23] and [24], which achieves comparable simulation accuracy to one-step delay decoupling model with large time-steps. However, its admittance matrix varies with time. In [25], the admittance-based modeling is proposed and developed into the Norton equivalent circuits and simultaneously solved with the overall network nodal equation without one-step time-delay. In [26], RTDS proposed the universal converter model (UCM). This model uses a state-space modeling method to solve the two-terminal circuits of the converter in strict tandem, eliminating the delay problem of the traditional controlled source algorithm.

In addition, with the application and development of SiC-based devices, the operating frequency of converters is expected to reach hundreds of kHz. This means that the time-step for RTS will become smaller, potentially reaching tens of nanoseconds (ns) [27], [28].

In all, the existing research has two main limitations.

1) The decoupling at the circuit level is contingent upon the half-step or one-step time-delay, which may give rise to inaccuracy. Furthermore, the requisite simulation time-step varies depending on the specific application scenario.
2) Decoupling at the circuit solution level, such as SSN or UCM, does not fully achieve the desired segmentation of the circuit. Moreover, the parallelism of these algorithms could be improved further.

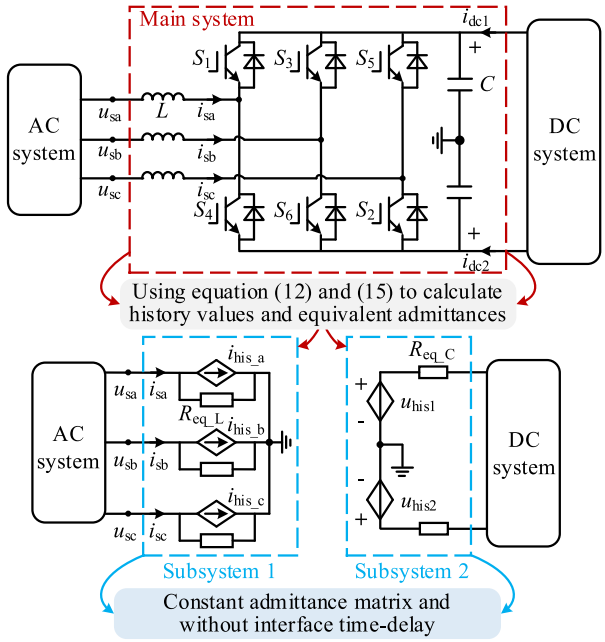

Fig. 1. Topology of a VSC and its equivalent circuit.

In this article, a simulation model with a constant admittance matrix for multiple grid-connected converters is proposed and applied to FPGA-based RTS. The contributions are listed as follows:

1) A RTS model integrated with the half-step prediction-correction method is proposed, which offers higher accuracy and a larger stability region compared with the traditional time-delay method.
2) An equivalent circuit for converter is derived, which has constant admittance matrix and no interface time-delay. Furthermore, the equivalent circuits for multiple grid-connected converters are also derived.
3) The FPGA-based hardware implementation and RTS solution engine for multiple grid-connected converters are designed.

The rest of this article is organized as follows. In Section II, the VSC dynamics, the derived circuit, the stability analysis, and the proposed method are illustrated. In Section III, the design of the solver engine and the hardware implementation process are proposed. The simulation and experimental validation results of the proposed model (PM) are presented in Sections IV and V, respectively. In the end, Section VI concludes this article.

II. Description of the PM

The PM for multiconverter system and the numerical stability region is described in this section.

A. Description of the VSC Dynamics

The topology of a VSC is illustrated in Fig. 1, which contains 2 capacitors, 3 inductors, and 6 power electronic switches (S_1 to S_6). The dynamic characteristics of capacitors can be described

in the following equation:

$$\begin{bmatrix} C\frac{\mathrm{d}u_{\mathrm{C1}}(t)}{\mathrm{d}t} \\ C\frac{\mathrm{d}u_{\mathrm{C2}}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} \frac{R_4}{R_{\mathrm{sum}}} & \frac{R_6}{R_{\mathrm{sum}}} & \frac{R_2}{R_{\mathrm{sum}}} \\ \frac{R_1}{R_{\mathrm{sum}}} & \frac{R_3}{R_{\mathrm{sum}}} & \frac{R_5}{R_{\mathrm{sum}}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{sa}}(t) \\ i_{\mathrm{sb}}(t) \\ i_{\mathrm{sc}}(t) \end{bmatrix} + \begin{bmatrix} i_{\mathrm{dc1}}(t) \\ i_{\mathrm{dc2}}(t) \end{bmatrix} \quad (1)$$

where R_k (k = 1, 2, …, 6) represents the resistance of 6 switches, respectively. R_{sum} represents the sum of resistance in the same bridge arm, which equals the summation of R_{on} (on-state resistance) and R_{off} (OFF-state resistance).

The (1) can be equivalently expressed as

$$\dot{\boldsymbol{u}}_{\mathrm{C}} = \boldsymbol{C}^{-1}\boldsymbol{M}_{\mathrm{C}}\boldsymbol{i}_{\mathrm{s}} + \boldsymbol{C}^{-1}\boldsymbol{i}_{\mathrm{dc}}. \quad (2)$$

Similarly, the dynamic characteristics of inductors can be described as follows:

$$\begin{bmatrix} L\frac{\mathrm{d}i_{\mathrm{sa}}(t)}{\mathrm{d}t} \\ L\frac{\mathrm{d}i_{\mathrm{sb}}(t)}{\mathrm{d}t} \\ L\frac{\mathrm{d}i_{\mathrm{sc}}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{sa}}(t) \\ u_{\mathrm{sb}}(t) \\ u_{\mathrm{sc}}(t) \end{bmatrix} - \begin{bmatrix} \frac{R_4}{R_{\mathrm{sum}}} & \frac{R_1}{R_{\mathrm{sum}}} \\ \frac{R_6}{R_{\mathrm{sum}}} & \frac{R_3}{R_{\mathrm{sum}}} \\ \frac{R_2}{R_{\mathrm{sum}}} & \frac{R_5}{R_{\mathrm{sum}}} \end{bmatrix} \begin{bmatrix} u_{\mathrm{C1}}(t) \\ u_{\mathrm{C2}}(t) \end{bmatrix} - \begin{bmatrix} R_{\mathrm{on}}i_{\mathrm{sa}}(t) \\ R_{\mathrm{on}}i_{\mathrm{sb}}(t) \\ R_{\mathrm{on}}i_{\mathrm{sc}}(t) \end{bmatrix}. \quad (3)$$

Equation (3) can be further equivalently expressed as follows:

$$\dot{\boldsymbol{i}}_{\mathrm{s}} = -\boldsymbol{L}^{-1}\boldsymbol{M}_{\mathrm{L}}\boldsymbol{u}_{\mathrm{C}} - \boldsymbol{L}^{-1}\boldsymbol{R}_{\mathrm{on}}\boldsymbol{i}_{\mathrm{s}} + \boldsymbol{L}^{-1}\boldsymbol{u}_{\mathrm{s}}. \quad (4)$$

Then, the dynamic characteristics of VSC can be described by state equation as follows:

$$\begin{bmatrix} \dot{\boldsymbol{u}}_{\mathrm{C}} \\ \dot{\boldsymbol{i}}_{\mathrm{s}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{0} & \boldsymbol{C}^{-1}\boldsymbol{M}_{\mathrm{C}} \\ -\boldsymbol{L}^{-1}\boldsymbol{M}_{\mathrm{L}} & -\boldsymbol{L}^{-1}\boldsymbol{R}_{\mathrm{on}} \end{bmatrix} \begin{bmatrix} \boldsymbol{u}_{\mathrm{C}} \\ \boldsymbol{i}_{\mathrm{s}} \end{bmatrix} + \begin{bmatrix} \boldsymbol{C}^{-1} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{L}^{-1} \end{bmatrix} \begin{bmatrix} \boldsymbol{i}_{\mathrm{dc}} \\ \boldsymbol{u}_{\mathrm{s}} \end{bmatrix}. \quad (5)$$

B. Proposed Half-Step Prediction-Correction Method

The integral format based on half-step prediction-correction of the proposed method is shown in the following equation:

$$\begin{cases} \int_t^{t+\frac{\Delta t}{2}} \dot{\boldsymbol{x}}(t) = \underbrace{\int_t^{t+\frac{\Delta t}{2}} (\boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{B}\boldsymbol{u}(t))}_{\mathrm{Half-stepexplicitintegral}} \\ \int_t^{t+\Delta t} \dot{\boldsymbol{x}}(t) = \underbrace{\int_t^{t+\Delta t} (\boldsymbol{A}_\alpha\boldsymbol{x}(t) + \boldsymbol{B}\boldsymbol{u}(t))}_{\mathrm{Trapezoidalintegral}} + \underbrace{\int_t^{t+\Delta t} \boldsymbol{A}_\beta\boldsymbol{x}(t)}_{\mathrm{Centralintegral}} \end{cases} \quad (6)$$

where $\boldsymbol{A}_\alpha$ is the diagonal part of state matrix $\boldsymbol{A}$, including the constant admittance elements; $\boldsymbol{A}_\beta$ is the nondiagonal part of $\boldsymbol{A}$, which contains the variable admittance elements; $\boldsymbol{x}$ is the matrix of state variables; $\boldsymbol{u}$ is the matrix of input variables; $\boldsymbol{B}$ is a coefficient matrix composed of fixed elements; Δt is simulation time-step.

As illustrated in (6), the proposed method incorporates half-step explicit, central, and trapezoidal integrals. The discrete state equation can be derived as follows:

$$\begin{cases} \hat{\boldsymbol{x}}\left(t+\frac{\Delta t}{2}\right) = \left(\frac{\Delta t}{2}\boldsymbol{A} + \boldsymbol{E}\right)\boldsymbol{x}(t) + \frac{\Delta t}{2}\boldsymbol{B}\boldsymbol{u}(t) \\ \boldsymbol{x}(t+\Delta t) = \left(\boldsymbol{E} - \frac{\Delta t}{2}\boldsymbol{A}_\alpha\right)^{-1}\left(\left(\boldsymbol{E} + \frac{\Delta t}{2}\boldsymbol{A}_\alpha\right)\boldsymbol{x}(t) \right. \\ \qquad \left. + \Delta t\boldsymbol{A}_\beta\hat{\boldsymbol{x}}\left(t+\frac{\Delta t}{2}\right)\right) \\ \qquad + \frac{\Delta t}{2}\left(\boldsymbol{E} - \frac{\Delta t}{2}\boldsymbol{A}_\alpha\right)^{-1}\boldsymbol{B}\left(\boldsymbol{u}(t+\Delta t) + \boldsymbol{u}(t)\right) \end{cases}. \quad (7)$$

Incorporating the predicted values into the correction step, (7) can be further derived as follows:

$$\boldsymbol{x}(t+\Delta t) = \boldsymbol{M}\boldsymbol{x}(t) + \boldsymbol{N}\boldsymbol{u}(t) + \boldsymbol{Y}\boldsymbol{u}(t+\Delta t) \quad (8)$$

where

$$\begin{cases} \boldsymbol{M} = \left(\boldsymbol{E} - \frac{\Delta t}{2}\boldsymbol{A}_\alpha\right)^{-1}\left(\left(\boldsymbol{E} + \frac{\Delta t}{2}\boldsymbol{A}_\alpha\right) \right. \\ \qquad \left. + \Delta t\boldsymbol{A}_\beta\left(\frac{\Delta t}{2}\boldsymbol{A} + \boldsymbol{E}\right)\right) \\ \boldsymbol{N} = \left(\boldsymbol{E} - \frac{\Delta t}{2}\boldsymbol{A}_\alpha\right)^{-1}\left(\frac{\Delta t^2}{2}\boldsymbol{A}_\beta\boldsymbol{B} + \frac{\Delta t}{2}\boldsymbol{B}\right) \\ \boldsymbol{Y} = \frac{\Delta t}{2}\left(\boldsymbol{E} - \frac{\Delta t}{2}\boldsymbol{A}_\alpha\right)^{-1}\boldsymbol{B} \end{cases}. \quad (9)$$

Equation(8) can be further expressed as a form of (10) containing two subsystems $\boldsymbol{x}_1$ and $\boldsymbol{x}_2$

$$\begin{bmatrix} \boldsymbol{x}_1(t+\Delta t) \\ \boldsymbol{x}_2(t+\Delta t) \end{bmatrix} = \boldsymbol{M}\begin{bmatrix} \boldsymbol{x}_1(t) \\ \boldsymbol{x}_2(t) \end{bmatrix} + \boldsymbol{N}\begin{bmatrix} \boldsymbol{u}_1(t) \\ \boldsymbol{u}_2(t) \end{bmatrix} + \boldsymbol{Y}\begin{bmatrix} \boldsymbol{u}_1(t+\Delta t) \\ \boldsymbol{u}_2(t+\Delta t) \end{bmatrix}. \quad (10)$$

From (10), we can get that that the proposed method does not require an iterative process, has a constant admittance matrix as the matrix $\boldsymbol{B}, \boldsymbol{A}_\alpha$ are all constant, and the subsystem $\boldsymbol{x}_1, \boldsymbol{x}_2$ can be solved in parallel.

C. Derived Companion Equivalent Circuit

Equation (10) can be further rewritten as the form of nodal voltage equation shown in (11), which contains the historical items

$$\begin{bmatrix} \boldsymbol{x}_1(t+\Delta t) \\ \boldsymbol{x}_2(t+\Delta t) \end{bmatrix} = \boldsymbol{Y}\begin{bmatrix} \boldsymbol{u}_1(t+\Delta t) \\ \boldsymbol{u}_2(t+\Delta t) \end{bmatrix} + \begin{bmatrix} \boldsymbol{x}_{\mathrm{his1}}(t) \\ \boldsymbol{x}_{\mathrm{his2}}(t) \end{bmatrix} \quad (11)$$

where the historical items can be expressed as

$$\begin{bmatrix} \boldsymbol{x}_{\mathrm{his1}}(t) \\ \boldsymbol{x}_{\mathrm{his2}}(t) \end{bmatrix} = \boldsymbol{M}\begin{bmatrix} \boldsymbol{x}_1(t) \\ \boldsymbol{x}_2(t) \end{bmatrix} + \boldsymbol{N}\begin{bmatrix} \boldsymbol{u}_1(t) \\ \boldsymbol{u}_2(t) \end{bmatrix}. \quad (12)$$

Then, the port of the dc and ac-side for the VSC can be represented as companion equivalent circuits according to (13) and (14), which are connected with the outside ac and dc systems, as shown in Fig. 1

$$\begin{bmatrix} u_{\mathrm{C1}}(t+\Delta t) \\ u_{\mathrm{C2}}(t+\Delta t) \end{bmatrix} = \begin{bmatrix} \frac{\Delta t}{2C} & 0 \\ 0 & \frac{\Delta t}{2C} \end{bmatrix}\begin{bmatrix} i_{\mathrm{dc1}}(t+\Delta t) \\ i_{\mathrm{dc2}}(t+\Delta t) \end{bmatrix} + \begin{bmatrix} u_{\mathrm{his1}}(t) \\ u_{\mathrm{his2}}(t) \end{bmatrix} \quad (13)$$

$$\begin{bmatrix} i_{\mathrm{sa}}(t+\Delta t) \\ i_{\mathrm{sb}}(t+\Delta t) \\ i_{\mathrm{sc}}(t+\Delta t) \end{bmatrix} = \begin{bmatrix} \frac{\Delta t}{2L+\Delta tR_{\mathrm{on}}} & 0 & 0 \\ 0 & \frac{\Delta t}{2L+\Delta tR_{\mathrm{on}}} & 0 \\ 0 & 0 & \frac{\Delta t}{2L+\Delta tR_{\mathrm{on}}} \end{bmatrix} \times \begin{bmatrix} u_{\mathrm{sa}}(t+\Delta t) \\ u_{\mathrm{sb}}(t+\Delta t) \\ u_{\mathrm{sc}}(t+\Delta t) \end{bmatrix} + \begin{bmatrix} i_{\mathrm{his\_a}}(t) \\ i_{\mathrm{his\_b}}(t) \\ i_{\mathrm{his\_c}}(t) \end{bmatrix}. \quad (14)$$

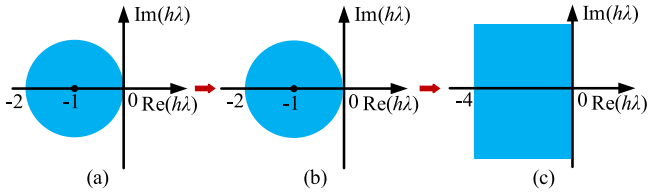

Fig. 2. Numerical stability regions of different methods. (a) One-step time-delay method. (b) Modified Euler method. (c) Proposed method.

The equivalent resistors of the derived companion circuit are fixed values and expressed as follows:

$$\begin{cases} R_{\text{eq\_L}} = \frac{2L+\Delta t R_{\text{on}}}{\Delta t} \\ R_{\text{eq\_C}} = \frac{\Delta t}{2C} \end{cases}. \tag{15}$$

Finally, the companion equivalent circuit of the VSC with a constant admittance matrix is derived. Furthermore, this model does not introduce time-delay and enables parallel simulation of circuits on both ac and dc sides of the converter.

D. Solution of Internal Electrical Variables of the VSC

Furthermore, the proposed method can also allow for the consideration of the internal characteristics of the converter. As an illustration, consider the upper bridge arm switch of phase-A in circuit Fig. 1. The voltage can be calculated using (16) after the solution of (13) and (14).

$$\begin{aligned} u_{\text{sw1}}(t+\Delta t) = {} & \frac{R_1}{R_{\text{sum}}}\left(u_{\text{C1}}(t+\Delta t) - u_{\text{C2}}(t+\Delta t)\right) \\ & - R_{\text{on}} i_{\text{sa}}(t+\Delta t). \end{aligned} \tag{16}$$

Similarly, the arm current can be calculated using the (17).

$$i_{\text{sw1}}(t+\Delta t) = \frac{R_4}{R_{\text{sum}}} i_{\text{sa}}(t+\Delta t). \tag{17}$$

Consequently, the PM not only preserves the port characteristics, but also reflects the internal electrical variables of the VSC.

E. Analysis of Numerical Stability

In order to demonstrate the advantages of the proposed method in terms of numerical stability, the numerical stability conditions, and numerical stability regions of different methods, including the traditional one-step time-delay method, the modified Euler method used in [29], and the PM are solved and presented as follows.

The numerical stability condition of the one-step time-delay method is presented in (18), with its numerical stability region is illustrated in Fig. 2(a)

$$\frac{x_{t+h}}{x_t} = |1 + h\lambda| < 1 \tag{18}$$

where λ is the characteristic root and h is simulation time-step.

In [29], the modified Euler method is used for simulation of the VSC, the numerical stability condition of the modified Euler method is presented in (19), while the numerical stability region is displayed in Fig. 2(b)

$$\frac{x_{t+h}}{x_t} = \left|1 + \frac{\lambda h}{2} + \frac{1}{2}\lambda h\,(1+\lambda h)\right| < 1. \tag{19}$$

The numerical stability condition of the proposed method is presented in (20) and its numerical stability region is illustrated in Fig. 2(c)

$$\frac{x_{t+h}}{x_t} = \left|\frac{1 + \frac{\lambda h}{2} + \frac{1}{2}\lambda h\,(1+\lambda h)}{1 - \frac{\lambda h}{2}}\right| < 1. \tag{20}$$

The numerical stability regions of different methods are illustrated in Fig. 2. As shown in Fig. 2, the numerical stability domains of both the traditional decoupling method based on one-step time-delay and the no time-delay decoupling method based on the modified Euler method proposed in [29] are all smaller than that of the method proposed in this article. In addition, since the proposed method considers the switch on-state resistance (denoted as R_{on}) during the derivation process, it can reflect the switch conduction loss. In contrast, the method in [29] directly uses a switch function model for switch modeling, ignoring the switch on-state resistance, and thus cannot account for conduction losses.

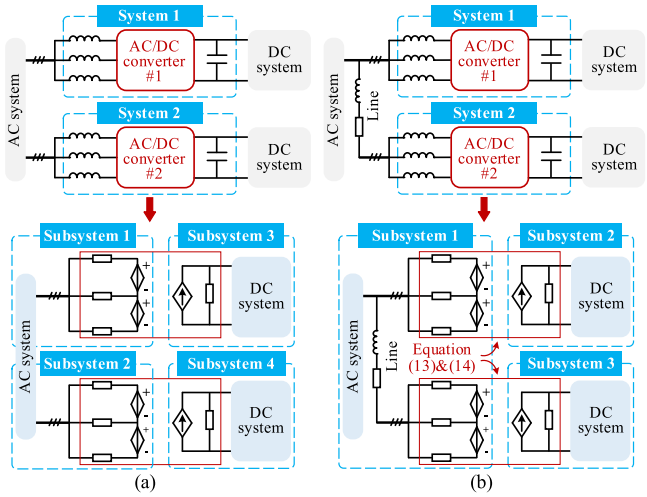

Fig. 3. Equivalent circuit of multiple grid-connected converter system. (a) Radial multiconverter system. (b) Trunk multiconverter system.

F. Application in Multiple Grid-Connected Converter System

The multiple grid-connected converter systems and the equivalent decoupling circuit of them are illustrated in Fig. 3(a) and (b), respectively.

Equations (13) and (14) indicate that the equivalent circuit of a single converter with both ac and dc sides decoupled can be obtained, as illustrated in Fig. 1. The decoupled converter ac and dc sides of the circuit can be solved in parallel using the node voltage method, while retaining the external ports, thus allowing access to any type of external circuits.

In the case of a multiple grid-connected converter system, it is essential to elucidate the way in which the method is to be applied in the given scenario, with particular attention paid to

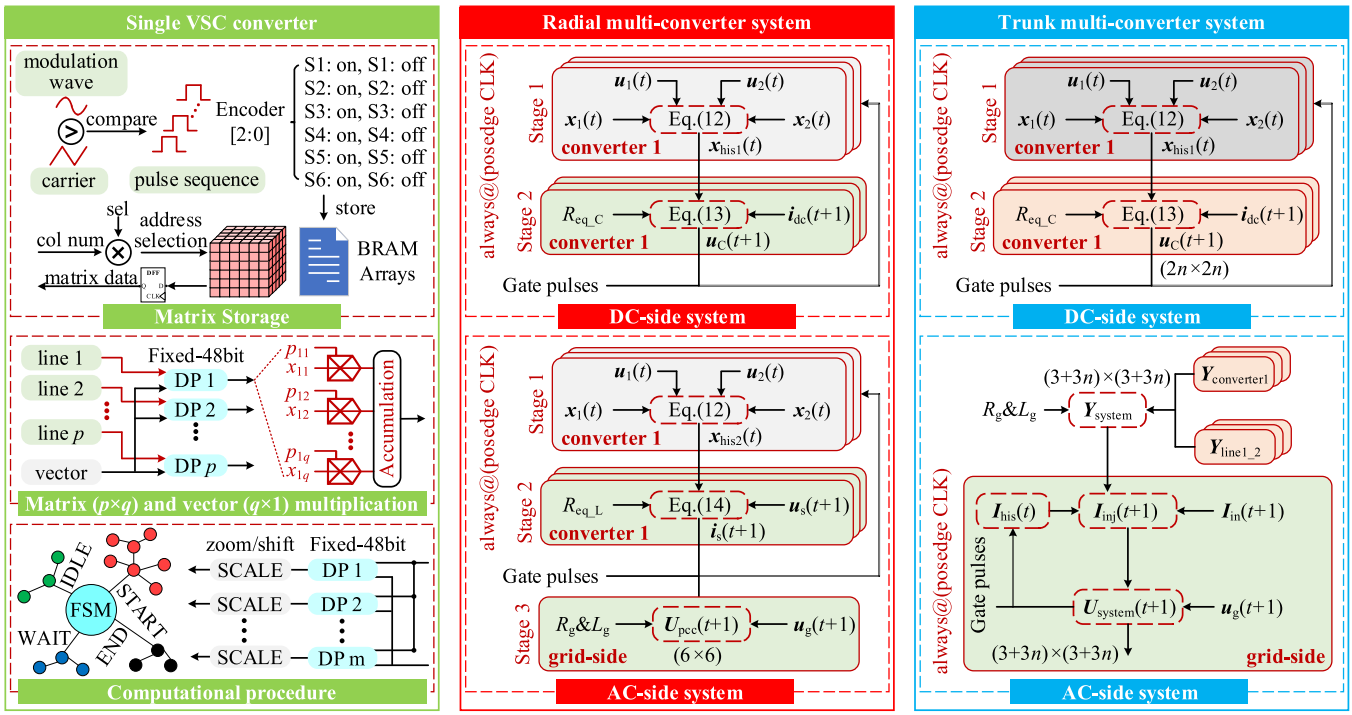

Fig. 4. FPGA-based solver engine design for multiconverter systems.

the connection mode of the ac/dc-side system. In the system depicted in Fig. 3(a), the dc-side between different converters is not interconnected, while the ac-side is collectively connected to the external ac system. For the system depicted in Fig. 3(b), there is a liaison line between different converters. According to the PM, the system depicted in Fig. 3(a) comprises two parallel converters that can be decoupled into four subsystems, whereas the system depicted in Fig. 3(b) can be decoupled into three subsystems. The several subsystems are all solved in parallel, as the number of converters increases, the computational burden of Fig. 3(a) does not increase for the ac-side subsystems, whereas Fig. 3(b) grows significantly with the increase in electrical node size.

Besides, the PM is also applicable for other types of power converters. The detailed analysis are as follows:

1) When dealing with other types of converter topologies, the state equation can be easily written due to the presence of capacitor on the dc-side and inductor on the ac-side. The differences between converters lie solely in their topology.
2) In the case of modular devices such as the PET, where the ac and dc-side ports are connected in series or parallel, the decoupling subsystems can be further addressed using the Thevenin or Norton equivalence theorem.
3) The proposed method relies on the presence of capacitors and inductors in the circuit but is unaffected by their placement on the ac- or dc-side of the circuit. However, most ac-dc converter topologies feature dc-side capacitors and ac-side inductors or dc-side capacitor and dc-side inductor, giving the proposed method considerable application potential.

III. FPGA-Based Hardware Implementation

This section mainly describes the implementation process of the PM on FPGA, including the design of the solver engine and the hardware implementation using the Verilog hardware description language, and the implementation of the PM is constructed on the Vivado 2023.2 platform.

A. Solver Engine Design

The objective of this section is to design a solution engine based on an FPGA and deploy the PM of VSC that has been derived. The solution engine is divided into three distinct parts, including a PWM switching signal generator, matrices calculation and storage in BRAM, and a dot product calculation pipeline array, as shown in Fig. 4.

In detail, the PWM switching signal generator is primarily responsible for generating the switching state of the IGBTs. In the FPGA, we utilize BRAM to store a sawtooth wave and a sine wave of one cycle. By encoding the current simulation time-step, the BRAM index address is calculated, enabling the generation of the waveform value comparison of the carrier and the three-phase electric generator after the PWM switching signal is encoded. Furthermore, the encoded PWM switching signal is employed to predict the memory address decoding generation of the correction matrix storage array. Upon the generation of the 3-bit switching signal, the memory access address will be automatically calculated according to the current simulation steps. From the storage array, the pipeline reads the matrix parameters required for this iteration. The finite state machine (FSM) controls the data flow of the three engine components and

accesses the matrix parameters to the dot product calculation pipeline array.

The FSM transitions from the initialization state to a waiting state upon loading the state vector data signal. In the waiting state, it begins reading the internal coefficient matrix and then transitions to the start state. Within the start state, multiply-accumulate operations are performed on the components of the selected state vector until all computations are completed, after which it transitions to the termination state. In the termination state, a buffer cycle is inserted to enhance the timing margin, and the computed result vector is pipelined for output. Finally, the FSM returns to the initialization state to repeat the process.

Besides, the PM enables the FSM to schedule the flow of the next switching signal generation to the matrix parameter reading in half-time-step of the dot product calculation over an extended period. This facilitates the formation of a closed-loop pipeline for the dot product array calculation, thereby reducing the calculation delay by half.

B. FPGA Implementation

In order to reduce the calculation time of the PM, fixed-point quantization is applied to the parameter matrix. The quantization bit is 56-bits, while the sinusoidal and sawtooth wave quantization bit is 30-bits. In order to reduce the demand on computing resources, all operations in the noncore solution operation utilize a fixed-point format with a width of 48-bits and an integer bit width of 24-bits. In the core dot product calculation, all fixed-point formats with a bit width of 64-bits and an integer bit width of 34-bits are calculated in order to achieve higher numerical accuracy and to reduce the loss of numerical calculation error in RTS process. Besides, the external physical controller has limited digital channels and cannot output multiple PWM signals simultaneously. Therefore, this article adopts a method where multiple converters on the same bridge arm reuse PWM signals. The PWM periodic signals are prestored in the FPGA RAM using an IP core.

The hardware description language Verilog is utilized for the programming of the register transfer level of the FPGA. The FSM is used to schedule the solver engine components in order to achieve small-step RTS iteration. In order to program and simulate in the FPGA, a test case is constructed on the PSCAD/EMTDC simulation platform for comparison and verification of the FPGA results. Finally, the entire design incorporates the 125-MHz DAC (digital to analog converter) component, which is programmed into the KU060 FPGA board using the AMD-Xilinx Vivado 2023.2 platform to complete the on-board deployment verification.

IV. Simulation Verification

A 10-kV grid-connected system containing three converters is built in the PSCAD/EMTDC simulation platform as a reference model (RM). All three converters adopt *P*/*Q* control strategy, which deliver 5, 4, and 10 MW active power to the grid side, respectively. The topology and control strategy flowchart of the test system are shown in Fig. 5, and the system parameters are presented in Table I.

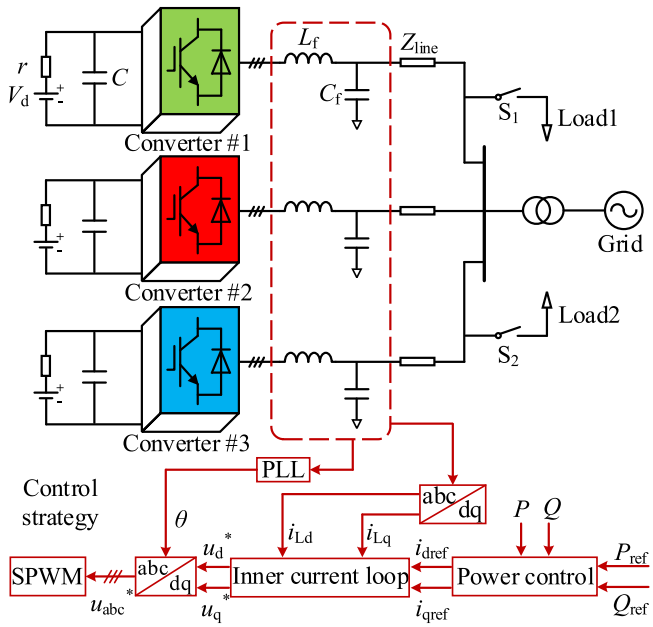

Fig. 5. Topology and control strategy of the test system.

TABLE I
Parameters of the Test System

Device	Quantity	Value
DC source	DC voltage V_d(kV)	25, 22, 50
	Resistance r(Ω)	1
	Operation frequency(kHz)	2
Converter #1	DC-side/AC-side capacitor C/C_f(μF)	2000, 30
	AC-side inductor L_f(H)	0.05
	Operation frequency(kHz)	1
Converter #2	DC-side/AC-side capacitor C/C_f(μF)	2000, 30
	AC-side inductor L_f(H)	0.01
	Operation frequency(kHz)	5
Converter #3	DC-side/AC-side capacitor C/C_f(μF)	2000, 80
	AC-side inductor L_f(H)	0.05
Short transmission line	Line inductance(H)	2e-4
	Line resistance(Ω)	1
Load	Impedance of load 1(Ω)	10+jω0.01
	Impedance of load 2(Ω)	15+jω0.01
Transformer	Short-circuit reactance/p.u.	0.1, 0.15
	Short-circuit resistance/p.u.	0.001, 0.001

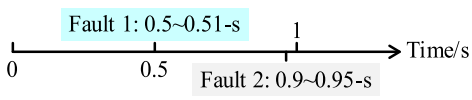

Fig. 6. Time setting of fault occurrence.

The simulation time-step is 10-μs and simulation time is set to 1.5 s. Two faults are set in the simulation process, as shown in Fig. 6. The simulation accuracy of the PM is verified and compared with the traditional one-step time-delay model (DM) and the RM.

A. AC-Side Short-Circuit Fault

At 0.5 s, the ac bus occurs an A-phase grounding fault, and the fault duration is 0.01 s. The simulation waveforms of the test system are shown in Fig. 7.

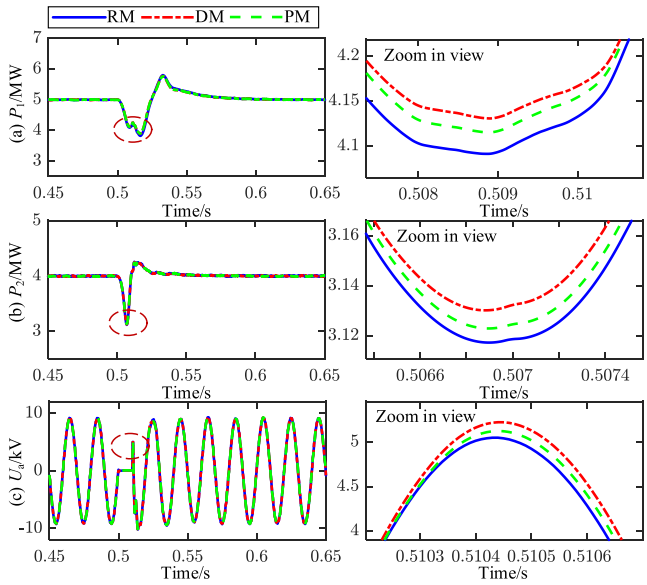

Fig. 7. Simulation results. (a) Active power of converter 1. (b) Active power of converter 2. (c) A-phase voltage of AC bus.

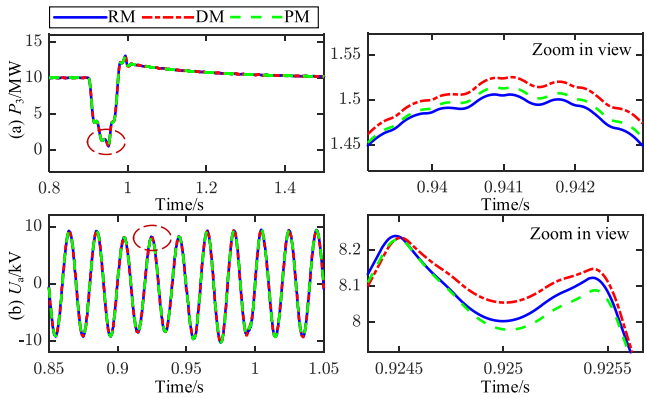

Fig. 8. Simulation results. (a) Active power of converter 3. (b) A-phase voltage of AC bus.

We can know from the above-mentioned simulation results that the active power of converters drops and restore after 0.05 s, the A-phase voltage of the ac bus drops to 0 and begins to recover at 0.51 s. The simulation waveforms of PM can fit that of RM well, and the local amplification waveform shows that its accuracy is higher than that of the DM.

B. DC-Side Short-Circuit Fault

At 0.9 s, the dc bus occurs a short-circuit fault of converter 3, and the fault is cleared after 0.05 s. The simulation waveforms of the test system are presented in Fig. 8.

Through the following Fig. 8, we can know that the active power of the converter 3 drops sharply during the short circuit of the dc-side, and the voltage amplitude of the A-phase at the ac bus decreases. The simulation waveforms of PM are closer to that of RM than that of DM, which proves that the PM has higher simulation accuracy.

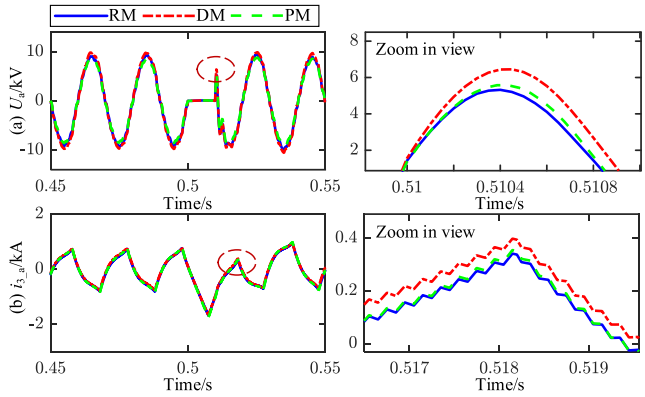

Fig. 9. Simulation results. (a) A-phase voltage of AC bus. (b) A-phase current of converter 3.

C. Large Time-Step Simulation

In order to further verify the simulation accuracy of the proposed method, a simulation test is carried out at a large time-step of 50-μs. The simulation working condition remained unchanged, and the simulation results are shown in Fig. 9.

The simulation results indicate that the simulation accuracy of the ac bus A-phase voltage of PM and the ac side A-phase current of converter 3 is superior to that of DM, as shown in Fig. 9. Furthermore, the maximum relative errors (MREs) of the simulation results of DM are greater than 10%, while those of PM are less than 4%. In the simulation scenario with a large time-step, the accuracy of PM is superior to that of DM.

D. Realistic Transmission Line Parameters

To further highlight the accuracy of the proposed method, we selected the output active power P_3 of converter 3 and the load power P_{load} as the test variables. The inductance of a short transmission line is 0.00195 H; the resistance of a short transmission line is 0.454 Ω. The parameter sources are from references [30].

As shown in Fig. 10, the simulation waveforms of PM are closer to those of RM than those of DM, which proves that the PM has higher simulation accuracy.

V. Experimental Verification

The effectiveness of PM is verified through a physical prototype, the RT-LAB simulator, and an FPGA-based real-time platform, as shown in Fig. 11.

A. Comparisons With Physical Prototype Platform

In this section, a physical prototype experimental platform is constructed to verify the effectiveness of the PM, as illustrated in Fig. 11(a).

The experimental platform adopts a rapid control prototyping controller, and the switching frequency of the converter is 5 kHz. For the converter, the V/F control strategy is used to control the voltage amplitude to be 20 V and the frequency of the load to be 50 Hz. The parameters of the test system are as follows: the

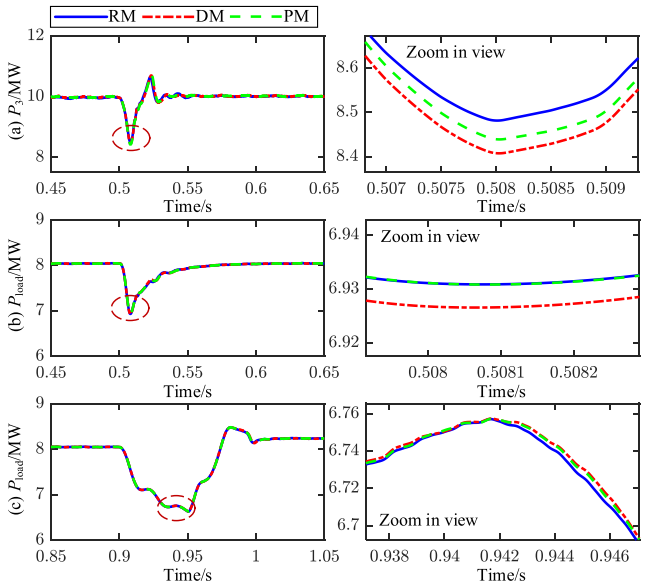

Fig. 10. Simulation results. (a) Active power of converter 3. (b) Active power of load. (c) Active power of load.

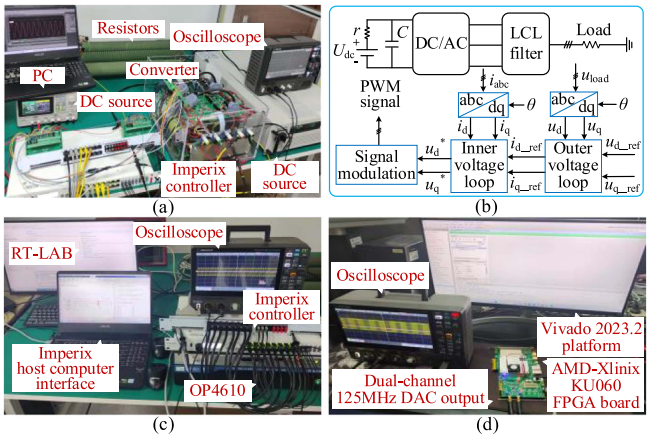

Fig. 11. Experimental platform. (a) Physical prototype platform. (b) Schematic diagram of the physical prototype. (c) RT-LAB HIL platform. (d) FPGA-based RTS platform.

voltage of the dc source is 100 V, the load resistor is 20 Ω, the dc-side capacitor C is $1360e^{-6}$ F, and the ac-side inductor is 0.005 H.

The reference value of the load voltage is changed from 20 to 10 V, the experimental and simulation results of A-phase load voltage are shown in Fig. 12.

Compared with Fig. 12(a), the simulation waveform in Fig. 12(b) is highly consistent with the experimental waveform, and the maximum error of the peak-to-peak value between them is 3.48% after calculation, which shows that the PM has high accuracy and is almost consistent with the actual converter operation results. The errors mainly come from the unavoidable hardware devices themselves.

The gate pulse of one switch in the upper arm is lost; the experimental and simulation results of A-phase load voltage are shown in Fig. 13. As shown in Fig. 13, the absence of a triggering

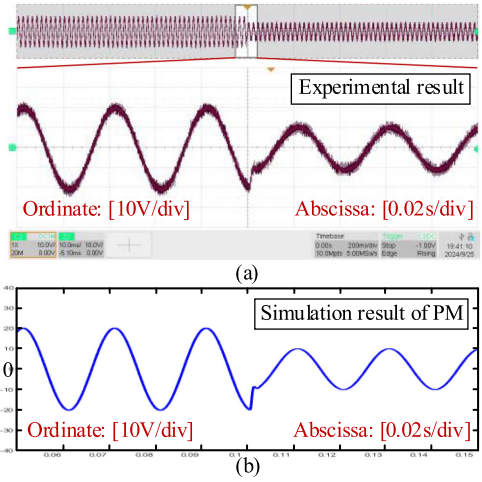

Fig. 12. Test results. (a) Experimental result of A-phase load voltage. (b) Simulation result of A-phase load voltage.

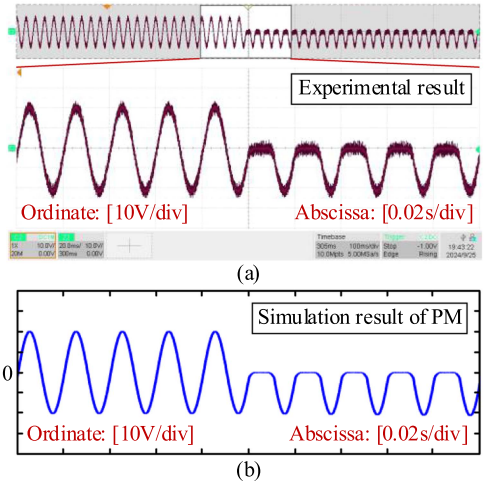

Fig. 13. Test results. (a) Experimental result of A-phase load voltage. (b) Simulation result of A-phase load voltage.

signal leads to the disappearance of the positive half-period of the A-phase load voltage waveform, and the simulation result is consistent with the experimental result.

B. FPGA-Based RTS Verification

In this section, we mainly verify the FPGA-based RTS performance of the PM and compare it with offline simulation results of the PSCAD/EMTDC.

1) Single Converter System: The test results using FPGA-based platform shown in Fig. 11(a) with 500 ns (50-clock cycles) of ac-side outlet current and dc-side voltage are presented in Fig. 14.

The performance for single converter system on XCKU060 FPGA is presented in Table II with different strategies.

As shown in Fig. 14, the MRE of the ac-side outlet current is 0.45% and the dc-side voltage is 0.6%, which manifests the high accuracy of the PM.

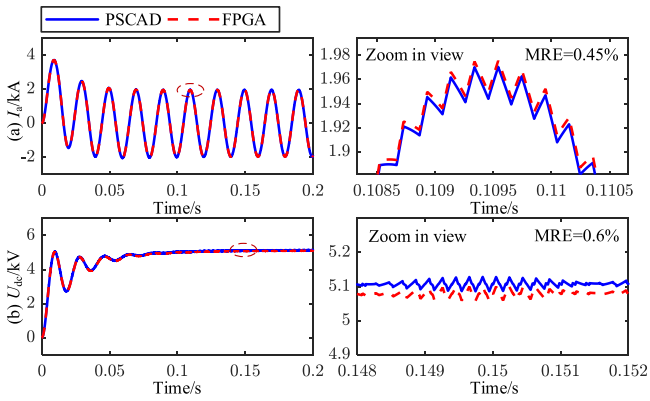

Fig. 14. Test results. (a) AC-side outlet current. (b) DC-side voltage.

TABLE II
PERFORMANCE OF THE SINGLE CONVERTER SYSTEM

Platform	Strategy	Frequency	LUTs	FFs	BRAMs	DSPs	Time-step
XCKU060	Tf	100 MHz	2593	2052	35.5	70	80 ns
	Rf	100 MHz	1316	1653	35.5	21	500 ns
	Tf	150 MHz	3005	3029	35.5	70	53 ns

Tf represents the time-step-first.
Rf represents the resource-first.

As illustrated in Table II, the experimental results for the single converter system on the XCKU060 FPGA, which is equipped with different strategies, including time-step first and resource first. The latency-first strategy typically exhibits lower time-step but higher resource consumption. For instance, strategy Tf on FPGA with 80-ns time-step demonstrates over 2×resource utilization in DSPs and LUTs compared to strategy Rf on FPGA with 500-ns time-step. Furthermore, enhancing clock frequency can further reduce time-step to 53 ns, but this will lead to higher hardware resource consumption.

2) Multiple Grid-Connected Converter System: The topologies of the multiple grid-connected converters system are shown in Fig. 15, which contains a radial multiconverter system and a trunk multiconverter system.

The parallel solution of a trunk multiconverter system is precluded by the presence of connecting lines between multiple converters, such as impedances R_{12} and L_{12}. Consequently, in contrast to the radial multiconverter system, the parallel solution of ac side systems is not feasible, resulting in a substantial increase in the computational burden.

Radial multiconverter system shown in Fig. 15(a): The percentage of hardware resources with different number of converters using a 500-ns RTS time-step is shown in Fig. 16. As the number of grid-connected converters increases, the utilization of FPGA hardware resources demonstrates a linear growth trend, with DSP resources representing the highest proportion, because DSPs are required to process a considerable number of matrix operations. At a converter count of 130, the proportion of DSP resources reaches 98.91%, indicating that a single board can simulate a grid-connected system comprising up to 130 converters with a 500-ns RTS time-step.

Besides, the percentage of hardware resources with different numbers of converters with a minimum 80-ns RTS time-step

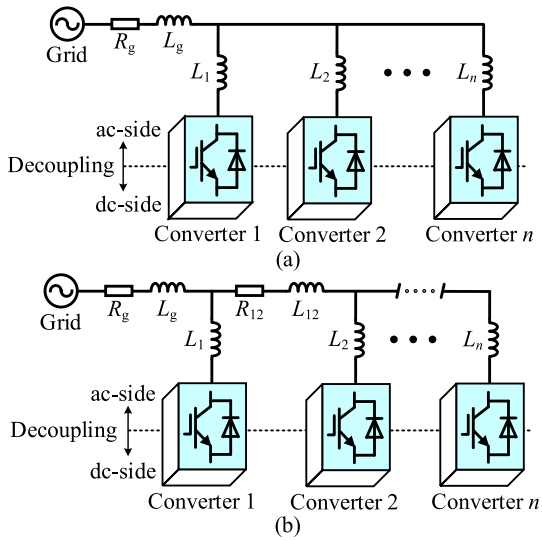

Fig. 15. Topology of multiconverter systems. (a) Radial multiconverter system. (b) Trunk multiconverter system.

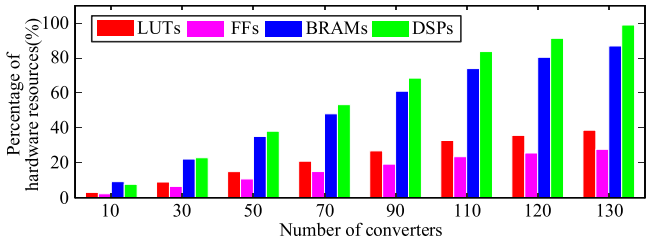

Fig. 16. Radial multiconverter system: percentage of hardware resources with various number of converters using 500 ns RTS time-step.

TABLE III
PERCENTAGE OF HARDWARE RESOURCE WITH 80 NS

Number	1	5	10	20	30	40
LUTs (331680)	0.78%	3.49%	6.89%	13.67%	20.47%	28.86%
FFs (663660)	0.31%	1.40%	2.77%	5.51%	8.24%	11.07%
BRAMs (1080)	3.29%	5.88%	9.12%	15.60%	22.08%	28.56%
DSPs (2760)	2.54%	12.68%	25.36%	50.72%	76.09%	100.00%

is shown in Table III for a radial multiconverter system. At a converter count of 40, the proportion of DSP resources reaches 100%, indicating that the single board can simulate a grid-connected system comprising up to 40 converters with an 80-ns RTS time-step. Obviously, a smaller time-step will result in an increase in the number of pipelines and therefore bring more resource consumption for FPGA simulation, so it is not feasible to achieve both small RTS time-step and low hardware resource consumption. The appropriate RTS time-step and advanced FPGA boards type should be selected according to the specific simulation requirements.

Trunk multiconverter system shown in Fig. 15(b): The percentage of hardware resources with different number of converters and RTS time-step is shown in Fig. 17.

TABLE IV
COMPARISONS OF FPGA SIMULATION SCALE AND TIME-STEP FOR MULTIPLE CONVERTER

Platform	Board	LUTs	FFs	BRAMs	DSPs	Radial multiconverter system	Trunk multiconverter system	Time-step(ns)
						–	11	500
FPGA	XCKU060	331680	663360	1080	2760	130	–	500
						40	–	80
RT-LAB	7K410T	406720	508400	795	1540	8	6	1000

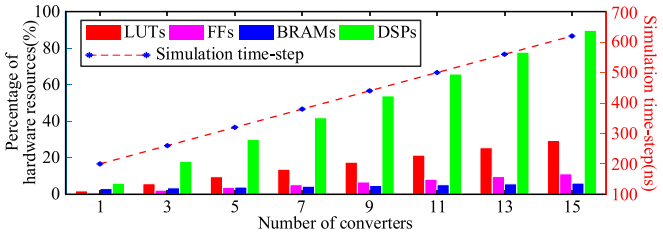

Fig. 17. Trunk multiconverter system: percentage of hardware resources with various number of converters and various RTS time-step.

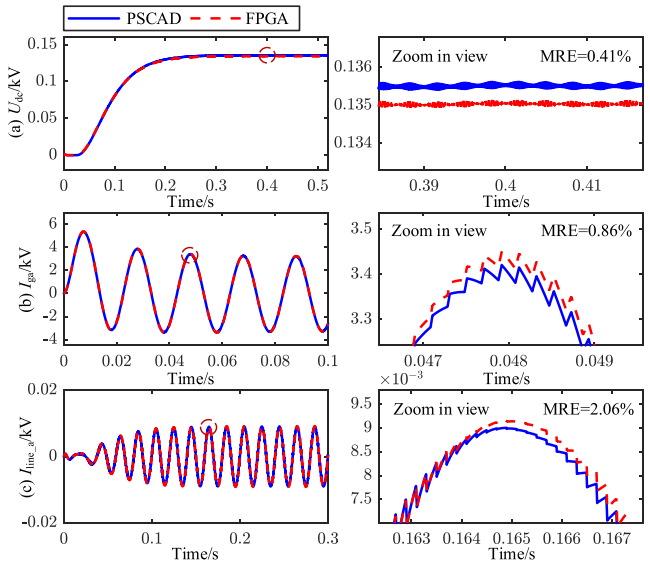

Fig. 18. Test results. (a) DC-side voltage of the #15 converter. (b) A-phase current of grid. (c) A-phase current of liaison line between #14 and #15 converter.

As the number of grid-connected converters increases, the utilization of FPGA hardware resources exhibits a linear growth trend, with DSP resources representing the highest proportion.

As the system scale of ac-side increases linearly, the RTS time-step also increases as equation $200+(N\text{-}1) \times 30$ ns in order to facilitate the scalable design, where N is the number of converters. At a converter count of 15, the proportion of DSPs resources reaches 89.78%, indicating that the single board can simulate a system comprising up to 15 converters with 620 ns RTS time-step, as shown in Fig. 17, and the board can simulate a system containing 11 converters with 500-ns RTS time-step.

The test results for trunk multiconverter system are shown in Fig. 18, which contains the dc-side voltage of the #15 converter $U_{\rm dc}$, the A-phase current of grid $I_{\rm ga}$, and the A-phase current of liaison line between #14 and #15 converter $I_{\rm line\_a}$.

TABLE V
COMPARISON WITH NODAL ANALYSIS METHOD

	Nodal analysis method		
Simulation scale [12]	DSPs	Time-step	System clock
8 three-phase lines, 2 converters	628	830 ns	
15 three-phase lines, 4 converters	1232	1430 ns	100 MHz
21 three-phase lines, 6 converters	1776	1970 ns	
Simulation scale	PM		
5 three-phase lines, 2 converters	333	230 ns	
11 three-phase lines, 4 converters	663	290 ns	100 MHz
17 three-phase lines, 6 converters	993	350 ns	

As shown in Fig. 18, the MRE of the $U_{\rm dc}$ is 0.41%, the $I_{\rm ga}$ is 0.86%, and the $I_{\rm line\_a}$ is 2.06%, which manifests the high accuracy of the PM.

3) Comparison of RTS Scale With RT-LAB: The simulation scale and time-step for radial and trunk multiconverter systems are compared with RT-LAB simulator, which are shown in Table IV. The PM displays certain advantages over RT-LAB in terms of both the scale of the simulation and time-step.

4) Comparison With Nodal Analysis Method: The DSP consumption and time-step of the nodal analysis method are analyzed as in Table V with a 100 MHz system clock. Compared with the trunk multi converter system, it has more DSP consumption, greater latency, and larger simulation scale. As the simulation scale increases, the time-step of the nodal analysis method rises rapidly. However, the PM grows slower in time-step and can simulate larger scale.

5) Comparison With Existing Representative Methods: Comparisons of FPGA resource utilization and time-step for a single converter are presented in Table VI. Compared with [37] and [38], the usage number of BRAMs is greater. However, the latency, LUTs, FFs, and BRAMs of the proposed are all lower than those of existing representative methods.

In addition, a summary of different methods is provided in Table VII. Several previous studies [18], [31], [34], [35], [36], [37], [38], [40] have reformulated circuits as differential algebraic equations (DAEs) through circuit equivalence analysis and algebraic integration transformations to reduce errors and improve the parallelism of individual circuits. However, these methods often introduce significant matrix overhead to derive DAE solvers, with limited consideration given to the intrinsic properties of the equations themselves or the hardware used.

For large-scale system, Yu et al. [14], Dufour et al. [20], Mirzahosseini and Iravani [32], and Milton et al. [33] perform global modeling by decomposing circuits and MVM reuse to alleviate computational overhead and latency issues, thus reducing the computational burden at each simulation time-step through

MVM iterations. However, reusing MVM introduces additional timing overheads. The RT-LAB commercial platform

TABLE VI
CONCLUSIONS OF FPGA RESOURCE UTILIZATION AND TIME-STEP FOR SINGLE CONVERTER

Benchmark	[31]	[31]	[32]	[34]	[36]	[41]	[37]	[38]	[38]	Proposed
Year	2018	2018	2019	2020	2022	2023	2024	2024	2024	2024
Platform	XC7K410T	XC7K410T	XC7VX485T	XC7K325T	XCKU060	XC7VX485T	XC7K325T	XC7K325T	XC7K410T	XCKU060
Frequency	–	–	175 MHz	–	142.8 MHz	–	50 MHz	100 MHz	–	100 MHz
LUTs	48 374	50 734	134 110	13 439	59 702	16 988	24 456	23 731	–	2593
FFs	51 874	53 350	129 734	11 699	79 603	16 024	15 896	15 753	–	2052
BRAMs	91.0	91.0	206.0	–	129.5	–	31.5	31.0	–	35.5
DSPs	157	211	325	337	1490	468	127	128	–	70
Time-step(ns)	463	475	800	100	455	100	500	500	500	80

TABLE VII
SUMMARY OF DIFFERENT METHODS

References	FPGA Platform	High Accuracy[1]	Small Time-step[2]	Scalable Application	Simulation Switches[3]
[13]	√	×	√	×	120
[14]	×	√	×	√	60
[20]	×	-	×	√	-
[31]	√	×	√	×	6
[32]	√	-	×	√	6
[33]	√	√	√	√	38
[34]	√	√	√	×	6
[35]	√	√	√	×	8
[36]	√	×	√	×	6
[37]	√	-	√	×	6
[38]	√	-	√	×	6
[39]	√	-	√	√	128
[40]	√	√	√	×	224
Proposed	√	√	√	√	780

[1] high accuracy represents related errors<1% of simulation.
[2] small time-step means that the simulation time-step≤500 ns.
[3] simulation switches represent the largest simulation size.

is limited by hardware resources; RTS can only perform 21 converters simulation at 500 ns time-step on each FPGA device, and can only operate up to 128 switches [39]. In contrast, the PM in this article can simulate up to 130 converters (780 switches). Besides, since the PM relies solely on the inductors and capacitors of the ac/dc-sides of the converter, it inherently features a scalable application. The ns-level RTS time-step used in this manuscript is for the circuit-solving part, where FPGA is utilized for small time-step simulation. For the physical controller system, a larger time-step of dozens of μs suffices.

VI. CONCLUSION

This article proposes a RTS model for multiple grid-connected converters system with constant admittance matrices, no interface time-delay decoupling, low hardware resource consumption, and small RTS time-step to address the challenges posed by increasing scale and operation frequency of PESs.

1) The simulation results demonstrate that the accuracy of the PM is superior to that of the one-step time-delay decoupling model. This advantage is more pronounced when the large time-step simulation is employed.
2) The FPGA-based simulation and physical phototype experimental results both demonstrate the high accuracy of the PM.
3) The FPGA-based RTS results indicate that the PM can achieve 500 ns (minimum up to 80 ns) RTS for a radial multiconverter system comprising 130 converters (780 switching devices) and 500-ns RTS in 50-clock cycles for a trunk multiconverter system comprising 11 converters (66 switching devices).
4) In comparison to the RT-LAB simulator, the nodal analysis method and existing methods, the PM exhibits certain advantages in terms of the simulation scale, hardware resource consumption and time-step.

The proposed method can be further applied to modeling and RTS of renewable energy stations, microgrids with multiple power converters, or distribution systems. Moreover, there is great potential to integrate physical controllers with the PM and deploy it on multiple FPGA boards for hardware-in-the-loop studies.

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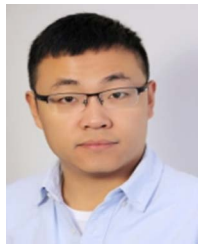

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