A Novel Single-Driver Series-Parallel IGBTs Solid State Circuit Breaker Component

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***Abstract*—Solid-state dc circuit breaker (SSCB) has become a key component for fast fault isolation in high-voltage dc systems. However, their effectiveness often relies on complex series and parallel connections of numerous switches. To address the low flexibility and redundancies problems inherent in conventional circuit breakers, this article proposes a single-drive series–parallel insulated gate bipolar transistors (IGBTs) all-solid-state dc circuit breaker component (SCBC). The innovative approach can precisely control multiple series and parallel IGBTs by using only one gate driver and a small number of passive components. In this novel configuration, a shutdown signal triggers the first-stage IGBTs. Once activated, the energy storage capacitor causes the subsequent IGBTs to shut down continuously. In SCBC, the main switches are connected in series and parallel, the breaking current capability is improved. In particular, the componentized design concept makes the topology is extensible and enhances the flexibility of SSCBs. Finally, the operating principle and design guidelines of SCBC are illustrated in detail through the creation of a mathematical model and topology, and their effectiveness is demonstrated through simulation and experimentation.**

***Index Terms*—IGBT, single drive, solid-state circuit breaker.**

I. Introduction

COMPARED with ac transmission system, dc transmission system has the advantages of low transmission loss and large power supply capacity [1], [2]. In addition, it has advantages in the fields of renewable energy [3], all-electric propulsion systems for ships [4], and energy storage [5]. The dc transmission system is characterized by low impedance and the absence of an over-zero crossing point, resulting in a rapid increase in current during short-circuit conditions [6], [7]. This phenomenon poses significant challenges to the efficacy of dc circuit breakers in safeguarding system integrity [8]. DC circuit breakers can be categorized into three types based on their operational principles: mechanical dc circuit breakers, hybrid dc circuit breakers, and all-solid-state dc circuit breakers (SSCB). Mechanical dc circuit breakers feature a straightforward design. However, they exhibit the longest interruption times, typically exceeding 10 ms [9]. Additionally, the inevitable arcing that occurs during operation leads to erosion of the switch, thereby diminishing both the reliability and operational efficiency of these breakers [10]. Hybrid dc circuit breakers combine mechanical switches with solid-state switches and other components arranged in parallel. While they offer improved performance, their opening speed is constrained by the mechanical switch, resulting in the opening time greater than 1 ms [11]. In contrast, all-solid-state dc circuit breakers effectively address these limitations. They utilize semiconductor devices to instantaneously interrupt short-circuit currents, while an energy-consuming branch absorbs the energy stored in the circuit [12]. This mechanism enables arc-free interruption [13], achieving breaking times less than 100 microseconds.

SSCB was first reported in the 1970s, including it is applied by NASA in 1973 in a 270 V dc aerospace power system [14]. Later, some scholars proposed to use fully controlled devices (IGBT, JFET, etc.) as the main switches of SSCB. However, current commercial fully controlled devices cannot withstand high operating voltage, switches in series is often required [15]. Existing switches series control usually equip a separate drive circuit for each level of power electronics devices. However, limited by the insulation capability of the circuit itself, designers need to electrically isolate the driver circuit from the main circuit to ensure stable operation of the control circuit. Kempkes et al. [16] proposed a design of six IGBTs with 4.5 kV withstand voltage in series. Each switch is controlled by a separate drive circuit to realize truncation at voltage and current of 10 kV/1000 A, respectively. Li et al. [17] used the same control method to design a 1 kV/2.9 kA SSCB prototype by virtue of the RB-IGCT.

The conventional driving method for circuit breakers presents several inherent limitations. As the voltage level escalates, the number of switches also need to increase, thereby imposing greater demands on both the capacity and quantity of isolation modules. The escalation results in a highly intricate circuit architecture, which is not conducive to a compact design and it is not conducive to expanding applications. Furthermore, the lack of synchronization among multiple gate signals poses a significant risk of circuit breaker malfunction and failure, thereby substantially diminishing the reliability of SSCB [18]. To mitigate these challenges, the implementation of a single driver circuit has emerged as a viable solution. In recent years, scholars have proposed a variety of design ideas for single-driver

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TABLE I
COMPARISON AND KEY PARAMETERS OF SINGLE-DRIVER SSCB

Ref	Voltage level	Breaking Current	expanding capability	Connection of switches
[19]	1.2 kV	4.5 A	No	Connected in series
[20]	6 kV	15 A		
[26]	3.3 kV	63 A		
[27]	3.5 kV	70 A	Yes	
This work	**5 kV**	**278 A**	**Yes**	**Connected in series and parallel**

circuit structures[19], [20], [21]. Wu et al. [22] proposed a single-drive structure with the aid of an external auxiliary power supply. It requires an equal number of isolation modules as the auxiliary power supply. This will increase the cost. Liu et al. [23] proposed a structure that uses a single gate driver to supply power to all switching gates. This places high demands on the power of the gate driver. Pang et al. [24] proposed a topology that implements a single drive function using an RC coupling structure. However, the first-level switch of this topology needs to withstand a higher level of voltage and is not suitable for SSCB. Through the continuous optimization of the single drive circuits, scholars also have successfully applied it to the field of SSCB and conducted characteristic analyses [25].

Wang et al. [26] proposed a method to control five series-connected JFETs using a single-driver unit. However, the current withstand capacity of this approach is insufficient for high-current interruption scenarios. Ren et al. [27] introduced an SiC MOSFET series topology wherein the driver unit activates the first stage module, with the remaining modules being driven by energy storage capacitors. Liang et al. [28] added a reverse diode between the gate and the emitter effectively inhibits charge sharing between metalized oxide varistors (MOVs) and the gate of the IGBTs, thereby aiding in the suppression of gate oscillation during the turn-OFF. Xie et al. [29] changed the position of the energy storage capacitors, and the consistency of the series switches at all levels was improved. Current research works on single driver circuits predominantly concentrate on control of series of switches and optimizing the single drive part. Although the level of voltage is enhanced, the upper limit of the breaking current is fixed and the flexibility is generally low. A comparative analysis of the work in this article against other topologies is presented in Table I. Where the bold values represent the performence parameters and structual advantages of this work.

In this article, a novel circuit breaker component (SCBC) is proposed. And the single driver part is optimized and analyzed in detail. It utilizes a single-stage driver with energy storage capacitors and shared resistors to achieve precise control of multiple series and parallel IGBTs. In addition, the SCBC is scalable and the number of SCBC applications can be selected according to the system parameters. This approach enables the SSCB to improve both voltage level and breaking current capability. After prototype testing, single-section SCBC can realize 2.5 kV reliable shutdown. The two-section series-connected SCBCs can achieve 5 kV/278 A reliable shutdown with a cut-OFF time of less than 1 μs. Making it provide better protection for applications such as dc microgrids with high fault current rise rates.

The rest of this article is organized as follows. Section II describes the working principle of the topology according to the topology details the state transition process and the passive component composition used in the circuit topology. Section III analyzes the effect of energy storage capacitor selection on the switching voltage equalization using simulation software. Section IV tests the prototype to demonstrate the feasibility and extensibility of the topology gives the experimental results of a successful breaking of 5 kV/278 A. Section V concludes this article.

II. COMPONENT TOPOLOGY AND OPERATING STATUS

A. Topology of SCBC

The topology can be conceptualized as a three-terminal component, with G serving as the drive input, C as the power input, and E functioning as both the drive and power output. This configuration comprises a power transmission branch and a drive branch. The electrical energy transmission branch is further categorized into a switching segment and an energy dissipation part. The topology of this design is shown in Fig. 1.

The switching segment is organized into four stages arranged in series and two stages arranged in parallel. Utilizing the same model of the primary switch, denoted as S_{nm}, where n represents the number of series stages ($n \geq 1$) and m signifies the number of parallel stages ($m \geq 1$). For the purposes of this study, the IGBT model IXYX50N170C from IXYX has been selected as the primary switch. The energy dissipation segment includes an *RC* buffer branch and a *MOV*. These serve to limit the overvoltage generated during the interruption of short-circuit current and facilitates dynamic voltage equalization within the main circuit. The drive branch primarily consists of energy storage capacitor C_n, static voltage equalizing resistor R_n, energy transfer diode D_n, transient voltage suppression diode D_{nm} (where $n \geq 2$), and gate resistor R_{nm}. Notably, only the first-stage switches necessitate a gate driver, while the gate drivers for the subsequent switches are substituted with passive components such as C_n. This design approach not only reduces development and application costs but also ensures uniform voltage distribution. The number of components utilized is contingent upon the level of the dc voltage source.

The storage capacitor C_n also referred to as the drive capacitor. They play a crucial role in the action of the main switches by releasing and absorbing charge to generate the necessary drive voltage. The static voltage equalizing resistor, R_n, facilitates static voltage equilibrium among the components during the stabilized shutdown phase of the main switches. Additionally, in conjunct with the transient voltage suppression diode, D_{nm}, it provides a pathway for leakage current. D_{nm} also offer the clamping voltage for stable conduction and stable shutdown of

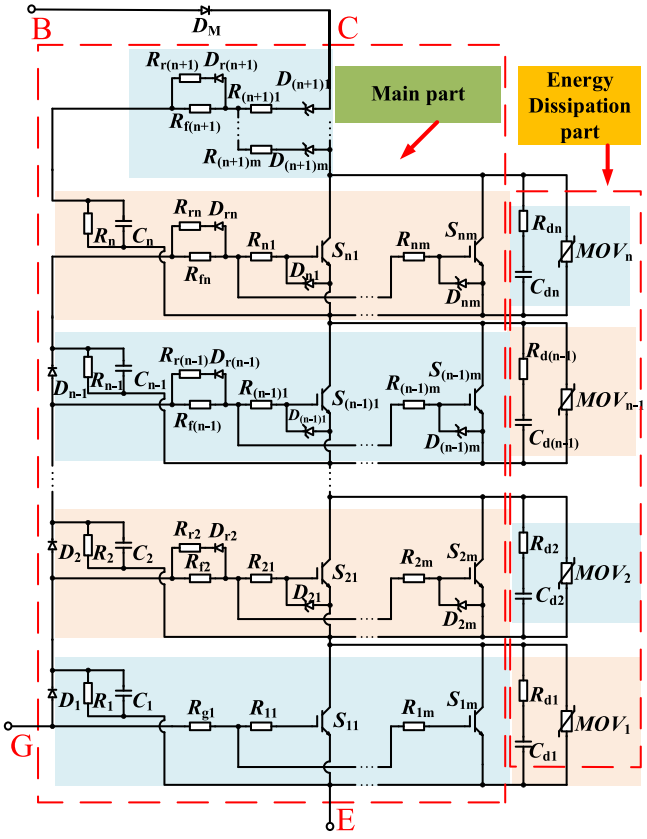

Fig. 1. Topology of SCBC.

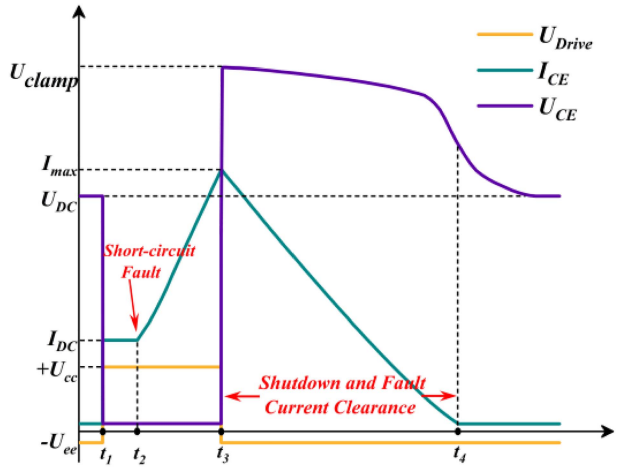

Fig. 2. Current and voltage waveforms during the fault interruption of the SCBC.

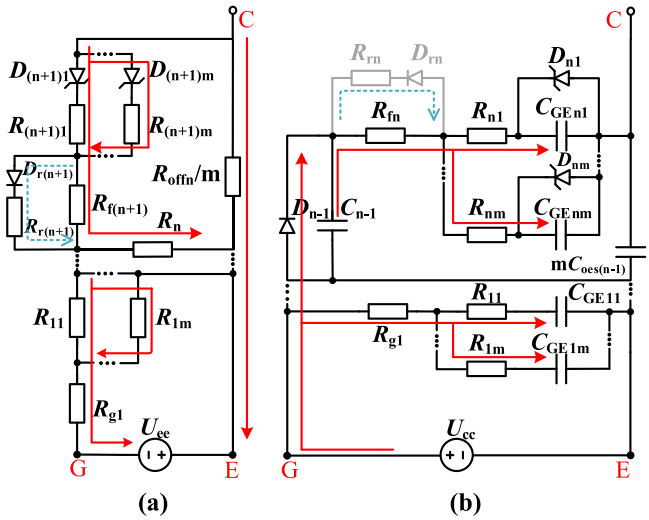

Fig. 3. Simplified circuit of single-driver series–parallel IGBTs element. (a) Stable shutdown state. (b) Conduction process.

S_{nm} ($n\geq 2$). The energy transfer diode, D_n, serves to provide the current path for the S_{nm} ($n\geq 2$) to guarantee the more reliable positive gate voltage. The gate resistor, R_{nm}, can offer the damping resistance for the drive branch, while $R_{\mathrm{g}1}$ and $R_{\mathrm{f}n}$ act as gate sharing resistors, collaborating with R_{nm} and reverse gate shared resistor $R_{\mathrm{r}n}$ to reduce the current equalization issues associated with the parallel switches configuration. It is important to note that, due to the inherent characteristics of the IGBT, current can flow in both directions. However, the SCBC is capable of interrupting the short-circuit current only when the current flows from the gate (G) terminal to the emitter (E) terminal. Corresponding current and voltage waveforms during the fault interruption of the SCBC are drawn as Fig. 2. Next, the analysis will go by the chronological order shown in Fig. 2.

B. Stable Shutdown State

Fig. 3(a) shows the equivalent circuit of a single-driver series–parallel IGBTs element in a stable shutdown state. The gate to emitter voltage $U_{\mathrm{GE}1m}$ of S_{1m} is directly controlled by the gate driver. And the forward conduction voltage drop U_{Tf}(nm) of D_{nm} ($n\geq 2$) made by the IGBT leakage current across the transient voltage suppression diode ensures the stable turn-OFF of S_{nm} ($n\geq 2$).

R_{off} denotes the equivalent turn-OFF resistance of the IGBTs, which can be expressed as follows:

$$R_{\mathrm{off}} = \frac{U_{\mathrm{CE}}(\mathrm{off})}{I_{\mathrm{CE}}(\mathrm{off})} \tag{1}$$

where the U_{CE} (off) of (1) represents the voltage between the collector and emitter when the nth stage IGBTs is stably turned OFF, and I_{CE} (off) represents the leakage current flowing through the collector at this time.

R_n's role is not only to provide a path for the leakage current, but also to realize the static equalization of all levels of switches in the OFF state. R_n's resistor should be much larger than the sum of the equivalent resistance of the other components of the branch road, and is much smaller than the $R_{\mathrm{off}n}/m$. In this case, the voltage distribution between the various stages of switches depends mainly on R_n under the stable shutdown state.

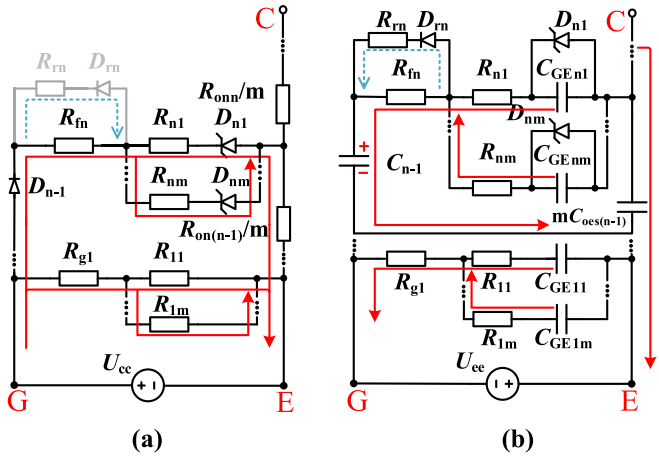

Fig. 4. Equivalent circuit of single-driver series–parallel IGBTs element. (a) Stable conduction status. (b) Shutdown process.

C. Conduction Process

Fig. 3(b) shows the simplified equivalent circuit of the conduction process of a single-driver series–parallel IGBTs component. At t_1, the voltage of the gate driver being changed from a low level $-U_{ee}$ to a high level $+U_{cc}$, the gate-emitter interelectrode capacitance C_{GE1m} of the 1st stage IGBTs are directly charged by the gate driver. Then, the simplified expression for the gate-emitter interelectrode voltage $U_{GE1m}(t)$ of the 1st stage IGBTs can be obtained,

$$U_{GE1m}(t) = U_{cc} - (U_{cc} + U_{ee})e^{-\frac{t}{(R_{1m}+mR_{g1})C_{GE1m}}}. \quad (2)$$

The voltage borne by S_{1m} decrease after they enter the active region. The gate emitter interpole capacitance C_{GE2m} of S_{2m} is charged by the drive current I_{D1} from the gate driver and the energy storage capacitance C_1. The fast discharge of energy storage capacitor can provide a signal for the switches to turn on. The above process is repeated to finally realize the conduction of each IGBT stage. After the conduction trigger delay time $\Delta t_{on\,n}$, the expression for the gate inter emitter voltage $U_{GE\,nm}(t)$ of the nth stage IGBT ($n\geq 2$) is as follows:

$$U_{GEnm}(t) = U_{C_{n-1}}(t) - U_{mC_{oes(n-1)}}(t) + \left(\frac{R_{nm}}{m} + R_{fn}\right)\left[C_{n-1}\frac{dU_{C_{n-1}}(t)}{dt} - I_{D_{n-1}}\right] \quad (3)$$

where $I_{D\,n\text{-}1}$ represents the drive current on the nth stage IGBTs emitted by the gate drive, and $U_{Cn\text{-}1}$ is the voltage when $C_{n\text{-}1}$ is discharged.

D. Stable Conduction State

Fig. 4(a) illustrates the equivalent circuit representing the stable conduction state of a single-driver series–parallel IGBTs element, which is not including *RC-MOV* branch. In particular, both fault detection and signal transmission require time after a short-circuit fault occurs. The main switches remain "ON" state throughout this process.

The gate-emitter voltage of S_{1m} is regulated directly by the gate driver. The reverse conduction voltage drop, denoted as $U_{Tr}(nm)$, across the transient voltage suppression diode is critical for maintaining stable conduction of $S_{nm}(n\geq 2)$. It is posited that during stable conduction of the SCBC, the forward conduction voltage drops across the energy transfer diode D_n are uniform U_D. And the conduction voltage drop for each IGBT stage is consistent U_{on}. Additionally, the equivalent turn-OFF resistances of the transient voltage suppression diode D_{nm} are assumed to be $R_T(\text{off})$. For $n\geq 2$, the following relationship holds:

$$U_{cc} = (n-1)U_D + mR_{fn}I_{Tr}(nm) + R_{nm}I_{Tr}(nm) + R_T(\text{off})I_{Tr}(nm) + (n-1)U_{on} \quad (4)$$

where $I_{Tr}(nm)$ is the current when the transient voltage suppression diode reverses conduction, and U_{cc} is the high level output of the gate driver.

According to (4), an expression for the minimum value of the inter-gate emitter voltage of the IGBTs at this time, U_{GEmin}, can be obtained

$$U_{GEmin} = \frac{U_{cc} - (n-1)(U_D + U_{on})}{mR_{fn} + R_n + R_T(\text{off})}R_T(\text{off}). \quad (5)$$

In order to keep the ON-state impedance of the IGBTs in the normal range, it is necessary to keep U_{GEmin} always larger or equal to the value of the inter-gate emitter voltage corresponding to the maximum on-state impedance of the IGBTs. This limits the value of the number n of IGBTs connected in series in the topology.

E. Shutdown and Fault Current Clearance Process

Fig. 4(b) shows the simplified equivalent circuit of the shutdown process of a single-driver series–parallel IGBTs element. At t_3, the voltage of the gate driver being changed from high level $+U_{cc}$ to low level $-U_{ee}$, the intergate emitter capacitance C_{GE1m} of S_{1m} is discharged directly to the gate driver. Then, the simplified expression for the intergate emitter voltage U_{GE1m}(t) of S_{1m} can be obtained

$$U_{GE1m}(t) = -U_{ee} + (U_{cc} + U_{ee})e^{-\frac{t}{(R_{1m}+mR_{g1})C_{GE1m}}}. \quad (6)$$

After a very brief delay, S_{1m} enters the active region, it shares more voltage in the main loop. Subsequently, the S_{2m} gate emitter interpole capacitance C_{GE2m} discharges to the energy storage capacitor C_1, constituting a negative gate voltage loop, so that S_{2m} receives a shutdown signal. Repeat the above process to finally realize the shutdown of each stage IGBT. Assuming that the sum of the nth stage device and channel voltage drops of each stage is $U_{mCoes(n\text{-}1)}$. According to the simplified circuit model of the turn-OFF process after the turn-OFF trigger delay time $\Delta t_{off\,n}$, the expression of the gate interemitter voltage $U_{GE\,nm}(t)$ of the nth stage IGBTs ($n\geq 2$) is as follows:

$$U_{GEnm}(t) = U_{C_{n-1}}(t) - U_{mC_{oes(n-1)}}(t) + \left(\frac{R_{nm}}{m} + \frac{R_{fn}R_{rn}}{R_{fn}+R_{rn}}\right)C_{n-1}\frac{dU_{C_{n-1}}(t)}{dt} \quad (7)$$

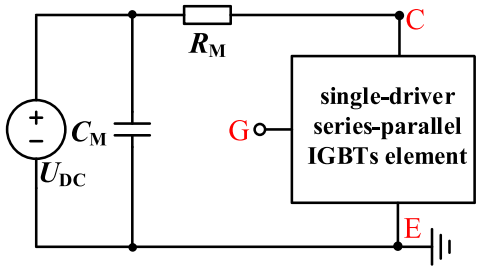

Fig. 5. Performance test connection diagram of single-driver series–parallel IGBTs element.

where $U_{Cn\text{-}1}$ is the voltage when $C_{n\text{-}1}$ is charged.

In order to obtain a good voltage equalization effect, the voltage between the gate emitters of each switch should be ensured to be the same as much as possible. From (7), if the $S_{(n\text{-}1)m}$ ON-state voltage drop is large, active voltage equalization can be achieved by increasing the values of R_{nm}, $R_{\mathrm{f}n}$, $C_{n\text{-}1}$, etc.

With S_{nm} entering the OFF state, the short-circuit current is transferred to the *RC* branch. Since the voltage of $C_{\mathrm{d}n}$ cannot be changed instantaneously. $R_{\mathrm{d}n}$ can be realized to suppress the inrush current. Ultimately, the dynamic uneven voltage caused by the different shutdown speeds of each IGBT can be reduced. When the *RC* branch voltage reaches the *MOV* action voltage, the *MOV* impedance changes from an open-circuit state to a high-conductivity state. The short-circuit current is commutated to the *MOV* branch so that the short-circuit energy is dissipated. Until the interruption is completely over, the voltage across the component is equal to the dc supply voltage.

F. Device Selection

The storage capacitance C_n plays a key role in the dynamic performance of single-drive series–parallel IGBTs element. It determines whether the 2nd to *n*th stage IGBTs can perform mutual switching between different states. The experimental test connection is showed in Fig. 5.

Assuming that the gate charge Q_g of the IGBTs at all levels from S_{2m} to S_{nm} ($n\geq 2$) are supplied by the energy storage capacitance, and considering that the gate resistor will consume charge. And thanks to the RC coupling structure selected by this topology, the values of all energy storage capacitors are the same. Sum of storage capacitance C_{total} can be obtained

$$C_{\mathrm{total}} > \frac{nmQ_g}{U_{\mathrm{CE}}(\mathrm{off})}. \tag{8}$$

Also, considering the main loop of the test where Fig. 5 is located, there is

$$U_{\mathrm{CE}}(\mathrm{off}) = \frac{R_{\mathrm{CE}}(\mathrm{off})}{R_{\mathrm{M}} + R_{\mathrm{CE}}(\mathrm{off})} U_{\mathrm{DC}}. \tag{9}$$

By bringing (8) into (9), we can obtain the following:

$$C_{\mathrm{total}} > \frac{nmQ_g}{U_{\mathrm{DC}}} \left(1 + \frac{R_M}{R_{\mathrm{CE}}(\mathrm{off})}\right). \tag{10}$$

From (10), if the resistance value of the load resistor R_M in the main loop becomes large, the value of the energy storage capacitor C_n must be increased properly in order to the designed topology to work stably.

The drive resistor not only provides damping for the gate circuit, but also has a significant impact on the switches voltage equalization as well as current equalization characteristics. This design adopts the gate shared resistor method [30]. For parallel IGBTs, in addition to a separate drive resistor for each IGBT, a common drive resistor is added on the common side. In the case of the first-stage IGBTs, the relationship driver resistors can be expressed as follows:

$$R_T = R_{\mathrm{g}1} + \frac{R_{1m}}{m} \tag{11}$$

$$\frac{R_{1m}}{m} = 0.1R_T \tag{12}$$

where R_T in (11) and (12) represents the selected drive resistor resistance value when there is only 1 IGBT.

Since the state switching from S_{2m} to S_{nm} relies on the energy storage capacitor, the transient current generated when the energy storage capacitor absorbs and releases charge is relatively large, especially during the release of charge. Therefore, for the selection of the driving resistor from S_{2m} to S_{nm}, the driving current must be limited. The maximum gate current must occur at the very beginning of the turn-OFF process and the conduction process. If the presence of stray inductance in the drive loop of the turn-OFF process is considered. In order to stay in the overdamped state, there is

$$R_{\mathrm{fr}n}(\min) + \frac{R_{nm}(\min)}{m} > 2\sqrt{\frac{L_{\mathrm{ss}}}{C_T}} \tag{13}$$

where $R_{\mathrm{fr}n}$ is the parallel value of $R_{\mathrm{f}n}$ and $R_{\mathrm{r}n}$, L_{ss} denotes the equivalent stray inductance of the drive loop. C_T is the parallel value of mC_{GE} and the equivalent stray capacitance of the drive loop.

The main reason for the uneven switch static voltage divider is the different equivalent turn-OFF resistances of each parallel IGBT. This situation can be improved by choosing the static voltage equalizing resistor R_n appropriately. Setting the most extreme case, S_{1m} has no leakage current, S_{2m} to S_{nm} flows the maximum leakage current I_{CEmax} (off). The voltage difference between the various levels of IGBTs does not exceed 10%. Then, there is

$$R_n \leq \frac{U_{\mathrm{CE(off)}}}{10mI_{\mathrm{CEmax}}(\mathrm{off})}. \tag{14}$$

However, R_n must not be too small to avoid too much leakage current flowing through the component. Approximating that the leakage current flows only through R_n. Consider the main loop where Fig. 5 is located, there is

$$R_n \geq \frac{U_{\mathrm{DC}} - R_M I_{\mathrm{CEmax}}(\mathrm{off})}{nI_{\mathrm{CEmax}}(\mathrm{off})}. \tag{15}$$

When the SSCB forcibly breaks the short-circuit current, the energy stored in the loop inductor generates a huge overvoltage on the power semiconductor device[6]. This has a huge impact on the reliability of the SSCB and may even lead to its permanent failure.

In this design, a two-stages *RC-MOV* buffer branch is chosen to guarantee reliable switch operation. When the switch starts to turn OFF, the main current is preferentially switched to the *RC* buffer branch. The rate of current rise will be decreased, there are two advantages to this. Reducing the dynamic voltage unevenness caused by the different turn-OFF times of each IGBT and the *MOV* voltage spike caused by the steep front effect. The buffer resistors suppress oscillations and inrush currents. If the voltage difference between the various switching stages does not exceed 10% of the rated intercollector voltage U_{CES} of the IGBT and the total current is I_0 and its maximum value is $I_{\max}$. the buffer capacitor C_d can be taken in the range

$$C_d \geq \frac{5I_{\max}\Delta t}{U_{\mathrm{CES}}} \tag{16}$$

where Δt is the time at which the nth stage IGBTs reach the Miller platform earlier than the $(n+1)$st stage IGBTs.

After the circuit breaker changes from the OFF state to the ON state, if it is required that the OFF operation can be performed again after t_r. The charge in C_{dn} must be released through the buffer resistor R_{dn} during the t_r time. This facilitates the reclosing operation. Thus, the value range of buffer resistance R_d is obtained

$$R_d \leq \frac{t_r}{2C_d}. \tag{17}$$

The *MOV* works on the principle that the resistance is inversely proportional to the applied voltage. When the voltage across the buffer branch reaches the operating voltage of the *MOV*, the current is switched from the buffer branch to the energy branch. The system energy is dissipated by the *MOV* in the form of heat and the fault current begins to drop. Therefore, after determining the number of switches, the energy required to be dissipated by the *MOV* is calculated for each level of switches so that the appropriate *MOV* can be selected. Assuming that the system voltage is U_1, the total inductance of the line is L_{M}, the maximum limiting voltage of the *MOV* is U_{MOV}. I_1 is the peak short-circuit current, the system residual energy *W* that needs to be absorbed by the *n MOV*s is

$$W = \frac{nU_{\mathrm{MOV}}L_M I_1^2}{2(nU_{\mathrm{MOV}} - U_1)}. \tag{18}$$

So, when selecting *MOV*, the maximum absorbed energy of *n* identical *MOV*s should be greater than *W*. When designing the circuit layout, the *MOV* and the main switches branch should be maximally compact. This can reduce the voltage spikes caused by the parasitic inductance of the branch and make the SCBC more stable.

III. Component Topology Simulation of Single-Driver Series–Parallel IGBTs Element

In order to verify the effectiveness of the single-driver series–parallel IGBTs element and test the effect of the energy storage capacitor on the switching voltage distribution situation. In this article, the simulation circuit is built in PSpice for testing, and the parameters are shown in Table II.

TABLE II
Components of the SSCB in Simulation

Descriptions	Value
Main DC Power Supply, U_{DC}	3 kV
IXYX50N170C of IXYX, S_{nm}	1.7 kV,178 A
Voltage regulating capacitor, C_M	20 μF
Load resistance, R_M	10/1000 Ω
Energy storage capacitance, C_n	1/100 nF
Static equalizing resistor, R_n	68 kΩ
Gate shared resistance of $S_{1\mathrm{m}}$, $R_{1\mathrm{g}}$	15 Ω
Forward shared resistance S_{nm}(n≥2), R_{fn}	120 Ω
Reverse shared resistance S_{nm}(n≥2), R_{rn}	30 Ω
Gate drive resistance of S_{1m}, R_{1m}	2 Ω
Gate drive resistance of S_{nm}(n≥2), R_{nm}	15 Ω
Pulse-width, pw	10/20/30/50 μs

Test loop is equal to Fig. 5. The single-driver series–parallel IGBTs element under different resistive loads and different single pulse width conditions are separately tested for switches voltage dividing in the simulation. Since the series switches in the SCBC is consecutively conducting, the voltage distribution between S_{nm} ($n \geq 2$) is more important. Therefore, $\mathrm{V_{s4-s1}}$, $\mathrm{V_{s4-s2}}$, $\mathrm{V_{s4-s3}}$, and $\mathrm{V_{s4}}$ are selected for measurement.

A. Energy Storage Capacitor Selection Test With Different Value of Resistive Load

In order to verify the influence of energy storage capacitors on switches voltage division characteristics. The single-driver series–parallel IGBTs element is tested under the conditions of supply voltage 3 kV, single pulse width pw = 20 μs, and energy storage capacitor $C_n = 1$ and 100 nF. The load is 10 and 1000 Ω resistors. The simulated waveforms of switching voltage distribution under different resistance values are obtained. σ indicates the ratio of imbalance for IGBTs' voltage after all switches are turned OFF

$$\sigma = \frac{U_{\max}(\mathrm{t}) - U_{\min}(\mathrm{t})}{\bar{U}(\mathrm{t})}. \tag{19}$$

From Fig. 6(a) and (b), it can be known that the voltage balance effect of all levels of IGBTs is excellent and σ is less than 2.6% when $R_M = 10$ Ω. But when $R_M = 1000$ Ω, all levels of IGBTs are obviously not voltage equalized, $\sigma_{\max}$ rising to 39.3%. Accordingly, it can be concluded that the selection of the energy storage capacitor has a great impact on the component performance. The switches in series sequence in the topology are turned on in sequence, so voltage equalization is very important for single-driver SSCB. According to (10), the energy storage capacitor needs to be selected with a larger capacitance value.

Keeping the other settings unchanged, the energy storage capacitor is changed to 100 nF. According to Fig. 6(c) and (d), σ is less than 4% when $R_M = 10$ Ω and $R_M = 1000$ Ω. It is proved that when the load resistance becomes larger, the value

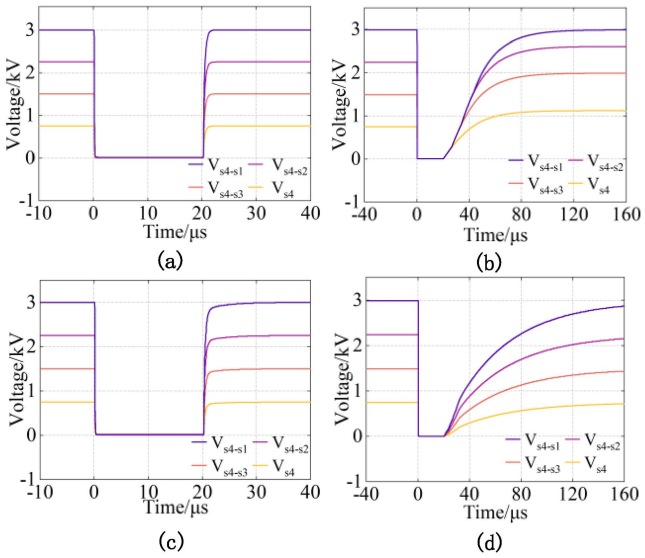

Fig. 6. Voltage distribution between switches (a) $C_n = 1$ nF, $R_{\mathrm{M}} = 10\ \Omega$. (b) $C_n = 1$ nF, $R_M = 1000\ \Omega$. (c) $C_n = 100$ nF, $R_M = 10\ \Omega$. (d) $C_n = 100$ nF, $R_M = 1000\ \Omega$.

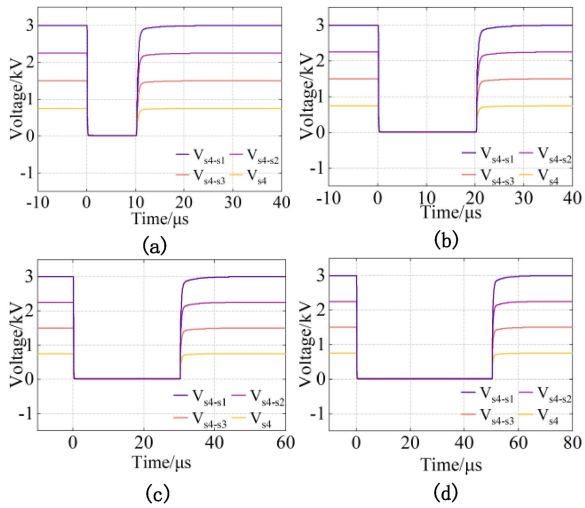

Fig. 7. Voltage distribution between switches with different single pulsewidths in simulation. (a) pw $= 10\ \mu$s. (b) pw $= 20\ \mu$s. (c) pw $= 30\ \mu$s. (d) pw $= 50\ \mu$s.

of the energy storage capacitor C_n must be increased to ensure the consistency and reliability of all levels of switches.

B. Voltage Balance Test With Different Single Pulsewidths

The influence of different signal pulse width on the voltage balance effect of the switches is also tested. Keeping the power supply voltage, storage capacitance is 100 nF. And load value is 10 Ω. And setting the pulsewidths to 10, 20, 30, and 50 μs. Respectively, the resulting simulation curves are shown in Fig. 7(a)–(d), which show that the driver circuit of the present design is not sensitive to the signal pulse width. Due to the overdamping effect of the driver resistor and the capacitive characteristics of the buffer branch, the values of σ the four pulse widths are very close and less than 5%. Therefore, the proposed

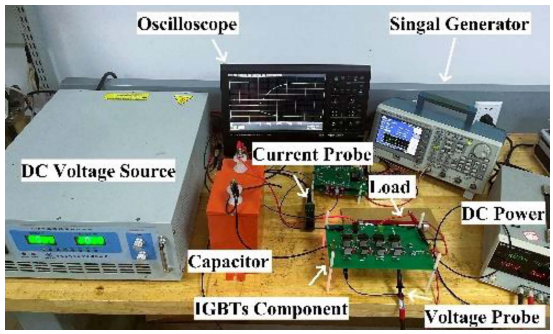

Fig. 8. Physical test bench for single-driver series–parallel IGBTs element.

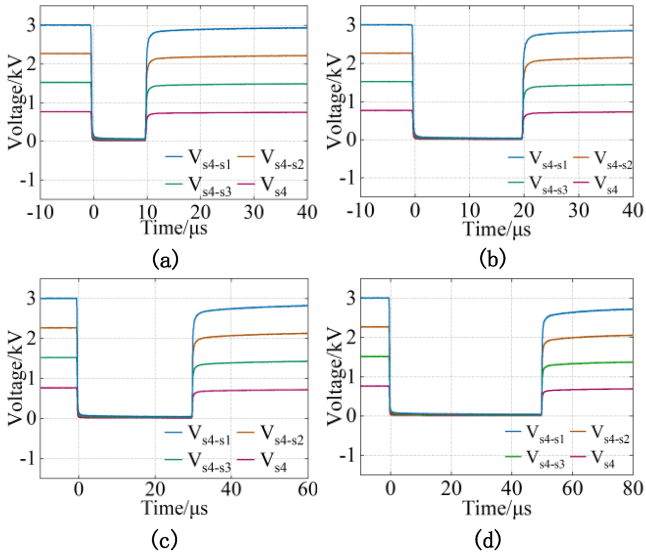

Fig. 9. Voltage distribution between switches with different single pulse widths in experiment. (a) pw $= 10\ \mu$s. (b) pw $= 20\ \mu$s. (c) pw $= 30\ \mu$s. (d) pw $= 50\ \mu$s.

circuit analysis model can realize good switching voltage divider performance.

IV. Experimental Results

IV. A. Single-Driver Series–Parallel IGBTs Element Test

In order to validate the effectiveness of the single-driver series–parallel IGBTs element, a prototype of the element was built, and the element building was accomplished using a double-sided printed circuit board. The parameters of the element are equal to Table II and C_n is 100 nF. A voltage probe model T3100B (100 MHz) and a Roche coil CWT MiniHF6B (23 MHz) were selected to conduct a comprehensive test of switching voltage and current. The oscilloscope is TELEDYNE LECROY HDO 6054. The experimental test rig is shown in Fig. 8.

The experimental waveforms of the voltage of $V_{s4\text{–}s1}$, $V_{s4\text{–}s2}$, $V_{s4\text{–}s3}$, and V_{s4} are shown in Fig. 9. Under the load resistance $R_{\mathrm{M}} = 10\ \Omega$ and signal pulsewidth pw $= 10$, 20, 30, and 50 μs. The σ between each series IGBTs are not more than 6%.

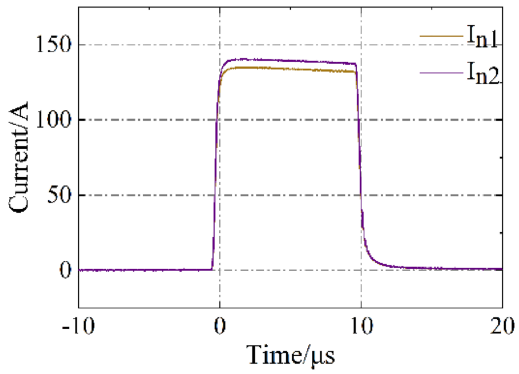

Fig. 10. Current distribution when pw = 10 μs.

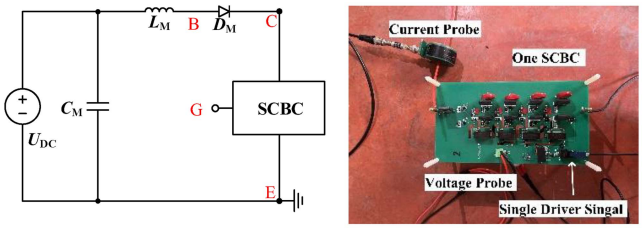

Fig. 11. (a) Experimental platform connection diagram. (b) Physical platform drawing.

TABLE III
BUFFER BRANCH PARAMETERS

Descriptions	Value
Energy storage capacitance, C_n	100 nF
Buffer capacitance, C_{dn}	68 nF
Buffer resistance, R_{dn}	2 Ω
Metal oxide rheostat, MOV	TMOV20RP550E

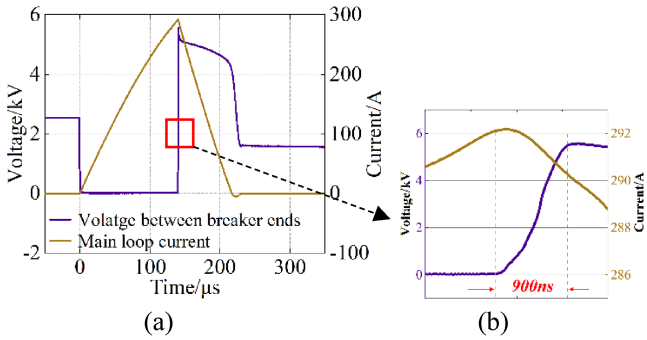

Fig. 12. (a) One SCBC experimental waveforms for 2.5 kV. (b) Magnification angle.

The active and passive voltage equalization devices play a key role.

In the same case, the experimental waveforms of the current flowing through the two parallel IGBTs are shown in Fig. 10. According to (20), $\delta_{\max}$ is 5.7%. Since the quality is worst when the signal width is 10 μs, hence only measured the current distribution with a signal width of 10 μs

$$\delta = \frac{I_{\max}(t) - I_{\min}(t)}{\bar{I}(t)}. \tag{20}$$

The experimental results show the single-driver series–parallel IGBTs element can work stably under loads with different resistance values and pulse widths, and no obvious voltage unevenness and current unevenness are observed.

B. Experimental Testing of SCBC

A single-drive series–parallel IGBTs element is combined with an energy-consuming branch to form a SCBC. First, an actual SCBC is tested. Fig. 11(a) shows the connection diagram of the experimental platform. The long distance line inductance in the system of modern dc transmission systems' usually reaches the millihenry level [31]. And the rising rate of the actual dc short-circuit current is several amperes per microsecond or more [32]. The inductance of the line and the rise rate of the short-circuit current approximately follow the following relationship:

$$L_{\text{eq}} \approx \frac{U_{\text{DC}}}{\mathrm{d}I_{\text{f}}(0)/\mathrm{d}t} \tag{21}$$

where $\mathrm{d}I_f(0)/\mathrm{d}t$ is the fault current rise rate at the initial moment of a short circuit.

In order to better simulate the fault environment, relevant tests of SCBC were conducted under the condition of $L_M = 1$ mH, and the experimental platform is shown in Fig. 11(b).

The buffer capacitance C_{dn} and other added parameters are shown in Table III. From Fig. 12(a), the SCBC achieves reliable interruption of 292 A short-circuit current at the overvoltage of 5.56 kV. Therefore, the rated breaking current of the circuit breaker can be increased by using the proposed design method. Fig. 12(b) shows a magnified view of the shutdown transition process. The cut-off time is the time from when the SSCB receives the trigger signal to it reaches the peak voltage. From Fig. 12(b), the short-circuit up to 292 A can be cut by one SCBC within 1 μs.

The experimental waveforms of the voltages of V_{s4-s1}, V_{s4-s2}, V_{s4-s3}, and V_{s4} are shown in Fig. 13(a). The switching voltage value during *MOV* operation is large. In this case, σ is not more than 7.5%, indicating that the voltage distribution between devices is approximately uniform. The voltage oscillation after the interruption is very small, which can further improve the reliability and stability of the SCBC. Fig. 13(c) shows a magnified view of the switches ON and OFF state transitions. The switches act in sequence and no obvious voltage imbalance is found during the state transitions. Since it is not possible to measure the collector voltages of the switches directly with a high-voltage probe. To observe the collector voltage of each switch can only by way of voltage subtraction in Fig. 13(a), and the results are shown in Fig. 14. The ON-time delays of the switches are nearly the same at all levels, about 150 ns, which is perfectly acceptable with respect to the overall turn-ON time.

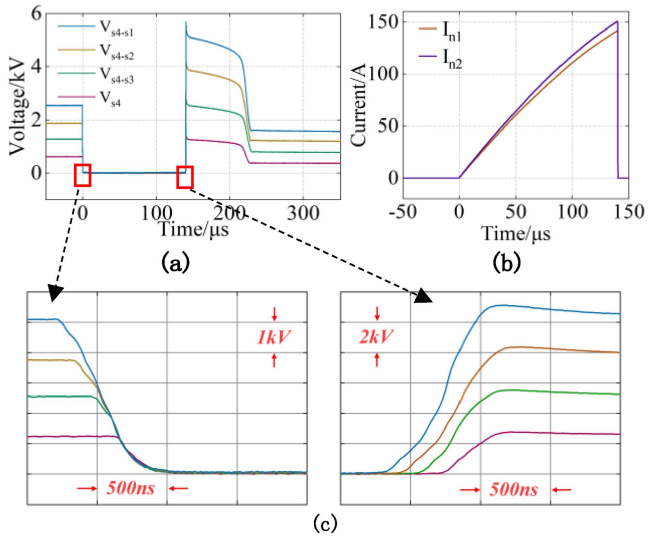

Fig. 13. (a) Voltage distribution between switches of one SCBC. (b) Current curve of S_{n1} and S_{n2}. (c) Voltage magnification diagram of conduction process and shutdown process.

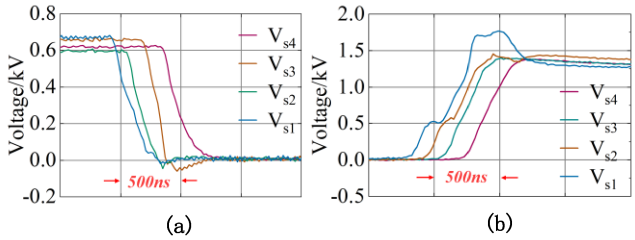

Fig. 14. (a) V_{CE} for every single switch's conduction. (b) V_{CE} for every single switch's shut down.

Fig. 13(b) demonstrates the current flowing through both IGBTs during SCBC shutdown with $\delta_{\max}$ of about 6.7%. The above conclusions show that all levels of switches have good voltage balance rate and current balance rate during the opening process. And the ON-state delay is basically the same, the SCBC guarantee excellent action consistency. As a consequence, single-section SCBC shutdown experiments demonstrate the feasibility of the proposed single-driver control mechanism and its ability to increase the breaking current.

Since the design is componentized, the component design can be carried out according to the device selection method proposed in this paper in combination with the actual requirements. In order to verify the scalability of the components, Fig. 15 shows the test diagram of a 5 kV SSCB, which consists of two single-driver dc circuit breaker components connected in series.

With a system voltage of 5 kV and a total equivalent inductance of $L_M = 1$ mH. The 5 kV SCBCs break a short-circuit current of 278 A, with a peak transient overvoltage of 11.07 kV, which is below the system withstand limit. Its experimental waveform is shown in Fig. 16(a).

The experimental waveform of switching voltage distribution is shown in Fig. 17. After calculation, σ does not exceed 10%

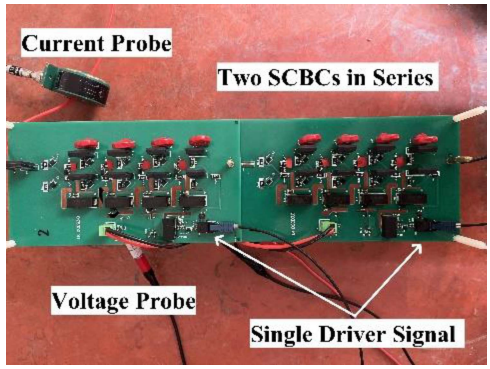

Fig. 15. 5 kV single-driver DC circuit breaker test.

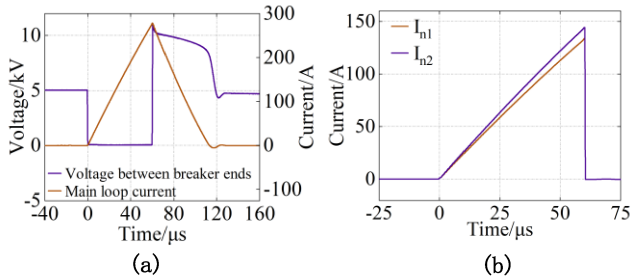

Fig. 16. (a) SCBC experimental waveforms for 5 kV. (b) Current curve of S_{n1} and S_{n2}.

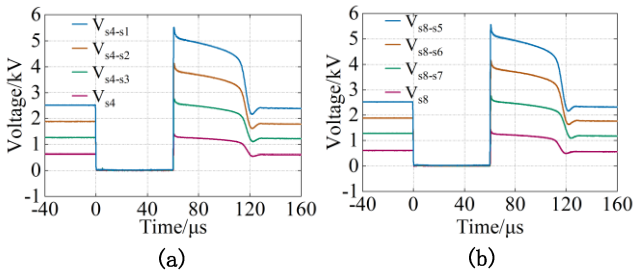

Fig. 17. Voltage distribution between switches of two SCBCs. (a) First component. (b) Second component.

during *MOV* clamping. During the breaking process, the maximum voltage of each switch does not exceed the limit voltage. Fig. 16(b) shows the IGBT current distribution in parallel during SCBC operation, where the $\delta_{\max}$ is 7.4%.

The experimental findings indicate that two 2.5 kV SCBCs in series are capable of reliably performing short-circuit shutdown operations in 5 kV dc power systems. This demonstrate the expandability of SCBC and the stability of the driver and main circuits after expansion. It is important to highlight that as the number of components increases, both the voltage unbalance rate and the current unbalance rate tend to rise during the transition states of switching. This phenomenon can be attributed to the uncontrollable parasitic parameters of the power devices, which contribute to increased uncertainty as the number of devices escalates. Nevertheless, the measured results presented in this study reveal that the deviation remains below 10%.

V. Conclusion

DC circuit breakers, crucial for fault isolation in dc systems, have become a hot research topic in the field of high-voltage appliances. The driving circuits of power electronic devices used in all-solid-state dc circuit breakers need further optimization. This article designs a new single-drive series parallel IGBTs SCBC. The main conclusions are as follows:

1) The design adopts single-driver unit to control series and parallel IGBTs at the same time. With the number of stages in parallel increasing, the breaking current capability can be improved. This also mean that the SCBC has greater capacity.
2) The single-drive mechanism reduces the structural redundancy issue of traditional drive systems, reducing the complexity of the circuit breaker. It greatly improves the compactness and reliability of SSCB.
3) By establishing a mathematical model and analyzing the topological structure, the four working states of the single-driver IGBT component were clarified. It was found that when an IGBT enters the active region, the next stage IGBT receives an action signal through the corresponding energy storage capacitor. On this basis, the turn-on and turn-off of each stage IGBT were ultimately completed. Additionally, the calculation methods for key devices and parameters were provided.
4) SCBC possesses expandability, and the number of SCBC applications can be rationally selected according to the system capacity. This approach makes SSCBs have higher flexibility and easy maintenance.

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