A Flexible Multimode Control Scheme With Variable Switching Frequency for Parallel Interleaved Three-Phase Inverters

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***Abstract*—In this article, a flexible multimode control scheme with variable switching frequency is proposed for parallel interleaved three-phase inverters. Three working modes are designed based on different operation sequence of inverters, corresponding to low, medium, and high power conditions. Since number of alternately controlled inverters is changed according to the load conditions, the principle of current transition is derived by establishing equivalent circuit model. Based on this, current balance strategy is realized by estimating duration of switches. Furthermore, the flexible mode-switching channel based mode-switching strategy is proposed to achieve fast and smooth transition among different modes. In the proposed scheme, only one field-oriented control (FOC) loop is configured while the drive pulses generated from FOC loop are reallocated to parallel legs for power distribution, thus greatly simplifying the control structure of the parallel inverters. The effectiveness of the proposed method is verified on three parallel inverters with three current sensors. Experimental results show that the proposed scheme can achieve both good dynamic and steady-state performances over wide range of switching frequency and output power.**

***Index Terms*—Drive pulse reallocation, interleaved switching, multimode control scheme, parallel interleaved inverters, permanent magnet synchronous machine, variable frequency.**

I. Introduction

PARALLEL connected two-level (2L) three-phase voltage source inverters (VSIs) are widely employed in electrical machine [1], photovoltaic systems [2], and shunt active-power filter [3], due to its advantage of simple modulation control, low current stress on semiconductors, and high fault tolerance [4]. However, the increased number of control variables and parameters in the single inverter or multiinverter system complicate the design of control strategy [5]. Thus, various control methods for parallel interleaved three-phase 2L inverters have been reported in recent research, such as carrier-based pulse width modulation interleaved switching based pulsewidth modulation (PWM).

Comparatively, carrier-based (CB) PWM has attracted more attention, level-shifted PWM (LS PWM) [6], [7] and phase-shifted PWM (PS PWM) [8], [9], [10], [11], [12], [13], [14], [15], [16] are the two most conventional schemes in CB PWM. LS PWM is commonly used in multilevel converters due to its easy realization [6], [7]. PS PWM shows excellent performance in current harmonic suppression. In the PS PWM based parallel inverters control system, the N paralleled 2L inverters can not only be analyzed as N independent inverters, but also as a single N+1 level inverter [17], [18], [19]. However, in PS PWM, circulating current (CC) is a serious problem caused by interleaved carriers, which can be regulated by proper PWM strategies [8]. Co-occurrence of $\boldsymbol{V_0}$ and $\boldsymbol{V_7}$ in different VSIs causes high common-mode voltage (CMV) and CC and hence $\boldsymbol{V_0}$ and $\boldsymbol{V_7}$ are excluded in papers [9] and [10]. For the PWM methods that contain zero voltage vectors, selection and adjustment of voltage vector sequences can effectively suppress CC [11], [12], [13]. Alternatively, other control freedoms are also introduced to suppress CC, including switching frequency [14], bypass capacitor-based leakage current [16], and carrier shift between three phases [20]. However, the single-minded pursuit of low CC can also cause other additional problems, such as high CMV peak [15], [18], large current ripples [20], and high switching losses [21]. Meanwhile, many PS PWM based methods and suppression algorithms for CMV suppression and CC suppression are only validated on two parallel-connected 2L inverters. As the structure of parallel VSIs becomes more complex, the original methods may no longer be applicable.

Synchronous switching based PWM [22], [23], [24] is a simple control method to avoid CC. Due to single carrier, different inverters share the same voltage vector and switching states. Although the additional current stress on the switches, degradedness of system efficiency and the risk of system breakdown caused by CC are avoided in this method, the total harmonic distortion (THD) of output current cannot be guaranteed.

In papers [25] and [26], a single carrier based interleaved switching strategy is proposed for three parallel half-bridge modules. Parallel legs are activated sequentially, which avoids CC caused by simultaneous conduction of upper and lower

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switches in different parallel legs and increases equivalent switching frequency of the system. However, each half-bridge modules connected in parallel needs to withstand rated current [23], which is not cost-effective and power-underutilized.

In the existing control methods designed for parallel inverters, interleaved carriers-based method suffers from the risk of CC [11]. Synchronized switching based method are unable to guarantee THD of current in low and medium load conditions.

Interleaved switching based strategy is constrained due to its higher current stress on power electronic device than that in ordinary parallel system [26].

To overcome above shortcomings, a flexible multimode control scheme with variable switching frequency is proposed on the basis of interleaved switching strategy. The proposed method contain single carrier-based three working modes, corresponding to low, medium and high power condition. The current balance between parallel inverters in different working modes is also considered. The different working modes increase the equivalent switching frequency of the parallel system, which guarantees the low THD of current in low and medium load conditions. The flexible mode switching channel (FMSC) are proposed to preciously manipulate the current during mode switching, which ensures the fast and smooth transition among different working modes. The zero sequence CC (ZSCC) caused by co-occurrence of $\boldsymbol{V_0}$ and $\boldsymbol{V_7}$ between parallel legs in each phase is avoided due to single carrier, so are the power losses caused by ZSCC. In addition, no modification of modulation strategy is required, so only one conventional field-oriented control (FOC) loop needs to be configured in the proposed scheme.

The rest of this article is organized as follows. In Section II, the working modes for different load conditions and corresponding drive pulse sequences are introduced, and the current balance strategy are proposed, then the switching losses in different working modes are analyzed. In Section III, mode-switching strategy and FMSC are discussed. In Section IV, the experimental results of flexible multimode control scheme with variable switching frequency and flexible mode switching strategy are given for further illustrations. Finally, Section V concludes the article.

II. Multimode Control Scheme With Variable Switching Frequency

A. Working Modes Under Different Load Condition

Fig. 1 shows the relationship between condition, working mode, VSI operation sequence and i_{peak} on VSI. i_{peak} represents the peak value of the current. The load condition of parallel VSIs is divided into three equal intervals, (0, 1/3 p.u.), (1/3, 2/3 p.u.) and (2/3, 1 p.u.), corresponding to the low, medium, and high power conditions, respectively. Three working modes correspond to these three conditions.

Working mode I corresponds to low power condition, in which three parallel VSIs are operated in turn. Only one VSI is responsible for power output in every switching cycle, neglecting the switching process between different VSIs.

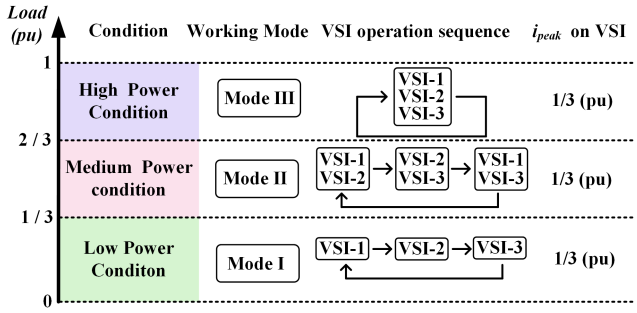

Fig. 1. Proposed working modes under different load conditions.

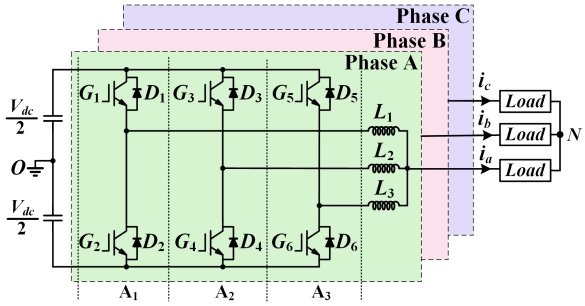

Fig. 2. Typical three parallel interleaved 2L-VSIs with a common DC link.

Working mode II is for medium power condition, in which each two VSIs are alternately operated for power output. In every switching cycle, one VSI operated in last cycle is shut down and a new one is activated. Complete VSI sequence in mode II is given in Fig. 1.

Working mode III is for high power condition. In this mode, three parallel VSIs are activated together, each VSI carries 1/3 of the total output power.

In summary, by applying proper mode in different load conditions, the i_{peak} on VSI is still 1/3 p.u. Compared to the half-bridge module that needs to withdraw rated current in traditional interleaved switching strategy [23], ordinary half-bridge module that withdraws 1/3 rated current can be chosen to build parallel system that contains three VSIs in the proposed scheme, hence the existing drawbacks of low power density and high cost can be avoided.

B. Analysis of Switching Sequences

To realize VSI operation sequences in Fig. 1, proper drive pulse sequences need to be designed. Considering the symmetry of the three phases, the drive pulse sequence in phase A is taken as the example for presentation while ignoring dead time, the voltage drop of semiconductor and the resistance of inductor. Fig. 2 shows the typical three parallel interleaved 2L-VSIs with a common dc link. The three parallel half bridge modules from left to right in phase A are defined as the A phase of VSI-1, VSI-2, and VSI-3, respectively, denoted as $\mathbf{A_1}$, $\mathbf{A_2}$, and $\mathbf{A_3}$, respectively. i_{a1}, i_{a2}, $i_{a3,}$ and i_a represents the output current of $\mathbf{A_1}$, $\mathbf{A_2}$, $\mathbf{A_3}$, and phase A, respectively. L_1, L_2, and L_3 have the same inductance value L. V_{dc} represents the dc link of parallel

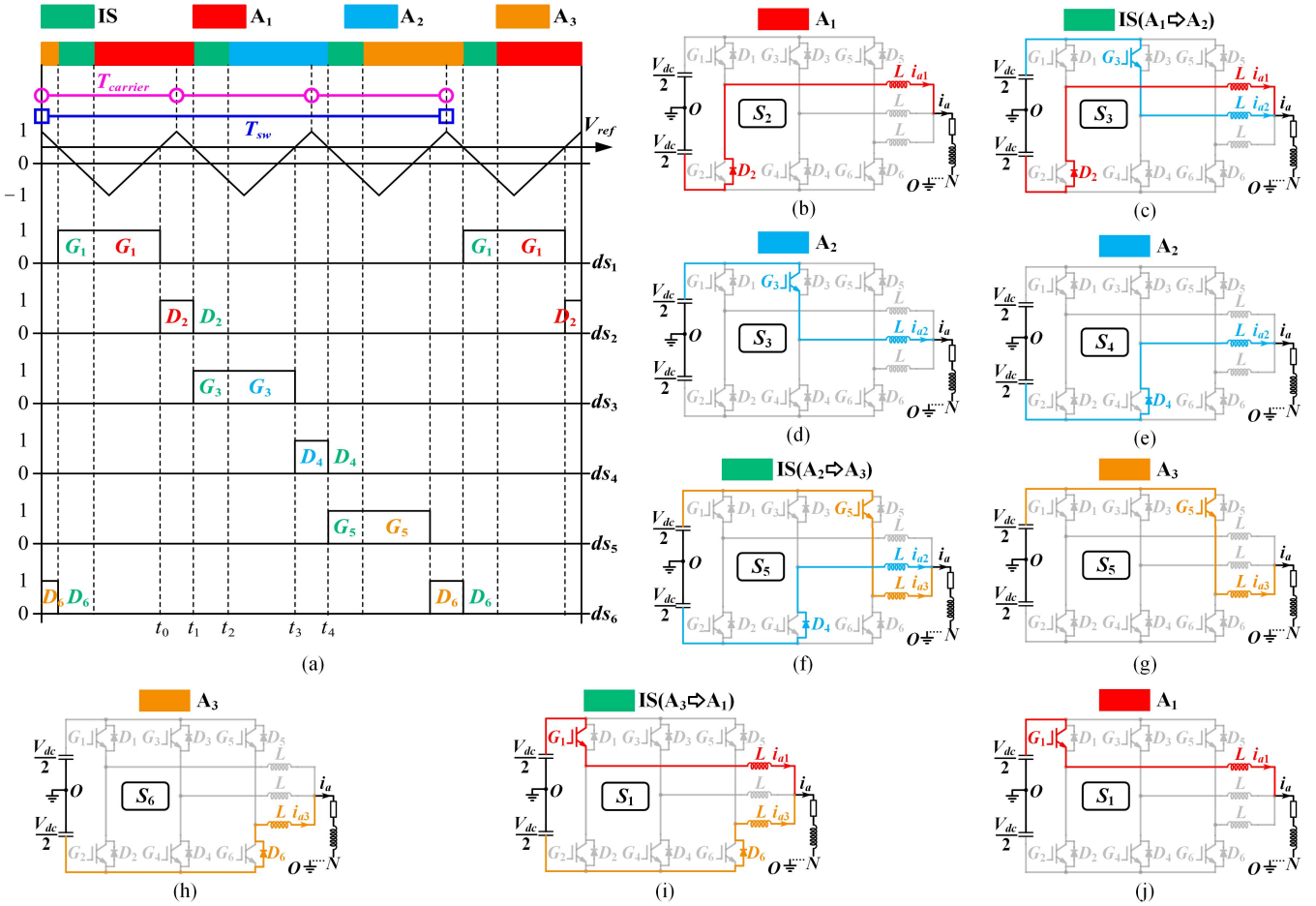

Fig. 3. Drive pulse sequence and current distribution on semiconductor of phase A in working mode I when $i_a \geq 0$. (a) drive pulse sequence. (b) S_2-A$_1$(t_0–t_1). (c) S_3-IS (t_1–t_2). (d) S_3-A$_2$(t_2–t_3). (e) S_4-A$_2$(t_3–t_4). (f) S_5-IS. (g) S_5-A$_3$. (h) S_6-A$_3$. (i) S_1-IS. (j) S_1-A$_1$.

TABLE I
NONZERO COMBINATIONS OF DRIVE PULSES IN ONE PHASE

S	Ds	S	Ds	S	Ds
S_1(100000)	ds_1=1	S_7(101000)	ds_1=1, ds_3=1	S_{13}(101010)	ds_1=1
S_2(010000)	ds_2=1	S_8(010100)	ds_2=1, ds_4=1		ds_3=1
S_3(001000)	ds_3=1	S_9(001010)	ds_3=1, ds_5=1		ds_5=1
S_4(000100)	ds_4=1	S_{10}(000101)	ds_4=1, ds_6=1	S_{14}(010101)	ds_2=1
S_5(000010)	ds_5=1	S_{11}(100010)	ds_1=1, ds_5=1		ds_4=1
S_6(000001)	ds_6=1	S_{12}(010001)	ds_2=1, ds_6=1		ds_6=1

VSIs. $\boldsymbol{ds_1}$–$\boldsymbol{ds_6}$ are defined as the drive pulses for G_1–G_6, which will be amplified by gate driver to control the state of G_1–G_6. $ds_j = 1$ means G_j is turned on, $ds_j = 0$ means G_j is turned OFF, $\forall j \in \{1, 2,..., 6\}$. The $\boldsymbol{S}$ is given to describe six drive pulses in single phase simultaneously. All the nonzero combinations of drive pulses used in flexible multimode control scheme have been listed in Table I.

$$\boldsymbol{S} = (\boldsymbol{ds_1 ds_2 ds_3 ds_4 ds_5 ds_6}). \tag{1}$$

1) Working Mode I: Fig. 3(a) shows interleaved drive pulse sequence of phase A in working mode I when $i_a \geq 0$. The PWM are sequentially distributed to the six switches, ensuring the operation sequence of $\mathbf{A_1}$-$\mathbf{A_2}$-$\mathbf{A_3}$-$\mathbf{A_1}$ and VSIs at the system level shown in Fig. 1. The time from t_0 to t_4 in Fig. 3(a) is chosen to analyze the transition from $\mathbf{A_1}$ to $\mathbf{A_2}$. During the transition, there will be a situation where current presents in multiple VSIs at the same time, which is defined as interim state (IS).

t_0–t_1($\boldsymbol{S_2}$): D_2 provides the continuous current path as shown in Fig. 3(b). $\mathbf{A_1}$ is on operation, i_{a1} is equal to i_a.

t_1–t_2($\boldsymbol{S_3}$): At t_1, G_3 is turned on and the current transition from $\mathbf{A_1}$ to $\mathbf{A_2}$ begins, i_{a1} drops while i_{a2} rises, corresponding current path is given in Fig. 3(c).

t_2–t_3($\boldsymbol{S_3}$): i_{a1} drops to 0 at t_2, IS ends. i_{a2} is equal to i_a, current only exists on G_3 as shown in Fig. 3(d), only $\mathbf{A_2}$ is on operation.

t_3–t_4($\boldsymbol{S_4}$): i_{a2} flows into the load through D_4 as shown in Fig. 3(e). $\mathbf{A_2}$ is still on operation.

The output voltage of phase A is defined as V_{AO}. Based on Kirchhoff's law, (2) can be listed to calculate the time for current transition from $\mathbf{A_1}$ to $\mathbf{A_2}$

$$\begin{cases} V_{dc}/2 + L\,(di_{a1}/dt) + V_{AO} = 0 \\ -V_{dc}/2 + L\,(di_{a2}/dt) + V_{AO} = 0 \\ \quad i_{a1} + i_{a2} - i_a = 0. \end{cases} \tag{2}$$

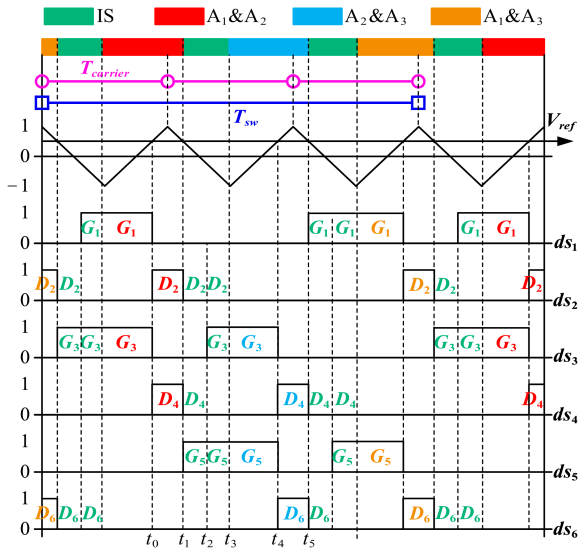

Fig. 4. Drive pulse sequence and current distribution on semiconductor of phase A in working mode II when $i_a \geq 0$.

Based on (2), V_{AO} and voltage drop across L_2 can be obtained

$$V_{AO} = 0 \tag{3}$$

$$L\left(di_{a2}/dt\right) = V_{dc}/2. \tag{4}$$

The switching time T_{sp1} can be derived by integrating each side of (4) in the interval $[t_1,t_2]$:

$$T_{sp1} = t_2 - t_1 = 2Li_a/V_{dc}. \tag{5}$$

In summary, when $i_a \geq 0$, the $\boldsymbol{S}$ sequence is $\boldsymbol{S_1}$-$\boldsymbol{S_2}$-$\boldsymbol{S_3}$-$\boldsymbol{S_4}$-$\boldsymbol{S_5}$-$\boldsymbol{S_6}$-$\boldsymbol{S_1}$ in working mode I. Diode in the lower bridge arm provides path for continuous current. The current transition within phase A begins when upper switch is turned ON. When $i_a<0$, the situation is opposite. The diode of upper bridge arm provides continuous path and current transition begins when the lower switch is turned ON. Thus, when $i_a<0$, the $\boldsymbol{S}$ sequence is $\boldsymbol{S_2}$-$\boldsymbol{S_1}$-$\boldsymbol{S_4}$-$\boldsymbol{S_3}$-$\boldsymbol{S_6}$-$\boldsymbol{S_5}$-$\boldsymbol{S_2}$. T_{carrier} and T_{sw} are defined as the carrier cycle and the switching cycle of semiconductor, respectively. In working mode I, the carrier frequency is equal to equivalent switching frequency of the parallel system, which is increased to three times the switching frequency of semiconductor switch.

2) Working Mode II: The $\boldsymbol{S}$ sequence considering current balance for working mode II when $i_a \geq 0$ is given in Fig. 4, which can achieve alternate control of each two parallel legs in phase A.

The interval $[t_0, t_5]$ in Fig. 4 contains the switching process from $(\mathbf{A_1\&A_2})$ to $(\mathbf{A_2\&A_3})$, which is taken to analyze the details. To ensure the current balance on two parallel legs, there are two ISs during transition, referred to as IS-1 and IS-2, respectively.

t_0–t_1($\boldsymbol{S_8}$): D_2 and D_4 provide the path for continuous current, as shown in Fig. 5(a).

t_1–t_2($\boldsymbol{S_5}$): At t_1, only G_5 is turned ON and IS-1 begins. Current is transited from $(\mathbf{A_1\&A_2})$ to $\mathbf{A_3}$ as shown in Fig. 5(b), i_{a1} and i_{a2} drop while i_{a3} rises.

TABLE II
CURRENT ON PARALLEL LEGS DURING SWITCHING PROCESS IN MODE II

	t_1	t_2	t_3
i_{a1}	$i_a/2$	$i_{a1}(t_2)$	0
i_{a2}	$i_a/2$	$i_{a1}(t_2)$	$i_{a1}(t_2)+i_{a1}(t_2)/2$
i_{a3}	0	$2[i_a/2-i_{a1}(t_2)]$	$2[i_a/2-i_{a1}(t_2)]+i_{a1}(t_2)/2$

t_2–t_3($\boldsymbol{S_9}$): At t_2, G_5 stays on and G_3 is turned ON, IS-1 ends, IS-2 begins. Current is transited from $\mathbf{A_1}$ to $(\mathbf{A_2\&A_3})$ as shown in Fig. 5(c), i_{a1} drops while i_{a2} and i_{a3} rise.

t_3–t_4($\boldsymbol{S_9}$): At t_3, i_{a1} drops to 0, IS-2 ends, current exists on $\mathbf{A_2}$ and $\mathbf{A_3}$ as shown in Fig. 5(d).

t_4–t_5($\boldsymbol{S_{10}}$): D_4 and D_6 provide paths for i_{a2} and i_{a3}, respectively as shown in Fig. 5(e).

The time interval $[t_1, t_2]$ is important in balancing the current on parallel legs. Thus, it is necessary to estimate the duration of $\boldsymbol{S_5}$. According to Fig. 5(b), the following equation can be obtained:

$$\begin{cases} V_{dc}/2 + L\left(di_{a1}/dt\right) + V_{AO} = 0 \\ V_{dc}/2 + L\left(di_{a2}/dt\right) + V_{AO} = 0 \\ -V_{dc}/2 + L\left(di_{a3}/dt\right) + V_{AO} = 0 \\ i_{a1} + i_{a2} + i_{a3} - i_a = 0. \end{cases} \tag{6}$$

Based on (6), the following equation can be obtained:

$$-2L\left(di_{a1}/dt\right) = -2L\left(di_{a2}/dt\right) = L\left(di_{a3}/dt\right). \tag{7}$$

From t_1 to t_2, the relationship between Δi_{a1}, Δi_{a2} and Δi_{a3} can be expressed as follows:

$$-2\Delta i_{a1\_21} = -2\Delta i_{a2\_21} = \Delta i_{a3\_21} \tag{8}$$

where $\Delta i_{a1\ 21}$, $\Delta i_{a2\ 21}$ and $\Delta i_{a3\ 21}$ corresponds to Δi_{a1}, Δi_{a2} and Δi_{a3} from t_1 to t_2, respectively.

From t_2 to t_3, $\boldsymbol{S}$ state is $\boldsymbol{S}_9$, i_{a2} and i_{a3} rise, while i_{a1} drops. The relationship between changes in current on the three parallel legs can be obtained

$$-\Delta i_{a1\_32} = 2\Delta i_{a2\_32} = 2\Delta i_{a3\_32} \tag{9}$$

where $\Delta i_{a1\ 32}$, $\Delta i_{a2\ 32}$, and $\Delta i_{a3\ 32}$ corresponds to Δi_{a1}, Δi_{a2}, and Δi_{a3} from t_2 to t_3, respectively.

Assume that i_{a1} and i_{a2} have the same amplitude $i_a/2$ from t_0 to t_1 before IS-1, define $i_{a1}(t_2)$ as the value of i_{a1} at t_2. Based on (8) and (9), the current values at $t_1$and t_3 can be derived and are listed in Table II.

At t_3, IS ends, i_{a2} and i_{a3} have the same amplitude, combining with (7), the duration of $\boldsymbol{S_5}$ can be derived

$$t_2 - t_1 = \frac{Li_a}{2V_{dc}}. \tag{10}$$

In (10), L is fixed, i_a and V_{dc} can be obtained from analog to digital converter at the beginning of each carrier cycle, so it is feasible to calculate duration of $\boldsymbol{S_1}$, $\boldsymbol{S_3}$ or $\boldsymbol{S_5}$ in working mode II.

In summary, when $i_a \geq 0$, the $\boldsymbol{S}$ sequence is $\boldsymbol{S_8}$-$\boldsymbol{S_5}$-$\boldsymbol{S_9}$-$\boldsymbol{S_{10}}$-$\boldsymbol{S_1}$-$\boldsymbol{S_{11}}$-$\boldsymbol{S_{12}}$-$\boldsymbol{S_3}$-$\boldsymbol{S_7}$-$\boldsymbol{S_8}$ in mode II. $\boldsymbol{S_1}$, $\boldsymbol{S_3}$ and $\boldsymbol{S_5}$ is added to delay the turn-on of G_5, G_1 and G_3, respectively, thus ensuring the current balance on parallel legs. When $i_a<0$, $\boldsymbol{S_2}$, $\boldsymbol{S_4}$ and

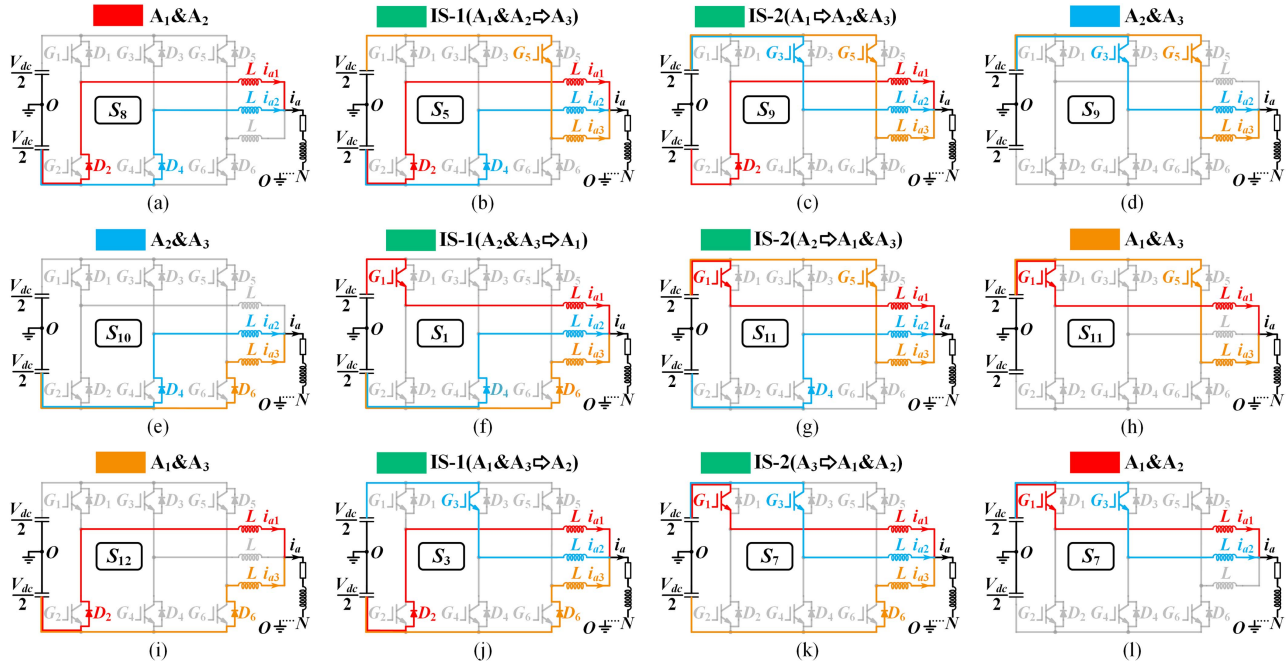

Fig. 5. Current path of phase A in working mode II when $i_a \geq 0$. (a) S_8-A1&A2($t_0 \sim t_1$). (b) S_5-IS-1($t_1 \sim t_2$). (c) S_9-IS-2($t_2 \sim t_3$). (d) S_9-A2&A3($t_3 \sim t_4$). (e) S_{10}-A2&A3($t_4 \sim t_5$). (f) S_1-IS-1. (g) S_{11}-IS-2. (h) S_{11}-A1&A3. (i) S_{12}-A1&A3. (j) S_3-IS-1. (k) S_7-IS-2. (l) S_7-A1&A2.

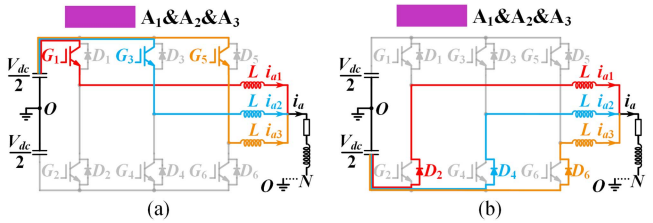

Fig. 6. Current path of phase A in working mode III when $i_a \geq 0$. (a) S_{13}. (b) S_{14}.

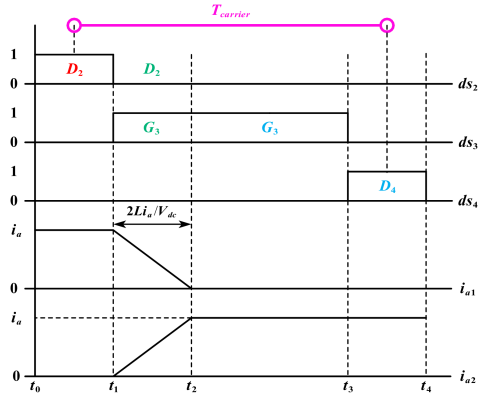

Fig. 7. Waveforms of drive pulses and current on parallel legs in phase A from t_0 to t_4 in working mode I when $i_a \geq 0$.

$\boldsymbol{S_6}$ can be associated to replace the $\boldsymbol{S_1}$, $\boldsymbol{S_3}$ and $\boldsymbol{S_5}$, thus the $\boldsymbol{S}$ sequence is $\boldsymbol{S_7}$-$\boldsymbol{S_6}$-$\boldsymbol{S_{10}}$-$\boldsymbol{S_9}$-$\boldsymbol{S_2}$-$\boldsymbol{S_{12}}$-$\boldsymbol{S_{11}}$-$\boldsymbol{S_4}$-$\boldsymbol{S_8}$-$\boldsymbol{S_7}$. In practice, to prevent frequent switching of current polarity near zero-crossing point, the hysteresis comparator is used. Even if $\boldsymbol{S}$ sequence is temporarily mismatched with actual current polarity, the duration of $\boldsymbol{S_1}$, $\boldsymbol{S_3}$ and $\boldsymbol{S_5}$ or $\boldsymbol{S_2}$, $\boldsymbol{S_4}$ and $\boldsymbol{S_6}$ is very short according to (10) and hence the impact caused by them can be ignored.

In the $\boldsymbol{S}$ sequences of working mode II, the equivalent switching frequency of parallel system is equal to carrier frequency, which is increased to 1.5 times the switching frequency of semiconductor switch.

3) Working Mode III: In working mode III, three inverters are operated synchronously, there are only S_{13} and S_{14} in working mode III. The current path in phase A when $i_a \geq 0$ is common, as given in Fig. 6. For the condition of $i_a < 0$, the diodes of upper bridge arms provide path for continuous current, and current flows into the inverters when switches of lower bridge arm are turned ON.

C. Analysis of Switching Losses

1) Working Mode I: The time interval [t_0, t_4] in Fig. 3(a) is selected to analyze the switching losses in T_{carrier}. According to (2)–(5), the waveforms of drive pulse and current on the parallel legs of phase A when $i_a \geq 0$ can be obtained, which has been given in Fig. 7. Due to the inductor connected with half-bridge module, sudden change of current on G_3 will not happen. When G_3 is turned ON at t_1, the current on G_3 is still hold to zero. Therefore, due to zero current switching (ZCS) of G_3, the turn-ON losses on G3 can be ignored. At t_3, i_{a2} is equal to i_a, and G_3 is turned OFF, so its turn-OFF losses need to be considered.

T_0 is defined as the fundamental period. The number of T_{carrier} in one T_0 can be expressed as T_0/T_{carrier}. $E_{\text{on}}(k)$, $E_{\text{off}}(k)$ represent the turn-ON, turn-OFF energy in the kth T_{carrier}. $P_{\text{SW1}}(k)$ is defined as the A-phase switching losses in kth T_{carrier}, and it can

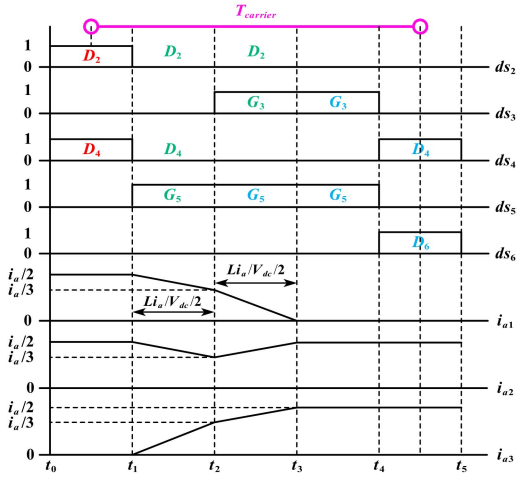

Fig. 8. Waveform of drive pulses and current on parallel legs in phase A from t_0 to t_5 in working mode II when $i_a \geq 0$.

be expressed as follows:

$$P_{\mathrm{SW1}}(k) = \frac{V_{dc}}{600}\frac{1}{T_{\mathrm{carrier}}}\left[E_{\mathrm{off}}(k)\right]. \tag{11}$$

According to the datasheet, $E_{\mathrm{on}}(k)$, $E_{\mathrm{off}}(k)$ is the function of current and are valid at $V_{CE} = 600$ V, so the gain of $V_{dc}/600$ is given in (11).

P_{SW1} is defined as the switching loess in working mode I, and it can be derived based on (11)

$$P_{\mathrm{SW1}} = 6 \times \frac{2}{T_0}\frac{V_{dc}}{600}\sum_{k=1}^{T_0/T_{\mathrm{carrier}}/2}\left\langle E_{\mathrm{off}}\left[i_a(k)\right]\right\rangle \tag{12}$$

where $i_a(k)$ represent the amplitude of i_a in the kth T_{carrier}. P_{SW1} represents the switching loss in working mode I.

Although the ZCS are realized due to the inductor, the additional conduction losses on D_2 are generated during time interval $[t_1, t_2]$, while the conduction losses on G3 is reduced. In the low current region, the collector–emitter saturation voltage and forward voltage have the closer value according to datasheet, increased conduction losses of diode are equal to the reduced conduction loess of switch, which has little influence on total conduction losses.

2) Working Mode II: The time interval $[t_0, t_5]$ in Fig. 4 is selected to analyze the switching losses in $\mathrm{T_{carrier}}$. According to (6)–(10) and Table II, the waveforms of drive pulse and current on the parallel legs of phase A when $i_a \geq 0$ can be obtained, which has been shown in Fig. 8. At t_1, G_5 is turned ON when i_{a3} is equal to zero. Therefore, the turn-ON losses on G_5 can be ignored due to ZCS. The turn-ON losses of G_3 are produced at t_2, due to presence of current on D_4. At t_4, the amplitude of i_{a2} and i_{a3} is $i_a/2$. G_3 and G_5 are turned OFF at t_4, which causes turn-OFF losses as usual.

$P_{\mathrm{SW2}}(k)$ is defined as the A-phase switching losses in the kth T_{carrier}, and it can be expressed as follows:

$$P_{\mathrm{SW2}}(k) = \frac{V_{dc}}{600}\frac{1}{T_{\mathrm{sw}}}\left\langle E_{\mathrm{on}}(k) + 2E_{\mathrm{off}}(k)\right\rangle. \tag{13}$$

Based on (13), the switching loess in working mode II can be expressed as follows:

$$P_{\mathrm{SW2}} = 6 \times \frac{V_{dc}}{600}\frac{2}{T_0}\sum_{k=1}^{T_0/T_{\mathrm{carrier}}/2}\left\langle \begin{matrix} E_{\mathrm{on}}\left[(i_a(k)/3)\right] \\ +2E_{\mathrm{off}}\left[(i_a(k)/2)\right] \end{matrix}\right\rangle. \tag{14}$$

Similarly, the additional conduction losses on D_2 and D_4 are generated during time interval $[t_1, t_2]$ and $[t_2, t_3]$, while the conduction losses on G_3 and G_5 are reduced. As the rise of current, the increase in the collector-emitter saturation voltage is more than that in forward voltage according to datasheet. Therefore, the total conduction losses are slightly reduced.

3) Working Mode II: P_{SW3} is defined as the switching losses in working mode III, and can be obtained according to the following [14]:

$$P_{\mathrm{SW3}} = 18 \times \frac{2}{T_0}\frac{V_{dc}}{600}\sum_{k=1}^{T_0/T_{\mathrm{carrier}}/2}\left\langle \begin{matrix} E_{\mathrm{on}}\left[i_a(k)/3\right] \\ +E_{\mathrm{off}}\left[i_a(k)/3\right] \end{matrix}\right\rangle. \tag{15}$$

III. Flexible Mode-Switching Strategy

Essentially, the core of the flexible mode-switching strategy is to make the current appear on the desirable branches and maintains current balance after switching. The moment of mode switching and the combination of drive pulse during transitions are the two important considerations in the design of flexible mode-switching strategy.

According to the analysis above, the current transition within the phase A requires two conditions: 1) The upper switch of any half-bridge module is turned ON. 2) Continuous current exists on the diode of lower bridge arm in the remaining half-bridge module. Based on these two principles, the FMSC between different working modes are designed to ensure fast and smooth transition. The start of FMSC is the $\boldsymbol{S}$ in the current working mode, the end of channel is the $\boldsymbol{S}$ in the next working mode. There may be additional $\boldsymbol{S}$in the middle to ensure the current balance after mode switching. The flexible mode-switching strategy are analyzed in phase A when $i_a \geq 0$.

A. Transition Between Working Mode I and Working Mode II

From mode I to mode II, the start of FMSC can be $\boldsymbol{S_2}$, $\boldsymbol{S_4}$ or $\boldsymbol{S_6}$, the end of FMSC can be $\boldsymbol{S_7}$, $\boldsymbol{S_9}$, or $\boldsymbol{S_{11}}$. Based on the principle of complementarity, the complete FMSCs can be derived by matching the $\boldsymbol{S}$ mentioned above. Taking the FMSC of $\boldsymbol{S_2}$–$\boldsymbol{S_9}$ for example. $\mathbf{A_1}$ is on operation in $\boldsymbol{S_2}$, i_{a1} is equal to i_a, $\mathbf{A_2}$ and $\mathbf{A_3}$ are spare as shown in Fig. 3(b). In the next carrier cycle,$\boldsymbol{S_2}$ is switched to $\boldsymbol{S_9}$, the current is transited from $\mathbf{A_1}$ to $(\mathbf{A_2}\&\mathbf{A_3})$ as shown in Fig. 5(c). When i_{a1} drops to 0, $\mathbf{A_2}$ and $\mathbf{A_3}$are activated instead of $\mathbf{A_1}$, as shown in Fig. 5(d), mode transition is end.

From mode II to mode I, similar FMSC of $\boldsymbol{S_{10}}$-$\boldsymbol{S_1}$ can be associated. All FMSCs between mode I and mode II when $i_a \geq 0$ are given in Fig. 9.

Complete FMSCs when $i_a \geq 0$ between mode I and mode II, relevant working VSI, current paths and combinations of drive pulses can be inquired in Table III. When $i_a < 0$, the FMSCs can be in inquired in Table IV.

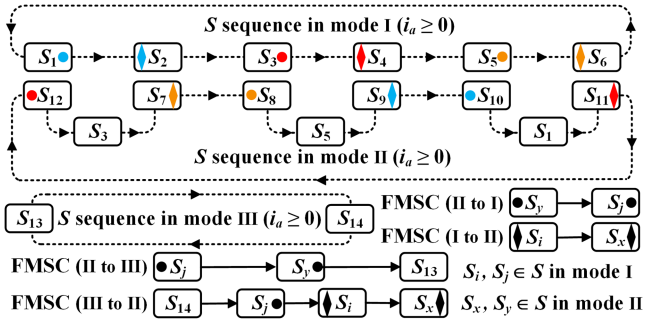

Fig. 9. FMSCs of phase A between different working modes when $i_a \geq 0$.

TABLE III
RELATIONSHIP BETWEEN DRIVE PULSE AND WORKING VSI AND CURRENT PATH FROM WORKING MODE I TO WORKING MODE II IN PHASE A WHEN CURRENT IS GREATER THAN OR EQUAL TO 0

$i_a \geq 0$	Mode I to mode II			Mode II to mode I		
FMSC	Woking VSI	S	Current path	Woking VSI	S	Current path
1	**A_1**	**S_2**	Fig. 3(b)	**A_1&A_2**	**S_8**	Fig. 5 (a)
	IS	**S_9**	Fig. 5(c)	IS	**S_5**	Fig. 5 (b)
	A_2&A_3	**S_9**	Fig. 5(d)	**A_3**	**S_5**	Fig. 3 (g)
2	**A_2**	**S_4**	Fig. 3(e)	**A_2&A_3**	**S_{10}**	Fig. 5 (e)
	IS	**S_{11}**	Fig. 5(g)	IS	**S_1**	Fig. 5 (f)
	A_1&A_3	**S_{11}**	Fig. 5(h)	**A_1**	**S_1**	Fig. 3 (j)
3	**A_3**	**S_6**	Fig. 3(h)	**A_1&A_3**	**S_{12}**	Fig. 5 (i)
	IS	**S_7**	Fig. 5(k)	IS	**S_3**	Fig. 5 (j)
	A_1&A_2	**S_7**	Fig. 5(l)	**A_2**	**S_3**	Fig. 3 (d)

TABLE IV
FMSCS BETWEEN DIFFERENT MODES WHEN CURRENT IS LESS THAN 0

I to II	II to I	III to II	II to III
S_1-S_{10}	**S_7-S_6**	**S_{13}-S_6-S_5-S_8**	**S_7-S_6-S_{14}**
S_3-S_{12}	**S_9-S_2**	**S_{13}-S_2-S_1-S_{10}**	**S_9-S_2-S_{14}**
S_5-S_8	**S_{11}-S_4**	**S_{13}-S_4-S_3-S_{12}**	**S_{11}-S_4-S_{14}**

B. Transition Between Working Mode II and Working Mode III

From mode III to mode II, the first step is making the current exist on one VSI, the second step is transiting the current to the other two spare VSIs. The FMSC of **S_{14}-S_5-S_6-S_7** is analyzed. By switching **S_{14}** to **S_5**, current is transited from (A1&A2&A3) to A3 as shown in Fig. 5(b). When i_{a1} and i_{a2} drop to 0, only A3 is activated, as shown in Fig. 3(g). Then**S_5** is switched to **S_6**, Fig. 3(h) shows the path of continuous current. Finally, **S_6** is switched to **S_7**, current is transited from A3 to (A1&A2) as shown in Fig. 5(k). When i_{a3} drops to 0, only A1 and A2 are activated as given in Fig. 5(l), the mode switching is finished.

From mode II to mode III, the first step is still making the current exist on one VSI, the second step is making the current exist on three VSIs through inductors. Thus, the FMSC of **S_8-S_5-S_{13}** can be associated, the corresponding current path during transition is Figs. 3(g), 5(a), (b) and 6(a). All FMSCs when $i_a \geq 0$ between mode II and mode III, relevant working VSI, current paths, and combinations of drive pulses can be inquired in Table V. When $i_a < 0$, the situation of current transition is similar, FMSCs among different modes are given in Table IV.

TABLE V
RELATIONSHIP BETWEEN DRIVE PULSE AND WORKING VSI AND CURRENT PATH FROM WORKING MODE II TO WORKING MODE III IN PHASE A WHEN CURRENT IS GREATER THAN OR EQUAL TO 0

$i_a \geq 0$	Mode III to mode II			Mode II to mode III		
FMSC	Woking VSI	S	Current path	Woking VSI	S	Current path
1	**A_1&A_2&A_3**	**S_{14}**	Fig. 6(b)	**A_1&A_2**	**S_8**	Fig. 5(a)
	IS-1	**S_5**	Fig. 5(b)	IS-1	**S_5**	Fig. 5(b)
	IS-2	**S_5**	Fig. 3(g)	IS-2	**S_5**	Fig. 3(g)
	IS-3	**S_6**	Fig. 3(h)	**A_1&A_2&A_3**	**S_{13}**	Fig. 6(a)
	IS-4	**S_7**	Fig. 5(k)	/	/	/
	A_1&A_2	**S_7**	Fig. 5(l)	/	/	/
2	**A_1&A_2&A_3**	**S_{14}**	Fig. 6(b)	**A_2&A_3**	**S_{10}**	Fig. 5(e)
	IS-1	**S_1**	Fig. 5(f)	IS-1	**S_1**	Fig. 5(f)
	IS-2	**S_1**	Fig. 3(j)	IS-2	**S_1**	Fig. 3(j)
	IS-3	**S_2**	Fig. 3(b)	**A_1&A_2&A_3**	**S_{13}**	Fig. 6(a)
	IS-4	**S_9**	Fig. 5(c)	/	/	/
	A_2&A_3	**S_9**	Fig. 5(d)	/	/	/
3	**A_1&A_2&A_3**	**S_{14}**	Fig. 6(b)	**A_1&A_3**	**S_{12}**	Fig. 5(i)
	IS-1	**S_3**	Fig. 5(j)	IS-1	**S_7**	Fig. 5(j)
	IS-2	**S_3**	Fig. 3(d)	IS-2	**S_7**	Fig. 3(d)
	IS-3	**S_4**	Fig. 3(e)	**A_1&A_2&A_3**	**S_{13}**	Fig. 6(a)
	IS-4	**S_{11}**	Fig. 5(g)	/	/	/
	A_1&A_3	**S_{11}**	Fig. 5(h)	/	/	/

IV. EXPERIMENT VERIFICATION

A. Experimental Platform and Hardware Introduction

The schematic diagram of test system and procedure of the proposed method is given in Fig. 10. The seven-segment SVPWM modulation is configured for generation of drive pulse, the rising edges and fall edges in each carrier cycle ensure the realization of different working modes and FMSC based mode-switching strategy. The proposed scheme is verified on MicroLabBox and programmable gate array (FPGA) based experimental platform as shown in Fig. 11. MicroLabBox dedicates FOC. The FPGA is employed to manipulate PWM signal and generate drive pulses of specific sequences, and its model is Cyclone IV EP4CE22F17C8N. For transmission signals from dSPACE to FPGA, the output signals of dSPACE are uniformly converted to left-aligned square waves. The transmitted signals contain the drive signal, current polarity, working mode, switching frequency. In each carrier cycle, the duty cycle of drive pulses and switching frequency can be obtained in FPGA by calculating the duration of the action of the high level. Since the current polarity and control mode are predefined with respect to the levels, FPGA can obtain the actual current polarity and control mode by reading the levels of current polarity signal and working mode signal. By building finite state machines in FPGA, the rules for drive pulses reallocation can be determined according to the signals from dSPACE in current carrier cycle. The insulated gate bipolar transistor (IGBT) half-bridge module for building parallel inverters is Infineon FF75R12RT4. The parameters of tested permanent magnet synchronous machine (PMSM) are given in Table VI. Tektronix MDO oscilloscope and current probes are used to measure and record current. ControlDesk software on PC is for debugging, recording and monitoring in the experiment. The sampling frequency of ControlDesk is set to 20 kHz. The frequency of IGBT is fixed to 3 kHz, the carrier

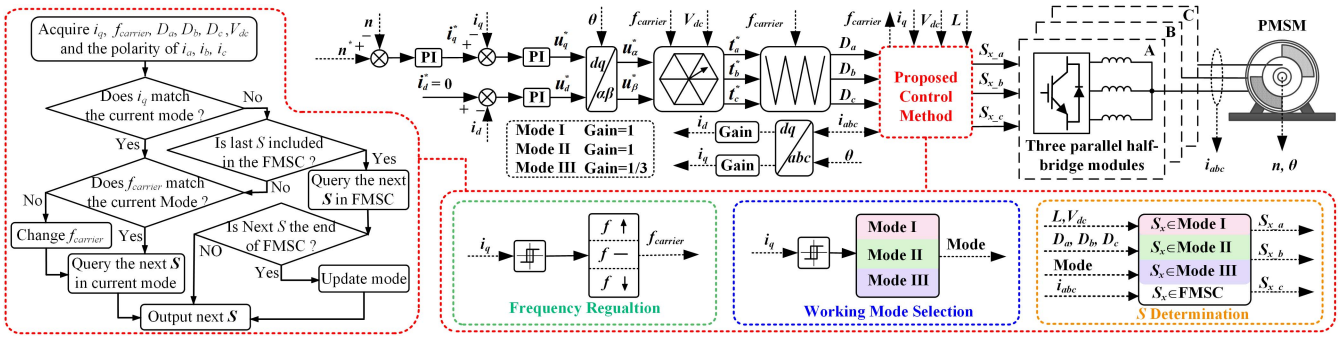

Fig. 10. Schematic diagram of test system and procedure of flexible multimode control with variable switching frequency.

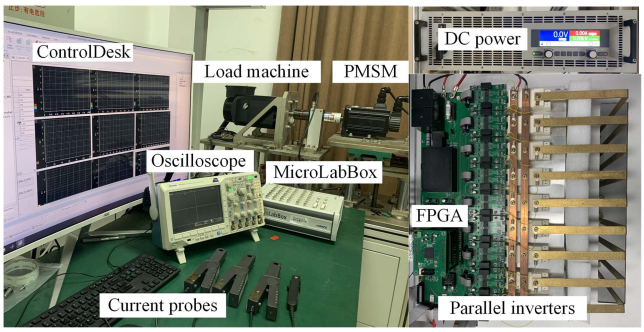

Fig. 11. Experimental platform and tested prototype PMSM.

TABLE VI
PARAMETERS OF TESTED PROTOTYPE PMSM

Parameters	Value	Parameters	Value
Rated current	9 A	dq-axis inductances	5.3 mH
Rated torque	11 N·m	Number of pole pairs	5
Permanent magnet flux linkage	189.2 mWb	Stator winding resistance	0.47 Ω

TABLE VII
THRESHOLDS IN EXPERIMENT VERIFICATION

Function	Direction	Object	Threshold
Current polarity	Positive to negative	i_a, i_b, i_c	–0.04 A
	Negative to positive		0.04 A
Working mode switching	Mode I to Mode II	i_q	2.8 A
	Mode I to Mode II		2.1 A
	Mode II to Mode III		5.8 A
	Mode III to Mode II		5.2 A

frequency in working mode I, II and III is set to 9, 4.5, and 3 kHz, respectively, so as the equivalent switching frequency of the parallel system. The dc bus voltage of parallel inverters is set to 100 V. The rotational speed of PMSM is set as 200 r/min. The inductor connected with half-bridge module has the inductance value of 1 mH. The thresholds for judgement of current polarity and working mode switching are given in Table VII. The load condition of paralleled VSIs is divided into three intervals, (0, 3 A), (3, 6 A), and (6, 9 A),

B. Different Working Modes

1) Working Mode I: In working mode I, the peak value of i_a, i_{a1}, i_{a2}, and i_{a3} and is 2.2, 2.5, 2.7, and 2.5 A, respectively. i_a is the envelope of i_{a1}, i_{a2}, or i_{a3} as shown in Fig. 12(a). According to Fig. 12(d) and (g), the operation sequence of $\mathbf{A_1}$-$\mathbf{A_2}$-$\mathbf{A_3}$-$\mathbf{A_1}$ can be found.

The interleaved sequence in mode I is similar to that in [25] and [26], the maximum current stress on IGBT and diode is approximately 3 A in the interval (0, 3 A).

2) Working Mode II: In working mode II, the peak value of i_a is 5.2 A and peak of i_{a1}, i_{a2} and i_{a3} is 3.1, 3.3, and 3.3 A as shown Fig. 12(b). According to Fig. 12(e) and (h), i_a is distributed over the two parallel legs. Based on Fig. 12(e) and (h), operation sequence of ($\mathbf{A_1}$&$\mathbf{A_2}$)–($\mathbf{A_2}$&$\mathbf{A_3}$)–($\mathbf{A_1}$&$\mathbf{A_3}$)–($\mathbf{A_1}$&$\mathbf{A_2}$) in mode II can also be derived. In the interval (3, 6 A), by applying alternate control of each two VSI instead of interleaved switching control, the maximum current stress on IGBT and diode is decreased from 6 A to approximately 3 A in mode II.

3) Working Mode III: In working mode III, three VSIs are operated synchronously. Current exists on all parallel legs in each phase, i_{a1}. i_{a2} and i_{a3} have relatively close amplitudes. According to Fig. 12(c), the peak value of i_a, i_{a1}, i_{a2}, and i_{a3} is 7.9, 2.7, 3.1, and 2.9 A, respectively. Due to synchronous operation of three VSIs in the interval (6, 9 A), the maximum current stress on IGBT and diode is still approximately 3 A in mode III.

In summary, considering that only single SVPWM module and three current sensors are configured in the proposed method, the errors in current amplitude between parallel legs in each phase can be anticipated.

C. Working Mode Switching

1) Transition Between Mode I and Mode II: To realize the transition from mode I to mode II, the load torque of PMSM is stepped from 2.5 to 6.5 N·m to make the i_q reach the threshold listed in Table VII. The waveforms of current and torque are given in Fig. 13(a). i_q rises from 2 to 5 A, so are the peak values of i_a, i_b, and i_c. The peak value of i_{a1}, i_{a2}, and i_{a3} is 2.5, 2.7, and 2.5 A in mode I, 3.1, 3.5, and 3.3 A, respectively, in mode II. In phase A, the mode is switched from mode I to mode II when

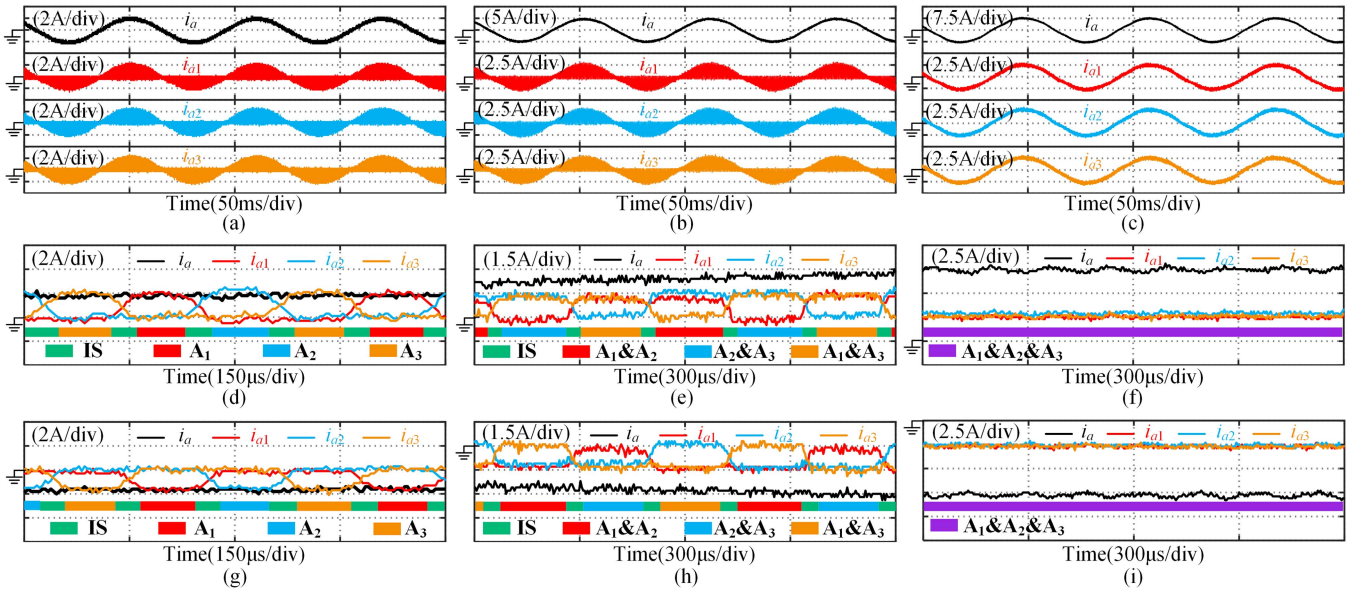

Fig. 12. Experimental current waveforms in different working modes. (a) Mode I (b) Mode II. (c) Mode III. (d) Details in mode I when $i_a \geq 0$. (e) Details in mode II when $i_a \geq 0$. (f) Details in mode III when $i_a \geq 0$. (g) Details in mode I when $i_a < 0$. (h) Details in mode II when $i_a < 0$. (i) Details in mode III when $i_a < 0$.

$i_a < 0$. According to the details of current in Fig. 13(d), i_{a1} drops to 0, while i_{a2} and i_{a3} rises to 1.5 A during mode transition, $\mathbf{A_2}$and $\mathbf{A_3}$are activated instead of $\mathbf{A_1}$, the FMSC of $\boldsymbol{S_1}$–$\boldsymbol{S_{10}}$ can also be derived.

To realize the transition from mode II to mode I, the load condition of PMSM is stepped from 6.5 to 2.5 N·m. i_q drops from 5 to 2 A, as shown in Fig. 13(b). The peak value of i_{a1}, i_{a2}, and i_{a3} is 3.1, 3.3, and 3.1 A, respectively, in mode II, 2.5, 2.7, and 2.5 A, respectively, in mode I. According to Fig. 13(e), current within phase A is transited from $(\mathbf{A_1}\&\mathbf{A_3})$ to $\mathbf{A_2}$ when $i_a > 0$, the FMSC of $\boldsymbol{S_{12}}$–$\boldsymbol{S_3}$ can also be found.

2) Transition Between Mode II and Mode III: To realize the mode switching from II to III, the load torque is stepped from 5.6 to 9.2 N·m. The waveforms are showed in Fig. 13(c). The peak of i_a, i_b, and i_c are increased from 4.33 to 6.77 A. The peaks of i_{a1}, i_{a2}, and i_{a3} is 2.4, 2.6, and 2.6 A, respectively, in mode II, 2.2, 2.6, and 2.6 A, respectively, in mode III. According to Fig. 13(f), the sequence of current transition within phase A is $(\mathbf{A_1}\&\mathbf{A_2})$-$\mathbf{A_3}$-$(\mathbf{A_1}\&\mathbf{A_2}\&\mathbf{A_3})$ when $i_a > 0$, the FMSCs of $\boldsymbol{S_8}$-$\boldsymbol{S_5}$-$\boldsymbol{S_{13}}$ can be found.

To realize the mode switching from mode II to mode III, the load torque is stepped from 9.6 to 5.7 N·m, the peak values of i_a, i_b, and i_c drop from 7.25 to 4.25 A. During transition, the amplitude of i_q across multiple thresholds listed in Table VII. Therefore, there are multiple mode-switching processes during transition from mode III to mode II. The complete mode switching sequence is III-II-I-II as shown in Fig. 13(g). Details are given in Fig. 13(h)–(j), respectively. First, the mode in phase A is switched from III to II due to fall of i_q. During mode switching, the sequence of current transition within phase A is $(\mathbf{A_1}\&\mathbf{A_2}\&\mathbf{A_3})$-$\mathbf{A_2}$-$(\mathbf{A_1}\&\mathbf{A_3})$ when $i_a < 0$, as shown in Fig. 13(h), the FMSC of $\boldsymbol{S_{13}}$-$\boldsymbol{S_4}$-$\boldsymbol{S_3}$-$\boldsymbol{S_{12}}$ can be derived. Second, the mode in phase A is switched from II to I as i_q falling further. The current within phase A is transited from $(\mathbf{A_2}\&\mathbf{A_3})$ to $\mathbf{A_1}$ when $i_a < 0$, as shown in Fig. 13(i), the FMSC of $\boldsymbol{S_9}$-$\boldsymbol{S_2}$ can be found. Finally, i_q rises, the mode in phase A is switched from I to II when $i_a > 0$, the current within phase A is transited from $\mathbf{A_2}$ to $(\mathbf{A_1}\&\mathbf{A_3})$ as shown in Fig. 13(j), the FMSC of $\boldsymbol{S_4}$–$\boldsymbol{S_{11}}$ can be derived.

D. Comparison

The interleaved carrier-based method [1] and synchronized operation-based method [22] are selected to compared with the proposed flexible multimode control scheme with variable switching frequency in THD, efficiency, switching losses and resource consumption. To simplify the expression, the interleaved carrier-based method [1] is named as Method 1. The synchronized operation-based method [22] is named as Method 2. During comparison, inductance value of inductor connected with each IGBT half-bridge module remains 1 mH, the switching frequency of IGBT is set to 3 kHz, the dc bus voltage of parallel inverters is set to 100 V. The rotational speed of PMSM is set as 200 r/min. The parameter of PI controllers in FOC loop are shared in three control schemes.

The spectrum and THD comparison of i_a under different control strategy has been shown in Fig. 14. Compared with the other two control strategies, the proposed method has better suppression of the third harmonic over a wide current range. In condition of $i_{\text{peak}} = 2$ A (working mode I) and $i_{\text{peak}} = 5$ A (working mode II), the suppression effect of the proposed method on the fifth harmonic is between Method 1 and Method 2 as shown in Fig. 14(a) and (b). In THD comparison, when $i_{\text{peak}} = 2$ A, Method 2 has the lowest THD value in three control strategies. The operation sequence in working mode I increases the equivalent switching frequency from 3 to 9 kHz,

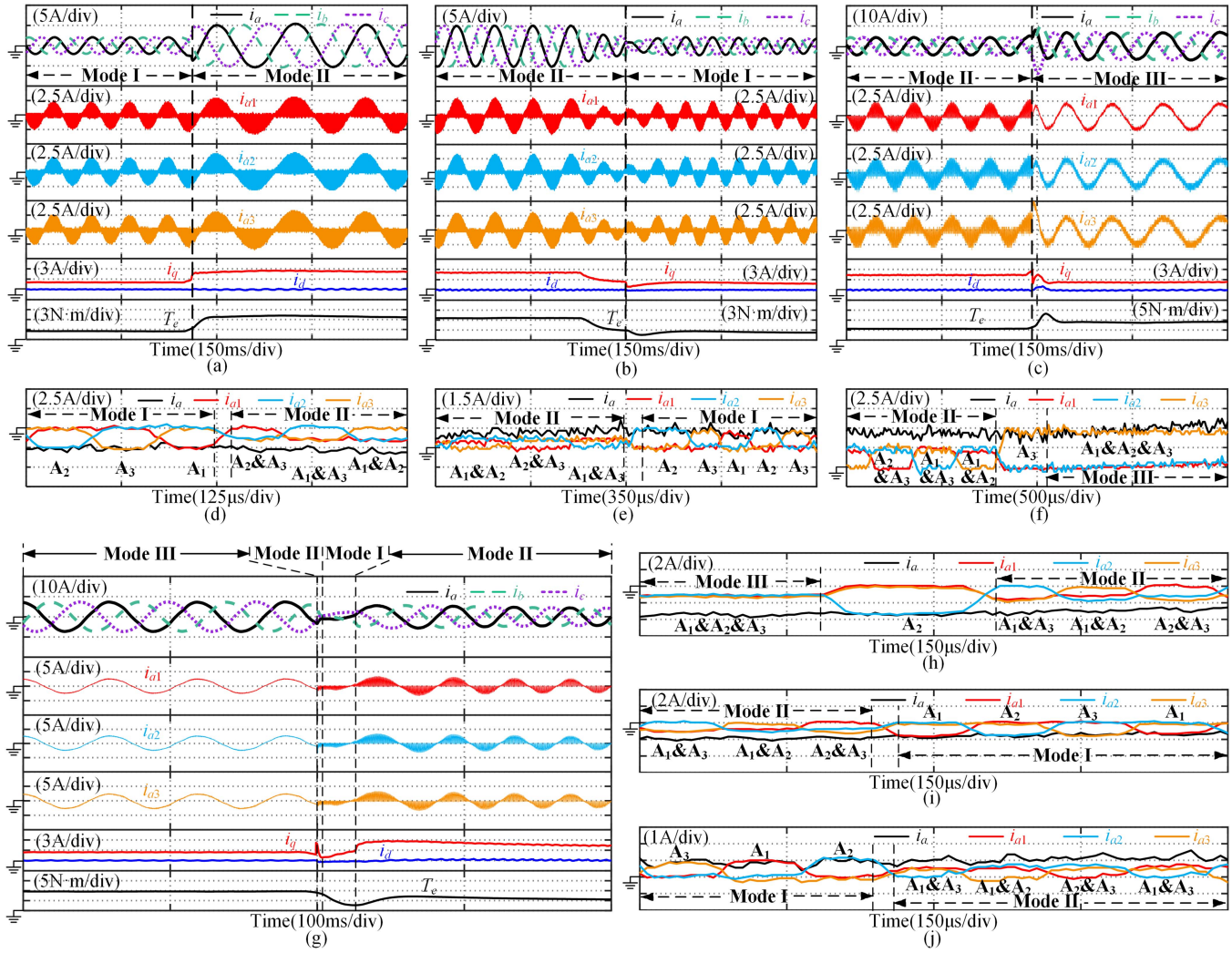

Fig. 13. Experimental current and torque waveforms during mode switching. (a) Mode I to mode II. (b) Mode II to mode I. (c) Mode II to mode III. (d) Details during mode I to mode II. (e) Details during mode II to mode I. (f) Details during mode II to mode III. (g) Mode III to mode II. (h) Details 1 during mode III to mode II. (i) Details 2 during mode III to mode II. (j) Details 3 during mode III to mode II.

TABLE VIII
COMPARISON OF SWITCHING LOSSES UNDER DIFFERENT CONTROL METHODS

i_{peak}	2 A	5 A	8 A
Method 1	9.12 W	10.33 W	11.53 W
Method 2	9.12 W	10.33 W	11.53 W
Proposed method	3.98 W (Mode I)	7.49 W (Mode II)	11.53 W (Mode III)

which reduces THD of i_a from 12.04% to 8.2%. When $i_{\text{peak}} = 5$ A, the VSI operation sequence in working mode II increases the equivalent switching frequency from 3kHz to 4.5kHz, which reduces THD of i_a from 5% to 4.25%. The THD of i_a under the proposed method and Method 1 are 4.25% and 4.40%, respectively. When $i_{\text{peak}} = 8$ A, the THD of i_a under Method 1 and proposed method is 2.95% and 3.78%, respectively.

According to (11)-(15), the switching losses under three control method can be calculated when $i_{\text{peak}} = 2$ A, $i_{\text{peak}} = 5$ A, and $i_{\text{peak}} = 8$ A, the results are listed in Table VIII. When $i_{\text{peak}} = 2$ A, the turn-OFF losses can be ignored due to ZCS in the working mode I, so the switching losses of semiconductor under proposed method is only 3.98 W. For the other two control scheme, turn-ON losses and turn-OFF losses need to be considered simultaneously. Therefore, when $i_{\text{peak}} = 2$ A, the switching losses under these two control methods is 9.12 W, which is higher than that under proposed method. When $i_{\text{peak}} = 5$ A, according to the analysis in Section II, a part of turn-ON losses can be ignored. Therefore, the difference between switching losses under the proposed method and the other two method becomes smaller. The switching losses under proposed method are 7.49 W. and the switching losses under the other two control methods are 10.33 W. When $i_{\text{peak}} = 8$ A, three control method have the same switching losses.

According to [14], the conductor losses of semiconductor and copper losses of inductor can be calculated. The input power of parallel inverters can be obtained from dc power supply. The efficiency results are given in Fig. 15. In the low current region, the efficiency of Method 1 is low. Due to the interleaved effect, the zero sequence circulate current (ZSCC) is unavoidable when

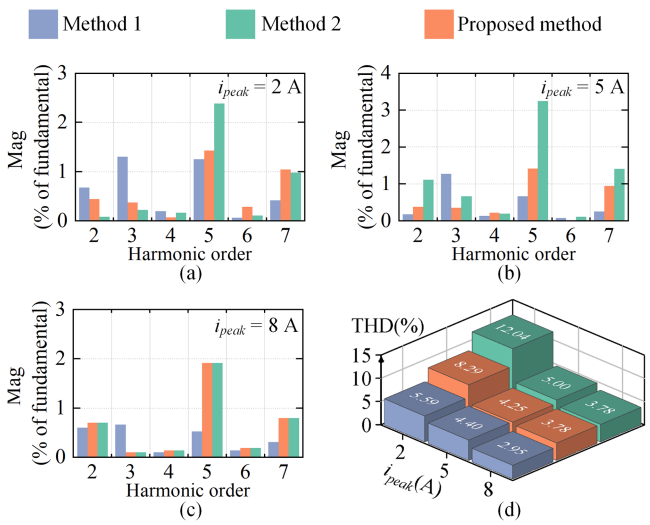

Fig. 14. Spectrum and THD comparison of i_a under different control strategies. (a) Spectrum comparison when $i_{\text{peak}} = 2$ A. (b) Spectrum comparison when $i_{\text{peak}} = 5$ A. (c) Spectrum comparison when $i_{\text{peak}} = 8$ A. (d) THD comparison.

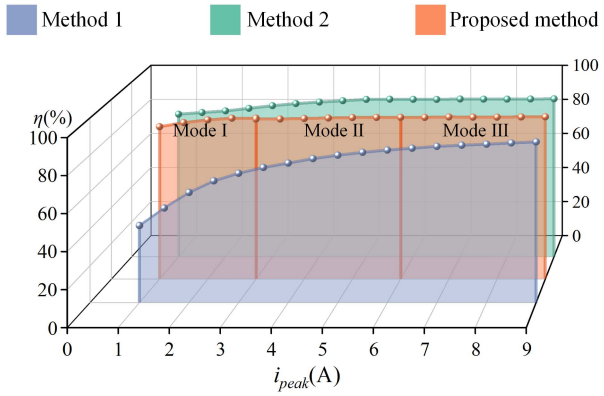

Fig. 15. Efficiency of parallel inverters under different control strategies.

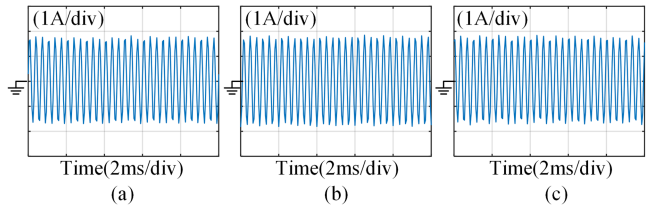

Fig. 16. Measured waveforms of ZSCC in Method 1. (a) $i_{\text{peak}} = 2$ A. (b) $i_{\text{peak}} = 5$ A. (c) $i_{\text{peak}} = 8$ A.

different zero vectors coexist in each phase, which degrades the efficiency. The measured value of ZSCC fluctuates between ± 1.9 A in full i_{peak} region, as shown in Fig. 16. Therefore, in low i_{peak} region, the low efficiency under Method 1 can be anticipated. For the proposed method and Method 2, there is no co-occurrence of different zero voltage vectors in each phase, the additional losses caused by ZSCC are avoided, so efficiency of these two methods are more than 81% in full current range. In current interval [1 A, 3 A], the average efficiency under proposed method is 86.2%, while the average efficiency under Method 2 is 83.76%. In current interval [3, 6 A], the average efficiency under proposed method is 89.6%, while the average efficiency under Method 2 is 88.8%. it can be seen that, the efficiency under proposed method is higher than that under Method 2 in current interval [1, 6 A] due to ZCS.

TABLE IX
COMPARISON OF RESOURCE CONSUMPTION UNDER DIFFERENT CONTROL STRATEGIES

item	Method 1	Method 2	Proposed method
Number of current sensors	9	3	3
Number of consumed logic elements in FPGA	2610	2200	1500
IP used in FPGA	PLL, LPM_Divide	PLL	PLL

The resource consumption under different control strategies is listed in Table IX. The Method 1 consumes more resources in hardware than the other two control methods. Meanwhile, CC in Method 1 is inevitable, which causes degradedness of system efficiency as shown in Fig. 15. As the number of parallel inverters rises, more current sensors are needed in Method 1. For the proposed method, the numbers of current sensors are fixed and do not vary with the number of parallel inverters, which means low resource consumption and high reliability.

E. Ablation Study

To systematically investigate the influence of proposed flexible mode-switching strategy and designed current balance strategy on system performance, four conditions are preset in ablation study. To simplify expression, the proposed flexible mode-switching strategy is named as factor 1, and designed current balance strategy is named as factor 2. In ablation study, working mode is transited from I to II. The experimental results of ablation study are given in Fig. 17. According to Fig. 17(c) and (d), the current is transited from $\mathbf{A_1}$ to ($\mathbf{A_2}$&$\mathbf{A_3}$) in one T_{carrier} with factor 1. Without factor 1, the current cannot be transited to ($\mathbf{A_2}$&$\mathbf{A_3}$) at once and caused additional turn-ON losses. According to Li et al. [14], the switching loss can be calculated. The switching losses in Fig. 17(d) is 16.3 mW with factor 1, while switching losses in Fig. 17(c) is 26.9 mW without factor 1. By applying factor 1, the switching losses during mode transition have been reduced by 39%. Without factor 1, it takes five T_{carrier} to reach current balance, while it takes only one T_{carrier} to reach current balance with FMSC. By applying factor 1, the transient process of the current on parallel legs is shortened by 75%. According to Fig. 17(b) and (d), the maximum current difference between the two parallel legs is only 0.4 A with factor 2. Without factor 2, the maximum current difference between two parallel legs is 2.4 A. Therefore, the experimental results of ablation study have illustrated the effectiveness and necessity of factor 1 (proposed flexible mode-switching strategy) and factor 2 (designed current balance strategy).

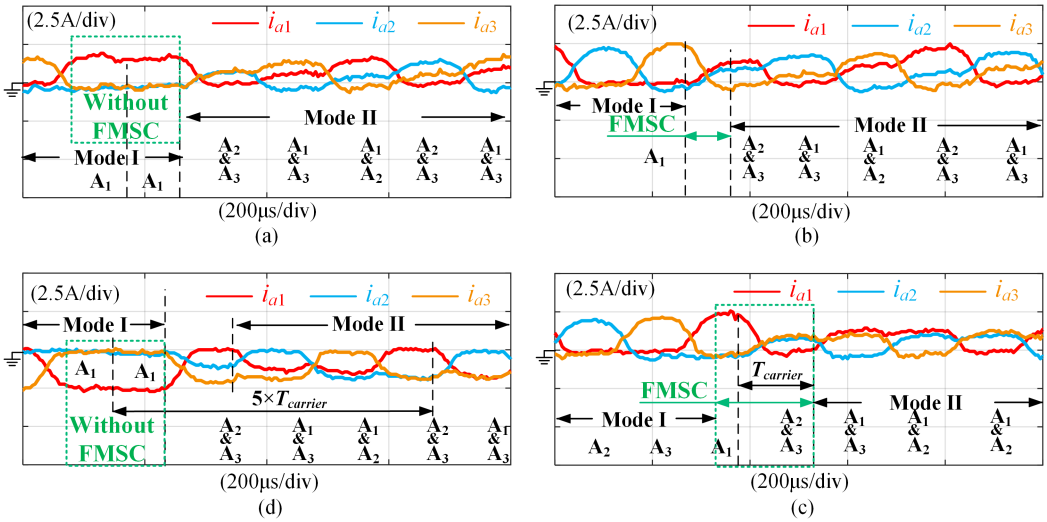

Fig. 17. Experimental results of ablation study. (a) Without factor 1 and factor 2. (b) Only With factor 1. (c) Only with factor 2. (d) With factor 1 and factor 2.

V. Conclusion

In this article, a flexible muti-mode control scheme with variable switching frequency for parallel interleaved three-phase inverters is proposed. The proposed scheme is verified on three parallel inverters fed PMSM drives with three current sensors. Experimental results validate the effectiveness of the proposed control scheme. The main contributions of this article are summarized as follows.

1) The current balancing strategy and the corresponding $\boldsymbol{S}$ sequences are proposed in working mode II to ensure the current balance on parallel VSIs.
2) The flexible mode-switching strategy based on FMSC are developed to ensures that mode switching is accomplished in two carrier cycles.
3) There is only one FOC loop in the proposed scheme. The allocation rules of drive pulses are modified instead of modulation strategy to realize the multi-inverter control, which simplifies the structure of control scheme.
4) For the N (N>3) parallel VSIs, the proposed scheme does not require additional FOC loop, nor does additional current sensors for each parallel legs, which shows the advantage of easy expandability.

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