Letters

A Fast-Transient One-Shot Droop Recovery Digital LDO With Reinforcement-Learning Droop Compensation for D2D Interfaces

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***Abstract*—This letter presents a digital low-dropout regulator featuring a one-shot voltage droop recovery and an ultrafast settling time of 8 ns, achieved through reinforcement-learning-based self-adaptive compensation (RL-SAC). The RL-SAC performs real-time background learning to identify the optimal current required to compensate for a given voltage droop. By iteratively learning the voltage droop, the RL-SAC enables the one-shot droop recovery, ensuring instant stabilization of the output voltage. A prototype was fabricated in a 40-nm CMOS process with an on-chip output capacitor of 100 pF. The prototype supports an input voltage V_{IN} range from 0.4 to 0.9 V. Measurement results demonstrated a droop settling time of 8 ns and a voltage droop of 145 mV against a load current step of 102 mA/ns at V_{IN} of 0.8 V and V_{OUT} of 0.75 V.**

***Index Terms*—Asynchronous, chiplet system, event-driven, fast transient response, low-dropout regulator (LDO), one-shot droop recovery, reinforcement-learning-based self-adaptive compensation (RL-SAC).**

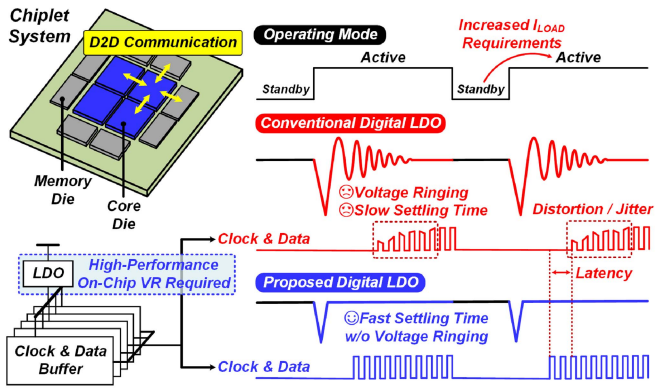

Fig. 1. Conceptual illustration showing requirement for high-performance LDOs in chiplet systems, due to voltage droop caused by standby-to-active mode transitions in D2D communication.

I. Introduction

In MODERN chiplet systems, dynamic switching between active and standby modes in die-to-die (D2D) communication is employed to enhance power efficiency. However, transitions from standby to active mode can induce abrupt increases in load current leading to significant voltage droop. As illustrated in Fig. 1, if the supply voltage does not recover promptly, then supply-sensitive components, such as data and clock buffers, may suffer from distortion, jitter, or increased latency, potentially resulting in functional errors. Therefore, rapid and accurate voltage droop recovery becomes essential to ensure reliable data and clock delivery, as well as to meet chiplet system latency requirements necessitating a high-performance on-chip voltage regulator. Digital low-dropout regulators (DLDOs) are considered a suitable solution because of their low input voltage operation, low dropout voltage, and fast transient response. Nevertheless, DLDOs face challenges, such as limited transient response due to clock frequency and steady-state limit cycle oscillations caused by current quantization error.

Several schemes for DLDOs targeting fast transient responses have been proposed. Among them, event-driven approaches [1], [2], [3], [4], [5] have been introduced, which detect voltage droop asynchronously and respond quickly. Despite fast initial compensation, it often results in ripple in output voltage during the subsequent regulation phase. In response to this limitation, a computational DLDO [6] has been proposed, which quantizes the voltage droop over a specified period and calculates the number of digital pass gates (DPGs) required for compensation. This computational technique enables rapid droop recovery, but it still has several limitations, including the need for a high-frequency clock due to synchronous computation [7], [8], [9], [10], voltage ripple caused by computation error, and increased

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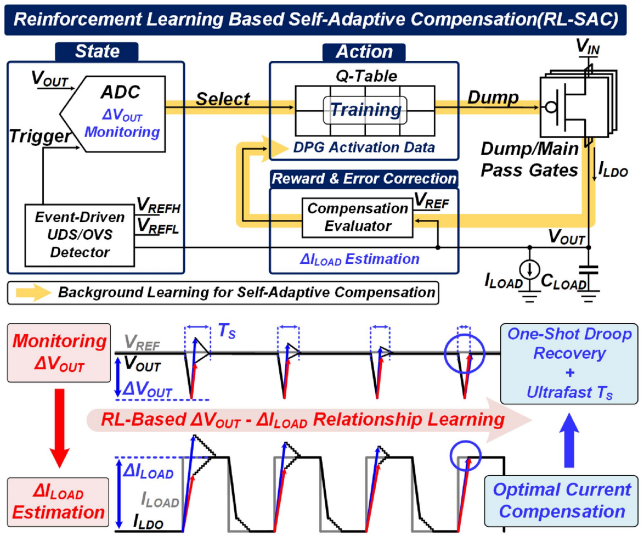

Fig. 2. Conceptual block diagram of proposed DLDO and operational principle of RL-SAC.

implementation complexity. Recently, a command-aware compensation scheme [11] was proposed, in which DPG activation is triggered by predefined control signals associated with load circuit operations. Although this method enables ultrafast droop response, it depends on an application-specific load profile, which restricts compensation to fixed values and limits adaptability to varying droop magnitudes and load current conditions.

To address these challenges, this letter presents a one-shot droop recovery DLDO with reinforcement-learning-based self-adaptive compensation (RL-SAC). The proposed RL-SAC employs reinforcement learning to associate the output voltage droop with the corresponding amount of required compensation current, and stores this learned relationship in a Q-table. By referencing the Q-table, the RL-SAC can rapidly infer the optimal number of DPGs to activate in response to a given voltage droop, enabling accurate one-shot recovery without the output voltage ripple and a high-frequency clock.

The rest of this letter is organized as follows. Section II introduces the overall architecture of the proposed DLDO. Section III describes the circuit implementation, and Section IV explains the measurement results. Finally, Section V concludes this letter.

II. Proposed Architecture

Fig. 2 shows the conceptual block diagram and the operational principle of the DLDO. The RL-SAC learns the output voltage variations caused by changes in load current ΔI_{LOAD} through the reinforcement learning. By leveraging this approach, the RL-SAC infers ΔI_{LOAD} from the given output voltage variations and compensates for the current variation in a single step, thus achieving a fast transient response. The RL-SAC senses a change in output voltage ΔV_{OUT} using an event-driven undershoot (UDS) and overshoot (OVS) detector. The following ADC quantizes ΔV_{OUT}, and the RL-SAC controller applies the trained control data for DPGs to compensate for the ΔI_{LOAD}. Because ADC output data play the role of an index of trained data by RL-SAC, there is no additional computing process to handle ΔV_{OUT}. From sensing ΔV_{OUT} to the DPG control, all procedures are carried out asynchronously without dependence on the operating clock frequency. As a result, the proposed DLDO can offer an ultrafast transient response.

The overall architecture of the proposed DLDO is shown in Fig. 3(a). The DLDO comprises four subsystems: 1) state, 2) action, 3) reward, and 4) error correction in the same manner with the reinforcement learning process. The state subsystem performs low-latency sensing of ΔV_{OUT} using the event-driven UDS/OVS detector and the self-triggering domino ADC [3], [4]. The action subsystem executes coarse-fine regulation via RL-SAC. Dump and main DPG arrays are composed of coarse and fine DPG arrays, respectively. The reward subsystem assesses compensation accuracy, with the controller updating the Q-table based on the evaluation. In the error correction subsystem, the subrange linear search block addresses residual V_{OUT} errors until the Q-table is trained accurately.

Fig. 3(b) shows the detailed RL-SAC operations. The domino ADC quantizes ΔV_{OUT} to ADC_OUT, and the Q-table selects the trained DPG control data providing optimized ΔI_{LOAD} compensation for the given ADC_OUT. The selected DPG control data are applied to the dump DPGs through the dump register, immediately compensating for ΔI_{LOAD}. The Q-table controller evaluates compensation accuracy and updates the Q-table to minimize V_{OUT} regulation error, learning the relationship between ΔV_{OUT} and ΔI_{LOAD}. After iterative training, the DPG control data in each Q-table align with ΔI_{LOAD}, achieving the one-shot droop recovery. To support these operations, the underlying structure of the Q-table and DPG arrays is organized to enable fast and adaptive compensation. The Q-table is structured with eight states and 32 actions, where the ADC-quantized state index is used to select a specific row in the table. Each row consists of 32 actions, and each action represents DPG activation data for 32 dump DPG cells, enabling rapid droop compensation through the dump DPGs. Both the Q-table and the dump DPG array are implemented in separate coarse and fine paths. The coarse path provides fast, large-step current compensation immediately after droop detection, while the fine path allows more precise adjustments within each coarse level. After this initial dump compensation, the Q-table controller evaluates the remaining regulation error, and additional residual compensation is applied through the main DPG array, which also consists of 32 DPG cells. Similar to the dump path, the main DPG array is also divided into coarse and fine stages to support both large-step and fine-grained regulation in the postcompensation phase. To further assess the effectiveness of Q-table updates in mitigating regulation error, the proposed dual-resolution Q-table-based approach is quantitatively compared with a design relying on finer ADC quantization. In this architecture, one coarse DPG step corresponds to approximately 20 fine DPG steps. Although the fine DPG consists of 32 steps, its range is deliberately extended to ensure seamless regulation across state boundaries. As a result, the control logic effectively maps 8 voltage states to 640 equivalent regulation levels. Achieving this resolution solely through ADC quantization would require more than 9 bits for

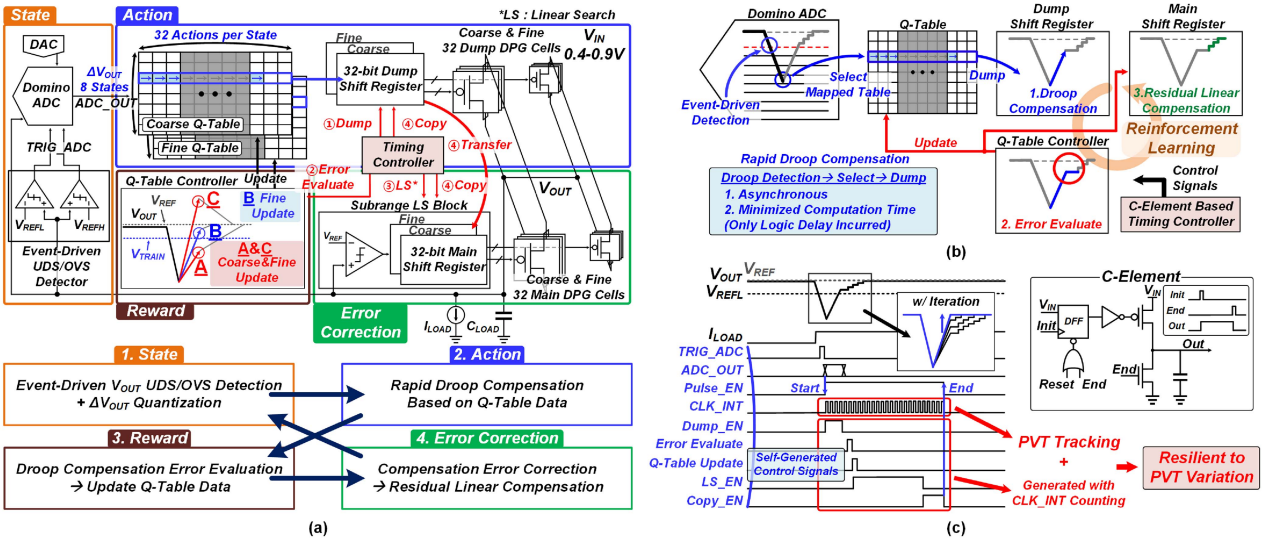

Fig. 3. (a) Overall architecture of proposed DLDO. (b) Operational principle. (c) Timing diagram of RL-SAC.

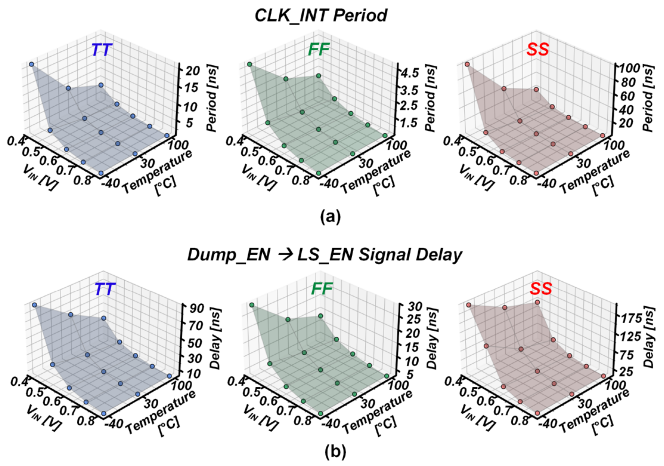

Fig. 4. Postlayout simulation results showing (a) self-adjusting period of CLK_INT and (b) delay between Dump_EN and LS_EN signals under PVT variation.

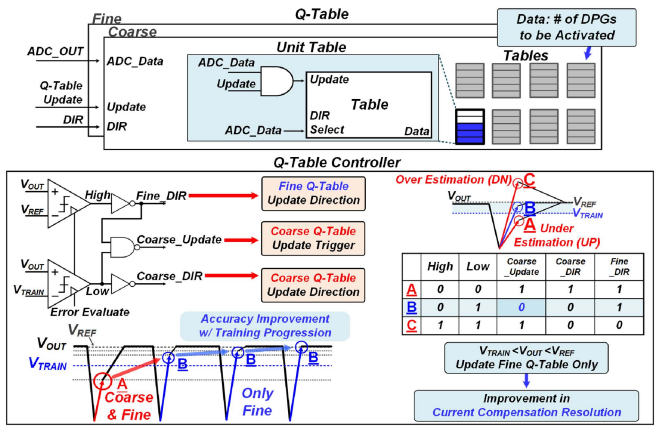

Fig. 5. Circuit implementation of Q-table and its controller.

high-resolution conversion and associated calibration circuits, resulting in significantly increased implementation complexity.

Fig. 3(c) shows the timing diagram of the RL-SAC operations. The timing diagram shows the asynchronous operation that allows the ultrafast transient response. Using C-element circuits, the asynchronous control signals are self-generated without an external high-frequency clock. The self-generated clock CLK_INT tracks process, voltage, and temperature (PVT) variations, and other control signals are generated by counting CLK_INT. Consequently, the RL-SAC operation demonstrates resilience to these variations by leveraging self-adaptive compensation integrated with the learning process. Fig. 4 presents the postlayout simulation results that demonstrate the PVT-tracking behavior of CLK_INT. To evaluate its sensitivity to PVT variations, the delays of the asynchronous control logic were also simulated under various operating conditions. At the slow process corner, the delay between Dump_EN and LS_EN increased, accompanied by a longer period of CLK_INT. In contrast, at the fast process corner, both the control logic delay and the CLK_INT period decreased. The same behavior was observed under variations in voltage and temperature as well. These results confirm that CLK_INT dynamically adjusts its timing in response to PVT-induced variations, maintaining consistent internal control signal coordination.

III. Circuit Implementation

Fig. 5 shows the circuit implementation of the Q-table and its controller. The Q-table is divided into coarse and fine tables, each mapping ADC_OUT values to the corresponding number of DPGs to activate. The controller updates the Q-table by evaluating the accuracy of the compensation. Based on the evaluation of the compensated V_{OUT} with V_{REF} and V_{TRAIN}, both the coarse Q-table and the fine Q-table are updated, or only the fine Q-table is updated to improve the compensation accuracy by adjusting the dump DPG control data.

Fig. 6 depicts the operational principle of the dump shift register (SR) and the main SR. The coarse-fine dump registers update

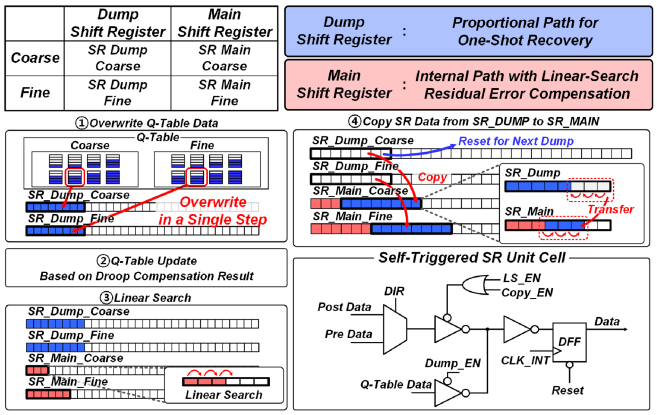

Fig. 6. Data flow in Q-table for RL-SAC and circuit implementation of asynchronous register unit for Q-table.

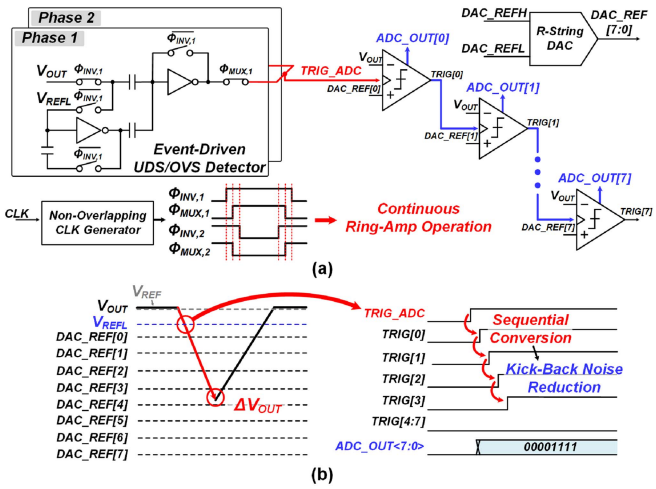

Fig. 7. (a) Circuit implementations. (b) timing diagram of event-driven UDS/OVS detector and domino ADC.

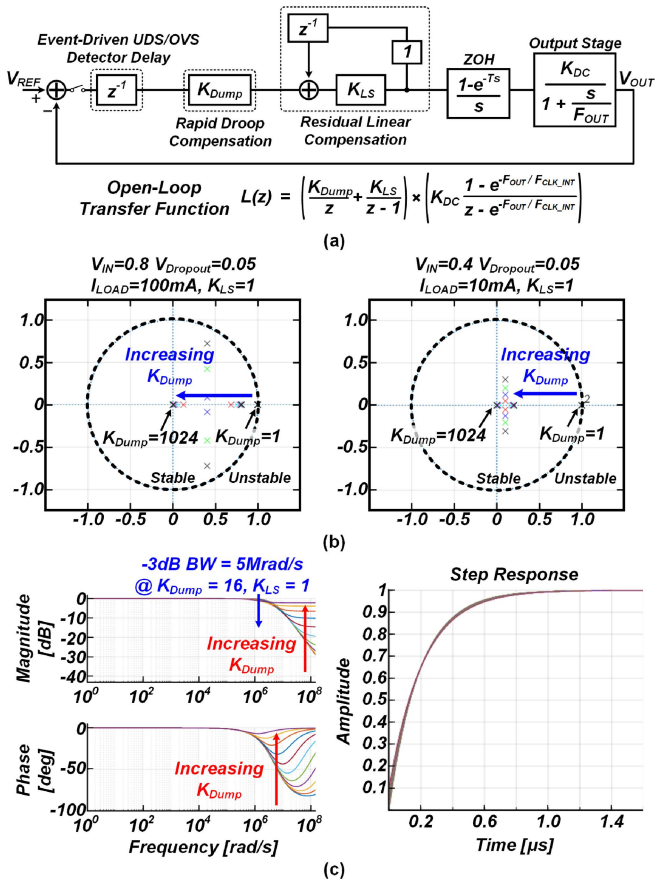

Fig. 8. (a) Discrete-time control model of proposed DLDO. (b) z-domain pole locations of corresponding open-loop transfer function for varying K_{Dump}. (c) Frequency-domain and time-domain bandwidth analysis of proposed DLDO under closed-loop control.

the dump DPG control based on ΔV_{OUT} and corresponding Q-table data. The linear-search regulation compensates for any residual error using the main SR after the reward procedure. Once the regulation is complete, the updated dump SR data are transferred to the main SR to preserve the compensation result and prepare it for overwriting new data when another voltage droop occurs.

Fig. 7(a) and (b) shows the circuit implementations and timing diagram of the event-driven UDS/OVS detector and domino ADC, respectively. The UDS/OVS detector employs a time-interleaved ring amplifier [12] functioning as a continuous-time comparator [5]. When the output voltage exceeds the thresholds, a trigger signal TRIG_ADC is generated to activate the domino ADC, initiating ΔV_{OUT} quantization. The domino ADC sequentially compares V_{OUT} with a series of reference voltages from an R-string DAC that operates in a domino-like manner. Since faster response leads to earlier compensation, the ADC operates in an event-driven manner, where prompt voltage droop detection by the UDS/OVS detector enables early activation of the quantization process, minimizing overall delay. The shorter quantization latency advances the initiation of droop compensation, which can contribute to improved transient performance.

Fig. 8(a) illustrates the discrete-time control model of the proposed DLDO and its open-loop transfer function derived for stability analysis. The model consists of an event-driven UDS/OVS detector, a rapid droop compensation path through the dump DPG driven by Q-table data, and a linear residual compensation path through the main DPG, followed by a zero-order hold and a continuous-time output stage. $F_{CLK\cdot INT}$ and F_{OUT} represent the equivalent operating frequencies of the compensation controller and output pole, respectively. The output stage gain K_{DC} corresponds to the current conversion ratio of the power stage. The rapid droop compensation and residual linear compensation paths are modeled with K_{Dump} and K_{LS}, which represent the gain of each control stage. The detector delay is represented by a one-clock delay to capture the response latency of the event-driven comparator logic. Using this discrete-time model, stability analysis of the proposed DLDO was performed, as shown in Fig. 8(b). Pole-zero analysis was conducted under V_{IN} of 0.4 and 0.8 V with I_{LOAD} of 10 and 100 mA, respectively. Since K_{Dump} is adaptively adjusted through reinforcement learning during Q-table updates, it can vary significantly depending on the learned compensation behavior. To reflect this variability, the compensation gain K_{Dump}

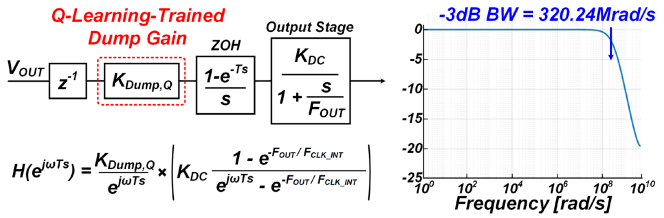

Fig. 9. Feedforward transfer function model and corresponding frequency-domain bandwidth analysis of proposed DLDO after learning.

was swept from 1 to 1024 in powers of two, with K_{LS} set to 1. This wide sweep ensures that stability is maintained across the full range of K_{Dump} values during learning. Even as K_{Dump} increases to enable faster compensation, the poles remain within the unit circle in the z-domain, confirming that the control loop maintains stability. These results indicate that the proposed RL-SAC maintains stable operation across wide voltage and load conditions, even with rapid compensation.

Figs. 8(c) and 9 show the behavioral model of the proposed DLDO for bandwidth analysis during two distinct operating phases, respectively: 1) the Q-learning-based adaptive control phase and 2) the postconvergence phase, where the system operates in feedforward-only mode. To analyze the transient response behavior of the proposed DLDO, both the closed-loop model during Q-learning and the feedforward model after Q-learning completion were evaluated. In the learning phase, a discrete-time closed-loop system was modeled using the feedback structure, including dump and linear compensation. As K_{Dump} is adaptively varied throughout the Q-learning process, it was swept from 1 to 1024 in powers of two to reflect its dynamic behavior during learning. Frequency-domain analysis showed a -3 dB bandwidth of 5 Mrad/s in a representative case with K_{Dump} set to 16, and time-domain step response confirmed stable settling without OVS within 1 μs. After Q-learning is completed and one-shot compensation becomes possible, the DLDO operates using a feedforward-only path with a fixed dump gain. This gain, denoted as $K_{Dump,\,Q}$, is selected directly from the pretrained Q-table after the Q-learning process has converged. In this phase, a simplified model was constructed by removing the feedback path, and the -3 dB bandwidth was measured to be significantly increased to 320.24 Mrad/s.

IV. Measurement Results

The prototype of the proposed DLDO was fabricated using a 40-nm CMOS process, occupying an active area of 0.048 mm^2 with an on-chip output capacitor of 100 pF. Fig. 10(a) shows the die photomicrograph of the prototype. Fig. 10(b) shows the measured current efficiency, achieving a peak current efficiency of 99.74%.

Fig. 11 shows the measured load transient responses. At a V_{IN} of 0.8 V, the prototype achieved a settling time of 8 ns and a voltage droop of 145 mV for a current step of 102 mA/ns. Owing to the fast transient response, the proposed DLDO can support load current toggling up to tens of MHz, indicating the potential applicability to high-frequency load transient environments,

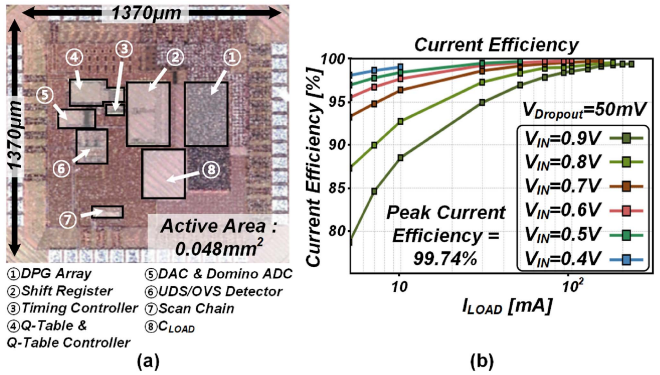

Fig. 10. (a) Die photomicrograph of fabricated DLDO. (b) Measured current efficiency.

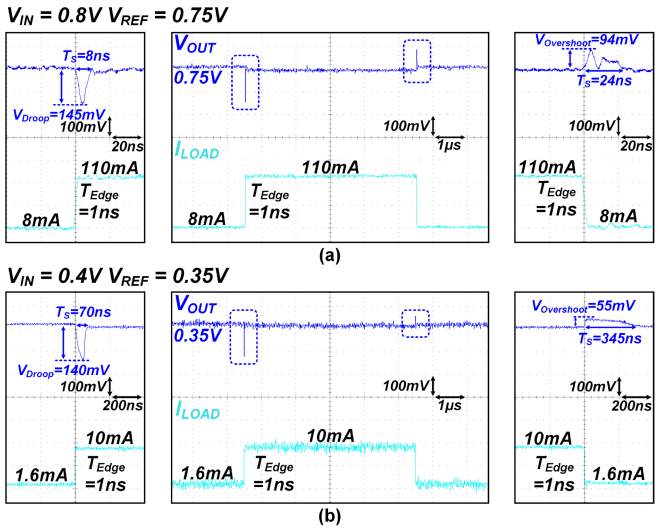

Fig. 11. Measured load transient responses at V_{IN} of (a) 0.8 and (b) 0.4 V.

which typically require fast voltage regulation in response to sub-MHz DVS frequency [14], [15]. For low V_{IN} of 0.4 V, the prototype demonstrated a settling time of 70 ns for a current step from 1.6 to 10 mA with an edge time T_{Edge} of 1 ns. The increased settling time at the V_{IN} of 0.4 V is mainly attributed to the extended digital logic delay in the asynchronous control path, as shown in Fig. 4.

Fig. 12 shows the measured load transient improvements by the RL-SAC, where the settling time and V_{OUT} error decrease as it learns the relationship between ΔV_{OUT} and ΔI_{LOAD}. The RL-SAC achieved 78% reduction in settling time and 95% decrease in voltage error after the one-shot droop recovery. Fig. 13(a) and (b) shows the measured load regulation up to 250 mA and the line regulation across a V_{IN} range from 0.4 to 0.9 V, respectively.

Table I presents the performance summary and comparison with the state-of-the-art works. The proposed DLDO achieves the ultrafast settling time of 8 ns without relying on the high-frequency clock, except for the only 100 kHz clock used in the continuous-time comparator. It also delivers a rapid transient response even at a low V_{IN} of 0.4 V, enabling energy efficient power management of chiplet systems. To reflect fast transient

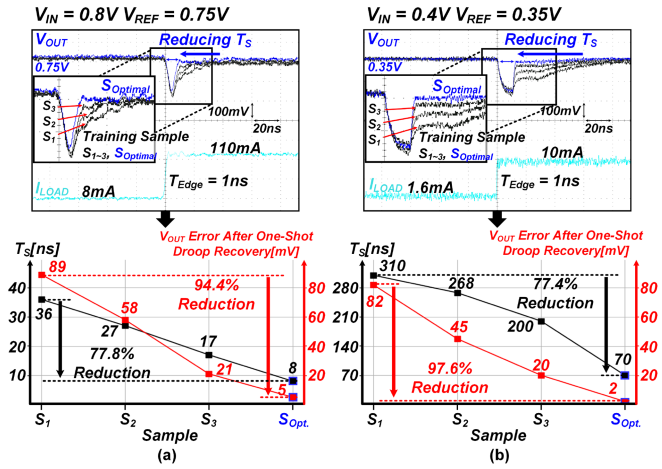

Fig. 12. Measured improvements in voltage droop and settling time during RL-SAC learning process at V_{IN} of (a) 0.8 and (b) 0.4 V.

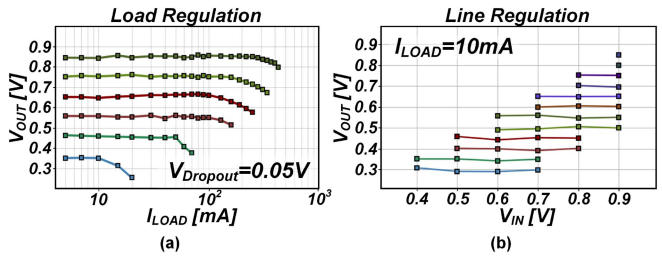

Fig. 13. Measured (a) load regulation and (b) line regulation.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Paper	This Work		ISSCC 2020 [12]		JSSC 2020 [7]	TPEL 2022 [5]	ISSCC 2024 [9]	TPEL 2024 [10]
Process [nm]	40		40		22	40	3 (GAAFET)	65
Type	Digital		Analog		Digital	Digital	Digital	Digital
Control Method	RL, Asynchronous		Ring Amplifier		Computational	Event-Driven	Computational ,Distributed	Computational
V_{IN} [V]	0.4 - 0.9		0.4 - 1.2		0.55 - 1.2	0.6 - 1.2	0.6 - 1.1	0.6 - 1.2
V_{OUT} [V]	0.3 - 0.85		0.2 - 1.18		0.5 - 1.15	0.55 - 1.15	0.55 - 1.12	0.55 - 1.15
$V_{Dropout,MIN}$ [V]	0.05		0.05		0.05	0.05	0.05	0.05
C_{LOAD} [nF]	0.1		0.09		7	0.15	320	0 - 0.01
$I_{LOAD,MAX}$ [mA]	250		400		2000	200	10000	26
I_Q [µA]	90 - 1340		4.4 - 1280		2400	6 - 550	18170	102 - 167
Peak Current Efficiency [%]	99.74		99.96		99.9	> 99.7	99.82	99.6
F_{CLK} [MHz]	0.1		N/A		1	1	500 - 1000	20
Measured V_{IN} / V_{OUT} [V]	0.8 / 0.75	0.4 / 0.35	1 / 0.9	0.4 / 0.35	1 / 0.95	1 / 0.95	0.82 / 0.77	0.6 / 0.55
V_{Droop} [mV] @ ΔI_{Step} [mA]	145 @102	140 @8.4	45 @200	78 @1.04	100 @500	140 @104.2	94 @6500	140 @26
T_{Edge} [ns]	1	1	10	10	0.25	1	1	20
Droop T_S [ns]	8	70	25	500	15	16	100*	95
[1]FoM_1 [ps]	1.03		0.06		6.70	1.06	12.94	0.35
[2]FoM_2 [ps]	4.66		32.22		7.32	3.70	14.33	64.58

*Estimated from measurement result.
[1]$FoM_1 = C_{LOAD}\cdot(V_{Droop}/\Delta I_{Step})(I_Q/\Delta I_{Step})$. Smaller FoM is better.
[2]$FoM_2 = (C_{LOAD}\cdot V_{Droop}/\Delta I_{Step}+\Delta I_{Step}/(2\cdot SR))\cdot(I_Q/\Delta I_{Step})$ [13]. Smaller FoM is better.

behavior, the proposed DLDO was evaluated with a T_{Edge} of 1 ns, corresponding to a slew rate of 102 mA/ns. In contrast, the authors in[10] and [12] used T_{Edge} of 20 and 10 ns, corresponding to slew rates of 1.3 and 20 mA/ns, respectively. While FoM_1 of this work is slightly lower than those of [10] and [12], this difference primarily results from the more stringent transient test conditions.

V. CONCLUSION

This letter presented a reinforcement-learning-based DLDO that achieves ultrafast one-shot droop recovery. By incorporating RL-SAC, the proposed DLDO dynamically learns the optimal current required for each voltage droop scenario, enabling rapid and precise voltage droop recovery. The RL-SAC operation showed significant improvements in the settling time and V_{OUT} error after one-shot droop recovery through continuous Q-table training. The DLDO achieves a fast settling time of 8 ns against a 102 mA/ns load current step at V_{IN} of 0.8 V.

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