Reliability Enhanced Fault-Tolerant Full-Bridge Modular Multilevel Converters Using Reconfiguration During Open-Circuit Failures

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***Abstract*—Modular multilevel converters (MMCs) are widely used in various applications due to their scalability, efficiency, and fault-tolerant capabilities. This article proposes a fault-tolerant methodology tailored for full-bridge (FB) submodules (SMs) in MMCs to enhance system reliability under open-circuit faults (OCFs) in insulated-gate bipolar transistors (IGBTs). The method adopts a hybrid approach, using control logic adjustments to reconfigure faulty SMs into half-bridge (HB) configuration for T2/T3 faults while employing redundant SMs for T1/T4 faults. Accurate fault detection and localization are achieved through established methods, such as state observers and voltage comparisons. It is shown using MCS that the proposed method can improve the 17 kV 10 MVA converter reliability by almost 25% over solely redundancy-based solution for given lifetime requirements. Finally, using a lab-scale FB MMC prototype, it is experimentally shown that the proposed reconfiguration technique can successfully localize the fault and revert to normal operating requirements by shifting from FB to HB SM configuration in approximately 20 ms of fault initiation.**

***Index Terms*—Fault tolerance, modular multilevel converter (MMC), reconfigurability, redundancy.**

I. Introduction

MODULAR multilevel converters (MMCs) are preferred topologies for many applications due to their reliability, efficiency, fault tolerance, performance, and modularity [1], [2], [3]. Since the invention of this technology, many literature works have addressed various aspects of MMC, including control, reliability, design, submodules (SMs), configurations, fault-tolerance, redundancy, and cost-efficient design [4], [5].

In most of the studies, the configuration of the SM is considered to be half-bridge (HB) due to its cost-effectiveness. However, many SM proposals and other SM configurations exist, among which the full-bridge (FB) is the most competitive option to handle dc link short-circuit faults [6]. Table I provides an overview of the existing MMC topologies with different SM configurations [6].

TABLE I
Commercially Available MMC Technologies

Manufacturer	Product Name	SM topology
Siemens	HVDC Plus	HB/FB
GE/Alstom	HVDC MaxSine	HB/FB
ABB	HVDC Light	HB
CEPRI	HVDC Flexible	HB

Since the FB SM will double the number of power electronics semiconductors, the capital cost of the MMC increases [7]. For this purpose, hybrid MMCs were introduced, where almost 60% of the SMs were configured as FB, and the rest as HB, to tolerate the dc link fault while reducing the capital cost [8]. There are also redundant SMs to tolerate the open-circuit fault (OCF) in the insulated-gate bipolar transistors (IGBTs) by bypassing the faulty SMs [6], [9]. Li et al. [10] achieved fault detection and localization for FB MMC using simulated capacitor voltage deviations. Zhou et al. [11] proposed the voting theorem concept to detect and localize the faulty IGBT SM. The hot-redundant redundancy concept is introduced in [12] to achieve fault-tolerant operation. Methods in [13] provided a complete flowchart of fault detection, localization, and tolerance by applying hot-redundant redundancy. Li et al. [14] achieved fault-tolerant operation of the MMC by using redundancy, while the modulation control strategy is adapted accordingly.

Fault-tolerant strategies for cascaded H-Bridge multilevel converters (CHBMCs) have been extensively studied. Xie et al. [15] introduced a constraint-based fault-tolerant control for CHBMCs, while [16] proposed a fast fault detection and localization algorithm for multiple open-switch faults. Raki et al.[17] developed a safe, fault-tolerant strategy for CHBMCs, and Wang et al.[18] presented a model predictive control for fault tolerance and power balancing.

Liu et al. [19] proposed a localization method based on a mathematical model. In [20], fault tolerance and ride-through operation are achieved by applying a novel operation scheme for medium-voltage applications. Yang et al. [21] proposed a fault-tolerance operation by alerting the control system to the measurements and sensors for SMs' capacitor voltage measurement.

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TABLE II
COMPARISON OF FAULT DETECTION, LOCALIZATION, AND REDUNDANCY METHODS

Ref	FD†	FL‡	FT*	Redundancy	SM	HC§
[21]	✓	✓	✓	k-out-n/load-sharing	HB	Yes
[20]			✓	k-out-n/load-sharing	HB	No
[14]			✓	load-sharing	HB	No
[13]	✓	✓	✓	k-out-n	HB	No
[12]			✓	k-out-n	HB	No
[11]	✓	✓		-	FB	No
[10]	✓	✓	✓	k-out-n	FB	No
[22]	✓			-	HB	Yes
[23]			✓	k-out-n	HB	No
[24]		✓		-	HB	No
[25], [26]	✓	✓		-	HB	No
[27]	✓	✓	✓	k-out-n	HB	No

† Fault Detection ‡ Fault Localization * Fault Tolerance
§ Hardware Changes

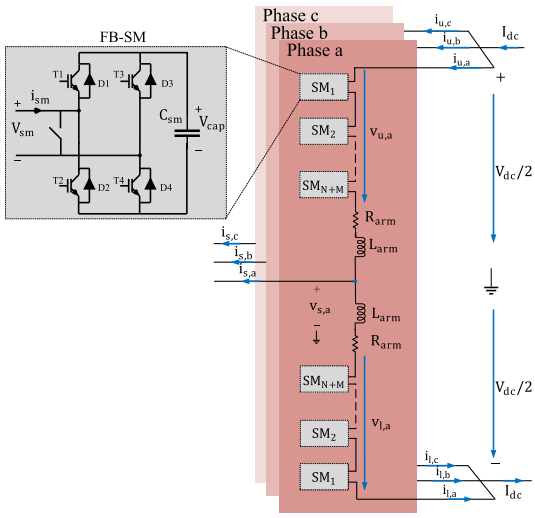

Fig. 1. MMC configuration with FBSM.

Liu et al. [22] proposed a detection method under light-load conditions of the MMC, where a variance parameter is applied to achieve precise fault detection. Razani et al. [23] proposed a fault-tolerance strategy in dc/dc MMC. Liu et al. [24] proposed a fault localization strategy for MMC, which is applicable when the MMC operates as an inverter (ac/dc) or rectifier (ac/dc). An overview of some relevant literature is provided in Table II.

As previously discussed, many studies address the OCF, ranging from detection concepts to localization and fault tolerance. In this study, it is proposed that FB to HB SM reconfiguration can be achieved to enhance the reliability of such fault tolerant FB MMCs.

The configuration of the MMC with FB SM is shown in Fig. 1. Fault tolerance should ensure continued operation in the event of an OCF in any of the four power electronic switches in the depicted SM. The proposed algorithm in this study aims to achieve OCF ride-through by selectively either applying reconfiguration from FB to HB or introducing redundant SMs, depending on the specific fault location obtained from the detection algorithm. As a consequence, the postfault operability of remaining components in the system is maximized, thus enhancing the reliability of the system over its useful lifetime. The main contributions of this study are as follows.

- Developed a FB to HB reconfigurability method during OCF in specific SM switches. (Section III-C).
- Quantified the reliability enhancement of MMCs in terms of B10 lifetime using the proposed reconfiguration method over an exclusively redundancy-based solution. (see Fig. 17, Table XI).
- Experimentally validated the postfault localization and reconfiguration based on the proposed method. (see Section V).

The rest of this article is organized as follows. Section II provides the basic mathematical model of the MMC's operation with redundant SMs and the behavior of the SM under OCF in any of the four IGBTs. Section III explains the methodology for fault detection, localization, and tolerance. The proposed algorithm for FB to HB SM reconfiguration is described in detail in this section. In Section IV, the reliability enhancement with the proposed fault-tolerant reconfiguration on the operational lifetime of an MMC is quantified. Further, a quantitative comparative analysis with existing studies, demonstrating the effectiveness of the proposed reconfiguration method, is presented. In Section V, a downscale experimental setup is used to validate the effectiveness of this strategy. Finally, Section VI concludes this article.

II. MMC Operation Concept and OCF Behaviour

A. Mathematical Models

The configuration of the 3-phase MMC with FB SM is given in Fig. 1. The redundant SMs are used to improve the reliability and provide active fault-tolerance ability in case of SM failure [3]. The modularity and scalability of MMC are obtained by connecting SMs in series, which makes the MMC applicable to many applications. From the FB SM configuration, it can be seen that four IGBTs and their body diode with a capacitor bank construct the FB SM. A bypass switch is also used to bypass the SM in case of SM failure. For each FB SM, the reconfiguration of the switches can provide different SM outputs, including zero, positive, and negative voltage. However, negative SM voltage, used to tolerate the dc link short-circuit in normal operation, is not considered in this study.

According to the circuitry of the MMC shown in Fig. 1 and based on Kirchhoff's law, the following equations can be obtained for phase a:

$$R_{\text{arm}} i_{\text{u,a}} + L_{\text{arm}} \frac{di_{\text{u,a}}}{dt} = \frac{1}{2} V_{dc} - v_{u,a} - v_{s,a} \tag{1}$$

$$R_{\text{arm}} i_{\text{l,a}} + L_{\text{arm}} \frac{di_{\text{l,a}}}{dt} = \frac{1}{2} V_{dc} - v_{l,a} - v_{s,a} \tag{2}$$

where $v_{u,a}$ and $v_{l,a}$ are defined as

$$v_{u,a} = \sum_{i=1}^{N+M} V_{\text{SM},i}^{u,a} \tag{3}$$

$$v_{l,a} = \sum_{i=1}^{N+M} V_{\text{SM},i}^{l,a} \tag{4}$$

$$i_{u,a} = i_{cir,a} + \frac{1}{2} i_{s,a} \tag{5}$$

$$i_{l,a} = i_{cir,a} - \frac{1}{2} i_{s,a}. \tag{6}$$

Here, $V_{\text{SM},i}^{u,a}$ and $V_{\text{SM},i}^{l,a}$ represent the voltage across the SM capacitors in the upper and lower arms, respectively. where $v_{u,a}$ and $v_{l,a}$ are the voltages of the upper arm and lower arm, respectively, and $i_{u,a}$ and $i_{l,a}$ are the upper arm and lower arm currents. $i_{\text{cir,a}}$ is the circulating current that is calculated as follows:

$$i_{\text{cir,a}} = \frac{1}{2}(i_{u,a} + i_{l,a}). \tag{7}$$

The dc and ac dynamics of the MMC can be obtained by summing and subtracting equations (2) and (3), respectively

$$2L_{\text{arm}} \frac{di_{\text{cir,a}}}{dt} + 2R_{\text{arm}} i_{\text{cir,a}} = V_{dc} - v_{u,a} - v_{l,a} \tag{8}$$

$$L_{\text{arm}} \frac{di_{\text{s,a}}}{dt} + R_{\text{arm}} i_{\text{s,a}} = v_{l,a} - v_{u,a} - 2v_{s,a}. \tag{9}$$

Ideally, the sum of $v_{u,a}$ and $v_{l,a}$ should equal V_{dc}, while $v_{u,a} - v_{l,a}$ should give perfectly sinusoidal ac outputs. So

$$v_{s,a} = m\cos(\omega t + \phi)\frac{V_{dc}}{2} \tag{10}$$

where m is the modulation index with a value between $[0, 1]$. Assuming that there is no voltage drop across the arm's resistance

$$v_{u,a} = (1 - m\cos(\omega t + \phi))\,\frac{V_{dc}}{2} \tag{11}$$

$$v_{l,a} = (1 + m\cos(\omega t + \phi))\,\frac{V_{dc}}{2}. \tag{12}$$

B. Load-Sharing Redundancy Operation

The redundant SMs are used to increase the reliability of the MMC in case of SM failure. However, there are several methods of operating the redundant SMs. In this article, the load-sharing redundancy is applied. In this redundancy strategy, all the existing SMs (both original and redundant) share the load, so the voltage across each SM will be lower. However, in the case of an SM failure, the voltage across the remaining SMs increases as follows:

$$v_{u,a-ref} = \frac{1}{N + M - F_{u,a}}\,(1 - m\cos(\omega t + \phi))\,\frac{V_{dc}}{2} \tag{13}$$

$$v_{l,a-ref} = \frac{1}{N + M - F_{l,a}}\,(1 + m\cos(\omega t + \phi))\,\frac{V_{dc}}{2} \tag{14}$$

where $F_{u,a}$ and $F_{l,a}$ are the number of faulty SMs in the upper and lower arms, respectively.

C. SM's Behavior in Case OCF

In this section, the FB SM behavior under various conditions is evaluated. These conditions include inserted, bypassed 1, and bypassed 2 states. For each state, we analyze the behavior during normal operation and in the event of an OCF in one of the four IGBTs (T1, T2, T3, and T4). The SM voltage behavior is explained in detail, focusing on the voltage across the capacitor (V_{cap}) and the SM's ability to charge or discharge under different current flow scenarios (i_{SM}). The behavior in these conditions is summarized in the following tables and figures.

1) Inserted Condition: In the inserted state, the SM is actively contributing to the output voltage, allowing for the generation of $+V_{\text{cap}}$ or $-V_{\text{cap}}$ based on the system's requirements and current flow. During normal operation, the SM can either charge or discharge its capacitor depending on the current direction (i_{SM}). In case of an OCF, the following holds.

1) Normal operation: The SM charges or discharges normally, with output voltages of $+V_{\text{cap}}$ depending on the current direction [in Table III (a) and Fig. 2(a)].
2) OCF in T1: When $i_{\text{SM}} < 0$, T1 fails to turn on, but the current forces to flow through D2, bypassing the capacitor. So, it is not possible to discharge the capacitor and its voltage only increases [in Table III (b) and Fig. 2(b)].
3) OCF in T2: Under an OCF in T2, the SM operates similarly and can be charged and discharged similarly to normal operation [in Table III (c) and Fig. 2(c)].
4) OCF in T3: A failure in T3 follows the same pattern, with the SM operating normally as OCF in T2 [in Table III (d) and Fig. 2(d)].
5) OCF in T4: This mirrors the case of T1. When $i_{\text{SM}} < 0$, the SM remains bypassed, preventing discharge [in Table III (e) and Fig. 2(e)].

Table III and Fig. 2 show the voltage outputs and current paths for the inserted condition, and it can be concluded that OCF in T1 and T4 will deteriorate the proper operation of the SM. At the same time, OCF in T2 and T3 does not impact inserting the SM.

2) Bypassed Condition 1: In bypassed condition 1, the SM is bypassed, preventing the capacitor from affecting the output voltage. However, some capacitor charging may still occur in faulty conditions depending on the current flow.

1) Normal operation: Shown in Table IV (a) and Fig. 3(a), the output voltage is zero, and the SM is fully bypassed, with no charging or discharging of the capacitor.
2) OCF in T1: When $i_{\text{SM}} < 0$, the SM is inserted and capacitor gets charged as shown in Table IV (b) and Fig. 3(b).
3) OCF in T2: The SM is not impacted in this case and can be bypassed as required as given in Table IV (c) and Fig. 3(c).
4) OCF in T3: In this scenario given in Table IV (d) and Fig. 3(d), an OCF in T3 increases the charging during bypassed conditions when $i_{\text{SM}} \geq 0$.
5) OCF in T4: The behavior mirrors OCF in T2 in Table IV (e) and Fig. 3(e), where the SM is bypassed as required.

Details of the current paths and SM voltage under bypass condition 1 are summarized in Table IV and Fig. 3. It can be concluded that OCF in T1 and T3 will impact the SM's operation under bypassed condition 1 and charge the SM more than normal operation.

3) Bypassed Condition 2: Bypassed condition 2 involves a different configuration of the bypass switches. The SM is inserted under certain fault conditions, which can cause the capacitor to charge in ways not typically seen in normal operation.

1) Normal operation: The SM remains bypassed with zero output voltage as given in Table V (a) and Fig. 4(a).

TABLE III
SM'S OUTPUT VOLTAGE FOR INSERTED CONDITION AND CONSIDERING T1-T4 OCFS CONDITION

	Normal, (a)	OCF in T1, (b)	OCF in T2, (c)	OCF in T3, (d)	OCF in T4, (e)
Switch State	{T1,T2,T3,T4} {on,off,off,on}	{T1,T2,T3,T4} {OCF,off,off,on}	{T1,T2,T3,T4} {on,OCF,off,on}	{T1,T2,T3,T4} {on,off,OCF,on}	{T1,T2,T3,T4} {on,off,off,OCF}
$i_{sm} \geq 0$	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = V_{Cap}$, Charge
$i_{sm} < 0$	$V_{sm} = V_{Cap}$, Discharge	$V_{sm} = 0$, –	$V_{sm} = V_{Cap}$, Discharge	$V_{sm} = V_{Cap}$, Discharge	$V_{sm} = 0$, –

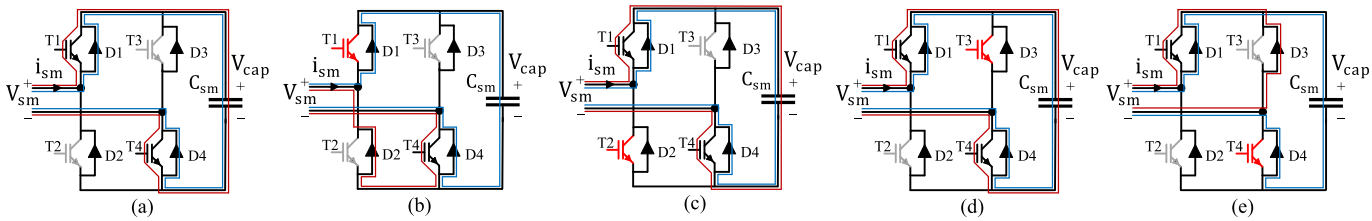

Fig. 2. SM's behavior for the inserted mode in case of (a) normal operation, (b) OCF in T1, (c) OCF in T2, (d) OCF in T3, and (e) OCF in T4.

TABLE IV
SM'S OUTPUT VOLTAGE FOR BYPASSED CONDITION 1 AND CONSIDERING T1-T4 OCFS CONDITION

	Normal, (a)	OCF in T1, (b)	OCF in T2, (c)	OCF in T3, (d)	OCF in T4, (e)
Switch State	{T1,T2,T3,T4} {on,off,on,off}	{T1,T2,T3,T4} {OCF,off,on,off}	{T1,T2,T3,T4} {on,OCF,on,off}	{T1,T2,T3,T4} {on,off,OCF,off}	{T1,T2,T3,T4} {on,off,on,OCF}
$i_{sm} \geq 0$	$V_{sm} = 0$, –	$V_{sm} = 0$, –	$V_{sm} = 0$, –	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = 0$, –
$i_{sm} < 0$	$V_{sm} = 0$, –	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = 0$, –	$V_{sm} = 0$, –	$V_{sm} = 0$, –

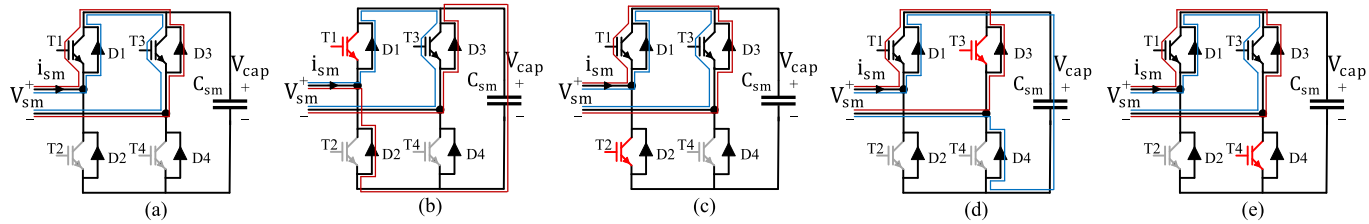

Fig. 3. SM's behavior for the bypassed mode 1 in case of (a) normal operation, (b) OCF in T1, (c), OCF in T2, (d), OCF in T3, and (e) OCF in T4.

TABLE V
SM'S OUTPUT VOLTAGE FOR BYPASSED CONDITION 2 AND CONSIDERING T1-T4 OCFS CONDITION

	Normal, (a)	OCF in T1, (b)	OCF in T2, (c)	OCF in T3, (d)	OCF in T4, (e)
Switch State	{T1,T2,T3,T4} {off,on,off,on}	{T1,T2,T3,T4} {OCF,on,off,on}	{T1,T2,T3,T4} {off,OCF,off,on}	{T1,T2,T3,T4} {off,on,OCF,on}	{T1,T2,T3,T4} {off,on,off,OCF}
$i_{sm} \geq 0$	$V_{sm} = 0$, –	$V_{sm} = 0$, –	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = 0$, –	$V_{sm} = 0$, –
$i_{sm} < 0$	$V_{sm} = 0$, –	$V_{sm} = 0$, –	$V_{sm} = 0$, –	$V_{sm} = 0$, –	$V_{sm} = V_{Cap}$, Charge

2) OCF in T1: The SM is bypassed as expected as detailed in Table V (b) and Fig. 4(b).
3) OCF in T2: The capacitor charges more than usual under bypassed condition 2, when $i_{SM} \geq 0$ as given in Table V (c) and Fig. 4(c).
4) OCF in T3: Similar to T1, the SM is unaffected and can be bypassed without any problem as given in Table V (d) and Fig. 4(d).
5) OCF in T4: In this case, the capacitor charges under bypassed condition 2, with increased V_{cap} during $i_{SM} < 0$ as given in Table V (e) and Fig. 4(e).

Table V and Fig. 4 describe this state's current path and voltage output. As it was explained, only OCF in T2 and T4 will affect the SM's behavior under bypassed condition 2, which causes the capacitor to charge more than the normal operation.

TABLE VI
CURRENT CHARACTERISTICS UNDER OCF

OCF in T2/T3	OCF in T1/T4
$\tilde{i}_{cir,a} \geq i_{cir,a}$	$\tilde{i}_{cir,a} < i_{cir,a}$

So, according to the explanations provided in Tables III–V and the dynamics of the MMC given in (8) and (9), the behavior of the circulating current is summarized in Table VI. As can be seen, it shows the ideal circulating current $\tilde{i}_{cir,a}$. For example, in case of a fault in T1/T4, the measured circulating current

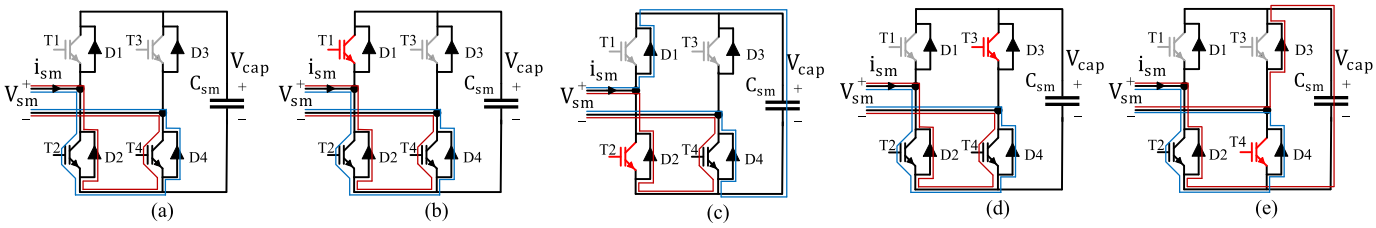

Fig. 4. SM's behavior for the bypassed mode 2 in case of (a) normal operation, (b) OCF in T1, (c) OCF in T2, (d) OCF in T3, and (e) OCF in T4.

$i_{cir,a}$ will be larger than the ideal values. These facts can be used later for fault detection and reconfigurability, which will be detailed in the subsequent section. Further details can be found in [13].

III. Methodology for Fault Detection, Localization, and Tolerance

A. Fault Detection

The state observer is one of the most widely used methods for fault detection, which is adopted in industry as well [13], [28], [29]. The working principle of this detector is to compare the measured output from the MMC with the observed value, and if the difference is greater than the threshold, the fault can be detected. By adopting this method, the fault can be detected within a few milliseconds, and it is even possible to determine in which pair of switches the OCF occurred, as explained in Section II-C.

The dynamics of the MMC in state-space form is given as

$$\dot{x} = Ax + Bv + De$$
$$y = Cx$$

with

$$x = \begin{pmatrix} i_{\text{cir,a}} \\ i_{s,a} \end{pmatrix}, v = \begin{pmatrix} v_{l,a} \\ v_{u,a} \end{pmatrix}, e = \begin{pmatrix} V_{dc} \\ v_{s,a} \end{pmatrix}$$
$$A = \begin{pmatrix} -\frac{R_{\text{arm}}}{L_{\text{arm}}} & 0 \\ 0 & -\frac{R_{\text{arm}}}{L_{\text{arm}}} \end{pmatrix}, B = \begin{pmatrix} \frac{-1}{2L_{\text{arm}}} & \frac{-1}{2L_{\text{arm}}} \\ \frac{1}{L_{arm}} & -\frac{1}{L_{arm}} \end{pmatrix}$$
$$C = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}, D = \begin{pmatrix} \frac{1}{2L_{\text{arm}}} & 0 \\ 0 & -\frac{2}{L_{\text{arm}}} \end{pmatrix}.$$

So, the observer is given as

$$\dot{\hat{x}} = A\hat{x} + Bv + De + K(y - \hat{y})$$
$$\hat{y} = C\hat{x}.$$

In which $\hat{x}$ is the estimated value the observer gives. Also, K is the observer gain, which is shown as follows: based on the eigenvalues of the matrix $A - KC$, its value should be chosen as follows to meet the stability condition:

$$K = \begin{pmatrix} k & 0 \\ 0 & k \end{pmatrix}, \quad k > -\frac{R_{\text{arm}}}{L_{\text{arm}}}.$$

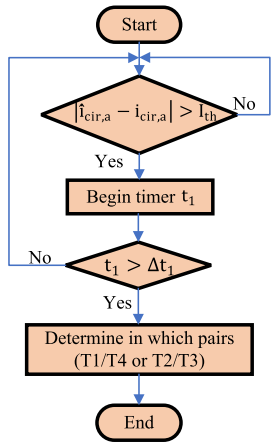

Fig. 5. Flowchart for the fault detection algorithm.

Therefore, by comparing the observed current $\hat{i}_{\text{cir,a}}$ and the real current $i_{\text{cir,a}}$, the detection algorithm is shown in Fig. 5. Hence, if there is no OCF, the measured $i_{\text{cir,a}}$ can track $\hat{i}_{\text{cir,a}}$ with a small error, also, the time step Δt and K should be appropriately selected to avoid false detection flags.

B. Fault Localization

Localization identifies the faulty SM by comparing voltage differences across capacitor voltages within the arm's capacitors, as given in [30]. Voltage differences are an effective metric because they directly reflect the charge imbalances caused by OCFs. When an IGBT fails, the associated capacitor voltage deviates from the expected range, providing a clear and measurable indicator of the fault's location. A threshold-based approach ensures precise identification without false positives. This phase also determines which IGBT pair (T1/T4 or T2/T3) contains the fault.

Fig. 6 shows the applied algorithm. If the threshold criterion is met, the timer starts, and if both conditions are met, the localization flag becomes high. Note that the threshold selection for fault localization should be 10% more than the capacitor voltage peak value during rated power operation to avoid false alarms.

C. Fault Tolerance

As discussed, OCF ride-through is achieved by selectively either applying reconfiguration from FB to HB or using arm-level

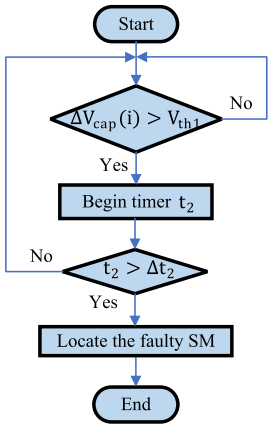

Fig. 6. Flowchart for the fault localization algorithm.

redundant SMs, depending on the specific fault location obtained from the detection algorithm. After fault detection, fault localization and tolerance are achieved by either reconfiguration - if OCF occurs in T2 or T3—or redundancy—if OCF occurs in T1 or T4. The proposed algorithm given in Fig. 8. The fault detection algorithm can identify which pair of IGBTs (T1/T4 or T2/T3) the fault occurred in, as the postfault behavior of the switches within each pair is identical. It is challenging to detect the exact IGBT in which the OCF occurred, which is addressed in this study.

1) Implementation: Fig. 7 shows the implementation of fault tolerance depending on the SM switch location T1–T4. For OCF in the switches T1 and T4, the entire faulty SM is permanently bypassed as shown in Fig. 7(a) and (d), respectively. In this article, load sharing based redundancy is used, thereby the capacitor voltage of each remaining SM in the given arm is increased corresponding to the operating dc link voltage. The fault tolerance in this case can be achieved by following the algorithm given in Fig. 9.

In the event of an OCF in switch T2, the switch T1 is permanently gated ON, allowing the SM to emulate an reconfigured HB using the remaining healthy branch T3–T4 as shown in Fig. 7(b). During both bypass and inserted state, T1/D1 provides a path for the current flow, as depicted. Similarly, when OCF occurs in switch T3, the complimentary location T4 is permanently gated ON to provide the current flow for the healthy HB branch T1/T2 as shown in Fig. 7(c).

It is important to note that although the proposed reconfiguration strategy provides a fault-tolerant operation, redundancy still remains necessary for T1/T4 faults. It, therefore, offers a backup fault-tolerant mechanism at the expense of increased control complexity. On the other hand, the proposed method maximizes the postfault operability of the remaining components, thus enhancing the reliability of the system over its useful lifetime, as quantified using Monte-Carlo Simulations (MCSs) in Section IV.

2) Healthy HB Branch Identification: Fig. 10 shows the algorithm to determine the specific switch among either T2 or T3 in which the OCF occurs, so that the remaining healthy branch can be used as a reconfigured HB. It is initially assumed that OCF occurs in T3 if the first voltage threshold is reached, and therefore T4 is permanently gate "ON" while intending to use the other branch with switches T1/T2 for reconfigured HB operation. In case branch T1/T2 is indeed the healthy branch, this mode of operation is continued. However, if the actual OCF has occurred in T2, this strategy will lead to a gradual increase in SM capacitor voltage, as explained in Table VII and Fig. 11 depending on the arm current direction. For example, the capacitor continues to charge even in bypass state when $i_{\text{sm}} \geq 0$.

Therefore, a second threshold (V_{th2}) is used to identify that actually switch T2 is in OCF, and the reconfiguration signals are shifted to operate the healthy HB with switches T3/T4 instead.

3) Protective Layer: The focus of this part is on designing a protective layer that ensures continuous operation of the MMC in the event of a fault. In case of false detection, the MMC will continue its operation while awaiting fault localization. The following two scenarios are notable.

Scenario 1: Fault on T1 but incorrectly detected on T2/T3

In this scenario, a fault occurs on T1, but the detection algorithm wrongly identifies the fault on T2/T3. The fault signal goes high upon fault detection, and the system awaits fault localization. During this time, the algorithm always keeps T2 OFF and T1 ON. However, in practice, T1 is OCF. The voltage of the SM will follow the behavior given in Table VIII and Fig. 12.

So, it can be understood that the voltage of the faulty SM keeps increasing; in that case, the second voltage threshold will be reached, and the algorithm assumes the faulty switch is T2. In that case, the algorithm will always adapt the switching signal to T2: OFF and T1: ON while in practice, T1 has OCF. The voltage of the SM will follow the behavior given in Table IX and Fig. 13.

Therefore, even in this case, the voltage of the faulty SMs keeps increasing. Please note that the same behavior will be followed in the case of OCF in T4 and false detection of T2/T3. For this purpose, a protection layer is implemented, as shown in Fig. 14 to handle this scenario. By introducing a third voltage threshold, the MMC ensures that if the capacitor voltage continues to increase beyond this limit, the faulty SM will be bypassed, preventing further instability.

Scenario 2: Fault on T2/T3 but incorrectly detected on T1/T4

In the case of a fault occurring on T2/T3, the detection algorithm incorrectly flags T1/T4 as faulty. In this case, the faulty SM will be directly bypassed, and the reconfiguration process will no longer be executed. In this scenario, the detection algorithm ensures a seamless transition by bypassing the correct faulty SM. These measures ensure accurate fault detection and localization, allowing the system to maintain stable and continuous operation even in false detections.

D. Robustness to Dynamic Operating Conditions

The performance of the proposed fault detection algorithm under dynamic conditions is evaluated by applying changes in load and dc link voltage as shown in Figs. 15 and 16, respectively. The results show that the observed circulating current closely follows the measured circulating current. Therefore, the

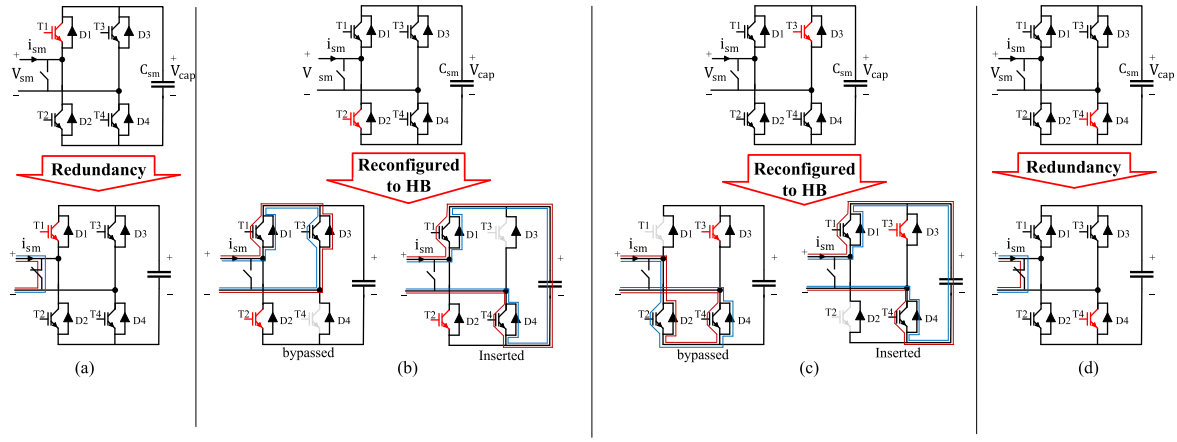

Fig. 7. Reconfiguration and redundancy of SM under OCF in all IGBTs to achieve fault tolerance operation if OCF occurs in (a) T1, (b) T2, (c) T3, or (d) T4.

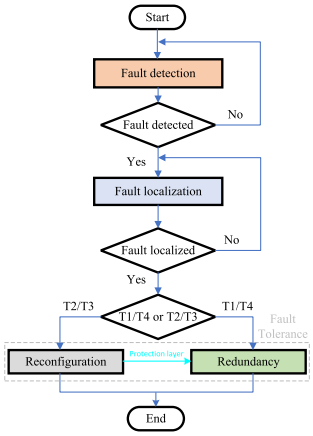

Fig. 8. Flowchart for the proposed algorithm to select the fault tolerance strategy.

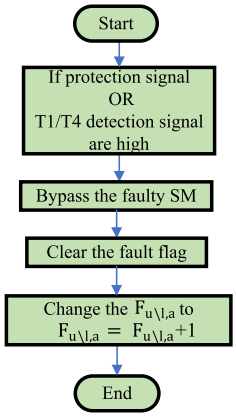

Fig. 9. Redundancy algorithm for OCF in T1 or T4.

TABLE VII
SM'S OUTPUT VOLTAGE UNDER T2 OCF CONDITION AND KEEPING RIGHT HB ALWAYS AS T3: OFF AND T4: ON AS PART OF RECONFIGURATION PROCESS

	Inserted, (a)	Bypassed, (b)
Switch State	{T1,T2,T3,T4} {on,OCF,off,on}	{T1,T2,T3,T4} {off,OCF,off,on}
$i_{sm} \geq 0$	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = V_{Cap}$, Charge
$i_{sm} < 0$	$V_{sm} = V_{Cap}$, Discharge	$V_{sm} = 0$, –

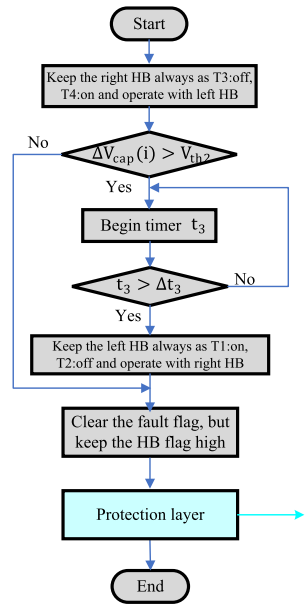

Fig. 10. Algorithm for health HB branch identification when OCF occurs in either T2 or T3.

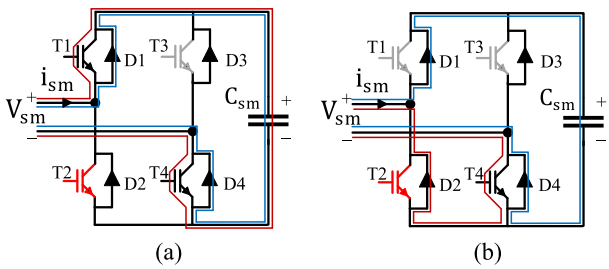

Fig. 11. SM's current behavior under T2 OCF while keeping the right HB as T3: OFF and T4: ON for (a) inserted and (b) bypassed conditions.

difference between the measured and observed current does not reach the threshold, and no fault flag is activated during such transients.

TABLE VIII
SM'S OUTPUT VOLTAGE BEHAVIOR UNDER T1 OCF WHILE DETECTION ALGORITHM DETECTS THE T3 FAULT BY MISTAKE BY KEEPING THE RIGHT HB AS T3: OFF AND T4: ON

	Inserted, (a)	Bypassed, (b)
Switch State	{T1,T2,T3,T4} {OCF,off,off,on}	{T1,T2,T3,T4} {OCF,on,off,on}
$i_{sm} \geq 0$	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = 0$, –
$i_{sm} < 0$	$V_{sm} = 0$, –	$V_{sm} = 0$, –

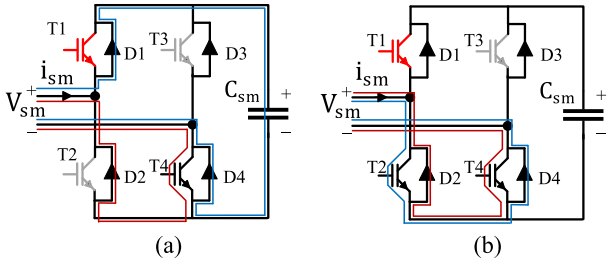

Fig. 12. SM's current behavior under T1 OCF while the detection algorithm detects the T3 fault by mistake by keeping the right HB as T3: OFF and T4: ON for (a) inserted and (b) bypassed conditions.

TABLE IX
SM'S OUTPUT VOLTAGE BEHAVIOR UNDER T1 OCF WHILE DETECTION ALGORITHM DETECTS THE T2 FAULT BY MISTAKE BY KEEPING THE LEFT HB AS T1: ON AND T2: OFF

	Inserted, (a)	Bypassed, (b)
Switch State	{T1,T2,T3,T4} {OCF,off,off,on}	{T1,T2,T3,T4} {OCF,off,on,off}
$i_{sm} \geq 0$	$V_{sm} = V_{Cap}$, Charge	$V_{sm} = 0$, –
$i_{sm} < 0$	$V_{sm} = 0$, –	$V_{sm} = V_{Cap}$, charge

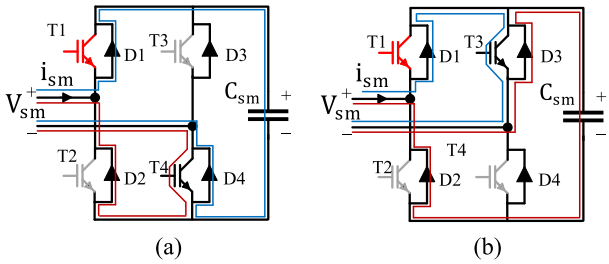

Fig. 13. SM's current behavior under T1 OCF while the detection algorithm detects the T2 fault by mistake by keeping the left HB as T1: ON and T2: OFF for (a) inserted and (b) bypassed conditions.

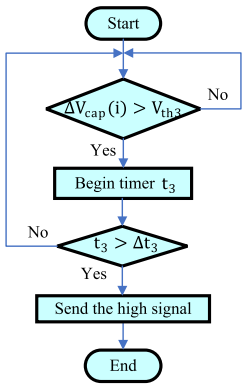

Fig. 14. Protection layer in case of a false signal.

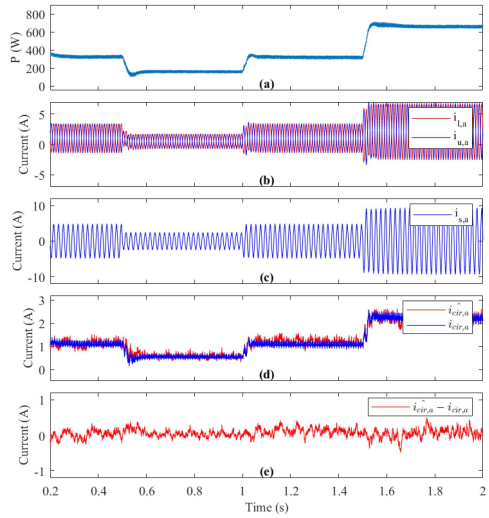

Fig. 15. Simulated performance of the proposed fault detection algorithm to load change for phase a. (a) Demanded load change, (b) upper and lower arm current, (c) output current, (d) measured and observed circulating current, and (e) the difference between measured and observed current.

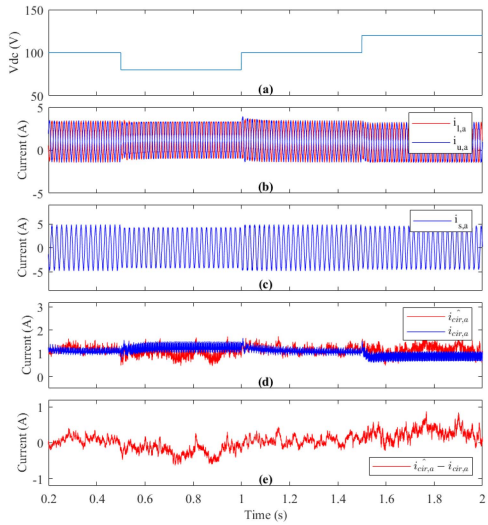

Fig. 16. Simulated performance of the proposed fault detection algorithm to DC link voltage change for phase a. (a) DC link voltage, (b) upper and lower arm current, (c) output current, (d) measured and observed circulating current, and (e) the difference between measured and observed current.

IV. QUANTIFIED SYSTEM RELIABILITY ENHANCEMENT WITH PROPOSED RECONFIGURATION METHOD

In this section, the reliability improvement through proposed FB to HB reconfiguration is quantified using MCS for an MMC with characteristics given in Table X [3].

Fig. 17 shows the increase in system reliability with the proposed algorithm as compared to the case where only conventional arm-level redundancy is used. It can be observed that the proposed technique leads to a higher B10 lifetime as the OCFs expressed as percentage of total switch failure events increase.

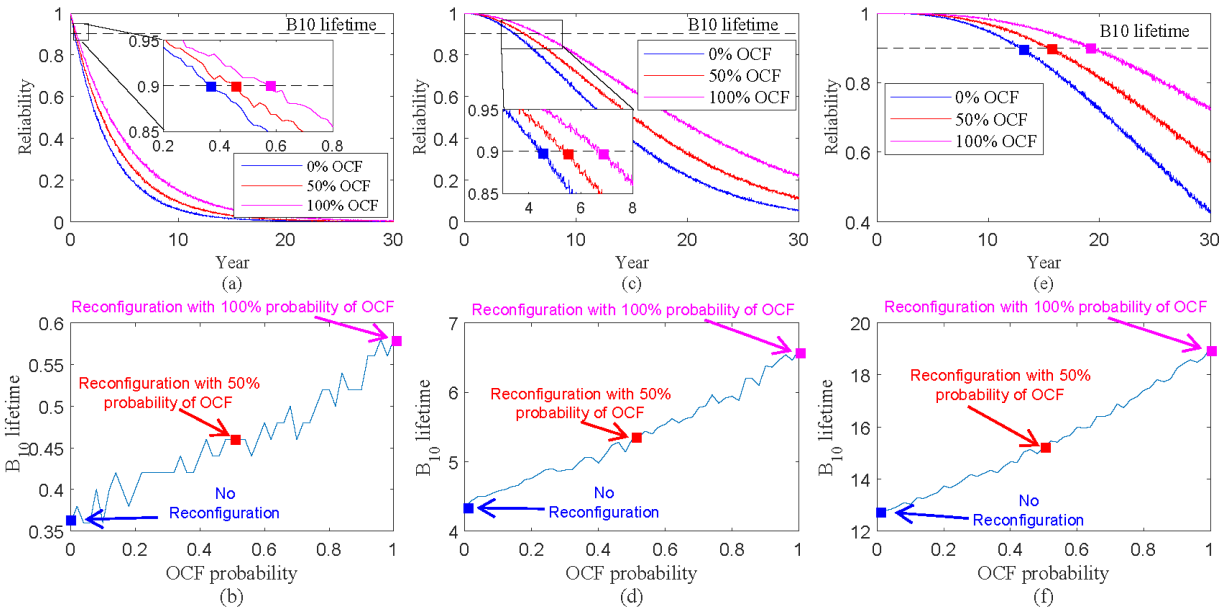

Fig. 17. Impact of reconfiguration on the reliability of the MMC where (a) and (b) there is no redundant SM, (c) and (d) there is one redundant SM in each arm, and (e) and (f) there are two redundant SMs in each arm.

TABLE X
MMC CHARACTERISTICS AND FAILURE RATES FOR RELIABILITY ANALYSIS

Symbols	Item	Value
$N_{\min}$	Minimum number of SMs	9
V_{dc}	Pole-to-pole DC voltage	17 kV
S_{MMC}	Rated power	10 MVA
V_{IGBT}	Rated IGBT Voltage	3300 V
$k_{\max}$	Capacitors voltage ripple	10%
S_{f}	Safety factor of IGBT	0.6
C_{SM}	SM capacitance	3.3 mF
N_{red}	Redundant per arm	0 or 1 or 2
$\lambda_{\text{base-IGBT}}$	IGBT base failure rate (MIL)	100 FIT
$\lambda_{\text{base-Cap}}$	DC capacitor base failure rate (MIL)	100 FIT

TABLE XI
B10 LIFETIME (YEARS) COMPARISON BETWEEN THE PROPOSED METHOD AND CONVENTIONAL REDUNDANCY APPROACHES

Ref	Without red†	With red‡	Proposed method
[31]	0.311	9.4	11.2
[32]	0.246	5.4	6.4
[33]	0.021	12.6	15.1
[33]	0.023	13.5	16.3
[34]	0.022	13.2	15.9

†: Refers to the original converter from the reference, assuming no arm-level redundant SM is considered.
‡: Refers to the original converter from the reference, assuming 10% arm-level redundant SM is included.

Fig. 17(a) and (b) shows that when no arm-level redundancy is applied, the B_{10} lifetime improves from 0.35 years to approximately 0.45 years and 0.55 years for 50% and 100% OCF failures, respectively. When one redundant SM per arm is considered, as shown in Fig. 17(c) and (d), the B_{10} lifetime increases from 4.2 years to 5.2 years and 6.5 years for 50% and 100% OCF failures, respectively. Similarly, with two redundant SMs per arm shown in Fig. 17(e) and (f), the B_{10} lifetime increasing from 12.8 years to 15 years and 18.7 years for 50% and 100% OCF failures, respectively. Therefore, results from MCS indicate that approximately 25%–50% reliability enhancement can be achieved with the proposed FB to HB SM reconfiguration technique for the same arm-level redundancy. Consequently, it can be inferred that the cost of arm-level redundancy can be lower for the given B10 lifetime requirements if the proposed SM-level reconfiguration under OCF is employed.

To demonstrate its effectiveness, the proposed reconfiguration method is applied to existing FB MMCs from various references listed in Table XI. The table compares the B10 lifetime across different FB MMCs, showing that the proposed method quantifies the enhancement in system reliability.

It can be seen that the proposed method improved the reliability by 20%–25%. However, like any control-based methodology, it has certain limitations. The detection and localization algorithms rely on predefined thresholds and delay times, which need careful tuning to balance sensitivity and robustness. While higher thresholds reduce the likelihood of false detections, they also delay fault response time, which may be critical in high-speed applications. Similarly, the reliance on a software-only approach might limit the fault-tolerant performance under extreme conditions, such as multiple simultaneous faults or transient scenarios with significant parameter variations. Future research could focus on improving the diagnostic algorithms to enhance accuracy and reduce diagnostic time under various operating conditions. Integrating advanced machine learning techniques for fault prediction and localization could further increase the system's robustness. Additionally, exploring hybrid methods that combine control-based and hardware-based

TABLE XII
MMC OPERATIONAL CHARACTERISTICS

Symbols	Item	Value
N+M	Number of SMs (including redundant)	3 + 1
V_{dc}	Pole-to-pole DC voltage	100 V
V_{SM}	Applied IGBT voltage	25 V
C_{SM}	SM capacitance	4 mF
L_{arm}	Arm inductance	4.3 mH
$R_{arm}(R)$	Arm resistance	0.5 Ω
$f_{Control}$ (NLM)	Transition rate of controller	2000 Hz
R_{Load}	Load resistance	10 Ω
k	Observer gain	5
I_{th}	Current threshold	5 A
V_{th1}	Voltage threshold 1	1 V
V_{th2}	Voltage threshold 2	1.5 V
V_{th3}	Voltage threshold 3	2 V
Δt_1	Delay time 1	2 ms
Δt_2	Delay time 2	1 ms
Δt_3	Delay time 3	1 ms

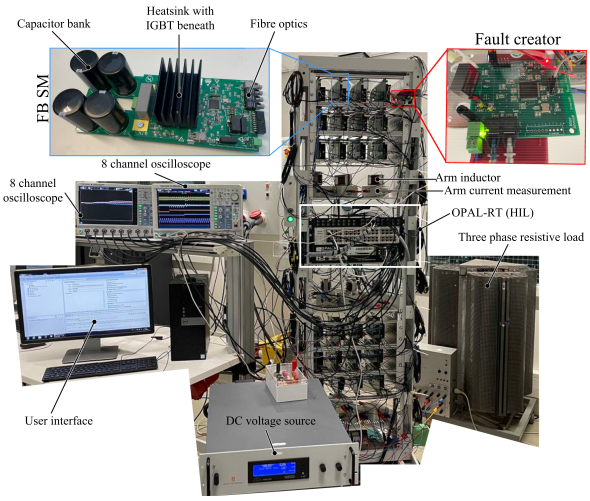

Fig. 18. Experimental prototype of the three-phase FB MMC setup.

redundancy might reduce the complexity of reconfiguration while maintaining high performance.

V. EXPERIMENTAL VALIDATION

In this section, the effectiveness of the proposed fault-tolerance methodology is validated, where a downscale MMC with the given characteristics in Table XII is used. Before presenting the results, it is essential to note that the effectiveness of the fault detection and fault-tolerant methodologies relies on carefully selected threshold values and control parameters. These thresholds are essential for distinguishing between normal operational variations and actual fault conditions while ensuring robust detection and localization. A general criteria is provided in Table XIII to select these thresholds.

As explained, the impact of both redundancy and reconfiguration is investigated. Here, the redundancy methodology is assumed to be load-sharing with $N = 3$ and $M = 1$, representing the redundant SMs. Fig. 18 presents a picture of the downscaled MMC in the lab. In this prototype, the OPAL-RT acts as the high-level controller, reads the analog and digital inputs from the hardware, and sends the gating signals. Each SM also has its local circuitry, which includes the protection circuitry. This study uses

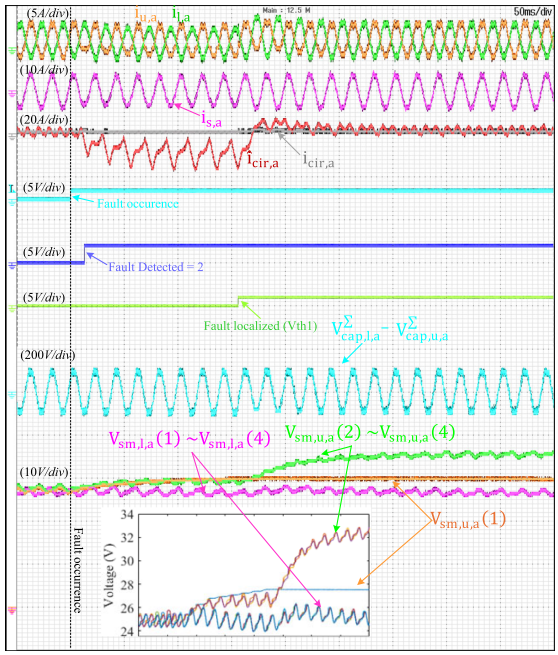

Fig. 19. Experimental results when the proposed algorithm is applied at T1 or T4 OCFs.

the nearest level modulation (NLM) for the modulation strategy. Also, the controller applied is adapted from [35].

In this article, a fault creator is used to mimic better the OCF scenario, which connects to one of the SMs and overwrites the gating signals from OPAL-RT. Hence, it is possible to keep any arbitrary IGBT open, which mimics the OCF.

A. OCF in T1 or T4

The characteristics of the MMC under OCF in T1 or T4 are identical; therefore, the results are only shown for OCF in T1. Fig. 19 shows the MMC behavior in the case of T1 OCF. As can be seen, the fault can be detected in less than 10 ms before the fault signal goes high, which is the output of the observer, by comparing the measured circulating current $i_{cir,a}$ with the ideal $i_{cir,a}$. It can be seen from this difference, $i_{cir,a} - \hat{i}_{cir,a}$, that the fault occurred in the pair of T1/T4. After the detection, the localization is achieved around 150 ms, and the difference between the faulty SM and the healthy ones will be more than V_{th1} . Other localization methods can perform localization faster, but this is not the scope of this study. Finally, after the faulty SM is localized, the voltage reference of the healthy SMs will be increased to 100/3 = 33.3 V.

B. OCF in T3

The behavior of the MMC under T3 OCF is shown in Fig. 20. As can be seen, in less than 10 ms, the observer detects the fault, and since $i_{cir,a} < \hat{i}_{cir,a}$ correctly determines it. The faulty SM is localized after less than 20 ms, where the first fault localization flag goes high. Based on the algorithm, which ensures the fault occurred on T3, the FB SM is reconfigured to HB by always keeping the T3: OFF and T4: ON. The sorting algorithm will balance the voltage of the SMs in a similar way to that of other

TABLE XIII
THRESHOLD SELECTION AND RANGE OF CHANGES IN DETECTED VARIABLES

Threshold	Selection Criteria	Value	Ref
I_{th}	Based on worst-case deviation in normal operation to ensure early fault detection while avoiding false flag, which should be greater than the rated value of circulating current.	$\geq i_{\text{cir,a,rated}}$	[13], [28]
V_{th1}†	Set more than 10% of capacitor voltage ripple and less than its withstanding value.	$\geq 1.1 \times V_{\text{SM,rated}}$	[13]
V_{th2}†	Used for refining fault localization by identifying excessive capacitor voltage deviations after initial detection. It is selected 2.5% above the V_{th1}.	$\geq 1.125 \times V_{\text{SM,rated}}$	-
V_{th3}†	Prevents excessive capacitor voltage accumulation in case of incorrect localization or reconfiguration. It is selected 5% on the top ofV_{th1}.	$\geq 1.15 \times V_{\text{SM,rated}}$	-
Δt_1*	Ensures transient variations and temporary fluctuations do not cause false fault detection. It should be a large enough value, but before the current enters obvious distortion.	2 ms	[13], [28]
Δt_2*	Allows time for assured localization of the faulty SM.	1 ms	[13], [28]
Δt_3*	Allows time for determining reconfiguration or protection layer to be executed	1 ms	-

†: In this study, the difference between capacitors' voltage is used to localize the faulty SM since the voltage reference alters after bypassing faulty SMs.
*: According to [28], these values are empirical. According to [13], redundancy type (e.g., standby and load-sharing) can affect the selection criteria.

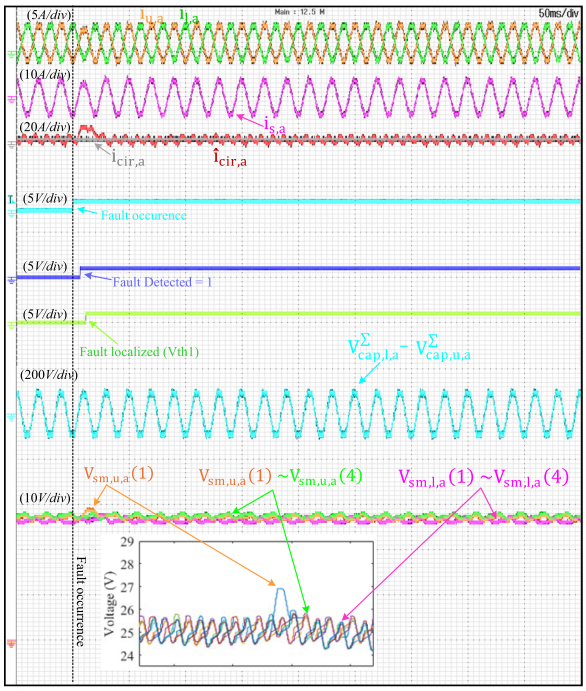

Fig. 20. Experimental results when the proposed algorithm is applied at T3 OCF.

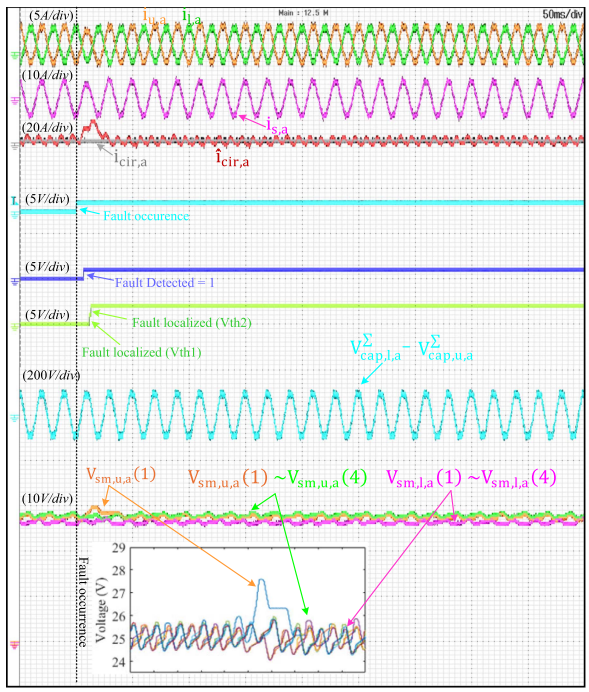

Fig. 21. Experimental results when the proposed algorithm is applied at T2 OCF.

healthy SMs. In this case, the number of levels remains the same, and the SM where the OCF occurred is reconfigured to HB.

C. OCF in T2

The behavior of the MMC in the case of OCF in T2 is identical to the T3 OCF. However, the reconfiguration algorithm first ensures that the OCF occurred in T2, as explained in Table VII. So, as can be seen, the SMs will be charged more, which, in this case, will cause the second voltage threshold to be reached. Hence, the controller realizes that the OCF occurred in T2 and reconfigures to HB by keeping the right HB across T1 ON and T2 OFF. The results are presented in Fig. 21, where the fault is ridden through in less than 20 ms, and reconfiguration is obtained.

The total harmonic distortion (THD) of the output current of the MMC was evaluated both before and after the fault ride-through process. The THD is calculated using the harmonic components of the output current to assess the impact of the fault and the effectiveness of the proposed fault-tolerant strategy. Table XIV below summarizes the THD values under different conditions, demonstrating the improvement in harmonic performance after the fault is mitigated.

TABLE XIV
THD OF OUTPUT CURRENT BEFORE AND AFTER FAULT RIDE-THROUGH

Fault on	Before (%)	After (%)
T1/T4	6.553	6.565
T2	6.270	6.445
T3	6.440	6.731

D. OCF in T1 and Wrong Detection Flag of T2/T3

The experimental validation highlights a scenario where an OCF occurs in T1, but the detection algorithm mistakenly flags the fault in T2/T3. In this scenario, the detection is forced to trigger an incorrect reconfiguration, where the faulty IGBT is assumed to be on T2/T3, resulting in the capacitor voltage

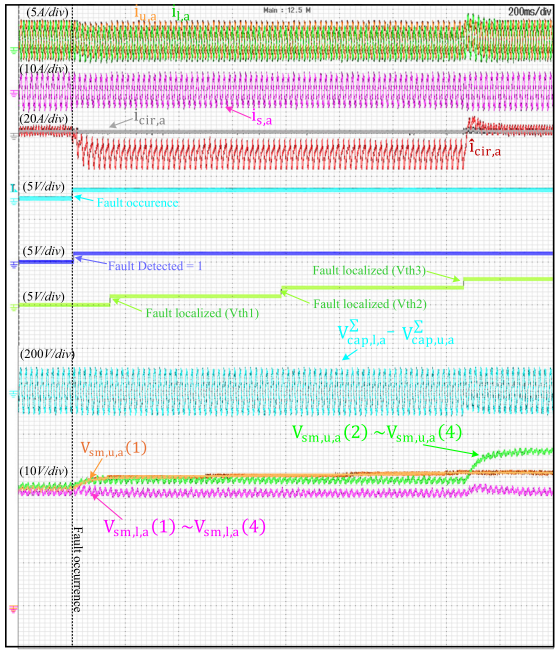

Fig. 22. Experimental results when an actual OCF occurs on T1/T4 while the detection algorithms detect a false flag on T2/T3.

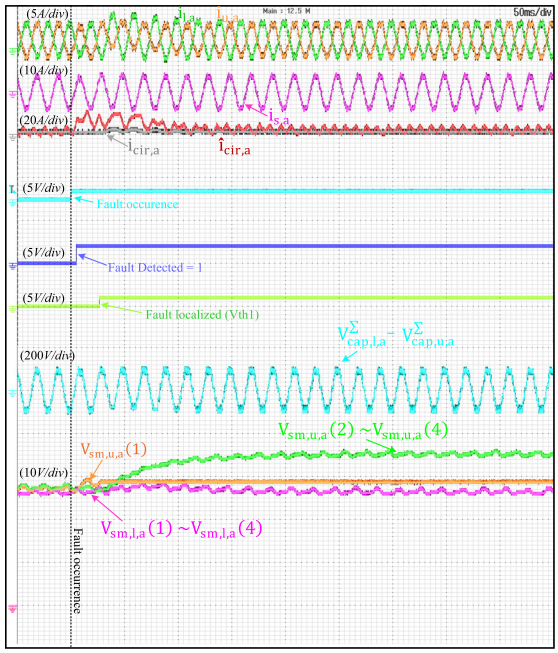

Fig. 23. Experimental results when an actual OCF occurs on T3 while the detection algorithms detect a false flag on T1/T4.

rising uncontrollably. The algorithm utilizes multiple voltage thresholds and delay times to verify the fault's location further. When the capacitor voltage exceeds V_{th3}, the protection layer recognizes the discrepancy and bypasses the SM, preventing further instability. This multistep approach ensures that even in cases of initial false detection, the system adapts to localize and reconfigure the faulty SM, maintaining continuous operation and minimizing downtime

E. OCF in T3 and Wrong Detection Flag of T1/T4

Considering the case of an OCF occurring in T2/T3, the detection algorithm is initially forced to misidentify the fault as being in T1 or T4. This leads to the faulty SM being bypassed directly and the continuous operation of the MMC system.

VI. Conclusion

This article presents a fault-tolerant reconfiguration methodology for FB reconfiguration that can potentially improve the operational lifetime of the MMC. It is shown that the proposed method can be applied specifically for OCFs in switches T2 and T3 of the FB SMs, wherein, permanent short-circuit of the complementary switches, that is, T1 and T4, respectively, can maintain normal operational requirements in postfault HB configuration. While arm-level redundancy is still necessary during OCFs in switches T1 and T4, it is shown using MCS that the proposed method can improve the 17 kV 10 MVA converter reliability by almost 25% over a solely redundancy-based solution for given lifetime requirements. It can be inferred, therefore, that this improved reliability can translate to equivalent cost savings related to reduced redundant SM requirements in MMC applications. Finally, using a lab-scale FB MMC prototype, it is experimentally shown that the proposed reconfiguration technique can successfully localize the fault and revert to normal operating requirements by shifting from FB to HB SM configuration in approximately 20 ms of fault initiation.

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