Real-Time Optimal Control of Dual-Bridge Series Resonant DC–AC Converters

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***Abstract*—Control plays a critical role in achieving efficient operation of dual-bridge series resonant dc–ac converters (DBSRC). However, realizing real-time, optimal, and robust control of DBSRC to maximize its efficiency is generally difficult, due to the complex interplay of control variables, efficiency, power demand, and voltage conversion ratio requirements. Here, we propose an optimal control strategy for DBSRC, suitable for real-time closed-loop controller implementation. The key to the strategy is the development of a closed-form analytical solution of the optimal control variables for maximum system efficiency and output power regulation. Detailed derivation of the optimal control solution is provided. The effectiveness of the proposed control strategy is validated on a 200-W DBSRC prototype. The results confirm that the proposed control strategy can achieve real-time and robust control performance, with over 2% efficiency improvement over the conventional single-phase-shift control strategy.**

***Index Terms*—Dual-active-bridge, optimal control, resonant converter, soft-switching, variable-frequency control.**

NOMENCLATURE

Acronyms

DBSRC	Dual-bridge series resonant dc–ac converters.
DAB	Dual active bridge.
SPS	Single-phase-shift.
ZVS	Zero-voltage switching.
Rms	Root-mean-square.
FHA	Fundamental harmonic analysis.
OCP	Optimal control point.
PI	Proportional-integral.
THDv	Total voltage harmonic distortion.
DB	Dead band time.
ISR	Interrupt service routine.

Parameters

L_{k}	Leakage inductor of transformer.
L_{r}	Resonant inductor.
C_{r}	Resonant capacitor.
L_{dc}	Filter inductor on the dc side.
C_{dc}	Filter capacitor on the dc side.
L_{g}	Filter inductor on the ac side.
C_{g1}, C_{g2}	Filter capacitors on the ac side.
C_{g3}, C_{g4}	Capacitor bridge on the ac side.
$\mathrm{S}_{1\_\mathrm{dc}}$–$\mathrm{S}_{4\_\mathrm{dc}}$	Switches on the dc side.
$\mathrm{S}_{1\_\mathrm{ac}}$–$\mathrm{S}_{2\_\mathrm{ac}}$	Switches on the ac side.
L_{m}	Magnetizing inductor
n_{Dg} (n_{D}:n_{g})	Turns ratio.
θ_{ab}, θ'_{ab}	Interphase shift.
α_{ac}, α'_{ac}	Intraphase shift.
f_{sw}	Switching frequency.
p_{DB}	Instantaneous output power in DBSRC.
$p_{\mathrm{DB(req)}}$	Required instantaneous output power in DBSRC.
p_{ac}	Ac load power.
v_g	Ac voltage.
i_g	Ac current.
V_{g}	Amplitudes of ac voltage.
I_{g}	Amplitudes of ac current.
P_{con}	Conduction losses.
P_{sw}	Switching losses.
P_{o}	Output power.
v_{ab}	Voltage across the midpoints of dc-side bridge.
v_{cd}	Voltage across the midpoints of ac-side bridge.
i_{ab}	Current on the primary side of transformer.
i_{cd}	Current on the secondary side of transformer.
$i_{\mathrm{ab.rms}}$	Rms current of i_{ab}.
v'_{cd}	Reflected voltage of v_{cd} on dc side.
i'_{cd}	Reflected current of i_{cd} on dc side.
ω_{r}	Resonant angular frequency of the resonant tank.
T	Interrupt service routine (ISR) period.
T_1	Execution time of the interrupt function on CPU1.
T_2	Communication time between CPU1 and CPU2.
T_{active}	Active computation time.

Variables

M	Voltage gain.
f_{sw_min}	Minimum switching frequency.
f_{sw_max}	Maximum switching frequency.
$i_{\mathrm{ab.rms}}$	Rms current of i_{ab}.
θ'_{ab_cr1}	Proposed optimal θ'_{ab} under the condition in (19.1).
θ'_{ab_cr2}	Proposed optimal θ'_{ab} under the condition in (19.2).
θ'_{ab_cr3}	Proposed optimal θ'_{ab} under the condition in (19.3).

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θ'_{ab_cr4}	Proposed optimal θ'_{ab} under the condition in (19.4).
f_{sw_cr1}	Proposed optimal f_{sw} when $M < 1$.
f_{sw_cr2}	Proposed optimal f_{sw} when $M > 1$.
$\alpha'_{\mathrm{ac\_cr}}$	Proposed optimal α'_{ac}.
$f_{\mathrm{sw\_op}}$	Optimal f_{sw}.
i_{g}^{*}	PI controller output of outer voltage loop.
v_{LC}	Voltage applied to the resonant tank.
φ	Phase difference between the v_{ab} and v_{LC}.
$\alpha'_{\mathrm{ac(A)}}$	α'_{ac} at Point A.
$\alpha'_{\mathrm{ac(B)}}$	α'_{ac} at Point B.
$\alpha'_{\mathrm{ac(C)}}$	α'_{ac} at Point C.
$\alpha'_{\mathrm{ac(D)}}$	α'_{ac} at Point D.
$\theta'_{\mathrm{ab(C)}}$	θ'_{ab} at Point C.
$\theta'_{\mathrm{ab(D)}}$	θ'_{ab} at Point D.

I. Introduction

SINGLE-stage single-phase dual-bridge series resonant dc–ac converters (DBSRC) (see Fig. 1) have gained increasing attention in applications such as solar inverters [1], [2], electric vehicles [3], and energy routers [4]. Compared to conventional two-stage single-phase dc–ac configurations (e.g., a dc–Jing hang stage and a dc–ac inverter stage), this type of converter has reduced component count, simpler circuit structure, and potentially higher power-conversion efficiency [5], [6], [7].

While it has been well understood that control has significant influence on DBSRC's efficiency [8], [9], realizing real-time optimal control of DBSRC for maximum efficiency is generally challenging. Typical degrees of control freedom in DBSRC include interphase shift of primary-side and secondary-side switches, intraphase shift between the primary and the secondary-side switches, and the operating frequency [10], [11], [12], [13]. While increasing the degrees of control compared to single-phase-shift (SPS) can reduce power losses, it also introduces control challenges [14], [15], [16]. The primary challenges in optimal real-time control of DBSRC are twofold: 1) the nonlinear and complex relationships between degrees of control freedom, system efficiency under varying operating points, particularly due to the wide voltage gain range [17], and 2) the need to simultaneously control the dynamic instantaneous power to meet the ac load demand while ensuring a high power factor and zero-voltage switching (ZVS). Consequently, optimal control solutions for DBSRC often come in an excessively complicated analytical form [18] or require iterative numerical solving [19], [25]. In both cases, a typical DSP used in power electronics struggles to meet the computational demands, making real-time optimal control difficult to implement.

Various control strategies with multiple control variables have been proposed to improve the efficiency of DBSRC or that of similar converters, such as dual active bridge (DAB) based dc–ac converter [18], [19], [20], [21], [22], [23], [24], [25], [26], [27]. However, due to the control complications, existing strategies generally seek a tradeoff between real-time control capability and maximum power efficiency. In particular, they either adopt 1) a real-time but non-optimal control strategy, which only considers limited sources of power losses (e.g., losses associated with backflow current of the input side [20], circulating power [21]) to simplify the control, or 2) an optimal but offline control strategy, where control variables at different operating points are precomputed offline and stored in lookup tables [4], [18], [19], [24], [25], [26]. The latter approach requires solving a multivariable, multiconstraint nonlinear optimization problem using advanced intelligent algorithm or numerical optimization tools. While effective for known and predetermined operating points, its robustness is limited, as storing control parameters for all possible operating conditions is impractical.

To address the above control challenge, this article proposes a real-time optimal control strategy for the DBSRC that features an online efficiency optimization block. Its core is the development of a set of closed-form analytical optimal control solutions that are general and applicable to any operating conditions. The derivation is made possible by leveraging the unique properties of DBSRC at different voltage conversion ratios, which will be explained in detail in the following. These properties allow us to significantly simplify the derivation process to achieve optimal or near-optimal performance. The performance of recently published works is summarized in Table III for comparison with this work.

The rest of this article is organized as follows. Section II details the optimal control problem of DBSRC studied in this article. Section III discusses the proposed solution to the control problem. Section IV presents a case study of the proposed control strategy. Section V outlines the architecture design for the control loop. Section VI provides experimental verification based on a laboratory prototype. Finally, Section VII concludes this article. Additionally, the Appendix includes the derivation of key variables and a nomenclature listing the acronyms, variables, and parameters used throughout the article.

II. Problem Formulation

A. Topology and Operating Principles

To facilitate understanding of the control challenges for achieving maximum efficiency and output power regulation, we first conduct a review of the basic circuit topology and the operating principles of the DBSRC. Fig. 1 illustrates the topology of the converter studied in this article. It consists of a full-bridge inverter on the dc side (i.e., S_{1_dc}–S_{4_dc}), a half-bridge cycloconverter on the ac side (i.e., S_{1_ac}–S_{2_ac}, C_{g3}, C_{g4}); a resonant tank (i.e., L_r and C_r) and a transformer with magnetizing inductance L_m and turns ratio n_{Dg} (n_D:n_g) for power transfer and galvanic isolation; an *LC* filter (i.e., L_{dc} and C_{dc}) for attenuating the low-frequency and high-frequency ripple on the dc voltage side V_{dc}; and a *CLC* filter (i.e., L_g, C_{g1}, and C_{g2}) for attenuating the high-frequency ripples on the ac voltage side v_g.

Fig. 2 shows the typical operating waveforms of the DBSRC. On the primary side of the transformer and before the resonant tank, the full-bridge inverter generates a three-level high-frequency voltage pulse train v_{ab}, with an amplitude of V_{dc}. On the secondary side of the transformer, the cycloconverter generates another set of high-frequency voltage pulse train v_{cd}, with an amplitude of $v_g/2$. The duty cycles of V_a, V_b, V_c are set to

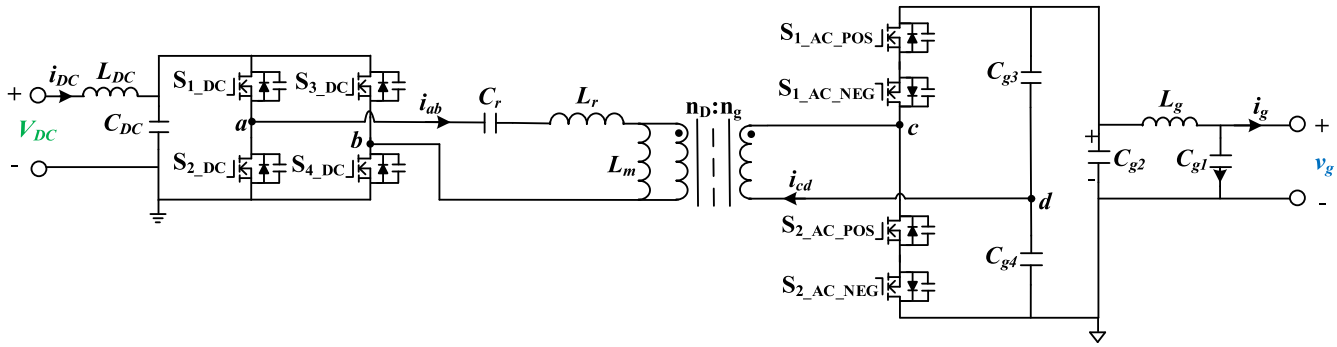

Fig. 1. Topology of the DBSRC studied in this article.

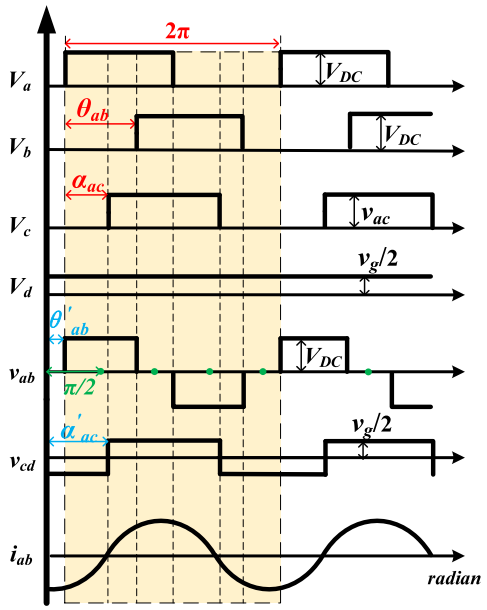

Fig. 2. Switching waveforms during $v_g > 0$.

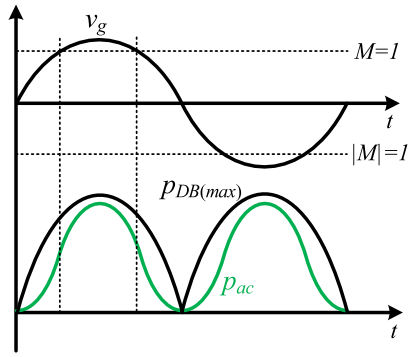

Fig. 3. Power transfer over one line period (note: M is the voltage conversion ratio, and $p_{\mathrm{DB}}(\max)$ is the maximum power that the DBSRC can transfer).

50%. With a half-bridge cycloconverter configuration, there are three possible control degrees of freedom: the interphase shift θ_{ab} of the two inverter legs' voltages (V_{a} and V_{b}), the intraphase shift α_{ac} between the inverter and the cycloconverter legs (V_{a} and V_{c}), and the operating frequency of the system f_{sw}.

In this article, all three control variables, θ_{ab}, α_{ac}, and f_{sw} are used to operate the converter. For ease of discussion, alternative control variables, α'_{ac} and θ'_{ab} (defined in (1) and shown in Fig. 2) are used in lieu of α_{ac} and θ_{ab} thereafter. α'_{ac} denotes the phase shift between the fundamental components of v_{ab} and v_{cd}, and θ'_{ab} denotes the time interval (in radians) when $v_{\mathrm{ab}} = 0$ for each quarter of the switching period

$$\begin{cases} \theta'_{ab} = \frac{\pi-\theta_{ab}}{2} \quad (0 \le \theta'_{ab} \le \frac{\pi}{2}) \\ \alpha'_{\mathrm{ac}} = \alpha_{\mathrm{ac}} + \frac{\pi}{2} - \frac{\theta_{ab}}{2} \quad (-\frac{\pi}{2} \le \alpha'_{\mathrm{ac}} \le \frac{\pi}{2}) \end{cases}. \tag{1}$$

B. Problem Formulation

The general problem considered in this article is how to control θ'_{ab}, α'_{ac}, and f_{sw} within their respective operating ranges such that 1) the power losses of the DBSRC are minimized, and 2) the instantaneous output power p_{DB} of the DBSRC matches the ac load power p_{ac}. For a resistive load, p_{ac} is given by (also see Fig. 3)

$$\begin{aligned} p_{\mathrm{ac}} &= V_g \sin(\omega_g t) I_g \sin(\omega_g t) \\ &= \frac{1}{2} V_g I_g - \frac{1}{2} V_g I_g \cos(2\omega_g t) \end{aligned} \tag{2}$$

where V_{g} and I_{g} are the amplitudes of ac voltage v_g and the ac current i_g.

The power losses of the system mainly include the conduction losses P_{con} and the switching losses P_{sw}. To minimize P_{con}, the conduction currents i_{ab} and i_{cd} on both sides of the system should be minimized; to minimize P_{sw}, ZVS turn-ON for all switches should be realized. Therefore, the general problem can be formulated as an optimization problem, as defined in

$$\min_{\alpha'_{\mathrm{ac}} \in \Lambda,\ \theta'_{ab} \in \Theta,\ f_{sw} \in \Gamma} i_{ab.\mathrm{rms}}\left(\alpha'_{\mathrm{ac}}, \theta'_{ab}, f_{sw}\right) \tag{3}$$

subject to

$$p_{DB}(\alpha'_{\mathrm{ac}}, \theta'_{ab}, f_{sw}) = p_{\mathrm{ac}} \tag{4}$$

$$\begin{cases} i_{ab}(t_{sw}; \alpha_{\mathrm{ac}}, \theta_{ab}, f_{sw})|_{t_{sw}=-\frac{\theta'_{ab}}{2\pi f_{sw}}} \le 0 & (5.1) \\ i_{ab}(t_{sw}; \alpha_{\mathrm{ac}}, \theta_{ab}, f_{sw})|_{t_{sw}=+\frac{\theta'_{ab}}{2\pi f_{sw}}} \le 0 & (5.2) \end{cases} \tag{5}$$

$$i_{ab}(t_{sw}; \alpha_{\mathrm{ac}}, \theta_{ab}, f_{sw})|_{t_{sw}=\frac{\alpha'_{\mathrm{ac}}}{2\pi f_{sw}}} \ge 0 \tag{6}$$

where

$$\Lambda = \left[-\frac{\pi}{2}, \frac{\pi}{2}\right] \tag{7}$$

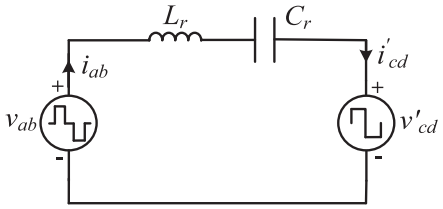

Fig. 4. DBSRC's equivalent circuit.

$$\Theta = \left[0, \frac{\pi}{2}\right] \tag{8}$$

$$\Gamma = \left[f_{sw\_\min}, f_{sw\_\max}\right]. \tag{9}$$

Here, (3) seeks to minimize $P_{\rm con}$ by minimizing $i_{ab.\rm rms}$, i.e., the root-mean-square (rms) value of i_{ab} over one switching period; (4) is the instantaneous power requirement for the transferred power $p_{\rm DB}$ in the DBSRC; (5) and (6) seek to minimize P_{sw} by achieving ZVS turn-ON for all switches on the primary and secondary sides, respectively; and (7)–(9) set the operating constraints for the control variables.

In (3), we have assumed that minimizing i_{ab} would also minimize $i_{\rm cd}$, and thus $P_{\rm con}$. This is a reasonable assumption since the magnetizing inductance $L_{\rm m}$ in the DBSRC is generally large, resulting in a negligible magnetizing current $i_{\rm Lm}$. Therefore $i_{\rm cd} = n_{Dg}*(i_{ab}\text{-}i_{\rm Lm}) \approx n_{Dg}*i_{ab}$. Such an assumption simplifies the optimization task as there is no need to derive the accurate mathematical expression for $i_{\rm cd}$, which can be complicated and computationally expensive from the control point of view. In (9), $f_{sw\_\min}$ must be set higher than the resonant frequency $f_{\rm r}$ of the resonant tank to ensure inductive region operation for the purpose of ZVS, and $f_{sw\_\max}$ can be set based on user specifications.

The mathematical expression of key state variables, like $i_{ab.\rm rms}$, $p_{\rm DB}$, can be obtained through fundamental harmonic analysis (FHA) of the equivalent circuit of the DBSRC, as shown in Fig. 4. Here, $v'_{\rm cd}$ and $i'_{\rm cd}$ are the reflected $v_{\rm cd}$ and $i_{\rm cd}$ from the secondary side (ac side) to the primary side (dc side), respectively. For example, $p_{\rm DB}$ can be derived as (10). The expressions of other key variables are shown in Appendix, e.g., $i_{ab.\rm rms}$ has been derived in Appendix A

$$\begin{aligned} p_{DB} &= \frac{4n_{Dg}V_{\rm dc}|v_g|\sin(\alpha'_{\rm ac})\cos(\theta'_{ab})}{L_r\pi^2(2\pi f_{sw} - \frac{{\omega_r}^2}{2\pi f_{sw}})} \\ &= p_{DB(\max)}\sin(\alpha'_{\rm ac})\cos(\theta'_{ab}) \end{aligned} \tag{10}$$

where $p_{\rm DB(max)}$ is the maximum power that the DBSRC can transfer with a switching frequency of f_{sw} (see (11)), and $\omega_{\rm r}$ is the resonant angular frequency of the $L_{\rm r}$-$C_{\rm r}$ resonant tank

$$p_{\rm DB(max)} = \frac{4n_{Dg}V_{\rm dc}|v_g|}{L_r\pi^2(2\pi f_{sw} - \frac{{\omega_r}^2}{2\pi f_{sw}})}. \tag{11}$$

III. Solving the Optimization Problem

A. General Analysis of the Optimization Problem

To facilitate the derivation, we transform (3) into its analytical form below. In particular, to achieve the objective in (3), ideally θ'_{ab}, $\alpha'_{\rm ac}$, and f_{sw} should meet (12), (13), and (14) simultaneously. The solutions of (12), (13), and (14) are the optimal values of control variables to minimize $i_{ab.\rm rms}$. Therefore, the optimization problem can be redefined as (12)–(14) and (4)–(9)

$$\frac{\partial i_{ab.\rm rms}}{\partial \theta'_{ab}} = 0 \tag{12}$$

$$\frac{\partial i_{ab.\rm rms}}{\partial f_{sw}} = 0 \tag{13}$$

$$\frac{\partial i_{ab.\rm rms}}{\partial \alpha\prime_{\rm ac}} = 0. \tag{14}$$

From (12)–(14) and (4)–(9), we can see that there are four equations and three inequalities. However, with three control degrees of freedom, one can only achieve three independent equations at the most. Therefore, it may or may not be possible to satisfy all optimization equations and inequalities. As will be discussed below, whether or not (12)–(14) and (4)–(9) can be achieved depends on the instantaneous voltage conversion ratio M (as defined in (15) and illustrated in Fig. 3) and the frequency constraints (9). For cases where only a limited optimization equations and inequalities can be achieved, careful tradeoff among the optimization equations is required

$$M = \frac{n_D}{n_g}\frac{|v_g|/2}{V_{\rm dc}} = n_{Dg}\frac{|v_g|/2}{V_{\rm dc}}. \tag{15}$$

B. Optimal Control Point: $M < 1$ and Without Frequency Limits

In this section, we show that (12)–(14) and (4)–(6) can be achieved simultaneously when $M < 1$ and without frequency limits. We also derive the corresponding optimal control conditions. The derivation is based on the following three key observations.

1) The joint solutions of (12) and (4) for θ'_{ab} and $\alpha'_{\rm ac}$ are identical to those of the boundary of (6) and (4), as shown in (19.3) and (20).
2) Subject to the solutions of 1), $i_{ab.\rm rms}$ is independent of f_{sw}, as shown in Appendix E.
3) Solutions of (12) and (14) for $\theta'_{\rm ab}$ and $\alpha'_{\rm ac}$ are identical [10].

As 1), 2), and 3) above suggest that we can mathematically remove (12), (13), and (14) from the optimization problem without altering the optimization results, and that the optimal θ'_{ab} and $\alpha'_{\rm ac}$ must satisfy (4) and the boundary of (6). The optimal solutions are, as shown in (19.3) and (20). Note that the optimal θ'_{ab} and $\alpha'_{\rm ac}$ are f_{sw} dependent.

To determine the optimal f_{sw}, we further illustrate the trajectories of θ'_{ab} and $\alpha'_{\rm ac}$ based on (4), (5), and (6) in Figs. 5 and 6 (for higher f_{sw}), Fig. 7 (for lower f_{sw}). It can be observed that.

1) At a higher f_{sw} ($f_{sw} > f_{sw\_cr1}$), the optimal θ'_{ab} and $\alpha'_{\rm ac}$ (i.e., corresponding to the optimal control point (OCP) in Fig. 6 where the (4) and (6) curves intersect) can also satisfy (5.1) and (5.2), but with excessive turn-OFF current to facilitate ZVS turn-ON and higher switching losses at elevated switching frequency.

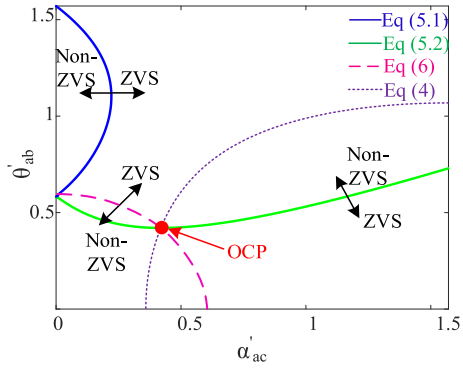

Fig. 5. Operation trajectories when $M < 1$ and $f_{sw} = f_{sw\_cr1}$.

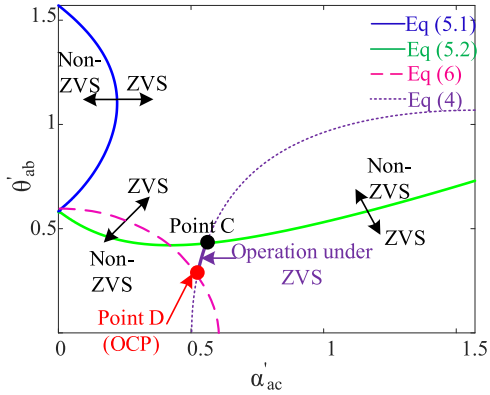

Fig. 6. Operation trajectories when $M < 1$ and $f_{sw\_cr1} < f_{sw\_min} = f_{sw}$.

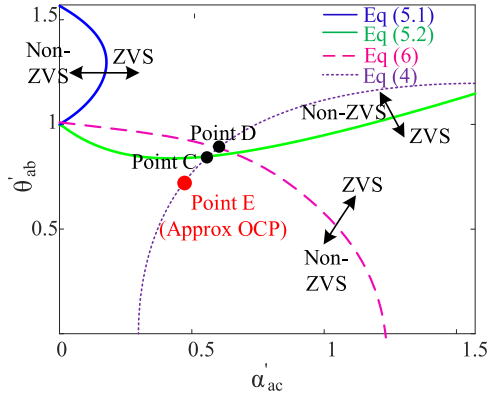

Fig. 7. Operation trajectories when $M < 1$ and $f_{sw\_cr1} > f_{sw\_max} = f_{sw}$.

2) At a lower f_{sw} ($f_{sw} < f_{sw\_cr1}$), the derived $\theta'_{\rm ab}$ and $\alpha'_{\rm ac}$ (corresponding to the point D in Fig. 7) can satisfy (6) but tend to lose (5.2) and, thus, higher switching losses.

Therefore, there exists a critical switching frequency f_{sw_cr1} at which the optimal θ'_{ab} and $\alpha'_{\rm ac}$ not only satisfy (6) but sit precisely on the curve associated with (5.2) (see Fig. 5). This f_{sw_cr1} is, thus, the optimal f_{sw}, as the corresponding switching losses are minimized. f_{sw_cr1} can be solved by combining (4) with the boundaries of (5.2) and (6), where the result is shown in (16) and the derivation is shown in Appendix B. The corresponding θ'_{ab} and $\alpha'_{\rm ac}$ are determined from (19.3) and (20). Equations (16)–(20) shown at the bottom of the next page.

C. Optimal Control Point: $M > 1$ and Without Frequency Limits

Unlike the $M < 1$ case, (12)–(14) become independent equations when $M > 1$. Thus, only three out of the four equations (12)–(14) and (4) can be achieved by controlling $\theta'_{\rm a}$, $\alpha'_{\rm ac}$, and f_{sw}. Here, we prioritize (12), (13), and (4). The reason for selecting these three equations to solve for OCP is as follows.

1) Solving (12) for θ'_{ab} gives a simple analytical solution (i.e., $\theta'_{ab} = \theta'_{ab\_cr1}$, see (19.1)). This simplicity is useful for real-time controller implementation.
2) Realizing (4) is essential for achieving a sinusoidal output voltage. Here, we solve (4) for α'_{ac} due to its easy controllability in the full power range, with the solution shown in (20).
3) Solving (13) for an analytical form of f_{sw} is challenging due to its complexity and nonlinearity. However, we show below that solving the boundary of (5.2) for f_{sw}, under the condition of OCP's θ'_{ab} and $\alpha'_{\rm ac}$ above, gives an analytical solution ($f_{sw} = f_{sw\_cr2}$, shown in (7) and Appendix C) that is almost identical to the OCP's f_{sw} solution obtained from direct numerical solving (13). Therefore, satisfying (13) would suggest that the ZVS condition (5.2) is automatically met. It also allows one to use analytical form of f_{sw} for controller implementation to approximate OCP's f_{sw}.

To show that f_{sw_cr2} is close to OCP's f_{sw}, Fig. 8 illustrates the relationship between $i_{ab.\rm rms}$ and f_{sw} under the following operating conditions: $v_{\rm g} = 115$ V, $p_{\rm ac} = 100$ W, $\theta'_{ab} = \theta'_{ab\_cr1}$, and $\alpha'_{\rm ac} = \alpha'_{\rm ac\_cr}$. The OCP's f_{sw} (see the f_{sw_op} point) occurs at 140.2 kHz where $i_{\rm ab.rms}$ is minimum. The OCP's f_{sw} is nearly identical to $f_{sw\_cr2} = 140.5$ kHz. The effectiveness of using f_{sw_cr2} to approximate OCP's f_{sw} will be further verified for a wider range of operating conditions in Section IV–B.

Fig. 9 further shows the trajectories of $\theta'_{\rm ab}$ and $\alpha'_{\rm ac}$ at $f_{sw} = f_{sw\_cr2}$. It can be observed that OCP's θ'_{ab} and $\alpha'_{\rm ac}$ precisely sit on the curves corresponding to (5.1) and (5.2). Such an observation suggests that the primary-side switching losses are minimized. On the other hand, Fig. 9 shows no curves corresponding to (6). The reason is that under the current condition and within the physical operating range of θ'_{ab} and $\alpha'_{\rm ac}$, ZVS turn-ON of the secondary-side switches is always achieved.

The $M = 1$ line and the two critical frequencies lines $f_{sw} = f_{sw\_cr1}$ and $f_{sw} = f_{sw\_cr2}$ define two operating regions of the DBSRC, referred to Region 1 and Region 2 in Fig. 10. In both regions, ZVS turn-ON of all switches can be achieved invariably. At the critical frequencies, optimal control performance can be achieved. Outside these regions (i.e., $f_{sw} < f_{sw\_cr1}$ or $f_{sw} < f_{sw\_cr2}$), ZVS turn-ON is lost for at least one switch in the DBSRC, resulting in nonoptimal solutions. It is noted that f_{sw_cr1} and f_{sw_cr2} yield the identical value at $M = 1$, as shown in (18).

D. Optimal Control Point With Frequency Limits

In Sections III–B and III–C, the optimal $f_{sw} = f_{sw\_cr}$ is shown to depend on M and $p_{\rm ac}$, both of which vary over time. Therefore, when considering the frequency limits specified in (9), i.e.,

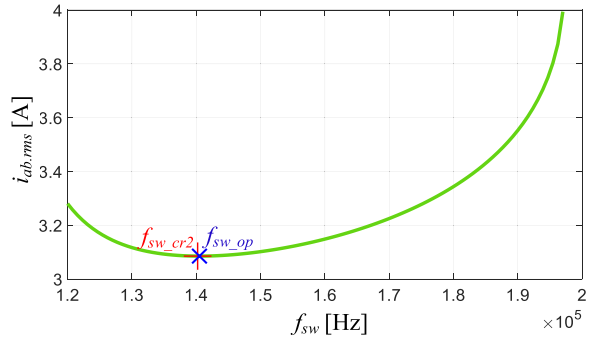

Fig. 8. $i_{ab.\mathrm{rms}}$ versus f_{sw} under $v_{\mathrm{g}} = 115$ V and $p_{\mathrm{ac}} = 100$ W.

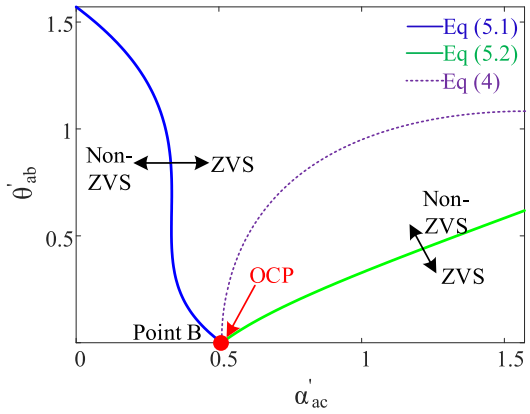

Fig. 9. Operation trajectories when $M > 1$ and $f_{\mathrm{sw}} = f_{\mathrm{sw\_cr2}}$.

$f_{sw\_\min} \le f_{sw} \le f_{sw\_\max}$, f_{sw_cr} may or may not fall inside these operating constraints due to the wide variation range of M and p_{ac}. Therefore, it is necessary to discuss the OCP when frequency limits are considered. Depending on where f_{sw_cr} lies with respect to $f_{sw\_\min}$ and $f_{sw\_\max}$, there are six possible

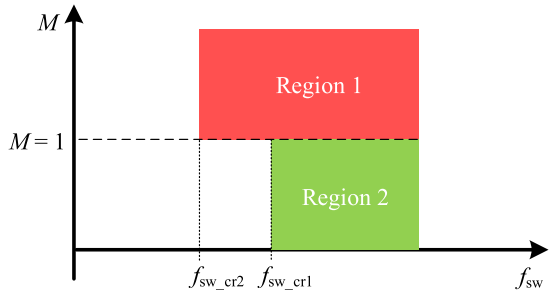

Fig. 10. ZVS region without frequency limits.

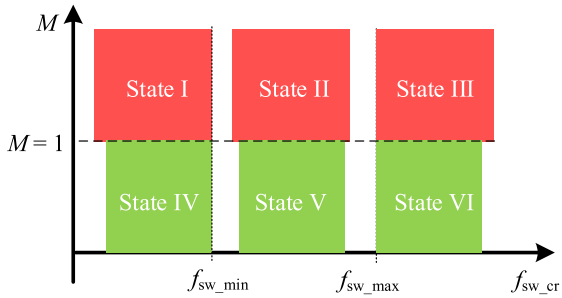

Fig. 11. Operating states considering f_{sw} constraints.

operating states, as shown in Fig. 11. The corresponding OCPs are discussed below.

State I: $M > 1$, $f_{sw\_cr2} < f_{sw\_\min} < f_{sw\_\max}$. In this state, the system operates inside Region 1. However, f_{sw_cr2} cannot be realized as it is less than $f_{sw\_\min}$. The trajectories of θ'_{ab} and α'_{ac} at a f_{sw} greater than f_{sw_cr2} are shown in Fig. 12. It shows that under $\{\theta'_{ab\_cr1}, \alpha'_{\mathrm{ac}\_cr}\}$ (Point A), the objectives from Section III–C can still be achieved, except that the system operates in the deep ZVS region rather than at its boundary. To minimize P_{sw}, f_{sw} should be minimized, i.e., $f_{sw} = f_{sw\_\min}$.

$$f_{sw\_cr1} = \frac{2C_r V_{\mathrm{dc}} |v_g| n_{Dg} \sqrt{\frac{|v_g| n_{Dg}(2V_{\mathrm{dc}} - |v_g| n_{Dg})}{4{V_{\mathrm{dc}}}^2}}}{2\pi^3 C_r L_r p_{\mathrm{ac}}} + \frac{\sqrt{C_r(\pi^4 L_r {p_{\mathrm{ac}}}^2 - C_r |v_g|^4 {n_{Dg}}^4 + 2C_r V_{\mathrm{dc}} |v_g|^3 {n_{Dg}}^3)}}{2\pi^3 C_r L_r p_{\mathrm{ac}}} \tag{16}$$

$$f_{sw\_cr2} = \frac{4C_r {V_{\mathrm{dc}}}^2 \sqrt{\frac{-4{V_{\mathrm{dc}}}^2 + {n_{Dg}}^2 {v_g}^2}{4{V_{\mathrm{dc}}}^2}}}{2\pi^3 C_r L_r p_{\mathrm{ac}}} + \frac{\sqrt{C_r(\pi^4 L_r {p_{\mathrm{ac}}}^2 - 16C_r {V_{\mathrm{dc}}}^4 + 4C_r {V_{\mathrm{dc}}}^2 {n_{Dg}}^2 {v_g}^2)}}{2\pi^3 C_r L_r p_{\mathrm{ac}}} \tag{17}$$

$$f_{sw\_cr1}|_{M=1} = f_{sw\_cr2}|_{M=1} = \frac{1}{2\pi\sqrt{C_r L_r}} = f_r \tag{18}$$

$$\begin{cases} \theta\prime_{ab\_cr1} = 0, \text{ when } M \ge 1 \quad (19.1) \\ \theta'_{ab\_cr2} = \arccos\left(\min\left\{1, \sqrt{M^2 + \left(\frac{p_{\mathrm{ac}}}{p_{DB(\max)}}\right)^2}\right\}\right), \text{ when } f_{sw\_cr1} \le f_{sw\_\min} \ \&\ M < 1 \quad (19.2) \\ \theta\prime_{ab\_cr3} = \arccos\left(\sqrt{M^2 + \left(\frac{p_{\mathrm{ac}}}{p_{DB(\max)}}\right)^2}\right), \text{ when } f_{sw\_\min} < f_{sw\_cr1} < f_{sw\_\max} \ \&\ M < 1 \quad (19.3) \\ \theta\prime_{ab\_cr4} \approx \max\left(\arccos\left(\frac{M + \sqrt{M^2 + 4\frac{p_{\mathrm{ac}}}{p_{DB(\max)}}}}{2}\right), \theta\prime_{ab\_cr2}|_{f_{sw}=f_{sw\_\max}}\right), \text{ when } f_{sw\_cr1} \ge f_{sw\_\max} \ \&\ M < 1 \quad (19.4) \end{cases} \tag{19}$$

$$\alpha\prime_{\mathrm{ac}\_cr} = \arcsin\left\{\frac{L_r \pi^2 (2\pi f_{sw} - \frac{{\omega_r}^2}{2\pi f_{sw}}) p_{\mathrm{ac}}}{4 n_{Dg} V_{\mathrm{dc}} |v_{\mathrm{ac}}| \cos(\theta'_{ab})}\right\} = \arcsin\left(\frac{p_{\mathrm{ac}}}{p_{DB(\max)} \cos(\theta'_{ab})}\right) \tag{20}$$

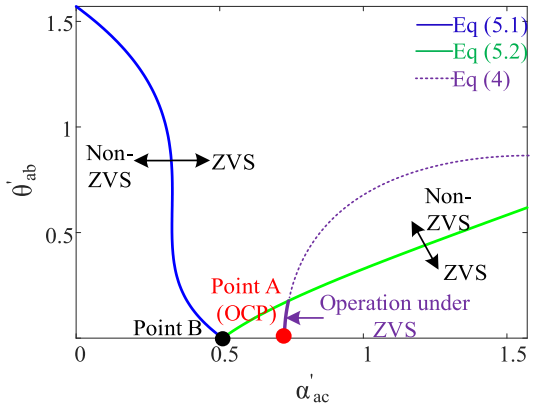

Fig. 12. Operation trajectories when $M > 1$ and $f_{sw\_cr2} < f_{sw\_min} = f_{sw}$.

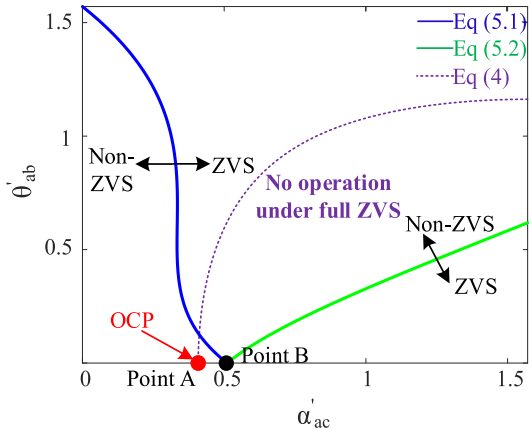

Fig. 13. Operation trajectories when $M > 1$ and $f_{sw\_cr2} > f_{sw\_max} = f_{sw}$.

Therefore, the corresponding OCP should be $\{\theta'_{ab\_cr1}, \alpha'_{ac\_cr}, f_{sw\_min}\}$.

State II: $M > 1, f_{sw\_min} < f_{sw\_cr2} < f_{sw\_max}$. In this state, the system always operates on the boundary of Region 1. Therefore, the optimal control solution is identical to the case without f_{sw} limits, $\{\theta'_{ab\_cr1}, \alpha'_{ac\_cr}, f_{sw\_cr2}\}$.

State III: $M > 1, f_{sw\_min} < f_{sw\_max} < f_{sw\_cr2}$. In this state, the system can only operate outside Region 1, i.e., ZVS cannot be achieved for all switches. The trajectories of θ'_{ab} and α'_{ac} at a f_{sw} lower than f_{sw_cr2} are shown in Fig. 13. In this case, $\{\theta'_{ab\_cr1}, \alpha'_{ac\_cr}\}$ (Point A) remains the optimal operating point due to the minimized rms current. The optimal θ'_{ab} and α'_{ac} are found to be identical to $\{\theta'_{ab\_cr1}, \alpha'_{ac\_cr}\}$ with $f_{sw} = f_{sw\_max}$.

State IV: $M < 1$, $f_{sw\_cr1} < f_{sw\_min} < f_{sw\_max}$. Similar to State I, the system operates inside Region 2 and f_{sw_cr1} cannot be achieved. The optimal solution is, thus $\{\theta'_{ab\_cr2}, \alpha'_{ac\_cr}, f_{sw\_min}\}$.

State V: $M < 1, f_{sw\_min} < f_{sw\_cr1} < f_{sw\_max}$. Similar to State II, the system always operates on the boundary of Region 2. Thus, the optimal control solution is $\{\theta'_{ab\_cr3}, \alpha'_{ac\_cr}, f_{sw\_cr1}\}$.

State VI: $M < 1$, $f_{sw\_min} < f_{sw\_max} < f_{sw\_cr1}$. Similar to State III, the system cannot operate within Region 2. The corresponding trajectories of θ'_{ab} and α'_{ac} at a f_{sw} lower than f_{sw_cr1} are shown in Fig. 7. In this case, Point C is the OCP

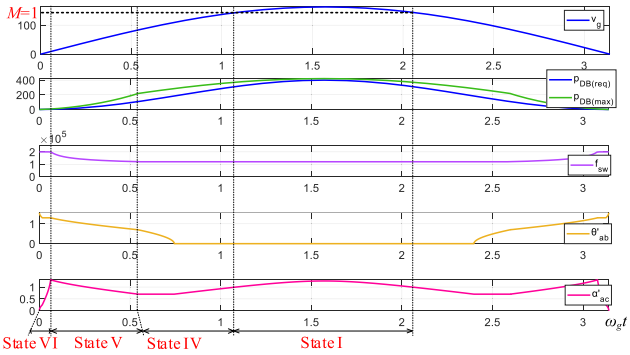

Fig. 14. Trajectories of control variables under heavy load.

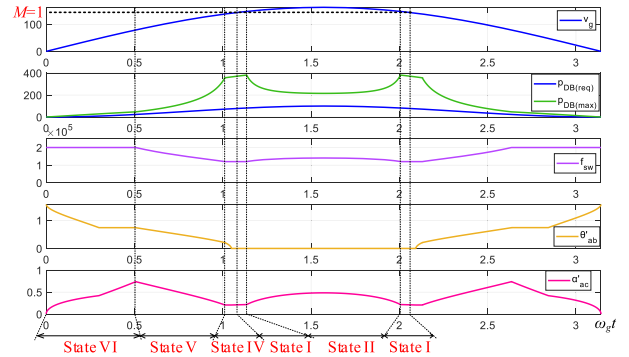

Fig. 15. Trajectories of control variables under light load.

because primary-side ZVS takes priority at low M for the efficiency optimization. It should be noted that deriving an exact analytical solution for Point C [from (37)] is challenging, thus, mathematical simplification techniques are applied, resulting in the approximate solution provided in (19.4), corresponding to Point E in Fig. 7. This solution represents a practical, albeit approximately suboptimal point, due to the simplification. Thus, the optimal control solution is $\{\theta'_{ab\_cr4}, \alpha'_{ac\_cr}, f_{sw\_max}\}$.

IV. Case Study

A. Trajectories of Optimal Control Point

Based on Section III–D, the trajectories of the control variables are plotted against v_g and p_{ac} (i.e., $p_{DB(req)}$) in Figs. 14 and 15, for heavy load (Max(p_{ac}) = 400 W) and light load (Max(p_{ac}) = 100 W), respectively.

As per Fig. 14, near the peak region of v_g, the system operates in State I. The system essentially operates with a SPS modulation, where θ'_{ab} is fixed while α'_{ac} is changing. As v_g decreases until M drops below 1, the system directly transitions to State IV (without going into State II and III), where the variation of θ'_{ab} is also observed. The system, thus, operates with an extended-phase-shift modulation. As v_g continues to decrease, the system enters State V, requiring dynamic variations of f_{sw}. Further reduction of v_g leads to a very low M with f_{sw} eventually reaching f_{sw_max}. This is when the system transitions to State VI. Similar States transitions can be observed from Fig. 15, except the State II is added. Note that State III does not appear until the system operates under much lighter load conditions.

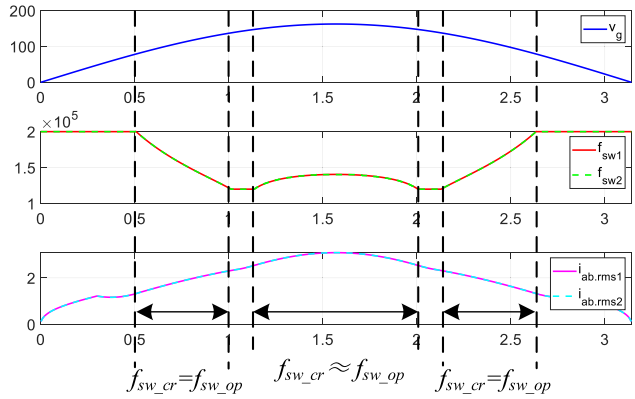

Fig. 16. Trajectories of f_{sw1} and f_{sw2}, and $i_{ab.\mathrm{rms}1}$ and $i_{ab.\mathrm{rms}2}$ under light load.

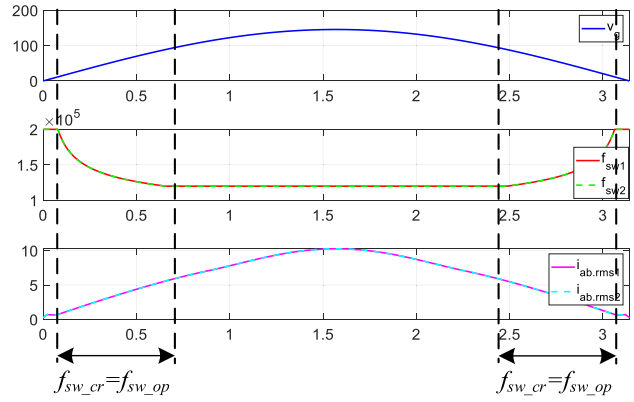

Fig. 17. Trajectories of $f_{\mathrm{sw}1}$ and $f_{\mathrm{sw}2}$, and $i_{\mathrm{ab.rms}1}$ and $i_{\mathrm{ab.rms}2}$ under heavy load.

It is important to note that the transition from one state to another is smooth and continuous over the entire range of line voltages and loads.

B. Verification of $\mathrm{F_{sw}}$ Approximation

To further verify the effectiveness of approximating f_{sw_cr} as f_{sw_op} in Section III–C, Fig. 16 shows two trajectories of switching frequency (i.e., f_{sw1} and f_{sw2}), and the corresponding $i_{ab.\mathrm{rms}}$ waveforms. Here, within the f_{sw} boundary [i.e., (9)], $f_{sw1} = f_{sw\_cr}$, and $f_{\mathrm{sw}2} = f_{sw\_op}$ (where f_{sw_op} at $M > 1$ is calculated through numerical sweeping). It can be observed that the f_{sw} and $i_{ab.\mathrm{rms}}$ trajectories are almost identical in both cases.

Additionally, as illustrated in Fig. 17, f_{sw_cr} consistently aligns with f_{sw_op} under heavy load conditions. This occurs because f_{sw} remains clamped at $f_{sw\_\min}$ throughout the $M > 1$ region.

These findings validate that using f_{sw_cr} as an approximation for f_{sw_op} is valid and does not significantly affect performance.

V. Controller Implementation

A. Control Architecture

Based on the above discussions, a cascaded control architecture is presented in Fig. 18. The architecture consists of an outer voltage regulation loop, an inner optimization loop for efficiency optimization, a polarity switch, and a modulation block.

The outer voltage regulation is realized through the control of $i_{\mathrm{g}}{}^*$, i.e., the reference output current. Here, a Proportional-Integral (PI) controller is used to determine $i_{\mathrm{g}}{}^*$ needed to minimize the voltage tracking error.

The optimization loop is realized by a state machine that can determine the optimal control variables $\{\theta'_{ab}, \alpha'_{\mathrm{ac}}, f_{sw}\}$ based on $i_g{}^*$, v_g, and V_{dc}. The state machine is constructed based on the discussions in Sections III–D and IV and, as shown in Fig. 19. In practice, to achieve ZVS for switches, margins are added to f_{sw_cr} and θ'_{ab_cr} to account for the output capacitance C_{oss} of semiconductor switches and PWM dead time.

The polarity switch ensures α'_{ac} changes in the correct direction. In particular, α'_{ac} should be proportional to the voltage tracking error during the positive half-cycle and inversely proportional during the negative half-cycle. The polarity of v_{g} is determined by a comparator that compares v_{g} with 0 V.

Finally, the modulation block receives the control signals $\{\theta'_{ab}, \alpha'_{\mathrm{ac}}, f_{sw}\}$ and converts them into gate driving signals.

B. Dynamic Performance

To further validate the effectiveness of the proposed control strategy, its dynamic response was evaluated under load transitions from full load to half load and vice versa.

Fig. 20 illustrates the dynamic waveforms of the output ac voltage and current. At t_1, the load is reduced from full load to half load, and at t_2, it returns to full load. As shown in Fig. 20, the output voltage quickly tracks its desired value. Additionally, a nearly identical dynamic response is observed with SPS control, confirming that the proposed real-time control algorithm does not compromise dynamic performance. Since the response is similar, the waveform of SPS control is not repetitively shown here.

C. Other Considerations

To further reduce the computation burden for real-time controller implementation, precomputation can be applied for the terms associated with the hardware parameters of the converter prototype that are typically constant.

1) Precomputation for (16) and (17): Equations (16) and (17) can be reconfigured as (21) and (22). In both equations, $a - k$ are constants derived from hardware parameters. These constants can be calculated offline in advance

$$f_{sw\_cr1} = \frac{\sqrt{hV_{\mathrm{dc}}|v_g|^3 - i|v_g|^4} + \sqrt{cp_{\mathrm{ac}}{}^2 - j|v_g|^4 + kV_{\mathrm{dc}}|v_g|^3}}{fp_{\mathrm{ac}}} \tag{21}$$

$$f_{sw\_cr2} = \frac{\sqrt{-aV_{\mathrm{dc}}{}^4 + bV_{\mathrm{dc}}{}^2|v_g|^2} + \sqrt{cp_{\mathrm{ac}}{}^2 - dV_{\mathrm{dc}}{}^4 + eV_{\mathrm{dc}}{}^2|v_g|^2}}{fp_{\mathrm{ac}}}. \tag{22}$$

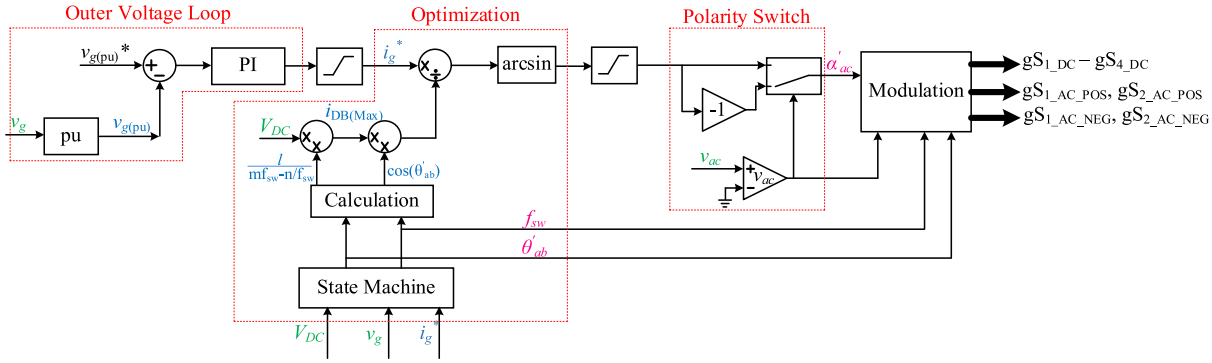

Fig. 18. Proposed control architecture for the DBSRC.

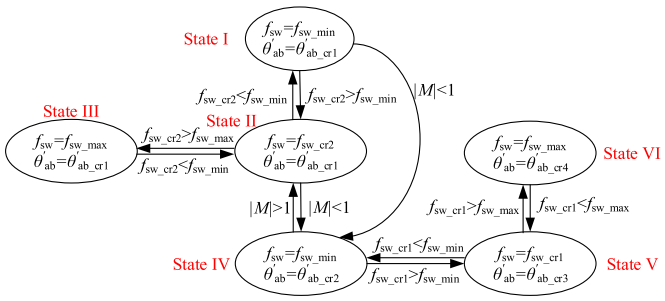

Fig. 19. State machine diagram of the proposed control strategy.

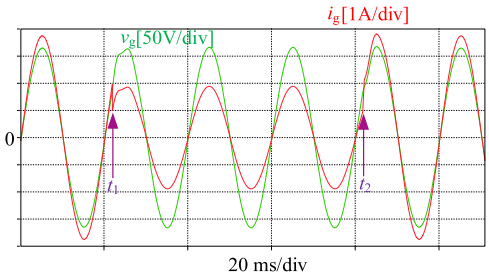

Fig. 20. Dynamic performance of the proposed control strategy.

2) Precomputation for constant terms in (19) and (20): Both equations share a common term, $p_{\rm ac}/p_{\rm DB(max)}$, which can be further derived as

$$\frac{p_{\rm ac}}{p_{DB(\max)}} = \frac{v_g i_g}{v_g i_{DB(\max)}} = \frac{i_g}{i_{DB(\max)}}. \tag{23}$$

Subsequently, the defined $i_{\rm DB(max)}$ in (23) can be deduced as

$$\begin{cases} i_{DB(\max)} = \dfrac{p_{DB(\max)}}{v_g} = \dfrac{4n_{Dg}V_{\rm dc}}{L_r\pi^2(2\pi f_{sw}-\frac{\omega_r{}^2}{2\pi f_{sw}})} = \dfrac{lV_{\rm dc}}{mf_{sw}-\frac{n}{fsw}} \\ l = 4n_{Dg},\ m = 2L_r\pi^3,\ n = \dfrac{L_r\pi\omega_r{}^2}{2} \end{cases}. \tag{24}$$

Here, l, m, and n are constant coefficients specific to the converter and are calculated offline in advance.

VI. Experimental Verifications

To evaluate the performance of the proposed control strategy for the DBSRC, a laboratory prototype was constructed, as shown in Fig. 21. Detailed system specifications and key circuit parameters are listed in Tables I and II. The semiconductor switches on the primary and secondary sides are implemented using Si and GaN devices, respectively. As a proof of concept, this article focuses on the operation under medium to heavy load (150 W–200 W). Given a switching frequency range between 120 kHz–200 kHz, this load range results in only a short period where f_{sw} is clamped to $f_{sw\_\max}$ (see Fig. 14). The proposed control method can also be applied to light load conditions. However, for light load operation, the duration in which f_{sw} is clamped to $f_{sw\_\max}$ is significantly increased (see Fig. 15), resulting in a wider switching frequency range (i.e., higher $f_{sw\_\max}$ required) and additional hardware design complications.

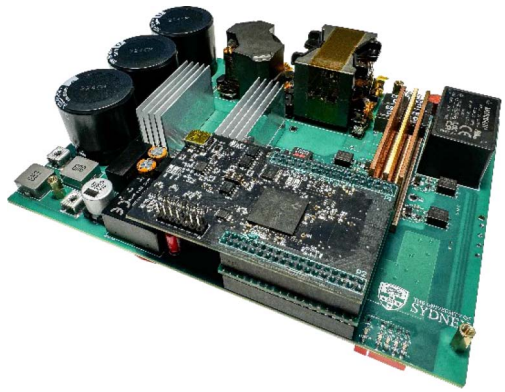

Fig. 21. DBSRC prototype.

TABLE I
Converter Specifications

Specifications	Value/Type
Dc Side Voltage ($V_{\rm dc}$)	36 V
Ac Side Voltage ($v_{\rm g}$)	115 V rms , 50 Hz
Output Power ($P_{\rm o}$)	200 W
Switching Frequency ($f_{\rm sw}$)	120–200 kHz
Dead Band Time (DB)	200 ns (Pri) /100 ns (Sec)

The measurement setup for the prototype includes the Tektronix MSO44 oscilloscope, the Tektronix TCP0030A current probe, the Tektronix THDP0200 differential probe, and the ZLG PA323 power analyzer.

The controller employed in this prototype is the TMS320F28388D from Texas Instruments. This DSP features

TABLE II
CONVERTER COMPONENT PARAMETERS

Components	Value/Type
Dc Side Filter	$L_f = 3.4\,\mu$H, $C_f = 14.1$ mF
Ac Side Filter	$C_{g2} = 2.2\,\mu$F, $L_g = 224\,\mu$H, $C_{g1} = 2.2\,\mu$F
Resonant inductor	$L_r = 10\,\mu$H
Transformer	$n_{Dg} = 9{:}18$, $L_m = 280\,\mu$H, $L_k = 0.46\,\mu$H
Resonant Capacitor	$C_r = 0.23\,\mu$F

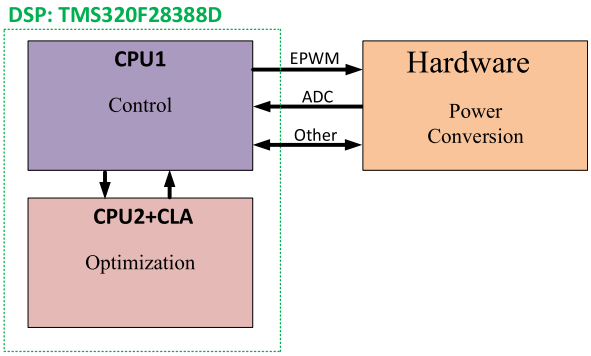

Fig. 22. Overall implementation framework of DBSRC prototype.

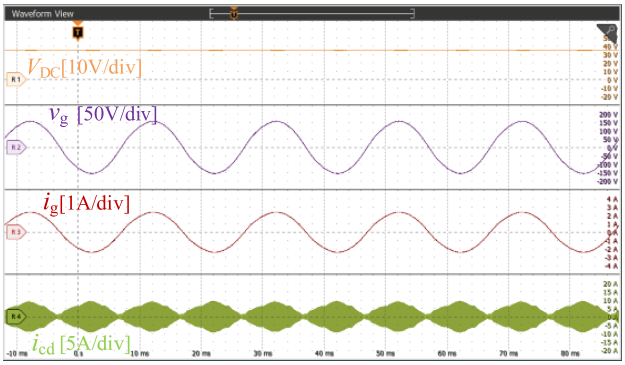

Fig. 23. Operating waveforms of V_{dc}, v_g, i_g, and i_{cd} under proposed control strategy at 200 W output.

specialized hardware blocks optimized for trigonometric calculations needed for executing (19) and (20). It also features two CPUs and two control law accelerators (CLAs) for enhancing the computation speed. Fig. 22 shows the allocation of the computing resources: CPU1 handles PI controller implementation, signal conditioning, and PWM modulation while CPU2 and the CLA handle the optimization part in Fig. 18.

A. Instantaneous Power Control and Conduction Currents

Figs. 23 and 24 illustrate the steady-state operating waveforms of the grid current i_g and the grid voltage v_g of the DBSRC at 200 W and 150 W, respectively, with the proposed control strategy. In both cases, v_g has a sinusoidal waveform, with a total voltage harmonic distortion (THDv) of 2.3% and

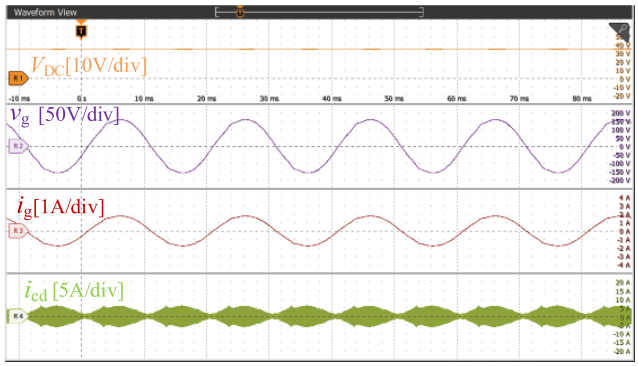

Fig. 24. Operating waveforms of V_{dc}, v_g, i_g, and i_{cd} under proposed control strategy at 150 W output.

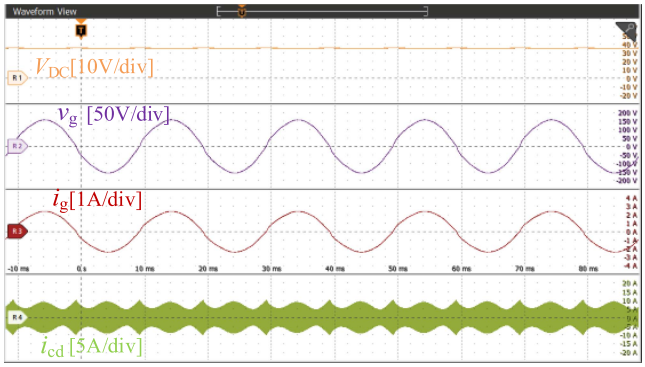

Fig. 25. Operating waveforms of V_{dc}, v_g, i_g, and i_{cd} under SPS control at 200 W output.

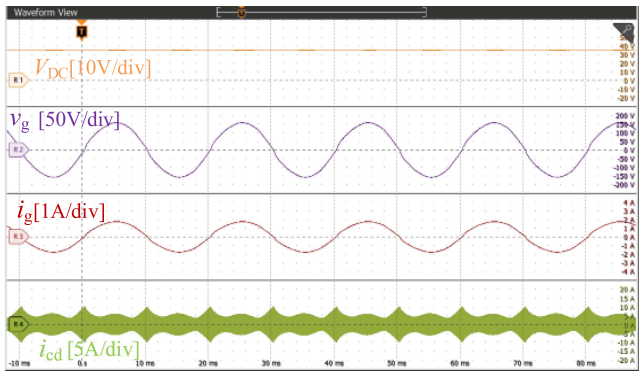

Fig. 26. Operating waveforms of V_{dc}, v_g, i_g, and i_{cd} under SPS control at 150 W output.

2.9%, respectively. These waveforms validate the effectiveness of the proposed control method for instantaneous output power control.

Figs. 25 and 26 further illustrate the operating waveforms of the same system with SPS control at 200 W and 150 W, respectively. The measured THDv is 4.3% and 4.5%, respectively, similar to those with the proposed control. A notable difference between the proposed control method and SPS is the rms current of i_{cd} (i.e., $i_{ab} * n_{Dg} = i_{ab} / 2$). In particular, the proposed control method results in reduced i_{cd} (and, thus, i_{ab}): The rms currents of i_{cd} in Figs. 23 and 26 are 4.2 A, 3.0 A, 5.1 A, and 4.1 A, respectively, representing 17.6% reduction at 200 W

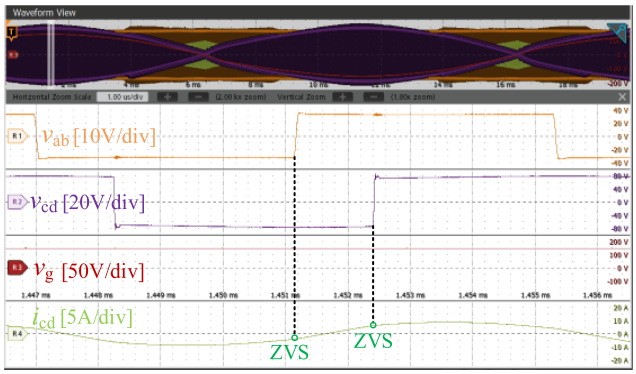

Fig. 27. Switching waveforms of SPS control at peak-voltage phase of v_g ($P_o = 200$ W). Note: Same for the waveforms with the proposed control.

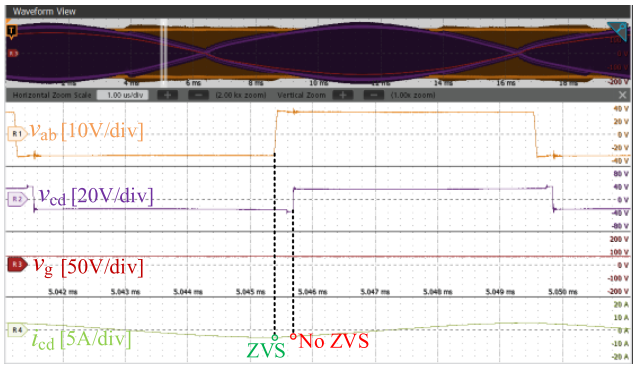

Fig. 28. Switching waveforms of SPS control in the low-voltage phase of v_g ($M < 0.5$ and $P_o = 200$ W).

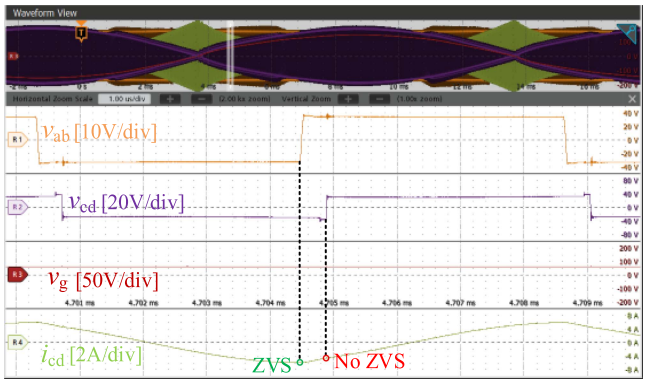

Fig. 29. Switching waveforms of SPS control in the low-voltage phase of v_g ($M < 0.5$ and $P_o = 150$ W).

output and 26.8% at 150 W output with the proposed control. These results confirm the effectiveness of the proposed control method in minimizing the conduction currents.

B. ZVS Performance

Figs. 27–29, respectively, illustrate the switching waveforms of the system with the SPS control under the three operating conditions.

1) Peak-voltage phase of v_g ($M \approx 1.13$) and full load ($P_o = 200$ W): ZVS turn-ON for all switches is achieved.

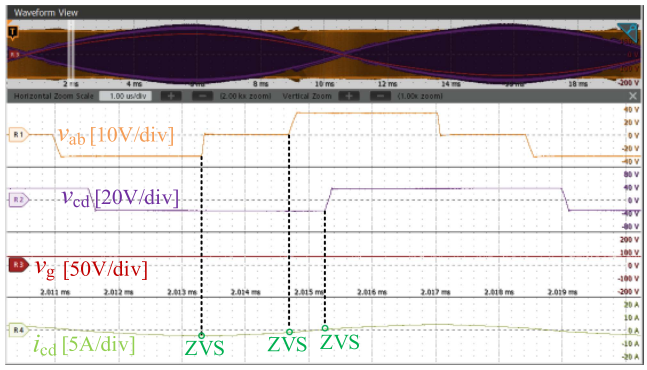

Fig. 30. Switching waveforms of proposed control strategy in the low-voltage phase of v_g ($M < 0.5$ and $P_o = 200$ W).

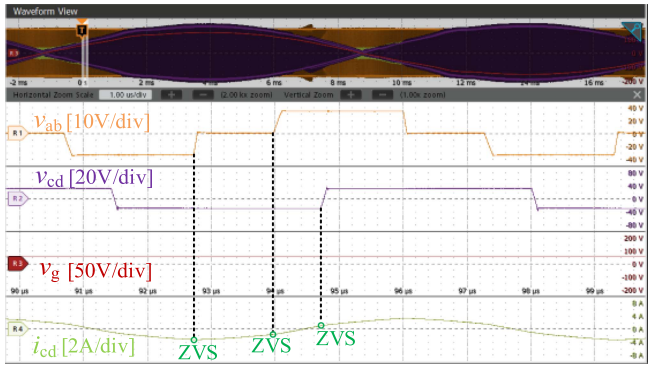

Fig. 31. Switching waveforms of proposed control strategy in the low-voltage phase of v_g ($M < 0.5$ and $P_o = 150$ W).

2) M $\approx$ 0.38 and full load ($P_o = 200$ W): Full ZVS turn-ON cannot be achieved.
3) M $\approx$ 0.38 and medium load ($P_o = 150$ W): Full ZVS turn-ON cannot be achieved.

Therefore, the system will suffer from the hard-switching problem with the conventional SPS control.

Figs. 30 and 31 further illustrate the switching waveforms of the system with the proposed control method under identical operating condition where ZVS cannot be achieved with SPS.

1) M $\approx$ 0.38 and full load ($P_o = 200$ W): The system is in State V of Fig. 19, with $f_{sw} = 134$ kHz and $\theta^*_{ab} = 0.58$.
2) M $\approx$ 0.38 and lighter load ($P_o = 150$ W): The system is in State V of Fig. 19, with $f_{sw} = 152$ kHz and $\theta^*_{ab} = 0.51$.

In both cases, the polarity of i_{cd} (i.e., i_{ab} / 2) at the switching instances meets the ZVS conditions of (5) and (6), leading to ZVS of all switches. These observations confirm that soft switching can be achieved with the proposed control method for a wider operating range than SPS control.

C. Computation Burden

The software implementation utilizes a time-critical interrupt service routine (ISR) framework. All control variables, including the switching frequency, are updated during each ISR period. The control ISR is executed at a fixed rate of 100 kHz using CPU Timer1, resulting in an ISR period $T = 10$ μs, which comprises $T = T_0 + T_1 + T_2$, as shown in Fig. 32. The main computational

TABLE III
PERFORMANCE COMPARISON OF RECENT DBSRCS/DAB

	[21]	[26]	[4]	[25]	This work
Year	2022	2023	2023	2024	2025
Topology	DBSRC (Cycloconverter)	DBSRC + Unfolder	DBSRC + Unfolder	DAB + Unfolder	DBSRC (Cycloconverter)
Control Degrees	2 Phase Shifts + Frequency	3 Phase Shifts	2 Phase Shifts + Frequency	3 Phase Shifts + Frequency	2 Phase Shifts + Frequency
Voltage Conversion	25-50 Vdc to 220 Vac	40 Vdc to 120 Vac	48 Vdc to 480 Y/208△ 3 ph Vac	40 Vdc to 120 Vac	36 Vdc to 115 Vac
Output Power	330 W	500 W	3.3 kW Each Phase	500 W	200 W
Switch Type	Si	GaN	GaN	GaN	GaN & Si
Realtime Optimization	Yes (Decrease reactive power)	No	No	No	Yes
Optimization Computation Burden	Implementable on a DSP	Not Implementable on a DSP	Not Implementable on a DSP	Not Implementable on a DSP	Implementable on a DSP
Peak Efficiency	96.87%	95.8%	97.2%	96.24%	96.5%
Switching Frequency	Max 80 kHz	100 kHz	50-300 kHz	50-150 kHz	120-200 kHz

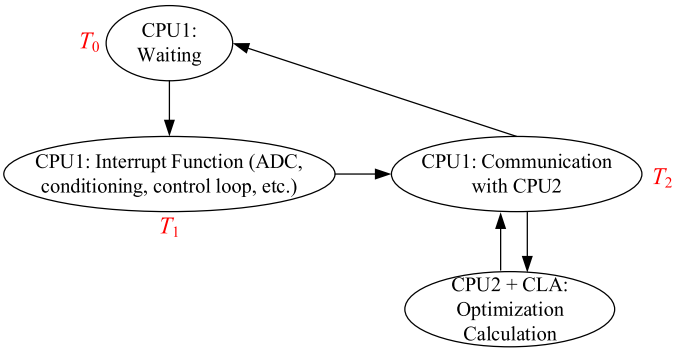

Fig. 32. Simplified software flow.

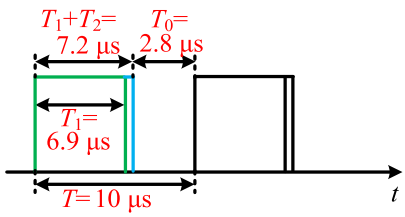

Fig. 33. Running time in flash.

workload consists of the execution of the interrupt function on CPU1 (T_1) and the optimization calculations on CPU2. It's noted that these two tasks are executed in parallel.

In the current experimental setup, the communication time T_2 between CPU1 and CPU2 is only 0.3 μs, as shown in Fig. 33. This short communication time indicates that the optimization calculations performed on CPU2 are completed before the interrupt function on CPU1 finishes execution. Consequently, CPU1 waits only 0.3 μs to exchange data with CPU2. If the calculations

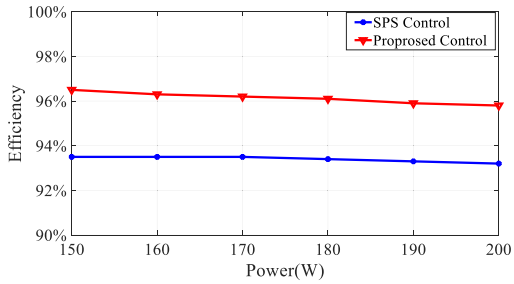

Fig. 34. Comparison of efficiency performance between proposed control strategy and SPS control method.

on CPU2 took longer than the execution time on CPU1, T_2 would be significantly longer, as CPU1 would have to wait for CPU2 to complete its computations before proceeding.

The overall computational burden can be quantified by calculating the active computation time $T_{\text{active}} = T_1 + T_2 = 7.2\ \mu$s. Given that the ISR period T is 10 μs, computational tasks occupy approximately 72% of this period. By further optimizing the software routines and computational algorithms, the computation time can be further reduced, enabling the system to operate at higher ISR frequencies if necessary.

D. Efficiency

Fig. 34 compares the efficiency performance of the system with the proposed control strategy and the SPS control method. The SPS method was selected as the benchmark for comparison due to its straightforward and fixed control logic, where the output power can be regulated solely through phase-shift control. For a fair comparison, both methods were tested with the same Dead Band Time, as shown in Table I, and the SPS control

was operated at a fixed switching frequency of 120 kHz to ensure consistent output power capacity. It is shown that the proposed control method achieves an efficiency greater than 95.8% throughout the entire load range, peaking at 96.5%. In contrast, SPS control achieves a peak efficiency of merely 93.8%, and the overall efficiency is around 2% lower at different loads than the proposed control method. These results demonstrate the effectiveness of the proposed control method in optimizing system efficiency.

Table III presents a detailed performance comparison of our proposed method with state-of-the-art DBSRCs. Notably, real-time optimal-efficiency control strategies like the one we propose are rare. The real-time control algorithm in [21] is based on a simplified control objective, namely decreasing reactive power, rather than achieving optimal efficiency directly. In terms of computational burden for real-time optimization, the methods in [4], [25], and [26] present challenges for direct implementation of their control algorithms on a typical DSP, mainly due to their reliance on nonanalytical solutions. Consequently, their practical implementation often involves the use of look-up tables generated offline. Among the efficiency values listed in the table, the efficiency of our proposed method is comparable to that of recently published works, even though a direct efficiency comparison is not entirely appropriate due to significant variations in operating conditions and parameters. Further efficiency improvements could be achieved by optimizing the design of hardware parameters. Additionally, considering hardware parameter variations under different voltage, current [28], and temperature conditions could further enhance our method's performance.

VII. Conclusion

This article presents an optimal control strategy for the DBSRC. The proposed strategy incorporates a simple closed-form analytical solution, enabling real-time optimization for maximum efficiency. Under the proposed control strategy, the rms current of the system is minimized and ZVS turn-ON is realized for a wider operating range, which significantly reduces both the conduction and switching losses of the system. Experimental results confirm the superiority of the proposed control strategy over the traditional SPS control method. More than 2% efficiency improvement has been achieved with the proposed control strategy over the test load range.

Appendix

This Appendix presents the derivations for i_{ab}, $f_{sw\_cr\_1}$, $f_{sw\_cr\_2}$ and other key variables.

A. Derivation for φ and $\mathrm{i_{ab}}$

By applying FHA to the equivalent circuit in Fig. 4, alongside the switching waveforms in Fig. 2, we derive the expressions for fundamental waveforms of v_{ab} and v'_{cd}

$$v_{ab}(t) = \frac{4V_{\mathrm{dc}}}{\pi}\cos(\theta'_{ab})\sin(\omega_{sw}t) \tag{25}$$

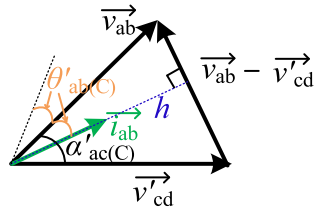

Fig. 35. Vector diagram of point C.

$$v'_{cd}(t) = \frac{2n_{Dg}v_{\mathrm{g}}}{\pi}\sin(\omega_{sw}t - \alpha'_{\mathrm{ac}}). \tag{26}$$

The voltage applied to the resonant tank is, thus, given by

$$v_{LC}(t) = v_{ab}(t) - v'_{cd}(t) = A\sin(\omega_{sw}t + \varphi). \tag{27}$$

Here, A represents the peak value of v_{LC}(t), and φ is the phase difference between the v_{ab} and v_{LC}, which is calculated as

$$\varphi = \cos^{-1}\left(\frac{\frac{4V_{\mathrm{dc}}}{\pi}\cos(\theta'_{ab}) - \frac{2n_{Dg}|v_g|}{\pi}\cos(\alpha'_{\mathrm{ac}})}{\sqrt{\left(\frac{4V_{\mathrm{dc}}}{\pi}\cos(\theta'_{ab}) - \frac{2n_{Dg}|v_g|}{\pi}\cos(\alpha'_{\mathrm{ac}})\right)^2 + \left(\frac{2n_{Dg}|v_g|}{\pi}\sin(\alpha'_{\mathrm{ac}})\right)^2}}\right). \tag{28}$$

Applying Ohm's law allows us to derive the resonant current

$$i_{ab}(t) = \frac{v_{LC}(t)}{(\omega_{sw}L_r - \frac{1}{\omega_{sw}C_r})\angle\frac{\pi}{2}} = -B\cos(\omega_{sw}t + \varphi) \tag{29}$$

where B denotes the peak value of i_{ab}(t), which is shown below

$$B = \frac{\sqrt{\left(\frac{4V_{\mathrm{dc}}}{\pi}\cos(\theta'_{ab})\right)^2 + \left(\frac{2n_{Dg}v_g}{\pi}\right)^2 - 2\left(\frac{4V_{\mathrm{dc}}}{\pi}\cos(\theta'_{ab})\right)\left(\frac{2n_{Dg}v_g}{\pi}\cos(\alpha'_{\mathrm{ac}})\right)}}{\omega_{sw}L_r - \frac{1}{\omega_{sw}C_r}}. \tag{30}$$

Therefore, the rms value of $\mathrm{i_{ab}}$ can be derived as

$$i_{ab.\mathrm{rms}} = \frac{\sqrt{\left(\frac{4V_{\mathrm{dc}}}{\pi}\cos(\theta'_{ab})\right)^2 + \left(\frac{2n_{Dg}v_g}{\pi}\right)^2 - 2\left(\frac{4V_{\mathrm{dc}}}{\pi}\cos(\theta'_{ab})\right)\left(\frac{2n_{Dg}v_g}{\pi}\cos(\alpha'_{\mathrm{ac}})\right)}}{\sqrt{2}(\omega_{sw}L_r - \frac{1}{\omega_{sw}C_r})} \tag{31}$$

which can be further deduced to

$$i_{ab.\mathrm{rms}} = \frac{4V_{\mathrm{dc}}}{\pi}\frac{\sqrt{(\cos(\theta'_{ab}))^2 + M^2 - 2M\cos(\theta'_{ab})\cos(\alpha'_{\mathrm{ac}})}}{\sqrt{2}(\omega_{sw}L_r - \frac{1}{\omega_{sw}C_r})}. \tag{32}$$

Applying normalization to (32) with nominal output current, (32) can be further derived as

$$\mathrm{rms}(i_{ab\_pu}) = \frac{\sqrt{(\cos(\theta'_{ab}))^2 + M^2 - 2M\cos(\theta'_{ab})\cos(\alpha'_{\mathrm{ac}})}}{\cos(\theta'_{ab})\sin(\alpha'_{\mathrm{ac}})}. \tag{33}$$

B. Derivation for $\mathrm{f_{sw\_cr1}}$

In the vector diagram in Fig. 35, representing Point C in Fig. 6, $\overrightarrow{v_{ab}}$ leads $\overrightarrow{v'_{cd}}$ by a phase angle of $\alpha'_{ab(C)}$, with the current $\overrightarrow{i_{ab}}$

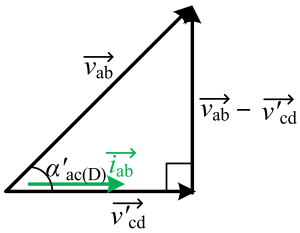

Fig. 36. Vector diagram of Point D.

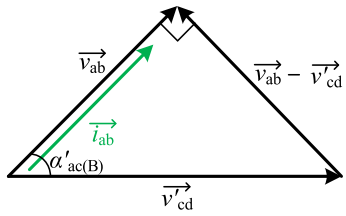

Fig. 37. Vector diagram of point B.

lagging $\overrightarrow{v_{ab}}$ by $\theta'_{ab(C)}$. This phase lag facilitates the critical ZVS condition for the primary side switches.

The magnitudes of $\overrightarrow{v_{ab}}$ and $\overrightarrow{v'_{cd}}$ can be computed as

$$|\overrightarrow{v_{ab}}| = \frac{4V_{\rm dc}}{\pi}\cos\theta'_{ab(C)} \tag{34}$$

$$\left|\overrightarrow{v\prime_{cd}}\right| = \frac{2n_{Dg}|v_g|}{\pi}. \tag{35}$$

Following from this, the height relative to $\overrightarrow{v_{ab}} - \overrightarrow{v'_{cd}}$

$$h = \frac{|\overrightarrow{v_{ab}}|\left|\overrightarrow{v\prime_{cd}}\right|\sin\alpha'_{ac(C)}}{\sqrt{|\overrightarrow{v_{ab}}|^2 + \left|\overrightarrow{v\prime_{cd}}\right|^2 - 2|\overrightarrow{v_{ab}}|\left|\overrightarrow{v\prime_{cd}}\right|\cos\alpha'_{ac(C)}}}\frac{4V_{\rm dc}}{\pi}$$

$$= \frac{\cos\theta'_{ab(C)}M\sin\alpha'_{ac(C)}}{\sqrt{(\cos\theta'_{ab(C)})^2 + M^2 - 2\cos\theta'_{ab(C)}M\cos\alpha'_{ac(C)}}}\frac{4V_{\rm dc}}{\pi}. \tag{36}$$

Therefore,

$$\cos\theta'_{ab(C)} = \frac{h}{|\overrightarrow{v_{ab}}|} = \frac{M\sin\alpha'_{ac(C)}}{\sqrt{(\cos\theta'_{ab(C)})^2 + M^2 - 2\cos\theta'_{ab(C)}M\cos\alpha'_{ac(C)}}}. \tag{37}$$

According to (10),

$$\sin(\alpha'_{ac(C)}) = \frac{p_{\rm ac}}{p_{DB(\max)}\cos(\theta'_{ab(C)})}. \tag{38}$$

Combing (37) and (38) allows for the derivation of

$$(\cos\theta'_{ab(C)})^2 = \frac{M\frac{p_{\rm ac}}{p_{DB(\max)}}}{\sqrt{\begin{array}{l}(\cos\theta'_{ab(C)})^2 + M^2 - 2M \\ \times\sqrt{(\cos\theta'_{ab(C)})^2 - (\frac{p_{\rm ac}}{p_{DB(\max)}})^2}\end{array}}}. \tag{39}$$

In another vector diagram shown in Fig. 36, corresponding to Point D in Fig. 6, $\overrightarrow{v_{ab}}$ leads $\overrightarrow{v'_{cd}}$ by a phase angle $\alpha'_{ac(D)}$, with $\overrightarrow{i_{ab}}$ in phase with $\overrightarrow{v'_{cd}}$. This alignment facilitates the critical ZVS condition for the secondary side switches. Therefore, $\overrightarrow{v_{ab}} - \overrightarrow{v'_{cd}}$ will lead $\overrightarrow{v'_{cd}}$ by 90°. According to Fig. 36

$$\cos\alpha'_{ac(D)} = \frac{\left|\overrightarrow{v\prime_{cd}}\right|}{|\overrightarrow{v_{ab}}|} = \frac{\frac{2n_{Dg}|v_g|}{\pi}}{\frac{4V_{\rm dc}}{\pi}\cos\theta'_{ab(D)}} = \frac{M}{\cos\theta'_{ab(D)}}. \tag{40}$$

Based on (10)

$$\sin(\alpha'_{ac(D)}) = \frac{p_{\rm ac}}{p_{DB(\max)}\cos(\theta'_{ab(D)})}. \tag{41}$$

Merging (40) and (41) enables the derivation of

$$\frac{p_{\rm ac}}{p_{DB(\max)}} = \sqrt{(\cos\theta'_{ab(D)})^2 - M^2}. \tag{42}$$

Thus, the y-axis value $\theta'_{ab(D)}$ of Point D is derived as

$$\theta'_{ab(D)} = \arccos\left(\sqrt{\left(\frac{p_{\rm ac}}{p_{DB(\max)}}\right)^2 + M^2}\right). \tag{43}$$

Considering the critical situation

$$\theta'_{ab(C)} = \theta'_{ab(D)}. \tag{44}$$

Combining (39), (43), and (44) results in

$$\frac{p_{\rm ac}}{p_{DB(\max)}} = \sqrt{M - M^2}. \tag{45}$$

Substituting (11) and (15) into (45) leads to

$$\frac{p_{DB}}{\frac{4n_{Dg}V_{\rm dc}|v_g|}{L_r\pi^2(2\pi f_{sw} - \frac{\omega_r^2}{2\pi f_{sw}})}} = \sqrt{n_{Dg}\frac{|v_g|/2}{V_{\rm dc}} - \left(n_{Dg}\frac{|v_g|/2}{V_{\rm dc}}\right)^2}. \tag{46}$$

Consequently, the solution for (46) is then finalized as (16). To ensure $\theta'_{ab(D)}$ must be smaller than or equal to $\theta'_{ab(C)}$, the following is derived:

$$f_{sw} \geq f_{sw\_cr1}. \tag{47}$$

C. *Derivation for* f_{sw_cr2}

In the vector diagram shown in Fig. 37, which corresponds to Point B in Fig. 12, the vector $\overrightarrow{v_{ab}}$ leads the vector $\overrightarrow{v'_{cd}}$ by a phase angle of $\alpha'_{ab(B)}$, and the current $\overrightarrow{i_{ab}}$ is in phase with $\overrightarrow{v_{ab}}$. This alignment facilitates the critical ZVS condition for the primary side switches. Consequently, the vector difference $\overrightarrow{v_{ab}} - \overrightarrow{v'_{cd}}$ will lead $\overrightarrow{v_{ab}}$ by 90°.

The magnitudes of $\overrightarrow{v_{ab}}$ and $\overrightarrow{v'_{cd}}$ can be computed as

$$|\overrightarrow{v_{ab}}| = \frac{4V_{\rm dc}}{\pi} \tag{48}$$

$$\left|\overrightarrow{v\prime_{cd}}\right| = \frac{2n_{Dg}|v_g|}{\pi}. \tag{49}$$

Following from this

$$\cos\alpha\prime_{\mathrm{ac}(B)} = \frac{|\overrightarrow{v_{ab}}|}{|\overrightarrow{v\prime_{cd}}|} = \frac{2V_{\mathrm{dc}}}{n_{Dg}|v_g|} = \frac{1}{M}. \tag{50}$$

The x-axis value $\alpha'_{\mathrm{ac}(B)}$ of Point B is then determined as

$$\alpha'_{\mathrm{ac}(B)} = \arccos\left(\frac{1}{M}\right) = \arcsin\left(\frac{\sqrt{M^2-1}}{M}\right). \tag{51}$$

Given the established relationship in (10) with the condition $\theta'_{ab(A)} = 0$, the output power should also be

$$p_{\mathrm{ac}} = \frac{4n_{Dg}V_{\mathrm{dc}}|v_g|\sin(\alpha'_{\mathrm{ac}(A)})}{L_r\pi^2(2\pi f_{sw} - \frac{\omega_r{}^2}{2\pi f_{sw}})}. \tag{52}$$

Consequently, the x-axis value $\alpha'_{ab(A)}$ of Point A is derived as

$$\alpha'_{\mathrm{ac}(A)} = \arcsin\left(\frac{L_r\pi^2(2\pi f_{sw} - \frac{\omega_r{}^2}{2\pi f_{sw}})p_{\mathrm{ac}}}{4n_{Dg}V_{\mathrm{dc}}|v_g|}\right). \tag{53}$$

Since the x-axis value $\alpha'_{\mathrm{ac}(A)}$ of Point A needs to be greater than or equal to the x-axis value $\alpha'_{\mathrm{ac}(B)}$ of Point B

$$\alpha'_{ac(A)} \geq \alpha'_{\mathrm{ac}(B)}. \tag{54}$$

Combining (51), (53) and (54), (55) is calculated out

$$\frac{L_r\pi^2(2\pi f_{sw} - \frac{\omega_r{}^2}{2\pi f_{sw}})p_{\mathrm{ac}}}{4n_{Dg}V_{\mathrm{dc}}|v_g|} \geq \frac{\sqrt{M^2-1}}{M}. \tag{55}$$

In addition, the resonant angular frequency of the L_r-C_r resonant tank can be derived as

$$\omega_r = \frac{1}{\sqrt{L_rC_r}}. \tag{56}$$

Substituting (15) and (56) into (55) results in (17) and

$$f_{sw} \geq f_{sw\_cr2}. \tag{57}$$

D. Derivation for $\mathrm{i}_{\mathrm{ab}.rms}$ at Point A

Substituting (19.1) into (31) and (20), respectively, we can obtain expressions

$$i_{ab.rms} = \frac{\sqrt{(\frac{4V_{\mathrm{dc}}}{\pi})^2 + (\frac{2n_{Dg}v_g}{\pi})^2 - 2(\frac{4V_{\mathrm{dc}}}{\pi})(\frac{2n_{Dg}v_g}{\pi}\cos(\alpha'_{\mathrm{ac}}))}}{\sqrt{2}(\omega_{sw}L_r - \frac{1}{\omega_{sw}C_r})} \tag{58}$$

$$\alpha'_{\mathrm{ac}} = \arcsin\left(\frac{p_{DB}\pi^2(\omega_{sw}L_r - \frac{1}{\omega_{sw}C_r})}{4V_{\mathrm{dc}}n_{Dg}|v_g|}\right). \tag{59}$$

Substituting (59) into (58), we can get

$$i_{ab.rms} = \frac{\sqrt{\begin{array}{l}\left(\frac{4V_{\mathrm{dc}}}{\pi}\right)^2 + \left(\frac{2n_{Dg}v_g}{\pi}\right)^2 - 2\left(\frac{4V_{\mathrm{dc}}}{\pi}\right) \\ \times\left(\frac{2n_{Dg}v_g}{\pi}\cos\left(\frac{p_{DB}\pi^2(\omega_{sw}L_r - \frac{1}{\omega_{sw}C_r})}{4V_{\mathrm{dc}}n_{Dg}|v_g|}\right)\right)\end{array}}}{\sqrt{2}(\omega_{sw}L_r - \frac{1}{\omega_{sw}C_r})}. \tag{60}$$

E. Optimal Frequency Under $M < 1$

In this scenario $M < 1$, the optimal values of θ'_{ab} and α'_{ac} have been determined, corresponding to the Point D in Fig. 6. At Point D, the resonant current i_{ab} is phase with v_{cd}, as illustrated in the phase diagram in Fig. 36. This in-phase condition means that the output power of DBSRC can be expressed as

$$p_{\mathrm{ac}} = \overrightarrow{i_{ab}} \cdot \overrightarrow{v\prime_{cd}} = \left|\overrightarrow{i_{ab}}\right| \cdot \left|\overrightarrow{v\prime_{cd}}\right| = i_{ab.\mathrm{rms}}\left|\overrightarrow{v\prime_{cd}}\right|. \tag{61}$$

Substituting (35) into (61), we obtain

$$i_{ab.\mathrm{rms}} = \frac{\pi p_{\mathrm{ac}}}{2n_{Dg}|v_g|}. \tag{62}$$

This indicates $i_{ab.\mathrm{rms}}$ is independent of f_{sw} under this scenario, meaning that increasing of f_{sw} does not help reduce the rms value of i_{ab}.

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