Modified Bridgeless SEPIC PFC Converter With Reduced Conduction Losses and Simple Structure for Medium-Line-Frequency Applications

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***Abstract*—Bridgeless power factor correction (PFC) converter has obtained much popularity in medium-line-frequency avionics applications due to its merit of optimized power losses. In this article, a modified bridgeless PFC converter based on single-ended primary-inductor converter (SEPIC) is demonstrated. The complete elimination of all input diodes and the presence of only two conducting semiconductors in power-flowing path result in lower conduction losses as compared to classic SEPIC PFC converters. A common set of energy-storage capacitor and inductor is employed to operate for both positive and negative half-line cycles, leading to higher component utilization as compared to dual-SEPIC PFC converters. Moreover, the voltage stresses on the semiconductors are greatly reduced with the split-capacitor output structure. The proposed converter is designed to operate in discontinuous conduction mode, and a near-unity power factor can be achieved with no current-loop control. The overall performance of the proposed converter is elaborated in terms of its working principle, control scheme, and characteristic analysis. Finally, a 300-W laboratory prototype with 115-Vrms/400-Hz ac input and 270-V dc output is developed, and the theoretical analysis is authenticated by means of experimental results.**

***Index Terms*—Bridgeless sepic PFC converter, discontinuous conduction mode (DCM), high component utilization, medium-line-frequency avionics applications, reduced conduction losses.**

I. Introduction

IN AVIONICS power supply systems, the nominal frequency of power generation is 400 Hz, which is 8 times the typical 50-Hz power frequency. As the key component for converting ac line power to 270-V dc bus, power factor correction (PFC) converter is essential to reducing the total harmonic distortion (THD) and to achieving a near-unity power factor (PF), and it is also required to show better performance in terms of volume and efficiency for such application [1], [2]. The conventional PFC converter comprises a diode bridge rectifier (DBR), followed by a dc–dc chopper, the type of which determines its working characteristic. The PFC accomplished with converters working in discontinuous conduction mode (DCM) is naturally obtained without the use of complex control loops for the input current (contrary to what happens with continuous conduction mode), and the control strategy is simplified as a simple voltage loop for the output voltage regulation. Thus, the input current sensor is not necessary and the control system becomes more robust and reliable [3].

Due to the simple structure, boost-type topologies are widely employed for PFC in medium-line-frequency applications [4]. However, in DCM, its input inductor current reaches zero in each switching cycle, resulting in larger current swing and the need for differential mode input filter [5]. Moreover, the average input current during a switching cycle has a distortion that can be observed in the line cycle. Adopting CRM control can improve its current shape, while the complexity of control algorithm is also increased [6], [7]. As compared to boost-type topologies, the PFC topologies based on single-ended primary-inductor converter (SEPIC) have the commendable input current characteristic in DCM. The input inductor current is continuous and the additional filter is not required. The shape of average input current is sinusoidal and the control strategy remains as a simple voltage loop [8]. These attributes make the SEPIC PFC converter also be considered as a good option for the medium-line-frequency low-power applications such as airplane seat and onboard computer power supplies [9], [10].

The conventional SEPIC PFC circuit, as depicted in Fig. 1(a), utilizes a DBR at input [11]. Since there are two diodes in DBR conducting at all times, considerable conduction losses occur in such circuit, which degrades the overall system efficiency. In an effort to reduce the power losses associated with the DBR, the implementation of the bridgeless structure has gained much attention and substantial research has been directed toward the development of the efficient bridgeless circuits. With respect to the conventional circuit, the bridgeless structure contributes to minimizing the conduction losses by reducing the number of semiconductors in the current path and, hence, high efficiency is obtained, as well as cost savings. Among bridgeless

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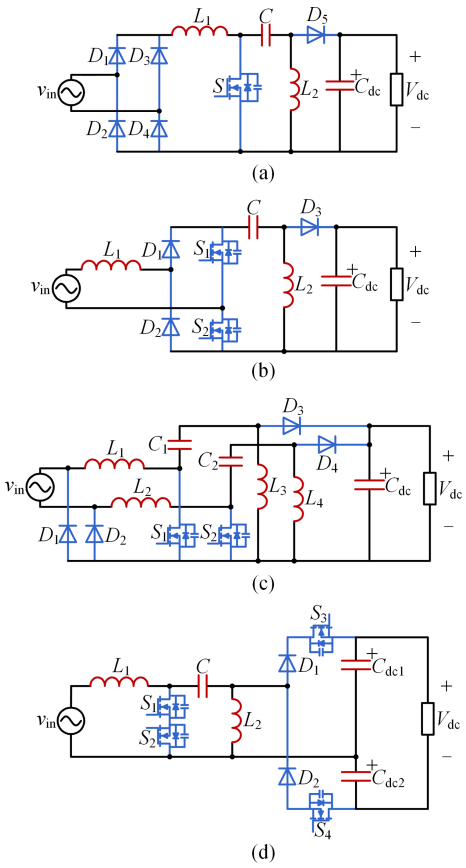

Fig. 1. Schematics of SEPIC PFC circuits. (a) Conventional SEPIC PFC with DBR [10]. (b) Totem-pole bridgeless SEPIC PFC [12]. (c) Dual-SEPIC bridgeless SEPIC PFC [13]. (d) Proposed bridgeless SEPIC PFC.

SEPIC-derived PFC circuits, totem-pole SEPIC [12] and dual-SEPIC [13] are two classic bridgeless topologies, as depicted in Fig. 1(b) and (c). Totem-pole SEPIC PFC circuit reduces the total number of semiconductors from six to five, however, there is still an input diode conducting at all times [14]. Dual-SEPIC PFC circuit employs two identical SEPIC units, operating in positive and negative half-line cycles, respectively. This dual-converter structural feature will inevitably increase the circuit complexity, and the component utilization is relatively low [15].

Furthermore, modified bridgeless SEPIC PFC circuits have also been investigated and demonstrated. The topologies in [16], [17], and [18], as the improved version of dual-SEPIC circuits, capable of broadening the gain range, are obtained by introducing the switched inductor network or a multiplier stage. Nevertheless, these circuits still have a larger number of passive components, along with the input diodes with continuous conduction. In [19] and [20], a supplementary inductor-capacitor cell, formed by diodes, is introduced into the totem-pole SEPIC circuit to improve the voltage gain, while the circuit complexity and power losses are also increased. In addition, the integrated structure [21], [22] and split-capacitor structure [23], [24], [25] have also been introduced into SEPIC PFC circuits. The integrated topology combines SEPIC PFC with dc–dc circuits by sharing switches, and the converter volume is greatly improved as compared to two-stage structure. The split-capacitor structure, consisting of two series-connected output capacitors with neutral point, has the merit of reduced voltage stresses on the semiconductors at the same output level. This output configuration has been applied to the dual-SEPIC PFC circuit, where two classic SEPIC units operate separately, and as such, it has the potential for improvement in component utilization.

In view of the mentioned above, a modified bridgeless PFC converter for medium-line-frequency avionics applications, is proposed, as depicted in Fig. 1(d). Inheriting from the SEPIC PFC topology, the proposed circuit still has the commendable input current characteristics and simpler control loop. Besides, its performance is also optimized in terms of power losses and component utilization. The key features associated with the proposed topology are as follows.

1) The presented topology removes all the input diodes, and there is no semiconductor conducting at all times. A maximum of two semiconductors conduct in the power-flowing path, and the conduction losses are reduced.
2) The presented topology adopts the split-capacitor output configuration to reduce voltage stress. Instead of two identical SEPIC units, only a set of input filter inductor, energy-storage inductor, and capacitor is needed in this topology to operate for both positive and negative half-line cycles, thus improving the utilization of passive components.
3) The presented topology is designed to operate in DCM, and the control algorithm is simplified to a voltage loop. The diodes are turned off at zero current, and the reverse recovery issue is avoided.

The rest of this article is organized as follows. The circuit configuration along with its working principle of step-up and step-down operating modes is analyzed in detail in Section II. Section III encompasses the characteristic analysis, parameter design. Section IV investigates the design of control system. Section V deals with the simulation and experimental results, observations, and comparisons. Finally, Section VI concludes this article.

II. Proposed Topology and Working Principle

A. Circuit Configuration

With reference to Fig. 1(d), the proposed SEPIC PFC circuit consists of input filter inductor (L_1), intermediate-storage cell and output rectifier. The intermediate-storage cell comprises a set of energy-storage capacitor (C) and energy-storage inductor (L_2), operating for either half-line cycle. The antiseries switches (S_1, S_2) are placed between input inductor and intermediate-storage cell to provide a bidirectional channel for the inductor currents. The output rectifier adopts a split-capacitor structure, including two output capacitors (C_{dc1}, C_{dc2}) and unidirectional-controllable switches formed by diode and switch in series (D_1, S_3 and D_2, S_4). The capacitance values of the output capacitors are equal, and the voltage across each output capacitor is half of the output voltage.

A quantitative comparison in relation to three components of input, intermediate-storage, and output, is given in Table I. The proposed circuit introduces two switches in the output rectifier,

TABLE I
QUANTITATIVE ANALYSIS OF DIFFERENT SEPIC PFC TOPOLOGIES

SEPIC PFC topologies	Input diodes and inductors	intermediate-storage cell	Output diodes/switches and capacitors
Conventional	4*D*/1*L*	1*L*/1*C*/1*S*	1*D*/1*C*
Totem-pole in [12]	2*D*/1*L*	1*L*/1*C*/2*S*	1*D*/1*C*
Dual-SEPIC in [13]	2*D*/2*L*	2*L*/2*C*/2*S*	2*D*/1*C*
Modified in [16]	2*D*/2*L*	1*L*/3*C*/2*S*/4*D*	1*D*/1*C*
Modified in [17]	2*D*/2*L*	2*L*/2*C*/2*S*/2*D*	2*D*/1*C*
Modified in [18]	2*D*/2*L*	2*L*/2*C*/1*S*/2*D*	2*D*/1*C*
Modified in [19]	2*D*/1*L*	2*L*/1*C*/2*S*	2*D*/1*C*
Modified in [20]	2*D*/1*L*	2*L*/3*C*/2*S*/1*D*	1*D*/1*C*
Modified in [23]	2*D*/1*L*	1*L*/2*C*/1*S*/2*D*	2*D*/2*C*
Modified in [24]	2*D*/1*L*	2*L*/2*C*/2*S*	2*D*/2*C*
Proposed	1*L*	1*L*/1*C*/2*S*	2*D*/2*S*/2*C*

S: Switch; *D*: Diode; *L*: Inductor; *C*: Capacitor.

while the total number of semiconductors in this circuit is the same as the conventional SEPIC PFC circuit. Compared with the totem-pole SEPIC PFC circuit [12] and its variants [19], [20], the proposed circuit is completely exempted from all the input diodes, thus optimizing power losses. Compared with the dual-SEPIC PFC circuit [13] and its variants [16], [17], [18], [23], [24], the proposed circuit requires only one set of input inductor, energy-storage inductor, and energy-storage capacitor, which operates for both positive and negative half-line cycles, thus improving component utilization.

B. Working Principle

The input line voltage ($v_{\rm in}$) is defined as

$$v_{\rm in} = V_{\rm m}\sin(2\pi f_{\rm l}\cdot t) \tag{1}$$

where $V_{\rm m}$ and $f_{\rm l}$ are the maximum value and the line frequency of the input voltage, respectively. The input voltage varies as a sine wave, and the output-port voltage is half of output voltage ($V_{\rm dc}/2$) due to the split-capacitor structure. Since the switching frequency is much higher than the line frequency, the voltages of the ac input and energy-storage capacitor can be considered as constant values $V_{\rm in}$ and $V_{\rm C}$ in each switching cycle.

In view of the sinusoidal variation in input voltage, the input voltage value ($V_{\rm in}$) can be lower or higher than the output-port voltage ($V_{\rm dc}/2$) and, hence, the operating mode of the converter is divided into two types: 1) step-up and 2) step-down. When $V_{\rm in}$ is lower than $V_{\rm dc}/2$, the converter operates in step-up mode and has six topological stages, of which three are for positive half-line cycle and the others are for negative half-line cycle; When $V_{\rm in}$ is higher than $V_{\rm dc}/2$, the converter operates in step-down mode and also has six topological stages, of which three are for positive half-line cycle and the others are for negative half-line cycle. Due to similar operating process, only the positive half-line cycle is illustrated in this section.

1) Step-Up Mode: In the step-up operating mode, S_2 and S_3 are always turned ON. The timing diagram of the gate signal $V_{\rm GS1}$ along with the other key waveforms for a time interval of one switching cycle are shown in Fig. 2 and the corresponding commutation states of the circuit are illustrated in Fig. 3.

The descriptions and analysis of three operating stages in the step-up mode are listed as follows.

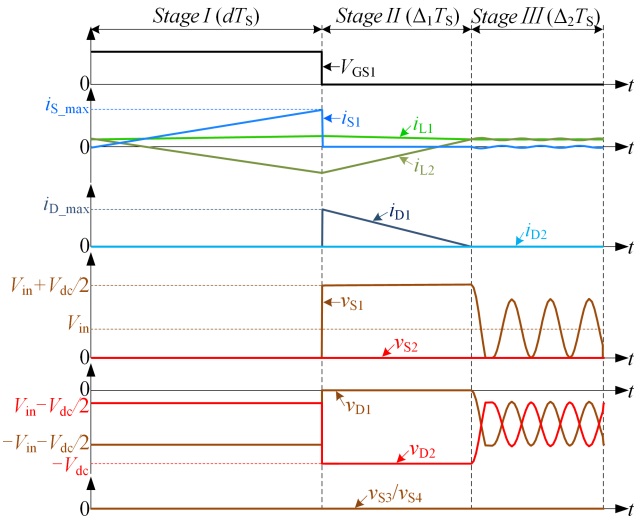

Fig. 2. Timing diagram of the proposed circuit during one switching cycle in the step-up mode for positive half-line cycle.

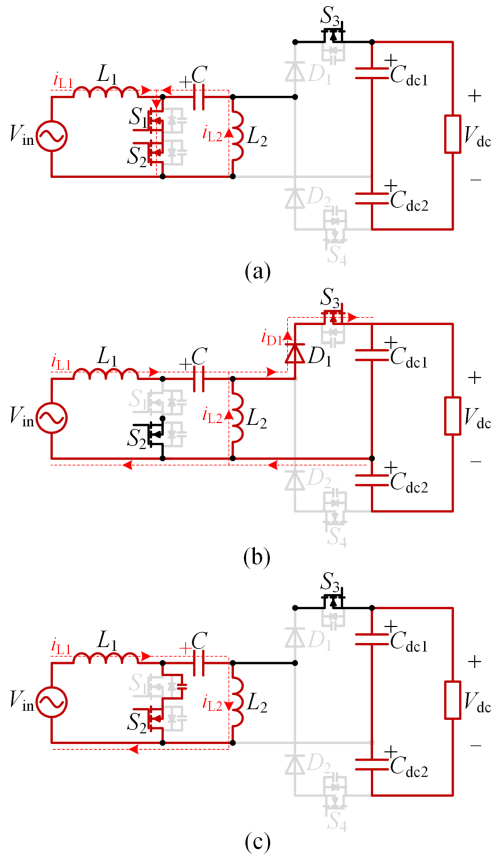

Fig. 3. Commutation states in the step-up mode for positive half-line cycle. (a) Stage I. (b) Stage II. (c) Stage III.

Stage I [$dT_{\rm S}$] *in* Fig. 3(a): S_1 is turned ON. D_1, D_2 are reverse-biased and withstand the voltages of $V_{\rm in}$–$V_{\rm dc}/2$ and $-V_{\rm in}$–$V_{\rm dc}/2$. The currents through inductors L_1 and L_2 ($i_{\rm L1}$, $i_{\rm L2}$) are increasing linearly with the slopes of $V_{\rm in}/L_1$ and $V_{\rm C}/L_2$, respectively. The current through S_1 ($i_{\rm S1}$) is the sum of currents

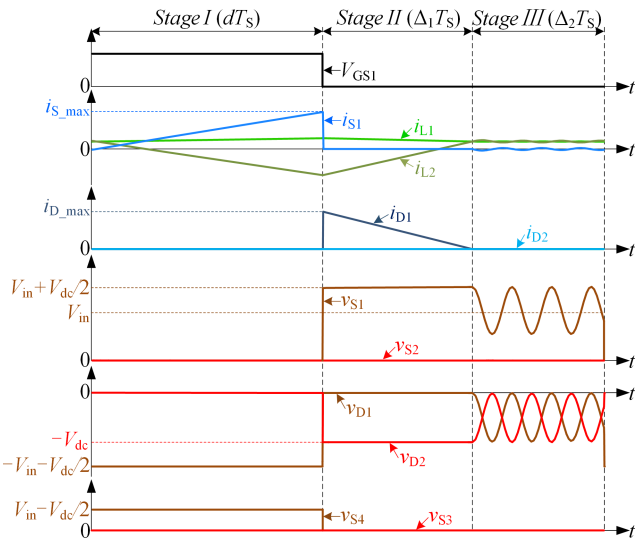

Fig. 4. Timing diagram of the proposed circuit during one switching cycle in the step-down mode for positive half-line cycle.

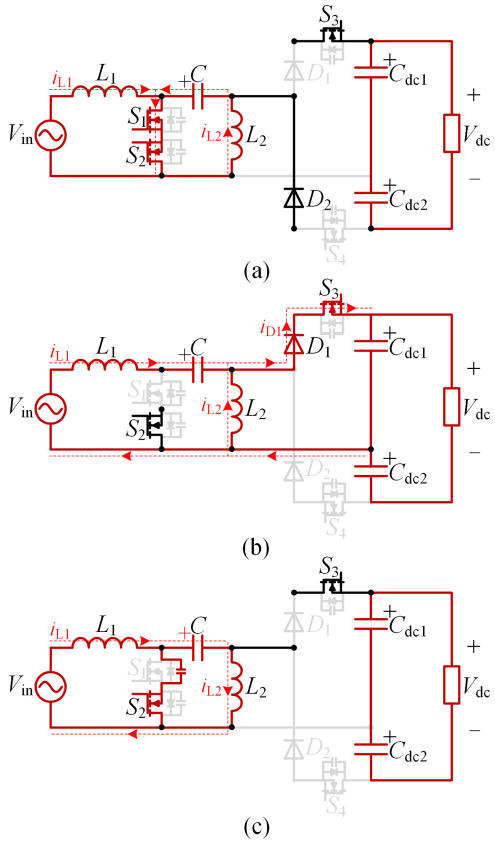

Fig. 5. Commutation states in the step-down mode for positive half-line cycle. (a) Stage I. (b) Stage II. (c) Stage III.

i_{L1} and i_{L2}. At the end of this stage, i_{S1} reaches to its peak (i_{S_max}), which is calculated as

$$i_{S\_max}=\frac{d}{f_S}\left(\frac{V_{in}}{L_1}+\frac{V_C}{L_2}\right) \tag{2}$$

where d is duty cycle, and f_S is switching frequency.

Stage II [$\Delta_1 T_S$] *in* Fig. 3(b): S_1 is turned OFF and withstands the voltage of $V_{in}+V_{dc}/2$. D_1 is forward-biased, while D_2 is still reverse-biased with the voltage of $-V_{dc}$. The energy stored in inductors L_1 and L_2 starts to transfer to the capacitors C, C_{dc1} and to the load through D_1 and S_3, and the currents i_{L1} and i_{L2} are decreasing linearly with the slopes of $(V_{in}-V_C-V_{dc}/2)/L_1$ and $(-V_{dc})/2L_2$, respectively. The current through D_1 (i_{D1}) is the sum of currents i_{L1} and i_{L2}, which decreases from its peak and reaches to zero at the end of this stage.

Stage III [$\Delta_2 T_S$] *in* Fig. 3(c): S_1 remains turned OFF, and the forward current in D_1 is null, thus, D_1 is turned OFF with zero current. In this subinterval, D_1, D_2 withstand reverse voltages and are reverse-biased. Inductor L_2 resonates in parallel with the parasitic capacitor of S_1. Since the capacitance value of the parasitic capacitor is generally in the pF range, i_{S1} is small and the currents through L_1 and L_2 are basically equal.

1) Step-Down Mode: In the step-down operating mode, the switches S_2 and S_3 are always turned ON, while S_4 needs to be always turned OFF. The timing diagram of the gate signal V_{GS1} along with the other key waveforms for a time interval of a switching cycle are shown in Fig. 4 and the commutation states are illustrated in Fig. 5.

The descriptions and analysis of three operating stages in the step-down mode are listed as follows.

Stage I [dT_S] *in* Fig. 5(a): S_1 is turned ON and D_2 is forward-biased. S_4 is turned OFF and withstands the voltage of $V_{in}-V_{dc}/2$, while D_1 is reverse-biased and withstand the reverse voltage of $-V_{in}-V_{dc}/2$. i_{L1} and i_{L2} are increasing linearly with the slopes of V_{in}/L_1 and V_C/L_2, respectively. i_{S1} is the sum of i_{L1} and i_{L2}, and reaches its peak at the end of this stage.

Stage II [$\Delta_1 T_S$] *in* Fig. 5(b): S_1 is turned OFF and withstands the voltage of $V_{in}+V_{dc}/2$. D_1 is forward-biased and D_2 is reverse-biased and withstand the reverse voltage of $-V_{dc}$. i_{L1} and i_{L2} are decreasing linearly with the slopes of $(V_{in}-V_C-V_{dc}/2)/L_1$ and $(-V_{dc})/2L_2$, respectively. i_{D1} decreases from its peak and reaches to zero at the end of this stage.

Stage III [$\Delta_2 T_S$] *in* Fig. 5(c): S_1 remains turned OFF, and D_1, D_2 are reverse-biased. The forward current in D_1 is null, thus, D_1 is turned OFF at zero current. The currents through L_1 and L_2 are basically equal.

From the preceding mode analysis, it can be found that the proposed circuit exhibits the same current behavior in the step-up and step-down modes, which can be expressed by a uniform expression. In terms of voltages across the semiconductors, the major difference between step-up and step-down modes is the operating states of output diode D_2 and switch S_4 during *Stage I*. In step-up mode, V_{in} is lower than $V_{dc}/2$, and the value of $V_{in}-V_{dc}/2$ is negative. D_2 is reverse-biased and withstands this voltage difference, while the voltage of S_4 is zero. In step-down mode, V_{in} is higher than $V_{dc}/2$. The value of $V_{in}-V_{dc}/2$ is positive, and D_2 is forward-biased. At this point, S_4 is turned OFF and withstands this voltage difference.

III. Characteristic Analysis

A. Static Gain

According to the volt-second balance principle, the average voltage of inductors L_1 and L_2 during a switching cycle is zero, expressed as

$$\begin{cases} V_{\text{in}}d + (V_{\text{in}} - V_{\text{C}} - \frac{V_{\text{dc}}}{2})\Delta_1 + \frac{L_1}{L_1+L_2}(V_{\text{in}} - V_{\text{C}})\Delta_2 = 0 \\ V_{\text{C}}d - \frac{V_{\text{dc}}}{2}\Delta_1 - \frac{L_2}{L_1+L_2}(V_{\text{in}} - V_{\text{C}})\Delta_2 = 0. \end{cases} \tag{3}$$

Based on (3) and the mathematical calculation, the voltage V_{C} and the voltage ratio $V_{\text{dc}}/V_{\text{in}}$ are calculated as

$$\begin{cases} V_{\text{C}}{=}V_{\text{in}} \\ \frac{V_{\text{dc}}}{V_{\text{in}}} = \frac{2d}{\Delta_1} \end{cases} \tag{4}$$

where Δ_1 corresponds to the duty ratio of *Stage II*.

From (4), it is clear that the energy-storage capacitor voltage is equal to the input voltage. In *Stage II*, the current of diode D_1 decreases linearly from the peak, and its waveform is triangular. Thus, the average current of output diode over a switching cycle ($i_{\text{D\_avg}}$) can be calculated as

$$i_{\text{D\_avg}}{=}\frac{d^2V_{\text{in}}^2}{L_{12}f_{\text{S}}V_{\text{dc}}} \tag{5}$$

where L_{12} is defined as the parallel inductance value of L_1 and L_2, expressed as

$$L_{12} = \frac{L_1 \cdot L_2}{L_1 + L_2}. \tag{6}$$

Based on (5), the averaged output current over a line cycle (I_{D}) can be calculated as

$$I_{\text{D}}{=}\frac{d^2V_{\text{m}}^2}{4L_{12}f_{\text{S}}V_{\text{dc}}}. \tag{7}$$

The static gain (M) of proposed circuit is defined by the ratio between output voltage (V_{dc}) and maximum input voltage (V_{m}). At steady state, I_{D} is equal to the average current through the load (R_{dc}) and, hence, the static gain is obtained, expressed as

$$M = \frac{V_{\text{dc}}}{V_{\text{m}}}{=}\frac{d}{2}\sqrt{\frac{R_{\text{dc}}}{L_{12}f_{\text{S}}}} = \frac{d}{\sqrt{K_{\text{DCM}}}} \tag{8}$$

where the dimensionless parameter K_{DCM} is defined as

$$K_{\text{DCM}}{=}\frac{4L_{12}f_{\text{S}}}{R_{\text{dc}}}. \tag{9}$$

From (8), it follows that static gain M depends on the values of duty cycle d and parameter K_{DCM}. K_{DCM} is calculated by the circuit parameters, and d is obtained by the control loop. When the working condition is determined, K_{DCM} is also determined, and M can be regulated flexibly by adjusting d.

B. Input Characteristics

Based on the input–output power balance, the expression of input current (i_{in}) can be obtained in combination with (1) and (5), described as

$$i_{\text{in}}{=}\frac{d^2}{2L_{12}f_{\text{S}}}V_{\text{m}}\sin(2\pi f_{\text{l}} \cdot t). \tag{10}$$

As seen in (10), when the circuit parameters and duty cycle are fixed, the input current of proposed circuit is proportional to input voltage in DCM. The input current follows the profile of the input voltage, and thus incorporating PFC.

Additionally, the effective input resistance (r_{e}) is derived as

$$r_{\text{e}}{=}\frac{2L_{12}f_{\text{S}}}{d^2}. \tag{11}$$

At steady state, the duty cycle and switching frequency maintain at a constant value, respectively. Examining (11), it can be easily seen that the ac input side of proposed circuit behaves as a linear resistor and, hence, the power factor is almost unity.

TABLE II
Voltage and Current Stress

Device	Voltage stress	Current stress
S_1, S_2	$V_{\text{m}}{+}V_{\text{dc}}/2$	dI_e
S_3, S_4	$V_{\text{m}}{-}V_{\text{dc}}/2$	dI_e
D_1, D_2	$V_{\text{m}}{+}V_{\text{dc}}/2$	dI_e

C. Device Stress

The voltage stresses and current stresses on the switches and diodes are presented in Table II, where variable I_{e} is defined as

$$I_{\text{e}}{=}\frac{V_{\text{m}}}{L_{12}f_{\text{S}}}. \tag{12}$$

As shown in Table II, the proportion of the output voltage in the voltage stress is decreased by half with the split-capacitor structure. Thus, at the same output voltage level, the switches S_1, S_2 and the diodes D_1, D_2 can be selected with lower voltage ratings.

D. Loss Analysis

The overall efficiency of the proposed circuit depends on the losses occurring in individual components. The semiconductors contribute to the losses in the form of conduction and switching losses, and the inductor losses comprise of core losses and copper losses that occurs in the equivalent series resistor.

Applying the model equations in [26] to the proposed circuit, the loss model of each component is calculated and tabulated in Table III, and the associated current expressions are given in Table IV.

As per the analysis in operating modes, there is no switch or diode in this circuit conducting continuously. A maximum of two semiconductors conducts in current-flowing path during a switching cycle. Meanwhile, to reduce switching losses, instead of being driven synchronously by a high-frequency signal, the antiseries switches S_1 and S_2 is designed with one operating at a high switching frequency and one being always turned ON for either half-line cycle. As for diodes, the reverse recovery losses can be ignored due to the achievement of zero-current turn-OFF operations.

TABLE III
LOSS MODELS OF COMPONENTS

Loss model	Expression
P_{S_con} (switch conduction loss)	$\sum_{x=1}^{4} r_{Sx\_on} \cdot I_{Sx\_rms}^2$
P_{S_sw} (switch switching loss)	$(t_r + t_f)(\pi V_m + 2V_{dc})/8\pi \cdot \sum_{x=1}^{4} I_{Sx\_max} f_{Sx}$
P_{D_sw} (diode conduction loss)	$\sum_{x=1}^{2} (V_{Fx} \cdot I_{Dx\_avg} + r_{Dx\_on} \cdot I_{Dx\_rms}^2)$
P_L (inductor loss)	$\sum_{x=1}^{2} (r_{Lx} \cdot I_{Lx\_rms}^2 + V_{e\_Lx} \cdot k_{Fe\_Lx})$
P_C (capacitor loss)	$r_C \cdot I_{C\_rms}^2 + \sum_{x=1}^{2} ESR_x \cdot I_{Cx\_rms}^2$

TABLE IV
RMS AND AVERAGE CURRENTS OF COMPONENTS

	Component	Current expression
Rms value	S_1, S_2	$dI_e\sqrt{d/6}$
	D_1, D_2, S_3, S_4	$(2dI_e\sqrt{\pi dM})/(3\pi M)$
	L_1	$\sqrt{2}d^2 I_e/4$
	L_2	$dI_e\sqrt{(4d-3d^2)/24}$
	C	$dI_e\sqrt{(3d^2+2d)/12}$
	C_{dc1}, C_{dc2}	$dI_e\sqrt{(64dM-9\pi d^2)/(144\pi M^2)}$
Average value	D_1, D_2	$(d^2 I_e)/(4M)$

E. Parameter Design

1) DCM Boundary: Referring to the commutation process, the boundary of DCM operation occurs when the duty ratio of *Stage III* (Δ_2) tends to zero, which can be concluded as

$$\Delta_1 \le 1 - d. \tag{13}$$

Substituting (4) and (8) into (13), the following condition for DCM can be obtained as:

$$K_{\mathrm{DCM}} \le \frac{1}{[M + 2\sin(2\pi f_l \cdot t)]^2}. \tag{14}$$

From (14), it can be noted that the maximum value of K_{DCM} is calculated at the peak line. The critical condition for operating at the boundary of DCM ($K_{\mathrm{DCM\_crit}}$) is expressed as per (15), the value of K_{DCM} should be less than $K_{\mathrm{DCM\_crit}}$ when designing circuit parameters

$$K_{\mathrm{DCM\_crit}} = \frac{1}{(M+2)^2}. \tag{15}$$

2) Design of the Inductor (L_1, L_2): Due to the CCM operation of the inductor L_1, the worst case of the peak line is selected, and the inductance value of L_1 is calculated as

$$L_1 = \frac{MV_m^2\sqrt{K_{\mathrm{DCM}}}}{2\alpha P_{dc} f_S} \tag{16}$$

where P_{dc} is the output power, and α is the ripple coefficient.

Based on (9), the parallel inductance value L_{12} is obtained as

$$L_{12} = \frac{V_{dc}^2 K_{\mathrm{DCM}}}{4P_{dc} f_S}. \tag{17}$$

Substituting the calculated values of L_1 and L_{12} into (6)), the inductance value of L_2 is calculated as

$$L_2 = \frac{L_1 \cdot L_{12}}{L_1 - L_{12}}. \tag{18}$$

3) Design of the Capacitor (C, C_{dc}): Examining (4), the energy-storage capacitor voltage presents a constant value in each switching cycle and follows the input voltage profile during the line cycle. To ensure that the energy-storage capacitor has a good voltage tracking performance and avoid the oscillation with the circuit inductors, the capacitance value of C can be obtained by the following equation:

$$C = \frac{1}{4\pi^2 f_r^2 (L_1 + L_2)} \tag{19}$$

where f_r is the resonant frequency, which is generally designed at about 10% of the switching frequency f_S.

Based on (5) and (12), the current relationship at the output during a line cycle can be expressed as

$$\frac{C_{dc}}{2}\frac{dV_{dc}}{dt} = \frac{d^2 I_e}{4M} - \frac{V_{dc}}{R_{dc}} - \frac{d^2 I_e}{4M}\cos(4\pi f_l \cdot t) \tag{20}$$

where C_{dc} is the capacitance value of the output capacitor.

Since the value of C_{dc} is larger, it can be considered that the dc component of the diode current flows into the load R_{dc} and the ac component flows into the output capacitor. Hence, it can be obtained that

$$\begin{cases} \frac{V_{dc}}{R_{dc}} = \frac{d^2 I_e}{4M} \\ \frac{C_{dc}}{2}\frac{dV_{dc}}{dt} = -\frac{d^2 I_e}{4M}\cos(4\pi f_l \cdot t). \end{cases} \tag{21}$$

Based on (21), the ripple voltage ($\tilde{v}_{\mathrm{dc\_ripple}}$) is calculated as

$$\tilde{v}_{\mathrm{dc\_ripple}} = -\frac{d^2 I_e}{8\pi f_l C_{dc} M}\sin(4\pi f_l \cdot t). \tag{22}$$

From (22), it is clearly seen that the oscillation frequency of $\tilde{v}_{\mathrm{dc\_ripple}}$ is twice the input line frequency, and its amplitude is directly related to the output capacitance value, which implies that the output capacitor needs to be large enough to minimize the ripple voltage. Based on (22, the capacitance value of C_{dc} is calculated as

$$C_{dc} = \frac{MK_{\mathrm{DCM}} I_e}{8\pi f_l v_{\mathrm{ripple\_m}}} \tag{23}$$

where $v_{\mathrm{ripple\_m}}$ is the ripple voltage amplitude.

IV. CONTROL SYSTEM DESIGN

As previously cited, the input current of proposed converter has commendable current-shaping ability with no current-loop control in DCM, and, hence, only a control loop for the output voltage is needed.

A. Small-Signal Modeling

According to the current relationship at output, the average model for the output voltage in relation to the duty cycle can be obtained as

$$\frac{C_{dc}}{2}\frac{dv_{dc}}{dt} = \frac{d^2 I_e V_m}{4v_{dc}} - \frac{v_{dc}}{R_{dc}}. \tag{24}$$

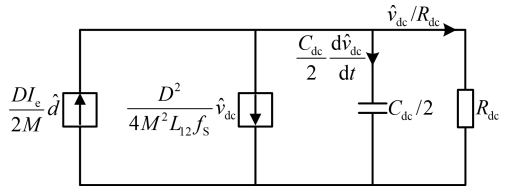

Fig. 6. Small-signal equivalent circuit.

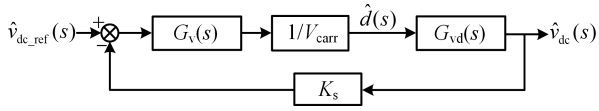

Fig. 7. Block diagram of output voltage closed-loop control.

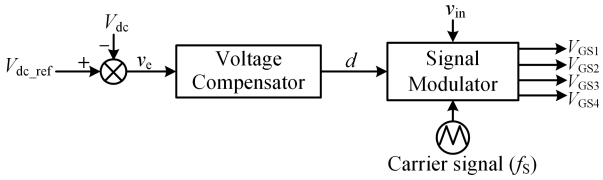

Fig. 8. Control scheme diagram.

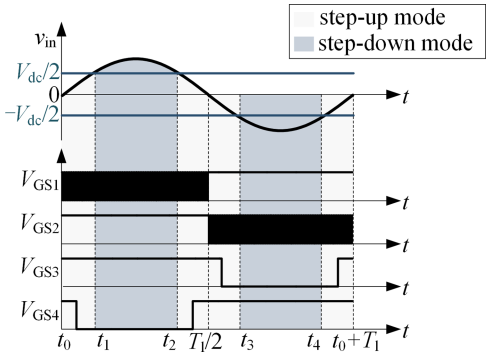

Fig. 9. Gate signal waveforms for switches in an AC line cycle.

Examining (24), it is noted that the average model equation is nonlinear. Applying disturbance ($\hat{d}$and $\hat{v}_{\rm dc}$) in the quiescent operating point (D and $V_{\rm dc}$), the perturbation equation can be formulated in partial function form as

$$\frac{C_{\rm dc}}{2}\frac{{\rm d}\hat{v}_{\rm dc}}{{\rm d}t}=\frac{DI_{\rm e}}{2M}\hat{d}-\frac{D^2}{4M^2L_{12}f_{\rm S}}\hat{v}_{\rm dc}-\frac{1}{R_{\rm dc}}\hat{v}_{\rm dc}. \tag{25}$$

According to (25), the equivalent circuit of the small-signal model is constructed, as depicted in Fig. 6 .

Applying Laplace transform to the perturbation equation and effecting the pertinent mathematical operations, the output-to-control transfer function $G_{\rm vd}(s)$ is calculated as

$$G_{\rm vd}(s)=\frac{\hat{v}_{\rm dc}(s)}{\hat{d}(s)}=\frac{DI_{\rm e}}{MC_{\rm dc}s+\frac{D^2}{2ML_{12}f_{\rm S}}+2\frac{M}{R_{\rm dc}}}=\frac{G_0}{1+s/\omega_0} \tag{26}$$

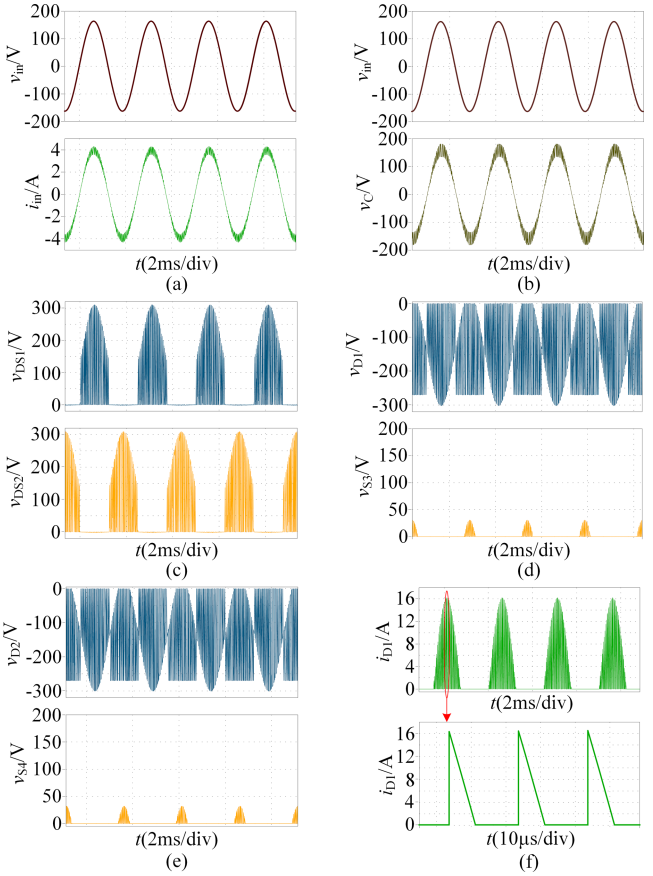

Fig. 10. Steady-state simulated results. (a) Input waveforms. (b)–(e) Voltage waveforms of C, S_1, S_2, D_1, D_2, S_3, S_4. (f) Diode current waveforms.

where the coefficients G_0, ω_0 is defined as

$$\begin{cases} G_0=\dfrac{2MDR_{\rm dc}I_{\rm e}L_{12}f_{\rm S}}{D^2R_{\rm dc}+4M^2L_{12}f_{\rm S}} \\ \omega_0=\dfrac{D^2R_{\rm dc}+4M^2L_{12}f_{\rm S}}{2M^2R_{\rm dc}C_{\rm dc}L_{12}f_{\rm S}}. \end{cases} \tag{27}$$

B. Closed-Loop Control

The closed-loop control for output voltage is shown in Fig. 7. Wherein, $K_{\rm s}$ is the voltage sampling coefficient, $V_{\rm carr}$ is the peak value of PWM carrier, and $G_{\rm v}(s)$ is the transfer function of the voltage compensator, expressed as

$$G_{\rm v}(s)=K_{\rm p}\left(1+\frac{1}{\tau s}\right) \tag{28}$$

where $K_{\rm p}$ and τ are the proportional and integral coefficients.

Recalling (22), the output voltage ripple frequency is twice the line frequency. To attenuate the excessive second-harmonic injection from the output voltage into duty cycle, the crossover frequency of voltage compensator is designed as 160 Hz, well below twice the line frequency (800 Hz).

Based on (26) and (28), the open-loop transfer function of the control system $G(s)$ can be derived as

$$G(s)=\frac{K_{\rm s}}{V_{\rm carr}}G_{\rm v}(s)G_{\rm vd}(s)=\frac{K_{\rm s}K_{\rm p}G_0(\tau s+1)}{V_{\rm carr}\tau s(1+s/\omega_0)}. \tag{29}$$

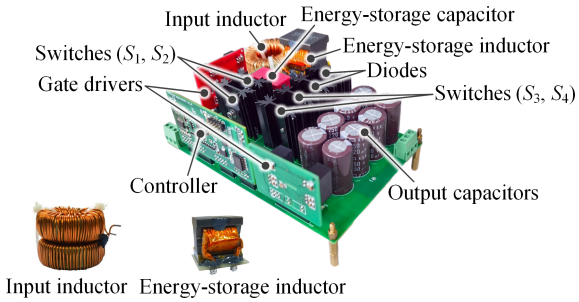

Fig. 11. Laboratory prototype.

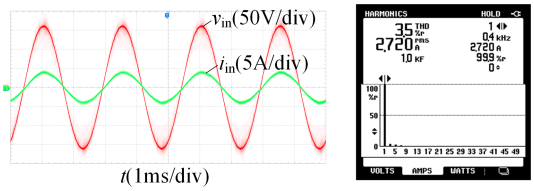

Fig. 12. (a) Measured input voltage and current waveforms at 115-Vrms/400-Hz input with rated load. (b) Input current harmonic analysis.

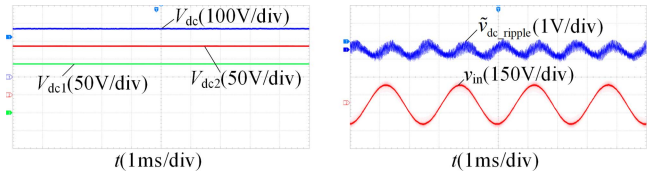

Fig. 13. (a) Measured voltage waveforms of the DC output and filter capacitors. (b) Measured output voltage ripple waveform simultaneous to input voltage.

As seen from (29), this system is the minimum phase system, which consists of left-half plane zero or pole. In comprehensive consideration of transient performance and stability, the phase margin of open-loop transfer function is designed as 45°.

C. Control Scheme

The control scheme of the proposed converter is depicted in Fig. 8. Based on the signals of the duty cycle, carrier, and input line voltage, the signal modulator generates the control signals V_{GS1}, V_{GS}, V_{GS3}, V_{GS4} to drive the switches S_1, S_2, S_3, S_4, and the gate signal waveforms over a line cycle are shown in Fig. 9.

As shown in Fig. 9, S_1 and S_2 are controlled to operate at a high switching frequency for half a line cycle, and S_3 and S_4 are controlled to operate at line frequency. During the positive half-line cycle, S_1 is driven by a high-frequency control signal with a duty cycle of d, S_2 and S_3 are driven to be always turned ON, whereas S_4 is always turned OFF within the interval of step-down mode. During the negative half-line cycle, S_2 is driven by a high-frequency control signal with a duty cycle of d, S_1 and S_4 are driven to be always turned ON, whereas S_3 is always turned OFF within the interval of the step-down mode.

V. Verification and Discussion

To validate the theoretical analysis of the proposed circuit, a 300-W prototype is designed with the following specifications.

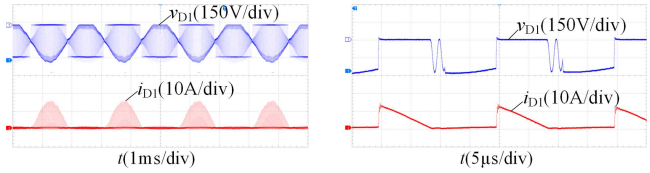

Fig. 14. Measured voltage and current waveforms of diode D_1. (a) Line cycle. (b) Switching cycle.

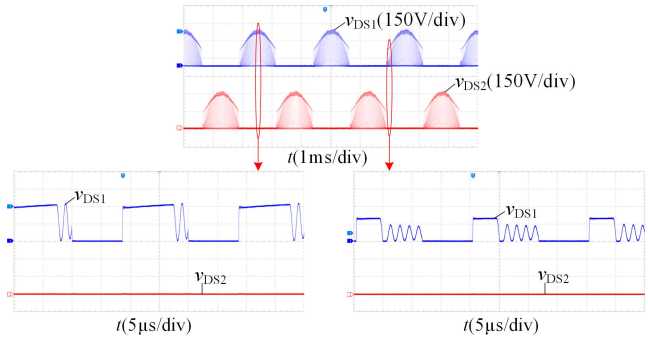

Fig. 15. Measured drain-source voltage waveforms of switches S_1 and S_2.

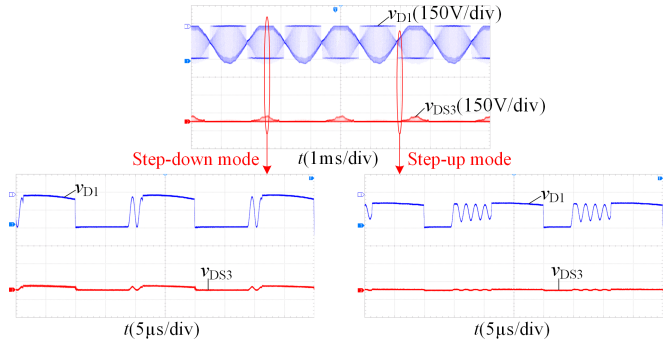

Fig. 16. Measured voltage waveforms of diode D_1 and switch S_3.

1) Input voltage: $v_{in} = 115$ Vrms±10% / 400 Hz.
2) Output voltage: $V_{dc} = 270$ V.
3) Switching frequency: $f_S = 50$ kHz.

A. Parameter Calculation

Based on the specifications and design equations, the values of the circuit parameters are calculated as follows.

1) Find K_{DCM_crit} from (15), and set K_{DCM} as 0.8 K_{DCM_crit}.
2) Find L_1 from (16), where $\alpha = 0.2$.
3) Calculate L_{12} from (17).
4) Find L_2 from (18).
5) Find C from (19), where $f_r = 10\% f_S$.
6) Find C_{dc} from (23), where $V_{ripple\_m} = 500$ mV.

From the above procedure, the circuit parameters are obtained and listed in Table V.

B. Simulation Results

PLECS software is utilized to undertake the simulations and analysis of the proposed circuit under the parameters shown in Table V. The circuit nominally operates at 115-Vrms ac mains

TABLE V
CONVERTER PARAMETERS

Component	Parameter
L_1 (Input inductor)	1.6 mH (Core: CH468060)
L_2 (Energy-storage inductor)	76 μH (Core: PQ26/20)
C (Energy-storage capacitor)	1 μF
$C_{dc1} = C_{dc2}$ (Output capacitors)	220 μF×4

TABLE VI
SELECTION FOR SEMICONDUCTORS

Component	Parameter
S_1/S_2 (MOSFETs)	IPZ60R060C7
S_3/S_4 (MOSFETs)	IRFP3710PBF
D_1/D_2 (Diodes)	HFA15TB60PBF

and regulates the dc output voltage at 270 V. The steady-state performance of the proposed circuit is demonstrated in Fig. 10.

The input waveforms in Fig. 10(a) verify the inherent power factor correction property of the proposed circuit. The input current presents a sinusoidal shape and in phase with the input voltage. Fig. 10(b) exhibits the voltage of the energy-storage capacitor along with the ac input voltage, and it is clearly seen that the capacitor voltage appears sinusoidal and closely tracks the input voltage. The expected voltage synchronization in (4) is fulfilled. Moreover, the voltage waveforms of switches and diodes are illustrated in Fig. 10(c)–(e). S_1 or S_2 operates at high switching frequency for half a line cycle, and always conducts for the other half. S_3 or S_4 withstands the voltage difference in step-down mode. The measured maximum voltage value of S_1, S_2, D_1, and D_2 is 302 V, basically equal to the theoretical stress value $V_m+V_{dc}/2$. The maximum voltage of S_3 and S_4 is measured as 32 V, basically equal to the theoretical stress value V_m-$V_{dc}/2$. Fig. 10(f) exhibits the waveforms of diode currents, and it is clearly seen that the DCM operations are achieved, as expected by the design.

C. Experimental Results

Based on the simulated results, a prototype shown in Fig. 11 is developed to validate the performance and analytical results of proposed converter. The circuit parameters are the same as those in simulation, as shown in Table V. A single-chip microcontroller (TMS320F280049C) is utilized to control the circuit, and the selection for semiconductors is given in Table VI.

The input voltage and current waveforms with rated load are shown in Fig. 12. The high-power-factor operation of the proposed converter is clearly brought out in the current waveform. The input current is sharped to be sinusoidal with a measured THD of 3.5% and in phase with the input line voltage with a measured power factor of 0.996.

The voltage waveforms of the dc output and filter capacitors are shown in Fig. 13, with average values of 270 V and 135 V, respectively. The output voltage ripple shows an amplitude of 500 mV and a frequency of 800 Hz, twice the frequency of the input voltage.

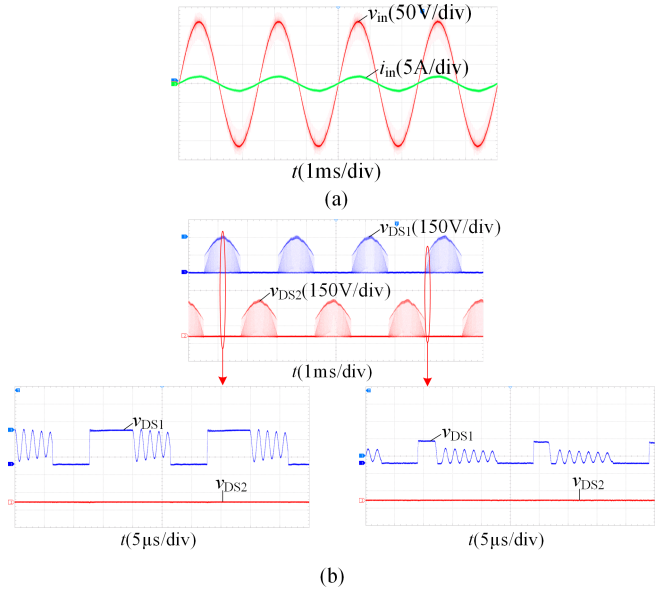

Fig. 17. Measured operating waveforms at 115-Vrms/ 400-Hz input with half load. (a) Input voltage and current. (b) Drain-source voltages of switches S_1, S_2.

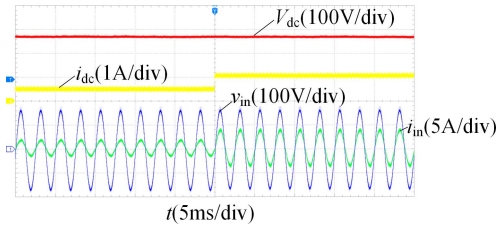

Fig. 18. Measured dynamic waveform with load changing from 50 to 100% of the rated power with closed-loop control.

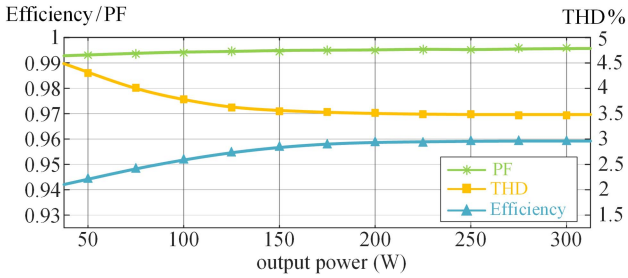

Fig. 19. Measured PF / THD / efficiency versus output power.

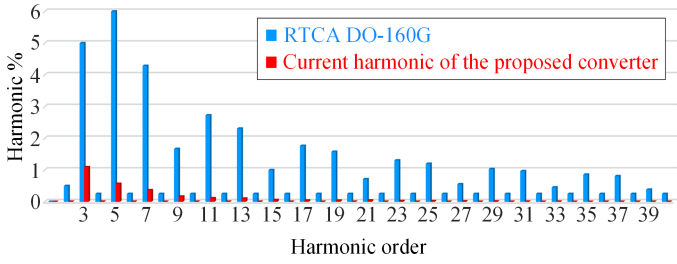

Fig. 20. Measured harmonic contents of the input current (40th) for DO-160G.

TABLE VII
COMPARISON OF PASSIVE COMPONENTS

SEPIC PFC circuits	Inductor		Capacitor	
	Value	Energy	Value	Energy
Conventional	$\begin{cases} L_1=\dfrac{dV_m}{\Delta I_{ripple\_m} f_S} \\ L_{12}=\dfrac{d^2V_m^2}{4f_S P_{dc}} \end{cases}$	$\begin{cases} E_{L1}=\dfrac{2L_1P_{dc}^2}{V_m^2} \\ E_{L2}=\dfrac{L_2}{2}\left(\dfrac{dV_m}{f_S L_2}-\dfrac{2P_{dc}}{V_m}\right)^2 \end{cases}$	$\begin{cases} C=\dfrac{1}{4\pi^2 f_r^2 (L_1+L_2)} \\ C_{dc}=\dfrac{P_{dc}}{4\pi f_l V_{dc} V_{ripple\_m}} \end{cases}$	$\begin{cases} E_C=\dfrac{1}{2}CV_m^2 \\ E_{Cdc}=\dfrac{1}{2}C_{dc}V_{dc}^2 \end{cases}$
Dual-SEPIC in [13]	$\begin{cases} L_1=\dfrac{dV_m}{\Delta I_{ripple\_m} f_S} \\ L_{12}=\dfrac{d^2V_m^2}{4f_S P_{dc}} \end{cases}$	$\begin{cases} E_{L1}=\dfrac{2L_1P_{dc}^2}{V_m^2} \\ E_{L2}=\dfrac{L_2}{2}\left(\dfrac{dV_m}{f_S L_2}-\dfrac{2P_{dc}}{V_m}\right)^2 \end{cases}$	$\begin{cases} C=\dfrac{1}{4\pi^2 f_r^2 (L_1+L_2)} \\ C_{dc}=\dfrac{P_{dc}}{4\pi f_l V_{dc} V_{ripple\_m}} \end{cases}$	$\begin{cases} E_C=\dfrac{1}{2}CV_m^2 \\ E_{Cdc}=\dfrac{1}{2}C_{dc}V_{dc}^2 \end{cases}$
Proposed	$\begin{cases} L_1=\dfrac{dV_m}{\Delta I_{ripple\_m} f_S} \\ L_{12}=\dfrac{d^2V_m^2}{4f_S P_{dc}} \end{cases}$	$\begin{cases} E_{L1}=\dfrac{2L_1P_{dc}^2}{V_m^2} \\ E_{L2}=\dfrac{L_2}{2}\left(\dfrac{dV_m}{f_S L_2}-\dfrac{2P_{dc}}{V_m}\right)^2 \end{cases}$	$\begin{cases} C=\dfrac{1}{4\pi^2 f_r^2 (L_1+L_2)} \\ C_{dc}=\dfrac{P_{dc}}{2\pi f_l V_{dc} V_{ripple\_m}} \end{cases}$	$\begin{cases} E_C=\dfrac{1}{2}CV_m^2 \\ E_{Cdc}=\dfrac{1}{4}C_{dc}V_{dc}^2 \end{cases}$

ΔI_{ripple_m}: Maximum input current ripple; V_{ripple_m}: Output voltage ripple amplitude.

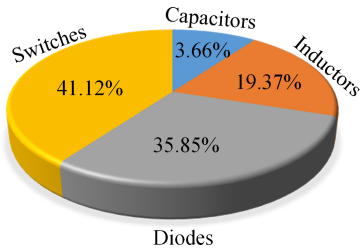

Fig. 21. Loss distribution of the proposed circuit.

The voltage and current waveforms of diode D_1 are shown in Fig. 14. It is evident that the diode is turned OFF at zero current, and the proposed converter operates in DCM.

The voltages across switches S_1 and S_2 are shown in Fig. 15, and it can be seen that the proposed circuit has three operating stages during one switching cycle. The voltage peak of S_1 and S_2 is measured as 307 V, approximately equal to the simulated value.

The voltages across diode D_1 and switch S_3 are shown in Fig. 16. It can be seen that D_1 is reverse-biased in the step-up mode and S_3 withstands the voltage difference in the step-down mode. The maximum voltage values of D_1 and S_3 are measured as 305 V and 36 V, approximately equal to the simulated values.

The operating waveforms with half load are shown in Fig. 17. The input current is pure sinusoidal and in phase with the input voltage, and the converter still exhibits three operating stages in a switching cycle.

Fig. 18 shows the converter responses to load changing from 50 to 100% with the closed-loop control, showing a satisfactory behavior. The output voltage maintains constant when the load step change occurs, and there is no oscillation around twice the input frequency of 800 Hz, which verifies the effectiveness of the closed-loop control.

D. Efficiency Analysis

Fig. 19 presents the curves of PF, THD, and efficiency, at 115-Vrms input and 270-V output with respect to variation of load. The power quality analyzer is used to conduct the tests.

As depicted in Fig. 19, the measured THD is observed to be within 5% limit, and the measured input current PF is close to unity (i.e., larger than 0.99). The maximum measured efficiency at rated load reaches 95.92%.

The measured harmonic contents of the input current at 400 Hz with rated load are shown in Fig. 20, where it is compared to RTCA DO-160G Std, and it can be seen that all harmonics are lower than the DO-160G limits.

Moreover, based on the relevant data and loss models given in Table III, the comprehensive losses occurring in the proposed circuit at rated load are calculated, and the loss distribution is presented in Fig. 21.

As shown in Fig. 21, it is clear that most of the losses are in the semiconductors, and these losses can be reduced by using the switches with lower ON-resistance and the diodes with lower forward-voltage drop. Regarding the inductors, the losses can be further reduced by optimizing the design methodology.

E. Comparative Analysis

A comparison in terms of inductance/capacitance value and inductor/capacitor energy is given in Table VIII. In view of the same working principle, the inductance values and energies of the proposed circuit have the same expressions as the classic SEPIC PFC circuits. The voltage of each output capacitor is reduced by half with the split-capacitor output structure, while the total energy of output capacitors in the proposed circuit is the same as that in the classic circuit due to the double output capacitance.

Table VIII draws a comparison among the proposed circuit, conventional SEPIC PFC circuit, and the other modified SEPIC PFC circuits presented in [12], [13], [16], [17], [18], [19], [20], [23], and [24]. From the quantitative comparison in relation to the count of conducting semiconductors, it can be clearly seen that the proposed circuit eliminates the diode that operates at all times and has lower conduction losses and higher efficiency with minimal number of conducting semiconductors in each operating stage as compared to other circuits. Simultaneously, the switching losses of the proposed circuit are reduced with

TABLE VIII
PERFORMANCE COMPARISON OF DIFFERENT SEPIC PFC CIRCUITS

SEPIC PFC circuits	Total number of passive elements	Total number of semiconductors	Conducting semiconductors			Voltage stress	Peak efficiency
			Stage I	*Stage II*	*Stage III*		
Conventional	4(2*L*/2*C*)	6(1*S*/5*D*)	1*S*2*D*	3*D*	2*D*	V_m+V_{dc}	93.5 % (100 W)
Totem-pole in [12]	4(2*L*/2*C*)	5(2*S*/3*D*)	2*S*1*D*	1*S*2*D*	1*S*1*D*	V_m+V_{dc}	94.5 % (100 W)
Dual-SEPIC in [13]	7(4*L*/3*C*)	6(2*S*/4*D*)	1*S*1*D*	2*D*	1*D*	V_m+V_{dc}	94 % (50 W)
Modified in [16]	7(3*L*/4*C*)	9(2*S*/7*D*)	1*S*2*D*	3*D*	1*D*	$(V_m+V_{dc})/2$	95.3 % (200 W)
Modified in [17]	7(4*L*/3*C*)	8(2*S*/6*D*)	1*S*2*D*	3*D*	1*D*	V_m+2V_{dc}	93.58 % (300 W)
Modified in [18]	7(4*L*/3*C*)	7(1*S*/6*D*)	1*S*2*D*	3*D*	1*D*	V_m+V_{dc}	94.5 % (450 W)
Modified in [19]	5(3*L*/2*C*)	6(2*S*/4*D*)	2*S*1*D*	1*S*3*D*	1*S*1*D*	V_m+2V_{dc}	93.1 % (300 W)
Modified in [20]	7(3*L*/4*C*)	6(2*S*/4*D*)	2*S*1*D*	1*S*3*D*	1*S*1*D*	V_m+V_{dc}	93.7 % (300 W)
Modified in [23]	6(2*L*/4*C*)	7(1*S*/6*D*)	1*S*3*D*	3*D*	2*D*	V_m+V_{dc}	91 % (400 W)
Modified in [24]	7(3*L*/4*C*)	6(2*S*/4*D*)	1*S*1*D*	2*D*	1*D*	$V_m+V_{dc}/2$	95.4 % (300 W)
Proposed	5(2*L*/3*C*)	6(4*S*/2*D*)	2*S*	1*S*1*D*	0	$V_m+V_{dc}/2$	95.92 % (300 W)

S: Switch; *D*: Diode; *L*: Inductor; *C*: Capacitor.

the decrease of voltage stress. Thus, the power losses associated with semiconductors are reduced and the size of the cooling fin is also minimized. Furthermore, as a modified version of dual-SEPIC, instead of integrating two SEPIC units, the proposed circuit employs one SEPIC unit with a common set of input inductor and energy-storage cell. The utilization of passive components is improved and the volume/weight is also reduced. As for semiconductors, the proposed circuit employs two more switches, resulting in the need for two more drivers.

VI. CONCLUSION

In this article, a modified bridgeless SEPIC PFC converter applied for medium-line-frequency applications is presented, analyzed, and validated. The antiseries switches are employed at the input side to provide a bidirectional channel for inductor currents. The unidirectional switches consisting of a diode and a switch in series are used at the output side to form the split-capacitor structure. In this configuration, the conduction losses are reduced with a maximum of two conducting semiconductors in the power-flowing path. Only one set of input filter inductor, energy-storage capacitor and inductor is needed, thus improving the passive component utilization. Time-domain analysis is presented to analyze the operating stages of the step-up and step-down modes, and the steady-state characteristics such as static gain and stress are described in detail to design parameters. In DCM, the input current over a switching cycle is proportional to the input voltage, and the PFC function can be achieved with no current-loop control. Finally, a 300-W laboratory prototype has been constructed, and test results corroborate the theoretical analysis. The proposed converter achieves high-power-factor operations with efficiency as high as 95.92% and current THD as low as 3.5%.

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