Modeling and Decoupled Control of the Three-Level Interleaved DC–DC Converter With Coupled Inductors

Ivan Z. Petrić, *Member, IEEE*

***Abstract*—For emerging high power dc–dc applications, such as those in power-to-x and energy storage systems, the three-level interleaved converter with coupled inductors offers several advantages, such as increased voltage and current ratings and a strong reduction of the output current ripple. However, due to series and parallel connections of the switching cells, voltage imbalance and circulating currents may appear, which is why their active suppression is necessary. This article presents small-signal modeling and control design of the three-level interleaved converter with coupled inductors, focusing on the coupling between the duty cycles of the switching cells and the state variables. Transformations of state variables and control inputs are proposed to diagonalize the system and facilitate decoupled closed-loop control. Digital control implementation is analyzed, focusing on modulation and oversampled filtering of the inductor currents used to suppress aliasing and feedback noise. The experimental verifications are performed on the three-level two-phase interleaved buck prototype, for powers up to 100 kW.**

***Index Terms*—Active balancing, energy storage systems (ESSs), high power dc–dc, interleaving, multilevel, power-to-x systems.**

I. Introduction

HIGH power dc–dc power electronic converters are crucial for many emerging power-to-x and energy storage systems (ESS) applications [1], [2], [3], [4], [5], [6], [7], [8]. These converters are typically cascaded with power factor correction rectifiers or inverters [6] to interface with the grid. In applications up to a few kVs, the intermediate dc-link is often split in two, using series-connected capacitor banks, to accommodate some of the most-commonly used high power rectifiers/inverters, e.g., the neutral-point clamped or T-type converters [9]. An example of such a system is shown in Fig. 1(a).

For a split dc-link, a promising step-down topology is the three-level buck converter [10], [11], [12], [13], as it allows using lower-voltage switches while reducing the output current ripple in case the phase-shifted pulsewidth modulation (PS-PWM) is applied [14]. To accommodate higher currents, several three-level legs (phases) can be interleaved. The most frequently reported configuration uses two interleaved phases, forming the three-level two-phase (3L-2P) buck converter [15], [16], [17], [18], [19], [20], illustrated in Fig. 1(b). The 3L-2P buck converter can further reduce the output current ripple if all four switching cells are switched in a phase-shifted manner. This, however, increases the individual phase currents ripples [21], which can be suppressed using coupled inductors [18].

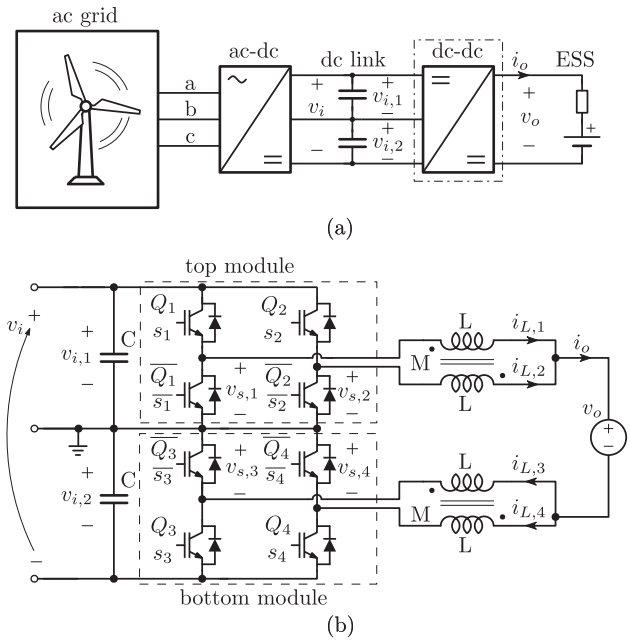

Fig. 1. (a) Illustration of an AC–DC system suitable for power-to-x or ESS applications. The output current is regulated by the analyzed DC–DC converter connected to a split DC-link. (b) The 3L-2P interleaved buck converter with coupled inductors.

Typical modulation of the three-level interleaved converter features phase-shifted switching signals with equal duty cycles, which is termed the symmetric PS-PWM. For ideally symmetric circuit, such modulation results in equal current sharing between the phases and a balanced dc-link [18]. However, due to asymmetric parasitics and component tolerances, timing mismatches between the cells, and more, the open-loop symmetric modulation inevitably results in low-frequency circulating currents and imbalance of the input voltages, deteriorating the converter's performance and potentially causing overvoltage or overcurrent failures. Therefore, alongside output current (or voltage) regulation, it is important to implement controllers for input voltage balancing and suppression of circulating currents. In the three-level interleaved converter with coupled inductors,

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The author is with the Hanwha Q CELLS America Inc., Santa Clara, CA 95054 USA (e-mail: ivan5ric@ieee.org).

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state variables are strongly coupled via duty cycles, which brings a challenge in preventing interactions between the abovementioned control systems.

Several papers propose solutions for input voltage balancing and output current control of the single-phase three-level buck converter [10], [11], [12], [22], [23], [24], [25]. The papers [5], [16], [26] analyze the 3L-2P buck with discrete phase inductors. In [5], sliding-mode control is proposed for the output current regulation and input voltage balancing. Circulating currents suppression is not considered and the paper does not analyze the system coupling. In [16] the authors implement the output current control, the input voltage balancing, and the top-module circulating current control. The bottom-module circulating current controller (CC) is lacking and no analysis is provided for the system coupling and loop interactions. In [26] the authors focussed on a higher level objective of power balance management between the 3L-2P buck and other converters sharing the same dc-link. Individual phase CCs are employed and a corrective action is added to mismatch the duty cycles to balance the input voltages. Again, the authors do not analyze loop interactions and the implemented control system remains coupled. The articles mentioned above do not consider coupled inductors, which would further increase interactions between the control loops. To the best of author's knowledge, a complete and detailed dynamic modeling, analysis of coupling, and a systematic design of a decoupling control system of even the 3L-2P buck converter is not present in the literature. Accordingly, the extension to the three-level N-phase configuration is lacking as well.

To fill in the gaps of previous research, the first objective of this article is to derive an averaged small-signal dynamic model of the 3L-2P converter with coupled inductors and use it to propose a decoupled control system that regulates the output current, suppresses the circulating currents, and balances the input dc-link voltages. This is achieved by proposing suitable state variable and control input transformations that decouple (diagonalize) the system, transforming it from a multiple-input multiple-output (MIMO) to four single-input single-output (SISO) control systems. The presentation follows by generalizing the approach to the three-level N-phase interleaved converter with coupled inductors. Subsequently, for the 3L-2P configuration that is experimentally tested, a procedure for designing individual control loops is provided, focusing on the digital modulation and the oversampled filtering of the inductor currents used to suppress noise and aliasing in practical implementations. The small-signal model and the designed control stage are validated with frequency response measurements and time-domain tests, both using control hardware-in-the-loop (C-HIL) and a hardware prototype. While the paper adopts terminology designated for the buck configuration, where the dc-link is considered as the input port, the methodology is applicable to the boost-type as well.

The main contributions of this article are as follows.

1) Small-signal modeling of the 3L-2P interleaved converter with coupled inductors that highlights the coupling between the duty cycles and the state variables.
2) Proposed transformations of state variables and control inputs that diagonalize the system, allowing for decoupled control of the output current (or voltage), circulating currents suppression, and input voltage balancing.
3) Extension and generalization of the proposed approach to the three-level N-phase interleaved configurations.
4) Detailed analysis of the proposed digital control system implementation, focused on modulation and oversampled averaging used for robust feedback signal acquisition.

The rest of this article is organized as follows. Section II recalls operating principles of the 3L-2P converter. Section III presents the averaged small-signal modeling and proposes a method for system decoupling. Section IV generalizes the approach to the three-level N-phase configuration. In Section V, the decoupled closed-loop systems are designed for the 3L-2P converter and the digital implementation is detailed. Section VI brings experimental verifications of the proposed control system. Finally, Section VII concludes this article.

II. Principle of Operation

The 3L-2P interleaved buck converter with coupled inductors is shown in Fig. 1(b). While Fig. 1(b) illustrates the bidirectional configuration, all following derivations remain valid for the continuous conduction mode of the unidirectional configuration, where the inner transistors ($\overline{Q_1} - \overline{Q_4}$) are replaced with diodes. It is assumed that the dc-link input voltage v_i is fixed and the output voltage v_o is considered to be a slowly varying external disturbance. The analyzed 3L-2P buck comprises two three-level buck phases, interleaved via coupled inductors. The coupled inductors are described by the self-inductance $L = L_\sigma + M$, the mutual inductance $M > 0$, and the leakage inductance L_σ [27]. The 3L-2P converter has four switching cells, each having the half-bridge structure. The top and bottom modules feature input capacitors C that, in balanced scenarios, split the input voltage v_i in two halves, i.e., $v_{i,1} = v_{i,2} = v_i/2$. The output current is shared between the two phases, relaxing also the current stress of the semiconductors. Such modular connection allows increasing the 3L-2P buck's voltage and current handling above the individual ratings of the chosen semiconductors, in which case, maintaining the input voltage balance and equal current sharing is crucial to prevent overvoltages or overcurrents.

The theory of operation and a detailed harmonic analysis of the 3L-2P converter can be found in [18]. In this article, only the basic operating principles are recalled. Each transistor Q_j is controlled using its logic switching signal s_j, which is defined by the modulation (switching) period T_{pwm}, phase angle, and duty cycle D_j. The switching frequency is labeled as $f_{\text{pwm}} = 1/T_{\text{pwm}}$. Complementary transistors and their logic switching signals are labeled as $\overline{Q_j}$ and $\overline{s_j}$. The switched node voltage of each switching cell is labeled as $v_{s,j}(t)$. The equivalent, common mode, switched node voltage v_s^{cm}, determines the converter's output [18] and is equal to

$$v_s^{\text{cm}}(t) = \frac{s_1(t) + s_2(t)}{2} v_{i,1}(t) + \frac{s_3(t) + s_4(t)}{2} v_{i,2}(t). \quad (1)$$

For balanced input voltages, $v_s^{\text{cm}}(t) = v_i(t)(s_1(t) + s_2(t) + s_3(t) + s_4(t))/4$. In steady-state, assuming zero resistances and voltage drops, the time integral of $v_s^{\text{cm}}(t)$ over T_{pwm} gives the average output voltage v_o. In nominal balanced conditions, a unique duty cycle is applied to all the switching cells, i.e.,

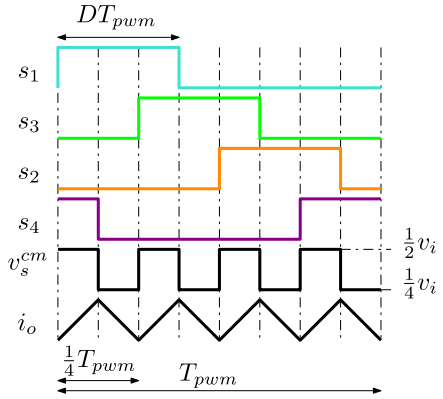

Fig. 2. The $\mathbb{N}$-*interleaving* PS-PWM switching pattern for the 3L-2P converter. The illustration shows symmetric modulation with $D = 3/8$. In balanced conditions, the common mode switching node voltage, which determines the output current i_o, is a square waveform with the period $T_{\text{pwm}}/4$.

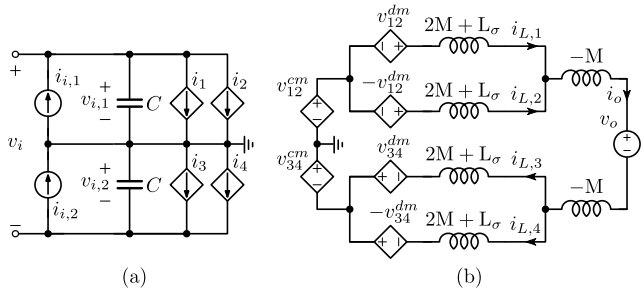

Fig. 3. Average circuits representation of the analyzed 3L-2P buck from Fig. 1(b): (a) the input side circuit and (b) the output side circuit.

$D_1 = D_2 = D_3 = D_4 = D$, yielding the average output voltage equal to $v_o = Dv_i$. For a perfectly symmetric 3L-2P power stage, such modulation does not generate circulating currents nor the voltage imbalance. However, in practical realizations some asymmetries are always present; hence, the open-loop symmetric modulation cannot ensure balanced operation. Rather, it can only be guaranteed via control.

The output current ripple is determined by $v_s^{\text{cm}}(t)$ and the leakage inductances of the coupled inductors [18]. The PS-PWM switching pattern determines the phase angles of the switching signals and has a decisive impact on the harmonic content of all currents and voltages [18]. Without the loss of generality, in this article, the, so-called, $\mathbb{N}$-*interleaving* is implemented, for which the switching signals are phase-shifted 90° apart in the sequence $s_1(t)$-$s_3(t)$-$s_2(t)$-$s_4(t)$. Note that the switching pattern selection does not have an impact on the proposed average modeling. As in other multi-cell converters, phase-shifting the switching signals brings a significant output ripple reduction, due to the harmonic cancellation effects [14]. For the 3L-2P buck, in nominal and balanced conditions, the output ripple frequency is increased four times with respect to the modulation frequency f_{pwm} and the voltage step of $v_s^{\text{cm}}(t)$ is reduced to $v_i/4$, bringing a total of 16 times reduction of the output current maximal peak-to-peak ripple, compared to the two-level single-phase buck converter with the same input voltage v_i, output inductance L_σ, and the switching frequency f_{pwm}. The $\mathbb{N}$-*interleaving* switching pattern and the resulting v_s^{cm} and i_o are shown in Fig. 2, illustrated for a symmetric balanced operation with $D = 3/8$. Concerning the switching ripple of individual phase currents, the phase-shifted interleaving increases their magnitudes [21], which results in increased losses of the converter. For this reason, the analyzed 3L-2P buck implementation features coupled inductors whose mutual inductances create high-impedance paths for the high-frequency circulating currents [18]. The mutual inductance value can be chosen based on targeted maximal phase current ripple, using the procedure from [18]. The inductors are designed to impede the circulating currents' ripple components only and not the low-frequency content. It is assumed that the coupled inductors operate in the linear region, considering that control is implemented to keep the low-frequency circulating currents close to zero.

In this article, the main control objective is to regulate the output current i_o, in order to enable the required energy flow. This can be simply replaced by the direct output voltage control, or by adding an outer voltage loop. Besides this, two more control goals appear. First, the input voltage must be balanced, i.e., $\Delta v_i = v_{i,2} - v_{i,1} \approx 0$. This ensures that semiconductors' voltages do not exceed their limits and also enables the frequency multiplication at the output. The second goal is to ensure near-zero low-frequency circulating currents, i.e., $\Delta i_{L,12} = i_{L,1} - i_{L,2} \approx 0$ and $\Delta i_{L,34} = i_{L,3} - i_{L,4} \approx 0$. Besides preventing overcurrent damages, this reduces losses, directly, by reducing the low-frequency currents flowing through the converter, and indirectly, by preventing saturation of the coupled inductors so that they can suppress the high-frequency circulating currents. As shown in the following section, the control objectives described above are coupled when the duty cycles of the switching cells are used as the control inputs.

III. Small-Signal Modeling

For dynamic modeling, switching harmonics are not considered and all variables are assumed to be averaged over T_{pwm}, which is not further emphasized by any symbol. Standard small ripple assumptions are adopted and the switching signals s_j are replaced by their continuous-time duty cycles d_j [28].

The large-signal average dynamics of the 3L-2P buck converter from Fig. 1(b) can be analyzed using the two circuits shown in Fig. 3 [18]. The circuit in Fig. 3(a) represents the input side and is used for modeling dynamics of the capacitor voltages. The circuit in Fig. 3(b) represents the output side and is used for modeling dynamics of the inductor currents. Parasitic resistances are not included in the model as their impact can typically be neglected for control design.

A. Input Side Dynamics

As the input voltage is assumed to be fixed, the only dynamics of interest is the one of the dc-link voltage imbalance Δv_i. The input voltages can be represented as $v_{i,1} = (v_i - \Delta v_i)/2$ and $v_{i,2} = (v_i + \Delta v_i)/2$. The two current sources, $i_{i,1}$ and $i_{i,2}$, model locally connected loads or the charging/discharging currents from an up-stream converter that is regulating the dc-link voltage v_i. The input current imbalance, $\Delta i_i = i_{i,1} - i_{i,2}$,

represents a disturbance to the system that impacts Δv_i. The analyzed 3L-2P buck converter impacts the dc-link voltages via the controlled current sources that are determined by the inductor currents and the respective duty cycles: $i_1 = d_1 i_{L,1}$, $i_2 = d_2 i_{L,2}$, $i_3 = d_3 i_{L,3}$, and $i_4 = d_4 i_{L,4}$. The input side nonlinear dynamic equation is

$$C\frac{d\Delta v_i}{dt} = (i_1 + i_2) - (i_3 + i_4) - \Delta i_i = d_1 i_{L,1} + d_2 i_{L,2} - d_3 i_{L,3} - d_4 i_{L,4} - \Delta i_i. \quad (2)$$

It is clear that, depending on phase currents, the 3L-2P converter can actively balance the dc-link voltage by appropriately modifying the duty cycles. The goal is to allow that without disturbing the current regulation.

B. Output Side Dynamics

The output side of the 3L-2P interleaved structure is effectively analyzed using the T-network representation of the coupled inductors and the common mode and the differential mode voltages produced by the top and bottom modules from Fig. 1(b) [18]

$$v_{12}^{\text{cm}} = \frac{d_1 + d_2}{2} v_{i,1} \quad v_{12}^{\text{dm}} = \frac{d_1 - d_2}{2} v_{i,1}$$
$$v_{34}^{\text{cm}} = \frac{d_3 + d_4}{2} v_{i,2} \quad v_{34}^{\text{dm}} = \frac{d_3 - d_4}{2} v_{i,2}. \quad (3)$$

The phase currents feature contributions from the common mode and the differential mode voltages. The first ones determine the portion that is shared amongst the phases and the second ones determine the circulating currents $\Delta i_{L,12}$ and $\Delta i_{L,34}$. In case of a perfectly symmetric converter circuit, such as the one shown in Fig. 3, it is enough to set $d_1 = d_2$ and $d_3 = d_4$ to prevent the circulating currents. However, in practice, the control system must drive the values of v_{12}^{dm} and v_{34}^{dm} to counteract the circuit asymmetries and actively suppress them.

From the Kirchhoff's first law, it always holds that $i_{L,1} + i_{L,2} = i_{L,3} + i_{L,4} = i_o$, meaning that only three of the inductor currents are independent state variables. The output side nonlinear dynamics, where only $i_{L,1}$ is fully expanded to condense the presentation, are given by

$$\frac{di_{L,1}}{dt} = \frac{1}{2L_\sigma}(v_{12}^{\text{cm}} + v_{34}^{\text{cm}} - v_o) + \frac{1}{2M + L_\sigma} v_{12}^{\text{dm}} = d_1 \frac{1}{2}\left(\frac{1}{2L_\sigma} + \frac{1}{2M + L_\sigma}\right) v_{i,1} + d_2 \frac{1}{2}\left(\frac{1}{2L_\sigma} - \frac{1}{2M + L_\sigma}\right) v_{i,1} + d_3 \frac{1}{4L_\sigma} v_{i,2} + d_4 \frac{1}{4L_\sigma} v_{i,2} - v_o \frac{1}{2L_\sigma}$$
$$\frac{di_{L,2}}{dt} = \frac{1}{2L_\sigma}(v_{12}^{\text{cm}} + v_{34}^{\text{cm}} - v_o) - \frac{1}{2M + L_\sigma} v_{12}^{\text{dm}}$$
$$\frac{di_{L,3}}{dt} = \frac{1}{2L_\sigma}(v_{12}^{\text{cm}} + v_{34}^{\text{cm}} - v_o) + \frac{1}{2M + L_\sigma} v_{34}^{\text{dm}}$$
$$i_{L,4} = i_{L,1} + i_{L,2} - i_{L,3}. \quad (4)$$

C. Linearization

Equations (2)–(4) describe a nonlinear dynamic system, with the state vector chosen as $[x]^T = [\Delta v_i \;\; i_{L,1} \;\; i_{L,2} \;\; i_{L,3}]$, the input vector $[u]^T = [d_1 \;\; d_2 \;\; d_3 \;\; d_4]$, and the disturbance vector $[\delta]^T = [\Delta i_i \;\; v_o]$, where T is the transpose operator.

For the purpose of the following small-signal analysis and controller design, the linearization is performed by adding perturbations to all the variables

$$[x] = [\tilde{x}] + [X]$$
$$[u] = [\tilde{u}] + [U]$$
$$[\delta] = [\tilde{\delta}] + [\Delta] \quad (5)$$

where the quiescent point input vector is chosen as $[U]^T = [D \;\; D \;\; D \;\; D]$, corresponding to the symmetric operation, for which, the steady-state solution of the output voltage is $V_o = DV_i$. The quiescent point state vector is $[X]^T = [\Delta V_i \;\; I_{L,1} \;\; I_{L,2} \;\; I_{L,3}]$. For the quiescent dc-link voltages, it holds that $V_{i,1} = \frac{1}{2}(V_i - \Delta V_i)$ and $V_{i,2} = \frac{1}{2}(V_i + \Delta V_i)$, where $V_i = v_i$ is the quiescent (assumed fixed) dc-link voltage. Further, as the input voltage is assumed to be fixed, $\tilde{v}_{i,2} = -\tilde{v}_{i,1} = \frac{1}{2}\Delta\tilde{v}_i$ holds. The quiescent circulating currents are labeled as $\Delta I_{L,12} = I_{L,1} - I_{L,2}$ and $\Delta I_{L,34} = I_{L,3} - I_{L,4}$. The quiescent point disturbance vector is chosen as $[\Delta]^T = [0 \;\; V_o]$. Note that it still holds that $\tilde{i}_{L,1} + \tilde{i}_{L,2} = \tilde{i}_{L,3} + \tilde{i}_{L,4} = \tilde{i}_o$ and $I_{L,1} + I_{L,2} = I_{L,3} + I_{L,4} = I_o$.

After neglecting the higher-order terms, the voltage imbalance small-signal dynamics is given by

$$\frac{d\Delta\tilde{v}_i}{dt} = \frac{1}{C}\left(\tilde{d}_1 I_{L,1} + \tilde{d}_2 I_{L,2} - \tilde{d}_3 I_{L,3} - \tilde{d}_4 I_{L,4} - \Delta\tilde{i}_i\right). \quad (6)$$

The linearized dynamics of the inductor currents is shown only for $i_{L,1}$ to keep the presentation concise

$$\frac{d\tilde{i}_{L,1}}{dt} = \tilde{d}_1 \frac{1}{2} V_{i,1}\left(\frac{1}{2L_\sigma} + \frac{1}{2M + L_\sigma}\right) + \tilde{d}_2 \frac{1}{2} V_{i,1}\left(\frac{1}{2L_\sigma} - \frac{1}{2M + L_\sigma}\right) + \tilde{d}_3 \frac{1}{4} V_{i,2} \frac{1}{L_\sigma} + \tilde{d}_4 \frac{1}{4} V_{i,2} \frac{1}{L_\sigma} - \tilde{v}_o \frac{1}{2L_\sigma}. \quad (7)$$

The remaining inductor currents can be obtained from (4) and (5), which results in the same form as (7) with changed signs and positions of $V_{i,1}$ and $V_{i,2}$.

Finally, the linearized and averaged dynamics of the system can be represented using the state-space form

$$\frac{d}{dt}\underset{4\times1}{[\tilde{x}]} = \underset{4\times4}{[B]} \cdot \underset{4\times1}{[\tilde{u}]} + \underset{4\times2}{[F]} \cdot \underset{2\times1}{[\tilde{\delta}]}. \quad (8)$$

The disturbance matrix $[F] = [[F_1] \;\; [F_2]]$ features columns equal to $[F_1]^T = -\frac{1}{C}[1 \;\; 0 \;\; 0 \;\; 0]$ and $[F_2]^T = -\frac{1}{2L_\sigma}[0 \;\; 1 \;\; 1 \;\; 1]$. Note that the state matrix $[A]$ is zero, which results from resistances not being included in the model and all quiescent duty cycles set to be equal. The matrix $[B]$, which is not expanded to keep the paper's compactness, is a dense matrix featuring

all nonzero elements, meaning that the system is fully coupled via the control input vector $[\tilde{u}]$. This prevents a straightforward implementation of decoupled closed-loop control.

Focusing on the previously defined objectives, i.e. control of the output current, suppression of the circulating currents, and balancing of the dc-link voltages, the state vector $[\tilde{x}]$ is modified to form $[\tilde{x}_m]$ as

$$[\tilde{x}_m]^T = [\Delta\tilde{v}_i \;\; \tilde{i}_o \;\; \Delta\tilde{i}_{L,12} \;\; \Delta\tilde{i}_{L,34}] =$$
$$[\tilde{x}(1) \;\; \tilde{x}(2)+\tilde{x}(3) \;\; \tilde{x}(2)-\tilde{x}(3) \;\; 2\tilde{x}(4)-\tilde{x}(2)-\tilde{x}(3)] \quad (9)$$

where $\tilde{x}(k)$ represents the k^{th} element of the vector $[\tilde{x}]$. To obtain the corresponding modified system matrices, the same linear transformation is applied to rows of $[B]$ and $[F]$ from (8), yielding

$$\underset{4\times1}{\frac{d}{dt}[\tilde{x}_m]} = \underset{4\times4}{[B_{m,1}]} \cdot \underset{4\times1}{[\tilde{u}]} + \underset{4\times2}{[F_m]} \cdot \underset{2\times1}{[\tilde{\delta}]}$$

$$[B_{m,1}] =$$
$$\begin{bmatrix} \frac{1}{C}I_{L,1} & \frac{1}{C}I_{L,2} & -\frac{1}{C}I_{L,3} & -\frac{1}{C}I_{L,4} \\ \frac{1}{2L_\sigma}V_{i,1} & \frac{1}{2L_\sigma}V_{i,1} & \frac{1}{2L_\sigma}V_{i,2} & \frac{1}{2L_\sigma}V_{i,2} \\ \frac{1}{2M+L_\sigma}V_{i,1} & -\frac{1}{2M+L_\sigma}V_{i,1} & 0 & 0 \\ 0 & 0 & \frac{1}{2M+L_\sigma}V_{i,2} & -\frac{1}{2M+L_\sigma}V_{i,2} \end{bmatrix}$$

$$[F_m]^T = \begin{bmatrix} -\frac{1}{C} & 0 & 0 & 0 \\ 0 & -\frac{1}{L_\sigma} & 0 & 0 \end{bmatrix}. \quad (10)$$

It can be seen that, while some sparsity is obtained, the system is still coupled as $[B_{m,1}]$ is not diagonal.

D. Control Input Transformation and Decoupled Dynamics

To diagonalize the system, the following properties are observed from $[B_{m,1}]$ in (10). It can be seen that the circulating currents are driven only by the scaled duty cycle differences of the respective module (top or bottom). The output current and the voltage imbalance are, on the other hand, determined by a weighted sum of all cells' duty cycles. Specifically, for a quiescent point representing the nominal balanced state ($V_{i,1} = V_{i,2} = V_i/2$ and $I_{L,1} = I_{L,2} = I_{L,3} = I_{L,4} = I_o/2$), it is clear that $\Delta\tilde{v}_i$ is driven by a scaled difference of sums of the top and bottom modules' duty cycles $(\tilde{d}_1+\tilde{d}_2)-(\tilde{d}_3+\tilde{d}_4)$ and that $\tilde{i}_o$ is driven by a scaled sum of all four duty cycles. These properties navigate toward utilizing suitable linear combinations of duty cycles to form common mode and differential mode control inputs. Similar reasoning can be found in papers discussing input-series output-parallel modular structures [29]. Motivated by the considerations above, the new control input vector is chosen as

$$\tilde{D}_{tb}^{\text{dm}} = \frac{1}{2}\left(\frac{\tilde{d}_1+\tilde{d}_2}{2} - \frac{\tilde{d}_3+\tilde{d}_4}{2}\right)$$
$$\tilde{D}_{tb}^{\text{cm}} = \frac{1}{2}\left(\frac{\tilde{d}_1+\tilde{d}_2}{2} + \frac{\tilde{d}_3+\tilde{d}_4}{2}\right)$$
$$\tilde{d}_{12}^{\text{dm}} = \frac{1}{2}\left(\tilde{d}_1-\tilde{d}_2\right)$$

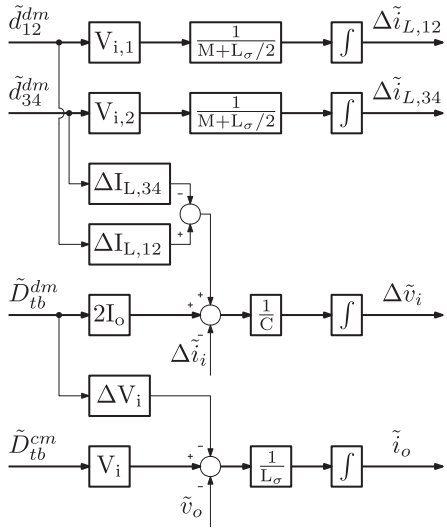

Fig. 4. Block diagram of the resulting small-signal 3L-2P buck dynamics. The only remaining coupling is present for nonzero quiescent input voltage imbalance ΔV_i and circulating currents $\Delta I_{L,12}$ and $\Delta I_{L,34}$.

$$\tilde{d}_{34}^{\text{dm}} = \frac{1}{2}\left(\tilde{d}_3-\tilde{d}_4\right)$$
$$[\tilde{u}_m] = [R]\cdot[\tilde{u}] = [\tilde{D}_{tb}^{\text{dm}} \;\; \tilde{D}_{tb}^{\text{cm}} \;\; \tilde{d}_{12}^{\text{dm}} \;\; \tilde{d}_{34}^{\text{dm}}]^T. \quad (11)$$

The matrix $[R]$ maps the linear transformation applied to the duty cycles in (11). The disturbance matrix $[F_m]$ remains the same, while the final matrix $[B_m]$ is simply obtained using the inverse transformation from (11), i.e., $[B_m] = [B_{m,1}]\cdot[R]^{-1}$.

The resulting small-signal state-space model is equal to

$$\underset{4\times1}{\frac{d}{dt}[\tilde{x}_m]} = \underset{4\times4}{[B_m]} \cdot \underset{4\times1}{[\tilde{u}_m]} + \underset{4\times2}{[F_m]} \cdot \underset{2\times1}{[\tilde{\delta}]}$$

$$[B_m] =$$
$$\begin{bmatrix} \frac{1}{C}2I_o & 0 & \frac{1}{C}\Delta I_{L,12} & -\frac{1}{C}\Delta I_{L,34} \\ -\frac{1}{L_\sigma}\Delta V_i & \frac{1}{L_\sigma}V_i & 0 & 0 \\ 0 & 0 & \frac{1}{M+L_\sigma/2}V_{i,1} & 0 \\ 0 & 0 & 0 & \frac{1}{M+L_\sigma/2}V_{i,2} \end{bmatrix}. \quad (12)$$

The block diagram corresponding to (12) is shown in Fig. 4. Some coupling still exists, determined by the quiescent values of ΔV_i, $\Delta I_{L,12}$, and $\Delta I_{L,34}$. With a control system that enables effective active voltage balancing and circulating currents suppression, these values can be assumed small. For zero quiescent dc-link voltage imbalance and circulating currents, the small-signal system is fully decoupled. From (12) and Fig. 4, the impact of the coupled inductors is seen as the output current dynamics is determined by the leakage inductance only, while the circulating currents are dominantly affected by the mutual inductance.

After the performed system decoupling, it is possible to control each modified state via a specific linear combination of duty cycles from (11), while keeping the others constant. To impact the dc-link imbalance, the control system should only modify $\tilde{D}_{tb}^{\text{dm}}$. For the output current, only $\tilde{D}_{tb}^{\text{cm}}$ should be affected.

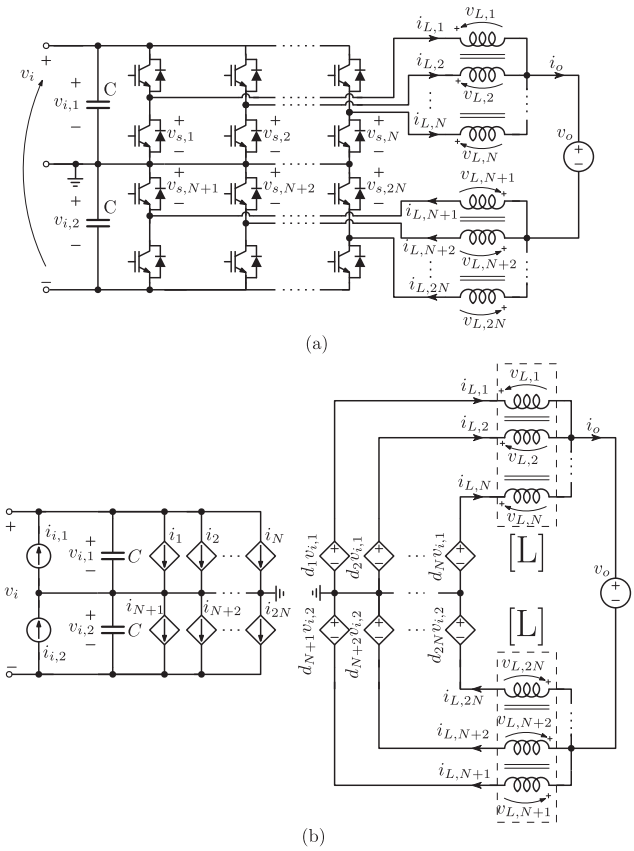

Fig. 5. (a) The three-level N-phase converter with coupled inductors. (b) The input and the output large-signal average circuits representation.

For the top and bottom circulating currents, the control system should only modify $\tilde{d}_{12}^{\text{dm}}$ and $\tilde{d}_{34}^{\text{dm}}$, respectively. To implement such a decoupled control algorithm, the inverse transformation from $[\tilde{u}_m]$ to $[\tilde{u}]$, $[R]^{-1}$, is calculated as

$$\begin{aligned}\tilde{d}_1 &= \tilde{D}_{tb}^{\text{cm}} + \tilde{D}_{tb}^{\text{dm}} + \tilde{d}_{12}^{\text{dm}}\\ \tilde{d}_2 &= \tilde{D}_{tb}^{\text{cm}} + \tilde{D}_{tb}^{\text{dm}} - \tilde{d}_{12}^{\text{dm}}\\ \tilde{d}_3 &= \tilde{D}_{tb}^{\text{cm}} - \tilde{D}_{tb}^{\text{dm}} + \tilde{d}_{34}^{\text{dm}}\\ \tilde{d}_4 &= \tilde{D}_{tb}^{\text{cm}} - \tilde{D}_{tb}^{\text{dm}} - \tilde{d}_{34}^{\text{dm}}.\end{aligned} \tag{13}$$

IV. Extension to the Three-Level N-Phase Converters

For increasing the power rating, more than two interleaved three-level phases can be employed [18]. The converter operation remains analogous to that described in Section II; the modulation still relies on PS-PWM, now with $2N$ switching signals, and the nominal operation requires balanced dc-link voltages and equal current sharing among the phases. This section generalizes the proposed decoupled modeling and control to the three-level N-phase interleaved converter with coupled inductors, illustrated in Fig. 5(a).

The average circuits representing the input and output side dynamics are shown in Fig. 5(b). The input voltage is again assumed to be fixed. The large-signal state vector is $[x]^T = [\Delta v_i \;\; i_{L,1} \;\; \dots \;\; i_{L,2N-1}]$, the large-signal input vector is $[u]^T = [d_1 \;\; d_2 \;\; \dots \;\; d_{2N}]$, and the large-signal disturbance vector is $[\delta]^T = [\Delta i_i \;\; v_o]$. In the same way as before, the model is linearized by introducing perturbations $[x] = [\tilde{x}] + [X]$, $[u] = [\tilde{u}] + [U]$, and $[\delta] = [\tilde{\delta}] + [\Delta]$ around the quiescent operating point determined by $[X]^T = [\Delta V_i \;\; I_{L,1} \;\; \dots \;\; I_{L,2N-1}]$, $[U]^T = [D \;\; D \;\; \dots \;\; D]^T$, $[\Delta] = [0 \;\; V_o = Dv_i]$.

From the imposed linearization, the small-signal input side dynamics is obtained as

$$\begin{aligned}\frac{d\Delta\tilde{v}_i}{dt} = \frac{1}{C}(&\tilde{d}_1 I_{L,1} + \dots + \tilde{d}_N I_{L,N} -\\ &\tilde{d}_{N+1} I_{L,N+1} - \dots - \tilde{d}_{2N} I_{L,2N} - \Delta\tilde{i}_i).\end{aligned} \tag{14}$$

For the output side, the two coupled inductors are described with the inductance matrix obtained using the same convention as for the 3L-2P case [27]

$$\underset{N\times N}{[L]} = \begin{bmatrix} L & -M & \dots & -M \\ -M & L & \dots & -M \\ \dots & \dots & \dots & \dots \\ -M & -M & \dots & L \end{bmatrix} \tag{15}$$

where $L = L_\sigma + (N-1)M$.

Solving the circuit from Fig. 5(b), under the imposed linearization and the quiescent point, the coupled inductor voltages can be expressed as

$$\underset{2N\times 1}{[\tilde{v}_L]} = \underset{2N\times 2N}{[V]} \cdot \underset{2N\times 1}{[\tilde{u}]} - \frac{1}{2}\underset{2N\times 1}{[1]} \cdot \tilde{v}_o \tag{16}$$

where [1] is the unity column vector and the matrix $[V]$ is found as

$$\underset{2N\times 2N}{[V]} = \begin{bmatrix} \underset{2N\times N}{[V_1]} & \underset{2N\times N}{[V_2]} \end{bmatrix}$$

$$[V_1] = \frac{V_{i,1}}{2N}\begin{bmatrix} 2N-1 & -1 & \dots & -1 \\ \dots & \dots & \dots & \dots \\ -1 & -1 & \dots & 2N-1 \\ 1 & 1 & \dots & 1 \\ \dots & \dots & \dots & \dots \\ 1 & 1 & \dots & 1 \end{bmatrix}$$

$$[V_2] = \frac{V_{i,2}}{2N}\begin{bmatrix} 1 & 1 & \dots & 1 \\ \dots & \dots & \dots & \dots \\ 1 & 1 & \dots & 1 \\ 2N-1 & -1 & \dots & -1 \\ \dots & \dots & \dots & \dots \\ -1 & -1 & \dots & 2N-1 \end{bmatrix}. \tag{17}$$

The small-signal phase current vector $[\tilde{i}_L]^T = [\tilde{i}_{L,1} \;\; \dots \;\; \tilde{i}_{L,2N}]$ is then found as

$$\frac{d}{dt}\underset{2N\times 1}{[\tilde{i}_L]} = \begin{bmatrix} [L]^{-1} & [0] \\ [0] & [L]^{-1} \end{bmatrix} \cdot \underset{2N\times 1}{[\tilde{v}_L]} \tag{18}$$

where [0] is the square zero matrix of order N.

Equations (14)–(18) describe the complete small-signal dynamics, and can be used to form the state-space model in the

same form as for the 3L-2P interleaved case in (8)

$$\frac{d}{dt}\underset{2N\times 1}{[\tilde{x}]} = \underset{2N\times 2N}{[B]} \cdot \underset{2N\times 1}{[\tilde{u}]} + \underset{2N\times 2}{[F]} \cdot \underset{2\times 1}{[\tilde{\delta}]}. \tag{19}$$

The matrices are not expanded, for paper's conciseness.

The next step is to introduce a suitable state vector transformation based on the targeted control objectives. Following the approach taken for the 3L-2P case, the modified state vector is selected as

$$\underset{2N\times 1}{[\tilde{x}_m]} = [\Delta\tilde{v}_i \;\; \tilde{i}_o \;\; \Delta\tilde{i}_{L,1} \;\; \ldots \;\; \Delta\tilde{i}_{L,N-1} \;\; \Delta\tilde{i}_{L,N+1} \;\; \ldots \;\; \Delta\tilde{i}_{L,2N-1}]^T, \tag{20}$$

where the output current is $\tilde{i}_o = \sum_{k=1}^{N} \tilde{i}_{L,k} = \sum_{k=1}^{N} \tilde{x}(k+1)$ and $2N-2$ circulating currents are defined as $\Delta\tilde{i}_{L,k} = N\tilde{i}_{L,k} - \tilde{i}_o = N\tilde{x}(k+1) - \sum_{k=1}^{N} \tilde{x}(k+1)$. Note that the labeling is slightly changed compared to the 3L-2P case such that, when used for $N=2$, $\Delta\tilde{i}_{L,1}$ corresponds to the previously used $\Delta\tilde{i}_{L,12}$, and same for the rest. This linear transformation corresponds to row manipulations of matrices $[B]$ and $[F]$ from (19), which forms the matrices $[B_{m,1}]$ and $[F_m]$, in the same way as in (10) for the 3L-2P case. The resulting matrices are not expanded here.

Finally, the control input vector is transformed in a way suitable for the control objectives. As a generalization of (11), the following transformation is proposed:

$$\underset{2N\times 1}{[\tilde{u}_m]} = \underset{2N\times 2N}{[R]} \cdot \underset{2N\times 1}{[\tilde{u}]} = [\tilde{D}_{tb}^{\text{dm}} \;\; \tilde{D}_{tb}^{\text{cm}} \;\; \tilde{d}_1^{\text{dm}} \;\; \ldots \;\; \tilde{d}_{N-1}^{\text{dm}} \;\; \tilde{d}_{N+1}^{\text{dm}} \;\; \ldots \;\; \tilde{d}_{2N-1}^{\text{dm}}]^T \tag{21}$$

in which $\tilde{D}_{tb}^{\text{dm}}$ represents the differential mode of the top and bottom modules' common mode (average) duty cycle values, $\tilde{D}_{tb}^{\text{cm}}$ represents the common mode value of all cells' duty cycles, and $\tilde{d}_k^{\text{dm}}$ represents the difference between the k^{th} cell's duty cycle and the common mode value of the duty cycles of the respective module (top or bottom). Comparing to the previous notation used for the 3L-2P case, the labeling is slightly changed such that, when used for $N=2$, $\tilde{d}_1^{\text{dm}}$ corresponds to previously used $\tilde{d}_{12}^{\text{dm}}$, and same for the rest. As an example, for $N=3$, the modified control inputs are $\tilde{D}_{tb}^{\text{dm}} = (\tilde{d}_1 + \tilde{d}_2 + \tilde{d}_3 - \tilde{d}_4 - \tilde{d}_5 - \tilde{d}_6)/6$, $\tilde{D}_{tb}^{\text{cm}} = (\tilde{d}_1 + \tilde{d}_2 + \tilde{d}_3 + \tilde{d}_4 + \tilde{d}_5 + \tilde{d}_6)/6$, $\tilde{d}_1^{\text{dm}} = \tilde{d}_1 - (\tilde{d}_1 + \tilde{d}_2 + \tilde{d}_3)/3$, $\tilde{d}_2^{\text{dm}} = \tilde{d}_2 - (\tilde{d}_1 + \tilde{d}_2 + \tilde{d}_3)/3$, $\tilde{d}_4^{\text{dm}} = \tilde{d}_4 - (\tilde{d}_4 + \tilde{d}_5 + \tilde{d}_6)/3$, $\tilde{d}_5^{\text{dm}} = \tilde{d}_5 - (\tilde{d}_4 + \tilde{d}_5 + \tilde{d}_6)/3$. The matrix $[R]$ can be represented in a general form as

$$\underset{2N\times 2N}{[R]} = [\underset{2N\times N}{[R_1]} \;\; \underset{2N\times N}{[R_2]}]$$

$$[R_1] = \frac{1}{N}\begin{bmatrix} 0.5 & 0.5 & \ldots & 0.5 & 0.5 \\ 0.5 & 0.5 & \ldots & 0.5 & 0.5 \\ N-1 & -1 & \ldots & -1 & -1 \\ \ldots & \ldots & \ldots & \ldots & \ldots \\ -1 & -1 & \ldots & N-1 & -1 \\ 0 & 0 & \ldots & 0 & 0 \\ \ldots & \ldots & \ldots & \ldots & \ldots \\ 0 & 0 & \ldots & 0 & 0 \end{bmatrix}$$

$$[R_2] = \frac{1}{N}\begin{bmatrix} -0.5 & -0.5 & \ldots & -0.5 & -0.5 \\ 0.5 & 0.5 & \ldots & 0.5 & 0.5 \\ 0 & 0 & \ldots & 0 & 0 \\ \ldots & \ldots & \ldots & \ldots & \ldots \\ 0 & 0 & \ldots & 0 & 0 \\ N-1 & -1 & \ldots & -1 & -1 \\ \ldots & \ldots & \ldots & \ldots & \ldots \\ -1 & -1 & \ldots & N-1 & -1 \end{bmatrix}. \tag{22}$$

The final MIMO model, shown in (23), is obtained using $[B_m] = [B_{m,1}] \cdot [R]^{-1}$.

$$\frac{d}{dt}\underset{2N\times 1}{[\tilde{x}_m]} = \underset{2N\times 2N}{[B_m]} \cdot \underset{2N\times 1}{[\tilde{u}_m]} + \underset{2N\times 2}{[F_m]} \cdot \underset{2\times 1}{[\tilde{\delta}]}. \tag{23}$$

The matrices $[B_m]$ and $[F_m]$ are expanded and shown at the bottom of this page. It can be seen that the system form is analogous to the one in (12). The matrix $[B_m]$ is completely diagonalized in case of zero quiescent values of the voltage imbalance and circulating currents. For nonzero values, coupling remains from the voltage balancer to the output current, as well as from the circulating CCs to the voltage balancer, in a form similar to Fig. 4. The proposed transformations are suitable for

$$[B_m] = \begin{bmatrix} \frac{2I_o}{C} & 0 & \frac{I_{L,1}-I_{L,N}}{C} & \ldots & \frac{I_{L,N-1}-I_{L,N}}{C} & -\frac{I_{L,N+1}-I_{L,2N}}{C} & \ldots & -\frac{I_{L,2N-1}-I_{L,2N}}{C} \\ -\frac{\Delta V_i}{2L_\sigma/N} & \frac{V_i}{2L_\sigma/N} & 0 & \ldots & 0 & 0 & \ldots & 0 \\ 0 & 0 & \frac{V_{i,1}}{M+L_\sigma/N} & \ldots & 0 & 0 & \ldots & 0 \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\ 0 & 0 & 0 & \ldots & \frac{V_{i,1}}{M+L_\sigma/N} & 0 & \ldots & 0 \\ 0 & 0 & 0 & \ldots & 0 & \frac{V_{i,2}}{M+L_\sigma/N} & \ldots & 0 \\ \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\ 0 & 0 & 0 & \ldots & 0 & 0 & \ldots & \frac{V_{i,2}}{M+L_\sigma/N} \end{bmatrix}$$

$$[F_m] = \begin{bmatrix} -\frac{1}{C} & 0 & 0 & \ldots & 0 & 0 & \ldots & 0 \\ 0 & -\frac{1}{2L_\sigma/N} & 0 & \ldots & 0 & 0 & \ldots & 0 \end{bmatrix}^T.$$

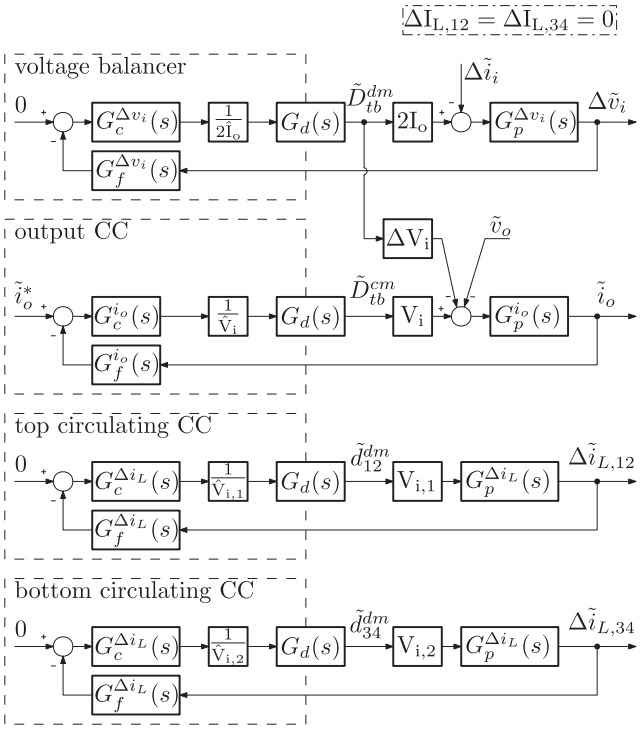

Fig. 6. S-domain block diagrams of the four closed-loop systems used to control the 3L-2P buck converter, based on modified control inputs and state variables shown in Fig. 4. Zero quiescent values of the circulating currents are assumed.

decoupled control of the output current, input voltage balancing, and circulating currents suppression of the three-level N-phase interleaved converter with coupled inductors. As a generalization of (13), the duty cycles of the $2N$ switching cells are obtained using the inverse transformation $[\tilde{u}] = [R]^{-1} \cdot [\tilde{u}_m]$.

Besides the structure shown in Fig. 5, different types of integrated coupled inductors can be considered [18], [19], which is left for future studies.

V. Control System Design

For all subsequent analyses and results, the 3L-2P buck converter from Fig. 1(b) is considered. The system parameters correspond to the experimentally tested hardware, with the main values summarized in Table I.

A. Closed-Loop S-Domain Representation

The s-domain representations of the proposed closed-loop systems are shown in Fig. 6, where the dashed lines highlight the digital control parts. All four control loops feature a compensator $G_c(s)$, a block $G_d(s)$ that models digital control delays, a plant transfer function $G_p(s)$, and a feedback filter $G_f(s)$. The quiescent point values are tracked via measurements to normalize the loop gains and, assuming their ideal estimation (e.g., $\hat{V}_i = V_i$), they do not impact the system dynamics. The s-domain plant

TABLE I
3L-2P Buck Converter Parameters

Description	label	value	unit
Nominal power	P_n	1	MW
Nominal input voltage	$v_{i,n}$	850	V
Mutual inductance	M	900	uH
Leakage inductance	L_σ	65	uH
Input capacitance	C	12	mF
Switching frequency	f_{pwm}	3	kHz
Control execution rate	$f_c = 4f_{\text{pwm}}$	12	kHz
Current sampling rate	$f_s = 100 f_{\text{pwm}}$	300	kHz

transfer functions are equal to

$$G_p^{\Delta v_i}(s) = \frac{\Delta \tilde{v}_i(s)}{\tilde{D}_{tb}^{\text{dm}}(s) 2I_o} = \frac{1}{sC}$$

$$G_p^{i_o}(s) = \frac{\tilde{i}_o(s)}{\tilde{D}_{tb}^{\text{cm}}(s) V_i} = \frac{1}{sL_\sigma}$$

$$G_p^{\Delta i_L}(s) = \frac{\Delta \tilde{i}_{L,12}(s)}{\tilde{d}_{12}^{\text{dm}}(s) V_{i,1}} = \frac{\Delta \tilde{i}_{L,34}(s)}{\tilde{d}_{34}^{\text{dm}}(s) V_{i,2}} = \frac{1}{s\,(M + L_\sigma/2)}. \tag{24}$$

Voltage balancing of large dc-link capacitors is targeted to operate on significantly longer time-scales than the CCs. This time-scale separation implies that circulating CCs can compensate any disturbances much faster than dynamics of the voltage balancing [30]. This allows assuming that $\Delta I_{L,12} = \Delta I_{L,34} = 0$, thus neglecting the coupling from the circulating CCs to the voltage balancer, as shown in Fig. 6. The voltage balancing loop features a disturbance coming from the input load imbalance, $\Delta \tilde{i}_i$. It is important to note that the active voltage balancing relies on the average output current. Hence, below a certain threshold of $\mathrm{I_o}$, the proposed control loop becomes ineffective and the balancing strategy must be changed, e.g., using an up-stream converter as in [22], [26].

The output current loop features two disturbances. The first one comes from the output voltage $\tilde{v}_o$. The second one comes from the voltage balancing control action, $\tilde{D}_{tb}^{\text{dm}}$, which is scaled by the quiescent imbalance value ΔV_i. Due to a relatively low value of L_σ, under large input side disturbances it may happen that the voltage balancer causes a non-negligible output current transient. For this reason, and given that the value of $\tilde{D}_{tb}^{\text{dm}}$ is readily available in the digital control system, the balancer-to-output-current disturbance suppression using an additional feedforward action is subsequently examined.

The two circulating currents are fully decoupled from the rest of the system.

B. Modulation, Sampling, and Filtering

A high-level block diagram of the proposed control system is shown in Fig. 7(a). In the figure, the output of the voltage balancer is also passed to the output CC, which illustrates

the possibility of using the additional feedforward term that suppresses the disturbance of the voltage balancing action on the output current. This feedforward action is illustrated in Fig. 7(b).

The control system is implemented using the F28379d digital signal processor (DSP) from Texas Instruments. All 4 control loop algorithms are executed within an *interrupt standard routine* (ISR) that runs at a rate equal to $f_c = 4f_{\text{pwm}}$, and is aligned with the peaks and valleys of the PS-PWM carriers. The controllers use estimated quiescent point values and feedback signals that are transformed to establish the modified state vector from (9). All measured signals in the digital domain are labeled with "$\hat{}$", highlighting that some processing is used to obtain them from the actual physical signals. After all four controllers are executed, (13) is used to calculate the individual duty cycle commands. Those form the commanded control input vector $[u]^*$ that is used to update the modulating waveform of each PWM carrier, at the corresponding peak or valley to prevent modulation nonlinearities [32], [33]. The chosen modulation strategy, termed multi-sampled double-update (MS-DU) [31], relies on calculating the control action four times per switching period, while the modulating waveform for each carrier is still updated only twice per switching period. For applications where very fast dynamics are important, multi-sampled multi-update (MS-MU) PS-PWM can be implemented instead [31], [34]. Finally, the comparisons between the modulating waveforms and the carriers result in the switching signals $[s]$.

The corresponding timing diagram is shown in Fig. 8(a). The control ISR instants are marked with black squares, while the modulating waveform update instants are marked with circles and coloured to match with the corresponding carrier. To accommodate the algorithm execution time, an additional one T_c step delay is introduced, which is illustrated by black arrows between the control and the update instants. The small-signal model of MS-DU PS-PWM [31] is

$$G_{\text{dpwm}}(s) = \frac{1}{2}\left(e^{-s(1-D)\frac{T_{\text{pwm}}}{2}} + e^{-sD\frac{T_{\text{pwm}}}{2}}\right) \tag{25}$$

which is often approximated by a simplified delay model, $e^{-s\frac{T_{\text{pwm}}}{4}}$ [31]. The s-domain equivalent delay block from Fig. 6 can, therefore, be represented as $G_d(s) = e^{-sT_c}G_{\text{dpwm}}(s)$.

Feedback sampling is performed using an analog-to-digital converter (ADC), at two distinct rates. Voltages are sampled with the rate equal to f_c and then filtered using first order digital low-pass filters. Voltages $v_{i,1}$ and $v_{i,2}$ are used to form the feedback signal $\Delta\hat{v}_i$ and the estimated quiescent point values used for gain normalizations $\hat{\text{V}}_{\text{i}}$, $\hat{\text{V}}_{\text{i,1}}$, $\hat{\text{V}}_{\text{i,2}}$, and $\Delta\hat{\text{V}}_{\text{i}}$.

The inductor currents are oversampled with the frequency $f_s = 100f_{\text{pwm}}$, buffered, and averaged. The oversampled moving average filter (MAF) is illustrated in Fig. 8(b). In the used DSP, the oversampling is organized by configuring the *direct memory access* (DMA) module to collect batches of inductor currents samples, which are then averaged over T_{pwm}. The filtered and decimated currents samples are used to form the feedback signals $\hat{i}_o$, $\Delta\hat{i}_{L,12}$, $\Delta\hat{i}_{L,34}$, and the quiescent value $\hat{\text{I}}_{\text{o}}$, used for gain normalization of the voltage balancer.

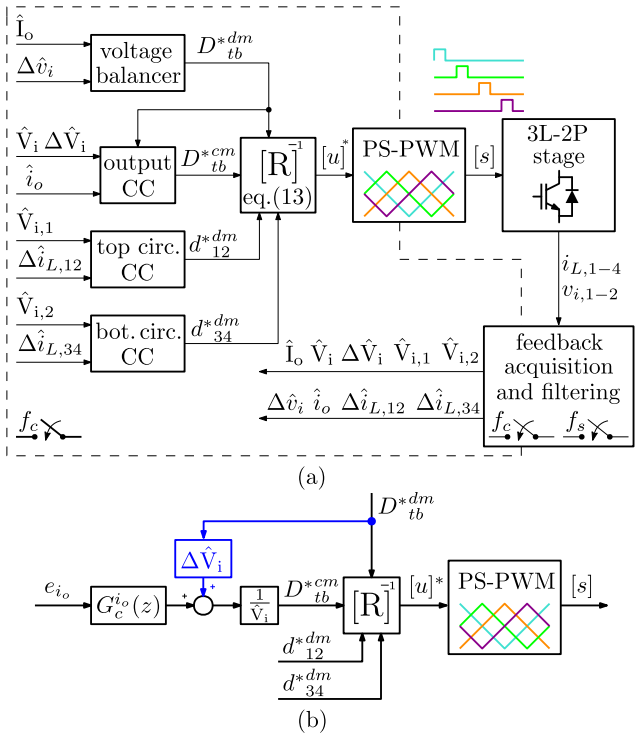

Fig. 7. (a) Block diagram illustration of the proposed control system featuring feedback acquisition and filtering, the four control loops from Fig. 6, the transformation from the commanded modified inputs $[u_m]^*$ to the commanded duty cycles $[u]^*$, and the digital PS-PWM that produces the switching signals $[s]$. (b) The feedforward action used to suppress the voltage balancing to output current disturbance from Fig. 6.

There are several reasons that motivate oversampled averaging of the 3L-2P converter's phase currents. First, the oversampling strongly suppresses feedback switching and wideband noise, significantly increasing the signal-to-noise ratio and output power quality [35], [36], [37], [38]. Second, it prevents low-frequency and high-frequency aliasing [34] that would inevitably appear if the system relied only on a few samples per switching period. Namely, the coupled inductor currents feature significant ripple harmonics, determined by all switching cells, which is why a robust sampling scheme is important. As an example of aliasing, Fig. 9 shows a simulation result of $i_{L,1}$ in a steady-state condition. The simulation is implemented in MATLAB/Simulink, using the converter parameters from Table I. The control system corresponds to the one described in this section, however, with the current sampling rate set to $f_c = 4f_{\text{pwm}}$ and aligned with peaks and valleys of the PS-PWM carriers. The input voltage is set to 850 V, the output voltage is set to 625 V, and the output current reference is set to 1000 A. The simulated circuit is ideal and symmetric. It can be seen that the sampled feedback signal features strong jump discontinuities, with an average value of samples that does not match the dc current. The aliasing comes from the loss of center-pulse sampling [28], which may also occur in current control loops of two-level converters [35]. These effects are more emphasized in the three-level interleaved buck with coupled inductors due to a more complex switching harmonic content. In practice,

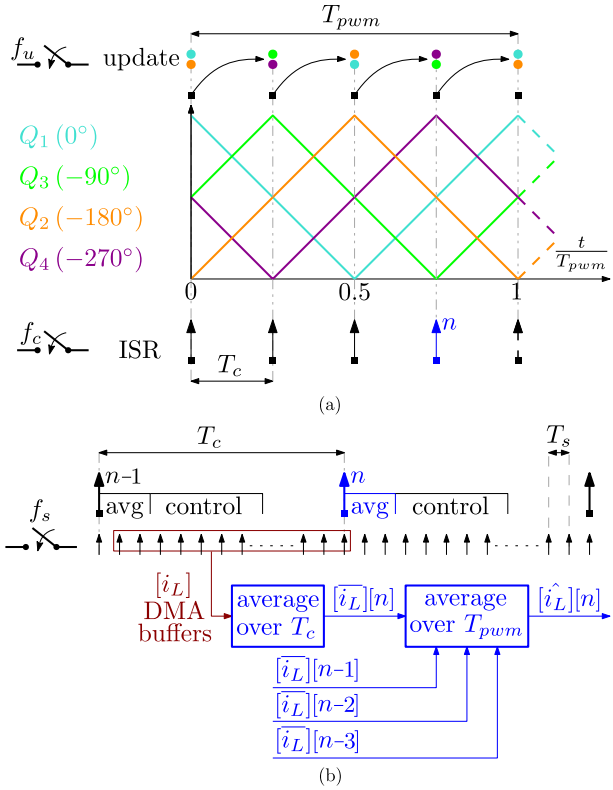

Fig. 8. Timing diagram of the proposed digital control system. (a) Synchronization between the PS-PWM carriers, the control ISR, and the modulating waveform update instants for the chosen MS-DU strategy [31]. (b) Implemented inductor currents acquisition scheme featuring oversampling with the rate f_s, buffering using the DMA, and averaging over T_{pwm}.

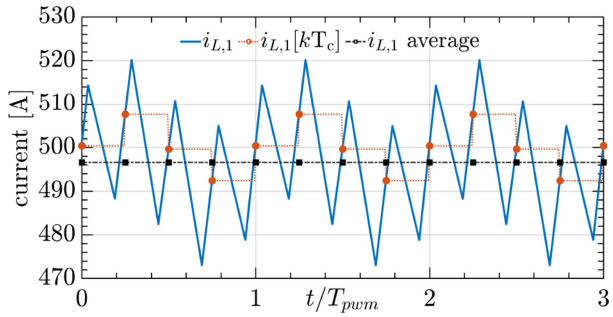

Fig. 9. Simulation result showing $i_{L,1}$ during steady-state operation of the 3L-2P buck described in Table I. The oversampled averaging is not used, yielding a DC error between the feedback samples and the inductor current.

aliasing errors are further increased due to parasitic resistances, filters, and delays in sensing and driving circuitry. Introducing the switching harmonics in the feedback signal also impacts linearity of the PS-PWM [32], [33]. This can be avoided by using only one sample per switching period, however, consequently increasing sensitivity to noise and low-frequency aliasing [34]. Although the proposed oversampling scheme is not theoretically necessary for the 3L-2P operation, lack of a robust sampling scheme would in practice yield tracking errors in the output and

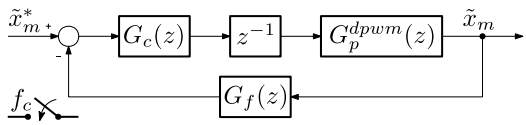

Fig. 10. Z-domain representation of the the closed-loop systems from Fig. 6, focused on reference tracking.

circulating currents, as well as output distortion in case of ac modulation [34].

C. Z-Domain Representation and Compensator Design

For more accurate closed-loop modeling, and an example compensator design, the analysis is performed in the Z-domain, with $z = e^{sT_c}$.

With respect to reference tracking, all four closed-loop systems from Fig. 6 can be represented using a small-signal block-diagram shown in Fig. 10. The one step computation delay is represented as z^{-1}. The plant transfer functions from (24) are discretized together with the MS-DU PS-PWM small-signal model (25), using the impulse-invariant approach [28]

$$G_p^{\text{dpwm}}(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}\left\{G_{\text{dpwm}}(s)G_p(s)\right\}\right\} \tag{26}$$

where $\mathcal{Z}$ and $\mathcal{L}^{-1}$ represent the Z-transform and the inverse Laplace transform, respectively. It is assumed that all controllers' outputs are ideally normalized by the estimated quiescent point values; hence, the products of the normalizations and the quiescent point gains in Fig. 6 are equal to 1. The open-loop $W_{ol}(z)$ and closed-loop $W_{cl}(z)$ transfer functions can be found as

$$\begin{aligned} W_{ol}(z) &= G_c(z)z^{-1}G_p^{\text{dpwm}}(z)G_f(z) \\ W_{cl}(z) &= \frac{G_c(z)z^{-1}G_p^{\text{dpwm}}(z)}{1+W_{ol}(z)}. \end{aligned} \tag{27}$$

For the analysis of all current control loops, to avoid using the modified Z-transform, the oversampled MAF over T_{pwm} is approximated with a FIR filter executed at f_c: $G_f^{\Delta i_L}(z) = G_f^{i_o}(z) = G_{\text{MAF}}(z) \approx (1 + 2z^{-1} + 2z^{-2} + 2z^{-3} + z^{-4})/8$. The proportional-integral (PI) compensators are used and the crossover frequencies of $W_{ol}^{\Delta i_L}(z)$ and $W_{ol}^{i_o}(z)$, $f_{bw}^{\Delta i_L}$ and $f_{bw}^{i_o}$, are set to 220 Hz with phase margins of 60°. The resulting circulating current compensators are discretized as $G_c^{\Delta i_L}(z) = k_p^{\Delta i_L} + k_i^{\Delta i_L} T_c \frac{z}{z-1}$, with $k_p^{\Delta i_L} = 1.3\ \Omega$ and $k_i^{\Delta i_L} = 178\ \Omega/s$. The output current compensator is discretized as $G_c^{i_o}(z) = k_p^{i_o} + k_i^{i_o} T_c \frac{z}{z-1}$, with $k_p^{i_o} = 0.09\ \Omega$ and $k_i^{i_o} = 12.4\ \Omega/s$.

The cut-off frequency ω_f of the first-order low-pass filter used to obtain $\Delta\hat{v}_i$ is set to 360 Hz. This filter is discretized as $G_f^{\Delta v_i}(z) = \alpha_f \frac{z}{z-(1-\alpha_f)}$, where $\alpha_f = \frac{\omega_f T_c}{\omega_f T_c + 1}$. The PI compensator is used and, for previously-mentioned time-scale separation, the voltage balancing loop crossover frequency $f_{bw}^{\Delta v_i}$ is set to 22 Hz, with the phase margin of 80°. The compensator is discretized as $G_c^{\Delta v_i}(z) = k_p^{\Delta v_i} + k_i^{\Delta v_i} T_c \frac{z}{z-1}$ with $k_p^{\Delta v_i} = 1.7$ S and $k_i^{\Delta v_i} = 22.9\ \text{S}/s$.

VI. Experimental Verifications

A. C-HIL Results

The first set of verifications is performed by emulating the power stage in the HIL platform Typhoon HIL 402, while the control is implemented in the same F28379d-based control board used in the subsequent hardware prototype validations. The control implementation corresponds to the one described in Section V. The HIL environment runs with 500 ns time step and features the 3L-2P buck from Fig. 1(b), with parameters listed in Table I. All measurement signals are sent to the physical control board using HIL analog outputs, and the switching signals are sent from the control board to the HIL digital inputs. The output of the 3L-2P buck is connected to a voltage source with $R_f = 16$ mΩ series resistance, to simply model an ESS load [3]. An output capacitor $C_f = 2$ mF is connected in parallel with the load. Such an output impedance configuration modifies the $G_p^{i_o}(s)$ in (24) by adding the parallel $R_f||C_f$ impedance in series to the leakage inductance L_σ. This output configuration boosts the phase margin of the output current control loop by approximately 10°, which is taken into account in the subsequently shown modeled responses. Note that this only impacts the output and not the circulating current control.

To verify the derived small-signal model, frequency responses of the closed-loop transfer functions from (27) are measured, for all four control systems. Measurements are performed at 9 frequencies, up to $f_{\text{pwm}}/2$, and compared with the analytical models. First, the converter is run with all four control systems enabled, at the operating point with $I_o = 1000$ A, $V_i = 850$ V, and $V_o = 625$ V. Then, for one-at-a-time control loop, the reference is perturbed by generating a signal in the HIL platform, which is then sent to the analog output and sampled by the control board to be used as a reference. The frequency response measurement block from Typhoon HIL is used to postprocess the reference and the output signals, and calculate the resulting frequency response. The output current reference is perturbed with 100 A magnitude, the circulating currents references are perturbed with 20 A magnitudes, and the voltage imbalance reference is perturbed with 20 V magnitude. From the results shown in Fig. 11, it is clear that the derived small-signal models accurately predict the measured frequency responses. As frequencies approach $f_{\text{pwm}}/2$, some modeling error is seen if the MS-DU PS-PWM is approximated by a delay $e^{-s\frac{T_{pwm}}{4}}$. An almost ideal match at all frequencies is obtained using the full MS-DU PS-PWM model from (25).

A time-domain result is shown in Fig. 12, to illustrate all controlled states during a transient imposed by a step change of the output current reference, from 500 A to 1600 A. It can be seen that the small-signal closed-loop model predicts-well the measured current step response. Moreover, even though a large transient is imposed to the output current, no other states are perturbed, verifying the decoupled nature of the designed control system.

The input current disturbance, affecting the voltage balance, is tested by imposing a 100 A pulsed difference between the input currents $\Delta i_i = i_{i,1} - i_{i,2}$ from Fig. 3(a). This is done

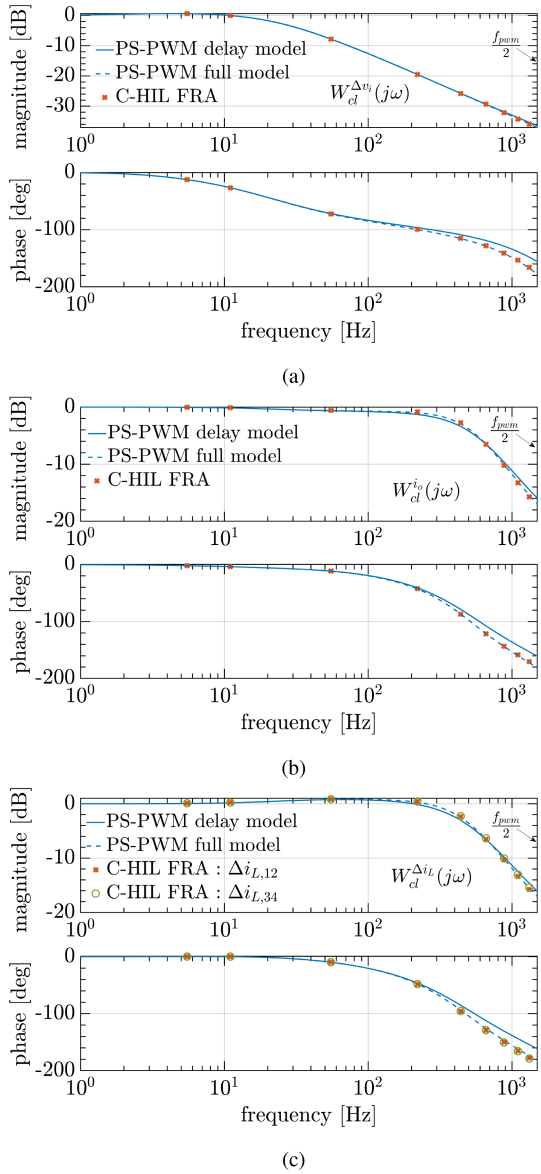

Fig. 11. C-HIL frequency response measurements of the designed closed-loop control systems and comparison with the analytical models obtained using (27) for (a) the voltage balancing loop, (b) the output current loop, and (c) the circulating current loops.

by adding a pulsed current source in parallel with the top module's input capacitor. The results are shown in Fig. 13. For clarity, all currents are plotted after post-processing to remove the switching ripple, while the output current is shown with the ripple as well. First, from Fig. 13(a), it can be seen that the disturbance caused by the unbalanced load at the input dc-link is compensated by the voltage-balancing controller, with dynamics that are well-predicted by the small-signal model (circular markers). The circulating currents are kept stiff at 0 A, confirming the decoupling between the voltage balancer and the circulating CCs. A small impact on the output current is seen, resulting from the balancer-to-output-current coupling described before. Suppression of this disturbance is tested using a feedforward action illustrated in Fig. 7(b). As seen from Fig. 13(b), the

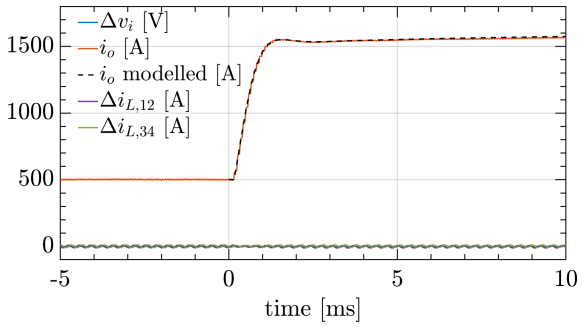

Fig. 12. C-HIL result showing a transient imposed by the output current step reference change from 500 A to 1600 A, for $v_i = 850$ V and $v_o = 625$ V. It can be seen that the states other than i_o are not affected, which verifies the decoupled nature of the proposed control system. The analytically-obtained trace of i_o is also shown (black dashed line).

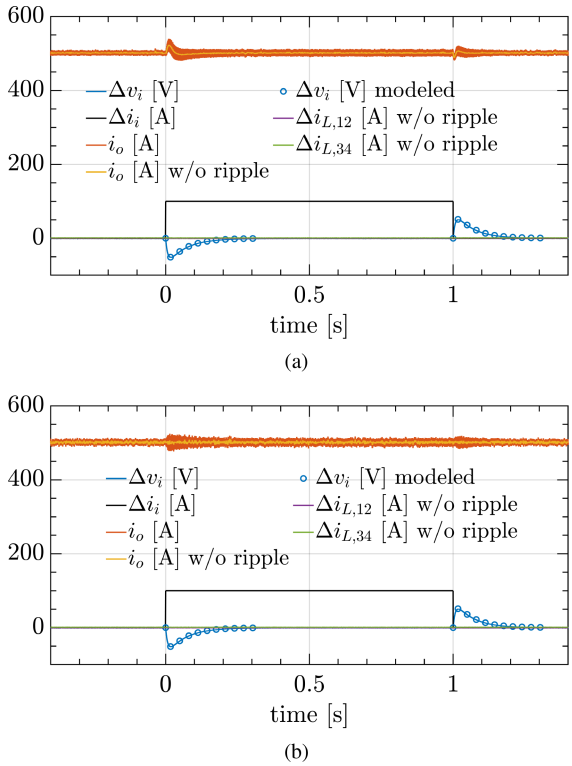

Fig. 13. C-HIL results showing transients when the top input capacitor from Fig. 1(b) is loaded with a 100 A pulsed-waveform current source: (a) without and (b) with the feedforward action from Fig. 7(b) that rejects the balancer-to-output-current coupling.

additional feedforward action is effective in removing the coupling between the voltage balancer and the output CC.

B. Results on the Hardware Prototype

For the following results, the hardware prototype of the 3L-2P buck is used. The input voltage is supplied from a 100 kW ac–dc laboratory power supply. A passive load is formed with a parallel $R_o||C_o$ branch, where $C_o = 1500$ uF and R_o is varied. The filtered output current flowing through the load resistor is labeled as i_{Ro}. Note that this configuration also changes the

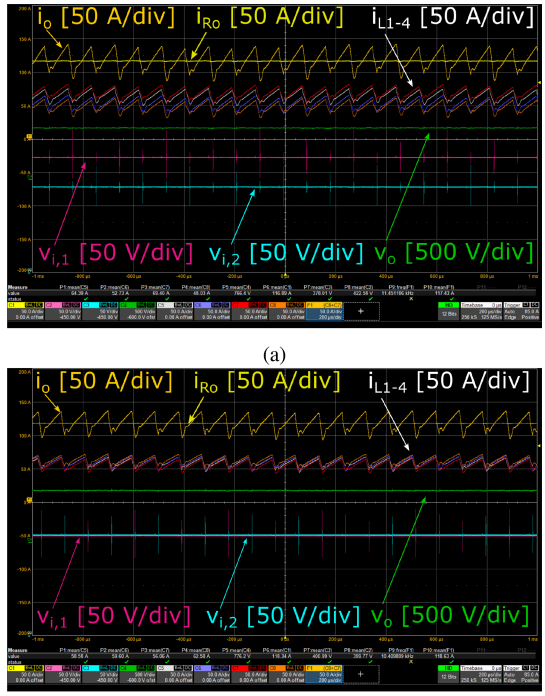

Fig. 14. Experimental results for $v_i = 800$ V, $i_o = 115$ A, $R_o = 6.6\ \Omega$, and the control system (a) without and (b) with circulating current control and input voltage balancing.

output current control plant transfer function with respect to the one from (24). The rest of the hardware and control parameters match those listed in Table I and Section V.

The first set of results in Figs. 14 and 15 shows the difference in converter's operation before and after enabling the circulating CCs and the voltage balancer. The input voltage is set to 800 V. For Fig. 14(a), the output current reference is set to 115 A with $R_o = 6.6\ \Omega$, resulting in ≈ 90 kW operation. The converter is started with only the output CC being active and, due to circuit asymmetries, significant mismatches in phase currents and input capacitors voltages appear. As seen from the oscilloscope measurements, the maximal circulating current features a dc level of ≈ 21 A, which is almost 20% of the output current. Considering the voltage imbalance, a difference of ≈ 45 V is seen. The subsequent result in Fig. 14(b) shows the same scenario with all control loops enabled. It can be seen that the maximal circulating currents are suppressed to 6 A, with the remaining dc level being caused by an imperfect calibration of current sensors. The input voltages are almost ideally balanced. For Fig. 15, the output current reference is set to 246 A with $R_o = 1.65\ \Omega$, resulting in ≈ 100 kW operation. Without enabling the circulating current control and voltage balancing, the results in Fig. 15(a) show the maximal dc phase current difference of ≈ 32 A and the voltage imbalance of ≈ 140 V. When all control loops are activated, as shown in Fig. 15(b), the maximal circulating current is suppressed to 12 A and the voltage imbalance practically disappears.

A transient condition is tested by changing the output current reference from 80 A to 110 A, with $v_i = 900$ V, which is shown

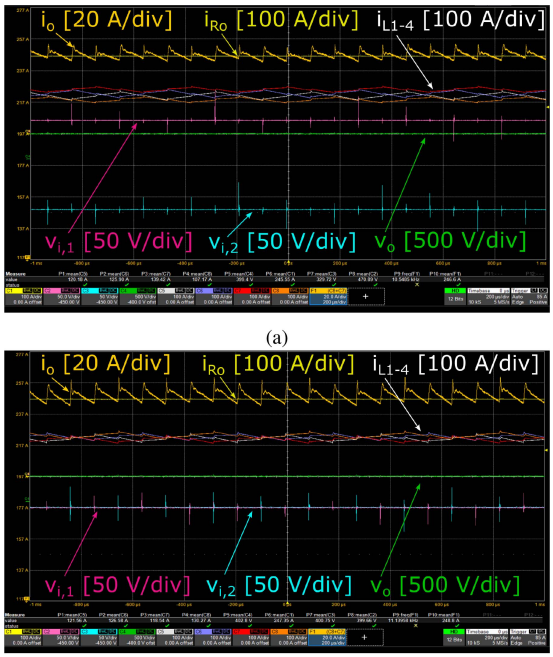

Fig. 15. Experimental results for $v_i = 800$ V, $i_o = 246$ A, $R_o = 1.65\ \Omega$, and the control system (a) without and (b) with circulating current control and input voltage balancing.

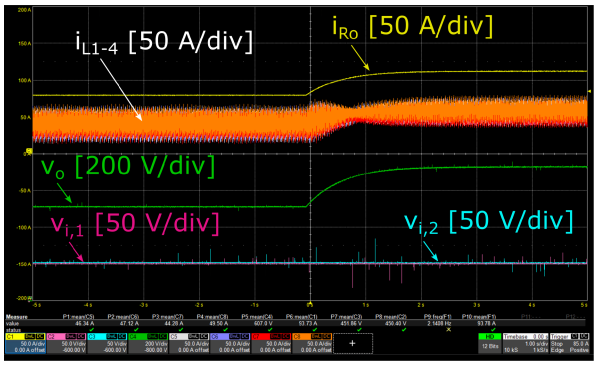

Fig. 16. Experimental result for $v_i = 900$ V, $R_o = 6.6\ \Omega$, and a transient imposed by changing the output current reference from 80 A to 110 A.

in Fig. 16. All control loops are enabled and it can be seen that the output current reference change does not disturb the voltage imbalance or the circulating currents, confirming again the decoupled nature of the proposed control system architecture.

VII. Conclusion

This article presents averaged small-signal modeling and control design of the three-level interleaved converter with coupled inductors. Focus is placed on the analysis of coupling between the duty cycles and the state variables. Transformations of state variables and control inputs are proposed to diagonalize the system and design decoupled control of the output current, circulating currents suppression, and input voltage balancing. The digital control system implementation is explained in detail, with a particular emphasis on the modulation and the oversampled filtering of the inductor currents. The small-signal model and the resulting decoupled closed-loop control systems are experimentally validated using frequency response measurements and time-domain tests, including steady-state and transient conditions.

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Ivan Z. Petrić (Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Belgrade, Belgrade, Serbia, in 2017 and 2018, respectively, and the Ph.D. degree in electrical engineering from the University of Padova, Padova, Italy, in 2023.

He is currently leading an R&D team at the Future Energy Technology Center, Hanwha Qcells Technologies, in Santa Clara, CA, USA. Since 2023, he has been an Affiliate Member of the Department of Electrical, Computer and Energy Engineering at the University of Colorado, Boulder, CO, USA. From 2018 to 2019, he was a Researcher with the Power Electronics, Machines and Control Group, University of Nottingham, Nottingham, U.K. In 2022, he was a Visiting Researcher with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, USA. His research interests include optimization, modeling, and control of power electronic converters, advanced modulation techniques, and grid-connected converters for renewable energy systems and smart microgrids.