Inherent Switching Reallocated CPS-PWM With Improved Voltage Balancing for MMC

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***Abstract*—Modular multilevel converter is an attractive solution in medium or high voltage applications, and voltage balancing is one of the most significant technical problems especially for CPS-PWM based MMCs. To solve this problem, in this article, an inherent switching reallocated CPS-PWM is proposed for MMC. Based on arm current directions, switching states of submodules (SMs), voltage sorting and carrier sorting results, proposed method divides SMs and carriers into inserting and bypassing groups for each, enabling switching reallocation within these four cooptimized groups to inherently balance capacitor voltages. This effectively prevents additional switchings. Besides, most computations of the proposed CPS-PWM are logical operations implemented in FPGA, so proposed method can achieve reallocation frequency equal to sampling frequency. Unlike other CPS-PWM based methods for voltage balancing, the inherent switching reallocated CPS-PWM not only has superior converge speed in dynamic processes which accommodate a wide power range, but also has excellent balancing accuracy especially considering capacitance differences. Owing to appropriate reallocation principles, the proposed CPS-PWM has lower switching loss compared to existing carrier reallocation methods. Finally, the feasibility and superiority of the proposed method are validated by simulation and experiment results.**

***Index Terms*—Carrier phase-shifted pulse width modulation (CPS-PWM), carrier reallocation, modular multilevel converter (MMC), voltage balancing.**

I. Introduction

MODULAR multilevel converter (MMC) is developing with great rapidity in medium and high-voltage applications, owing to its high efficiency, low dv/dt, flexible scalability and fault tolerant capability, etc [1], [2].

The carrier phase-shifted pulse width modulation (CPS-PWM) with low harmonic distortion is more suitable for MMC in medium voltage applications with a relatively small number of submodules (SMs) compared to high-voltage applications.

With the advancement of Si-based and SiC-based power devices, the number of SMs required in applications can be reduced in the future, probably making CPS-PWM popular in higher-voltage applications of MMCs.

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Voltage balancing of SM capacitors is a key issue in the MMC. Under the NLM method, this is generally resolved by SM voltage sort-plus-select [3], [4]. However, for numerous medium-voltage applications adopting CPS-PWM, sort-plus-select cannot be directly used due to the asynchronous switching actions of SMs. Although the natural balancing mechanism of MMC under CPS-PWM was proved in [5] and [6], the slow response of the natural convergence process cannot be accepted in practical applications. Besides, it is probably influenced by circuit parameters, current harmonics and switching frequency.

Several types of voltage balancing methods based on CPS-PWM have been introduced in [7], [8], [9], [10], [11], [12], [13], [14], [15], and [16]. In the hierarchical closed-loop control scheme [7], [8], voltage balancing is separated into each individual SM. However, in order not to affect the control performance of the higher layer, the weight of separated balancing control in the overall control system is relatively low, resulting in a slow response of voltage balancing [9]. Thus, when the differences of SM capacitance values are relatively large (> 0.05 p.u.), the effect of voltage balancing drops significantly. By adding an energy feedback circuit, the modified MMC topology have inherent capacitor voltage self-balancing capability [10], [11], [12], but correspondingly result in additional equipment cost, loss and circuit complexity. The authors in [13] proposed a voltage balancing method which is robust against output power, but the design process is also complicated. Moreover, voltage balancing control is still required in these schemes with fewer sensors, and much more complicated than that of the common sensor-based scheme.

In [14], [15], and [16], the switching signals generated by CPS-PWM are redistributed to SMs based on their contribution to capacitor charge transfer in each carrier cycle. However, the change of modulating signals during a carrier cycle was ignored in [14]. Besides, the average switching frequency was increased due to the pulse change of switching signals at the instance of reallocation. In [15], voltage balancing cannot be maintained when the high-frequency component of arm current is small. To guarantee the stability of capacitor voltages, some sacrifices of output performance will be necessary. Sorting and sampling frequency are reduced to fundamental frequency in [16], which makes it easy to accomplish heavier calculation in one sampling period, but the balancing performance is also worse with the decrease of sorting frequency.

As analyzed above, the voltage balancing effects of existing CPS-PWM based schemes for MMC are not satisfactory.

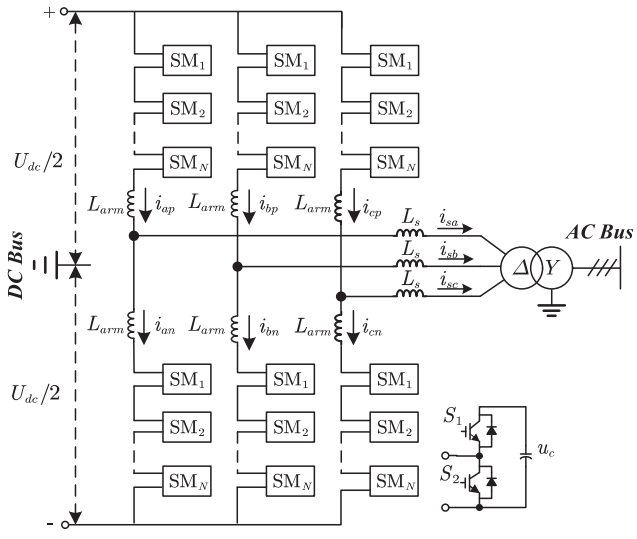

Fig. 1. Typical configuration of half-bridge MMCs.

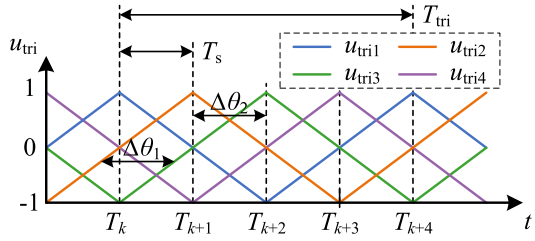

Fig. 2. Phase-shifted triangular carrier waves of CPS-PWM.

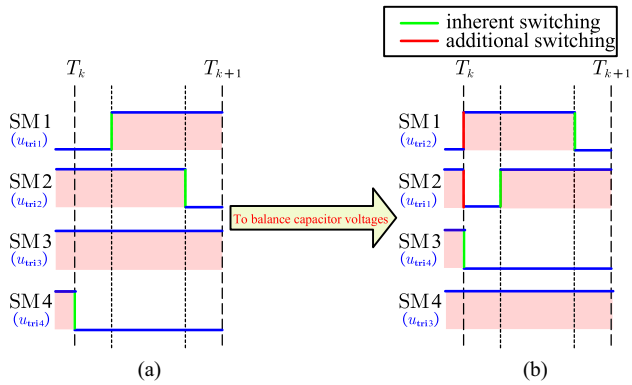

Fig. 3. Inherent and additional switchings under existing CPS-PWM. (a) switching example of CPS-PWM without carrier reallocation and (b) switching example of CPS-PWM with carrier reallocation.

Besides, the tradeoff between switching frequency and voltage balancing performance is a common problem. In this article, extending the switching utilization concept for voltage balancing in previous work [17], [18], an inherent switching reallocated CPS-PWM method is proposed for MMC. Considering arm current directions, SM switching states, capacitor voltage sorting, and carrier sorting results, this method groups both SMs and carriers into bypassing group and inserting group for each, then inherent switching actions are reallocated within these cooptimized groups to balance capacitor voltages. Besides, the feasibility of the proposed reallocation in FPGA is illustrated in this article. Compared with the existing CPS-PWM based methods [8], [13], [14], the proposed CPS-PWM method has superior dynamic and steady-state performance in voltage balancing. It has a lower switching loss compared to existing carrier reallocation methods. Simulation and experimental results under different conditions are presented in this article to validate the feasibility and performance of the proposed CPS-PWM method.

II. Novel Inherent Switching Reallocated CPS-PWM for MMC

A. Characteristics of Conventional CPS-PWM

The typical three-phase MMC has six arms, and each arm consists of N series-connected SMs and an inductor. As an example, the typical half-bridge MMC is analyzed in this article. As shown in Fig. 1, each SM is mainly composed of an upper switch S_1, a lower switch S_2, and a capacitor.

N triangular carriers with the same frequency of f_{tri} are required for an arm with N SMs. In order to effectively eliminate the high-order harmonic of arm current, the phase-shifted angle $\Delta\theta_1$ of each carrier should be $2\pi/N$ [19]. Assuming the sampling and control frequency f_{s} is equal to the equivalent switching frequency Nf_{tri}, the angle variation of any carrier between T_k and T_{k+1} can be calculated as

$$\Delta\theta_2 = \frac{f_{\text{tri}}}{f_{\text{s}}} \cdot 2\pi = \frac{2\pi}{N}. \tag{1}$$

Taking the upper arm of phase a as an example, with 4 SMs in the arm as shown in Fig. 2. Following two kinds of switching are called inherent switchings in this article. First, there must be 2 switchings caused by intersections of modulating signals and carriers in each arm during a sampling cycle when $f_{\text{s}} = Nf_{\text{tri}}$. Second, notably at the moment of updating modulating signal u_{m}, one or more changes of switchings may be caused at T_{k} by the step change of u_{m}. The inherent switchings are marked in green in Fig. 3.

To achieve capacitor voltage balance, carrier reallocation methods are adopted, but they may cause additional switchings, which are marked in red in Fig. 3. These additional switchings are caused by improper reallocation without considering initial switching states, so the switching loss increases.

B. Inherent Switching Reallocated CPS-PWM

By grouping carriers and SMs during the reallocation process, the proposed inherent switching reallocated CPS-PWM theoretically prevents additional switchings, and it can easily operate at the frequency of sampling/control. There are the following two mandatory principles.

Principle 1 (P1): SMs with higher capacitor voltages are supposed to discharge or to be bypassed (not charge); SMs with lower capacitor voltages are supposed to charge or to be bypassed (not discharge).

Principle 2 (P2): Only inherent switchings are utilized and no additional switchings occur.

There is necessary information in the reallocation process of proposed CPS-PWM.

i1): Initial switching states/groups of SMs.
i2): Arm current directions.
i3): Sorting result of capacitor voltages.
i4): Sorting result of carrier average values during next sampling cycle.

It is worth knowing that all information for reallocation is easy to obtain with FPGA. i1 can be obtained by comparing the modulating signal with the carriers. i2 is known directly from sampling. i3 and i4 can be rapidly done with bitonic sorting. i4 includes add and divide operations to calculate average values, but the dividing operation can be removed because the sorting result will not change with the divisor which is always 2.

Initially, carriers $u_{\text{tri}1}$, $u_{\text{tri}2}$, $u_{\text{tri}3}$, and $u_{\text{tri}4}$ are corresponding to SM1, SM2, SM3, and SM4 respectively. The proposed CPS-PWM reallocates carriers to SMs each sampling cycle as shown in Fig. 5(c) and (e). Only inherent switching mentioned in Section II-A is required and redistributed to SMs in proposed scheme, so switching timing $(t_1, \ldots, t_8)$ and switching frequency of proposed CPS-PWM [Fig. 5(c) and (e)] are the same as the CPS-PWM without voltage balancing control [Fig. 5(b)]. Proposed CPS-PWM includes the following four steps.

Step 1: Based on Principle 2, initial switching states of SMs should be determined. If $u_{\text{tri}i}$ at T_k is greater than the previous modulating signal u'_{m} at T_{k-1}, the related SMj (to which the $u_{\text{tri}i}$ is allocated at T_{k-1}), is assigned to the bypassing group, otherwise, it is assigned to the inserting group.

Step 2: Based on Principle 2, carriers should also be divided into two groups by their amplitudes. If $u_{\text{tri}i}$ is greater than the updated modulating signal u_{m}, then $u_{\text{tri}i}$ is assigned to the bypassing group, otherwise, it is assigned to the inserting group.

Step 3: Based on Principle 2, one-to-one correspondence within the groups should be checked. If there is switching at T_k, sorting for capacitor voltages $u_{\text{cap}i}$ is needed for choosing SMs to move between two groups. Based on Principle 1, arm current and sorting result of capacitor voltages will be used to find the redundant SMs that need to be moved to the other group. If arm current is positive, redundant SMs with higher capacitor voltages tend to join bypassing group and the ones with lower capacitor voltages tend to join inserting group; otherwise the opposite is the case. If there is no switching at T_k, the SM groups remain unchanged based on the initial switching states (i1) from Step 1.

Step 4: Based on Principle 1, sort carriers according to the average value $u^*_{\text{tri}i}$ in this sampling cycle. If two carriers have the same average value during a sampling cycle, the carrier with lower initial value are considered as having the larger average value than the one with higher initial value, because the former tends to increase in the next sampling cycle. Reassign the carriers to SMs according to the sorting results of carriers and capacitor voltages. The carriers with larger average values

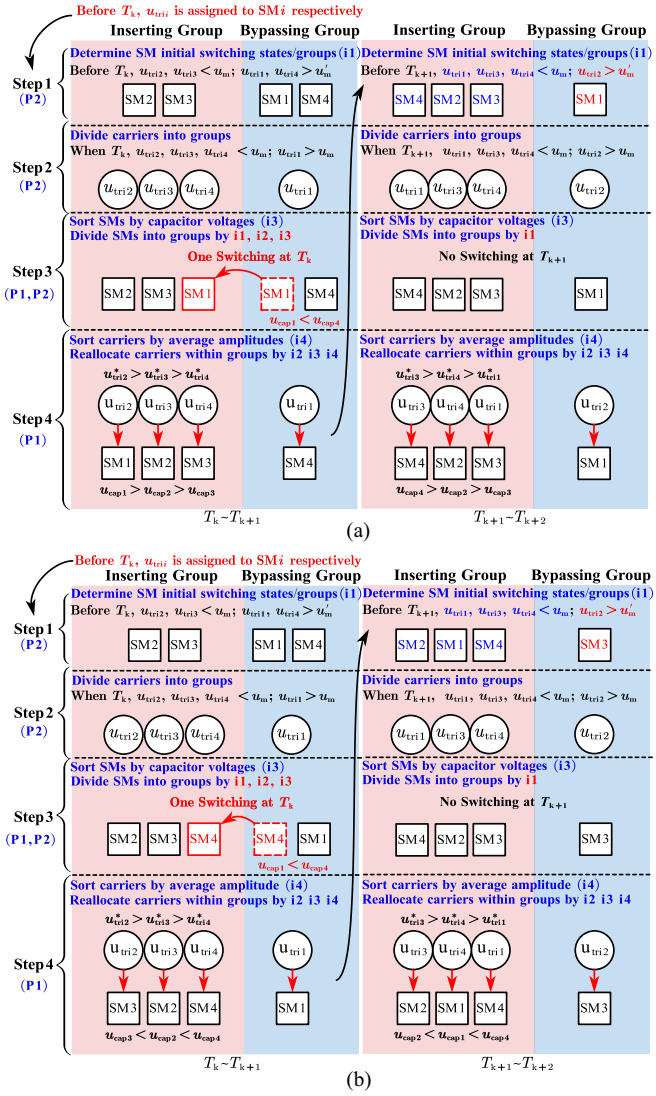

Fig. 4. Inherent switching reallocation examples during $T_k \sim T_{k+2}$, (a) if i_{ap} is positive and (b) if i_{ap} is negative.

are more potential for bypassing the SMs. Therefore, if the arm current is positive, higher carriers are reassigned to the SMs with higher capacitor voltages and the lower carriers are reassigned to the SMs with lower capacitor voltages; otherwise the opposite applies.

Fig. 4 gives the examples of two sampling cycles from Fig. 5 during $T_k \sim T_{k+2}$. Here are the explanations for Fig. 4(a).

$T_k \sim T_{k+1}$: SM1, SM4, and u_{tri1} are assigned to bypassing groups while the rest SMs and carriers are in inserting groups. Due to the modulation signal updating, one inserting switching occurs at T_k and SM1 has the lowest capacitor voltage in SM bypassing group, SM1 is changed to SM inserting group to make the numbers of carriers and SMs equal. For bypassing groups, u_{tri1} is assigned to SM4. And for inserting groups, according to the sorting results in Step 2, u_{tri2}, u_{tri3}, and u_{tri4} are reassigned to SM1, SM2, and SM3, respectively.

$T_{k+1} \sim T_{k+2}$: SM1 and u_{tri2} are assigned to bypassing groups while the rest SMs and carriers are in inserting groups.

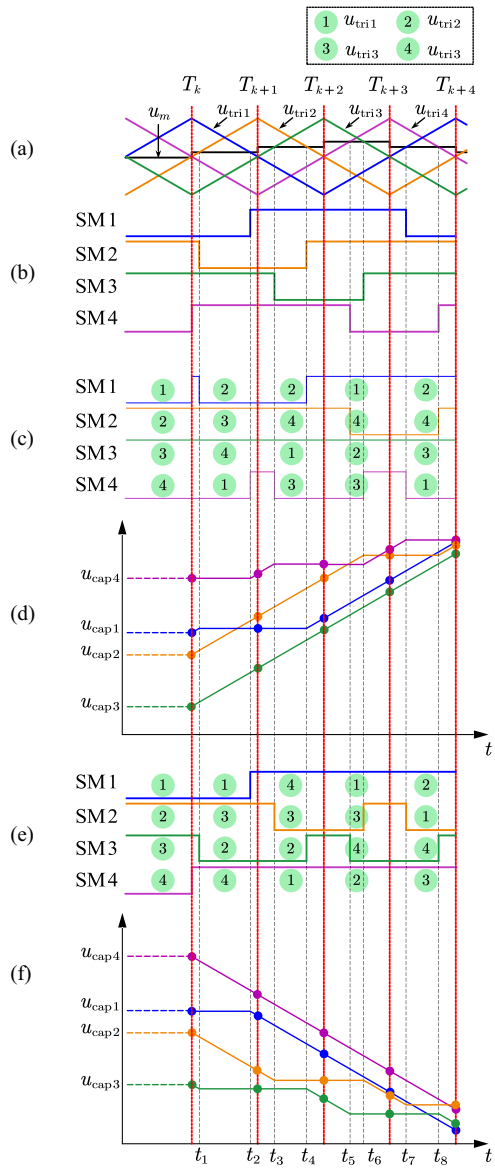

Fig. 5. Principles of CPS-PWM with conventional CPS-PWM and with inherent switching reallocated CPS-PWM. (a) Modulating signal and carriers. (b) Switching signals with conventional CPS-PWM. (c) Switching signals under proposed CPS-PWM when i_{ap} is positive. (d) Capacitor voltage balancing process of proposed CPS-PWM when i_{ap} is positive.(e) Switching signals under proposed CPS-PWM when i_{ap} is negative. (f) Capacitor voltage balancing process of proposed CPS-PWM when i_{ap} is negative.

Because no switching occurs at T_{k+1}, there is no regrouping process. It is worth noticing that u_{tri2} has been reallocated to SM1 during last control period, so SM1 should be in bypassing group for $u_{tri2} > u_m$. For bypassing groups, u_{tri2} is assigned to SM1. And for inserting group, according to sorting results in Step 2, u_{tri3}, u_{tri4}, and u_{tri1} are assigned to SM4, SM2, and SM3, respectively.

Similar analysis in $T_{k+1} \sim T_{k+2}$ can be applied to $T_{k+2} \sim T_{k+4}$. The reallocation results are also shown in Fig. 5(c) and the capacitor voltages are gradually balanced with proposed CPS-PWM as shown in Fig. 5(d). Correspondingly, the results when i_{ap} is negative are also shown in Figs. 4(b) and 5(e)–(f).

C. Feasibility of Proposed Inherent Switching Reallocated CPS-PWM With FPGA

As described previously, compared with conventional CPS-PWM, a reallocation process mentioned in II-*B* is added to the beginning of each sampling cycle and there is no additional modification for CPS-PWM. Sorting for both carriers and voltages in each sampling cycle is required for the proposed inherent switching reallocated CPS-PWM. Then time consumed by the reallocation process need to be evaluated to ensure the feasibility of the proposed method.

Steps 1 or 2 can be accomplished in one FPGA clock period by presenting possible situation, i.e.,, trade space for time. The parallel sorting algorithm method [20] is introduced in Step 2, which only takes $\log_2 N(\log_2 N + 1)$ clocks for sorting N SMs. Assuming the clock frequency of FPGA is 200 MHz, even when the number of SMs N is large as 256, only 36 clock cycles of FPGA are required and the computation cost is 0.18 μs. What is more, the sorting for carriers and SMs shown in Fig. 4 can also be accomplished in parallel with FPGA to trade space for time.

Thus, with the adoption of parallel sorting method in FPGA, even there are hundreds of SMs in an arm bridge, the consumed time is less than 1 μs, which can be easily neglected comparing to other computation process.

D. Comparison of Different Voltage Balancing Schemes Based on CPS-PWM

Generally, capacitor voltage balancing schemes for CPS-PWM based MMC can be divided into following two types.

1) *PI-based methods:* Individual control loop based schemes without no sorting process [8], [13]. For type 1, the main problem lays in the process of designing parameters to have both good output performance and balancing effectiveness. And usually they have a slow convergence speed [8], but [13] which improves the converge speed.
2) *Carrier reallocated methods:* Signal reallocation based schemes with sorting process [14], [16]. For type 2, the contradiction between computational burden in sorting process and its effectiveness is the main concern. The authors in [14] show an example of calculating circuit variables in SMs for sorting, but the calculation is not accurate and the computation burden is still high. Methods like [16] choose a lower sorting frequency to solve the problem but the process is more complicated and the balancing performance is sacrified.

The proposed inherent switching reallocated CPS-PWM is similar to carrier reallocation based methods, but they differ a lot. The proposed method is a modified version of conventional CPS-PWM and even has the same switching frequency. PI controller-based methods [8], [13] are considered having the same switching loss with proper parameter design. By contrast, carrier reallocation based methods [14], [16] are considered having a larger switching loss because of additional switchings mentioned in Section II-A. But the frequency of reallocation is low in method [16], so the increased switching loss is negligible

TABLE I
COMPARISON OF DIFFERENT VOLTAGE BALANCING SCHEMES BASED ON CPS-PWM

	PI-based Method		Carrier Reallocated Method		Proposed
	[8]	[13]	[14]	[16]	
Switching loss	Same	Same	Higher	Slightly higher	Same
Robustness against power change	Low	High	Medium	-	High
Converge speed of voltage balancing	Low	High	Low	Medium	Very high
Steady-state voltage balancing accuracy	High	High	Medium	-	High
Robustness with unequal capacitance	Medium	Medium	Low	-	High
Complexity	Hard	Hard	Easy	Medium	Easy
Computational burden	Medium	Medium	Medium	Low	Low
Current sensor	Need	Need	No need	No need	Need

TABLE II
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Simulation	Experimental
DC-link voltage, U_{dc}	6 kV	480 V
AC phase voltage (rms), U_s	1.70 kV	135.8 V
Rated output power, S_n	500 kW	1200 W
Number of SMs per arm, N	6	6
Arm inductance, L_{arm}	5 mH	3 mH
AC inductance, L_s	5 mH	3 mH
SM capacitance, C_{sm}	3 mF	2 mF
Sample frequency, f_s	10 kHz	10 kHz
Carrier frequency, f_{tri}	1.67 kHz	1.67 kHz

in when carrier frequency is not low. The proposed CPS-PWM prevents the additional switching at the instant of signal distribution, thus, having a lower switching loss than other carrier reallocation methods. The overall comparison between main methods of both types is summarized in Table I .

Generally, PI controller-based methods are considered more complex because they are more difficult in controller design. For method [14], the circuit based calculation is simple. Method in [16] has a complex procedure in carrier reallocation including circuit based calculation. The proposed method requires no additional controller design for controller. Only a few add/subtract operations, together with sorting and grouping (logical operations) are included in the computation. Thus, proposed method can be computed fastly in FPGA and can promote the reallocation frequency to the same as the sampling frequency. By contrast, the low reallocation frequency in methods [14], [16] results in inferior voltage balancing performance compared to PI controller-based methods [8], [13]. The detailed comparison in voltage balancing is accomplished in simulations and experiments.

III. SIMULATION STUDIES

To verify the effectiveness of the proposed CPS-PWM method, a single phase MMC system is modeled in MATLAB/Simulink and the system parameters are shown in Table II.

A. Dynamic Performance Evaluation

Convergence speed and the robustness against output power of different methods are compared in Fig. 6. The power reference is initially set to 1.0 p.u. and all methods use [8] until the power reference is changed to 0.5 p.u. at 0.1 s. SM1 and SM6 are set to 1200 V and 800 V initially while the other SMs are set to rated voltage 1000 V. After 0.1 s, three different methods are activated. Notably, the first two methods which will be influenced by parameters are set to have a close converge speed at unit output power in the following simulations.

TABLE III
COMPARISON OF VOLTAGE BALANCING TIME OF DIFFERENT METHODS (UNIT: S)

	Simulation			Experiment		
Output Power (p.u.)	1.0	0.5	0.25	1.0	0.5	0.25
Method in [8]	0.278	0.510	0.818	0.070	0.156	0.325
Method in [13]	0.272	0.322	0.388	0.060	0.091	0.135
Method in [14]	3.080	3.690	5.610		–	
Proposed	0.018	0.035	0.056	0.020	0.036	0.071
Theoretical (Proposed)	0.020	0.040	0.080	0.020	0.040	0.080

Besides, the model is also simulated under different output power conditions as shown in Fig. 6(a)–(c). And the statistic results are summarized in Table III. The simulation result shows that the improved PI-based method in [13] exhibits significantly better robustness to output power variations than [8]. Although the method in [14] is robust to output power changes, the converge speed is far slower than the other ones. By contrast, the proposed CPS-PWM method demonstrates significantly faster convergence speed and the balancing performance is less relevant to output power.

The theoretical convergence time of the proposed method can be calculated and verified in the following part. Since the capacitor voltage has the following equation:

$$\Delta u_{\mathrm{c}} = \frac{1}{C}\int_{t_1}^{t_4} i_{\mathrm{ap}} dt \tag{2}$$

where Δu_{c} is the change of capacitor voltage during one fundamental period, t_1 and t_4 are the beginning and ending of the time duration, and C is the capacitor value. The expression for arm current in single phase MMC is

$$i_{\mathrm{ap}} = \frac{1}{2} I_{\mathrm{s,peak}} \sin(\omega t + \varphi) + I_{\mathrm{cir,dc}} \tag{3}$$

$$I_{\mathrm{cir,dc}} = S_{\mathrm{n}} / U_{\mathrm{dc}} \tag{4}$$

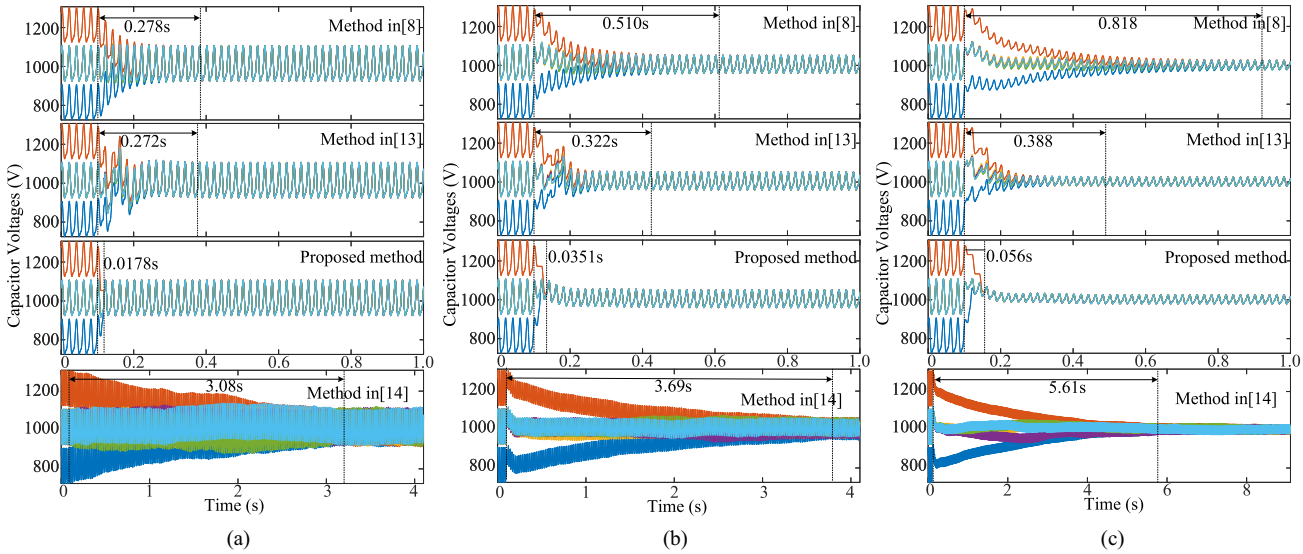

Fig. 6. Simulation waveforms of SM capacitor voltages under dynamic process, (a) S = 1.0 p.u., (b) S=0.5 p.u., and (c) S=0.25 p.u.

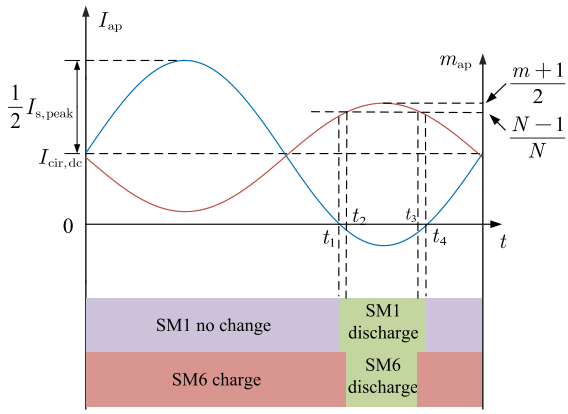

Fig. 7. Waveforms of arm current and arm insertion index.

$$I_{\mathrm{s,peak}} = 2S_{\mathrm{n}}/U_{\mathrm{S,peak}} \tag{5}$$

$$U_{\mathrm{S,peak}} = \frac{1}{2}mU_{\mathrm{dc}} \tag{6}$$

where $I_{\mathrm{s,peak}}$ is the amplitude of ac output current, ω is the angular frequency, φ is the power factor angle, $I_{\mathrm{cir,dc}}$ is the dc component of circulating current, S_{n} is the rated power, U_{dc} is the dc voltage, and $U_{\mathrm{S,peak}}$ is the amplitude of ac output voltage.

The ac part of circulating current is ignored in (3). Then, the charging/discharging model of proposed method in the case of simulation can be easily established as shown in Fig. 7.

In the simulation, SM1 always has the priority in discharging when it has a higher capacitor voltage. So capacitor voltage of SM1 is remaining constant when arm current is positive and discharging when arm current is negative. On the other hand, SM6 always has the priority in charging, so it is charging whenever the arm current is positive. For this case, when the arm current is negative and insertion index m_{ap} is greater than $(N-1)/N$, SM6 is also discharging during t_2 and t_3. Therefore, the converge time for voltage balancing in the simulation case is only determined by SM1 because SM6 has more time in charging, then the Δu_{c} during one period can be calculated as

$$\Delta u_{\mathrm{c}} = \frac{1}{C}\int_{t_1}^{t_4} \left(S_{\mathrm{n}}/U_{\mathrm{S,peak}} \sin\left(\omega t + \varphi\right) + S_{\mathrm{n}}/U_{\mathrm{dc}}\right) dt \tag{7}$$

$$t_{\mathrm{balance}} = \Delta U_{\mathrm{c}}/\Delta u_{\mathrm{c}} * 0.02 \tag{8}$$

where ΔU_{c} is the capacitor voltage difference between the SM and the average value, t_{balance} is the voltage balancing time. Substituting the simulation parameters, $\Delta u_{\mathrm{c}} = 200$ V. Therefore, SM1 with a initial $\Delta U_{\mathrm{c}} = 200$ V will need at most $t_{\mathrm{balance}} = 0.02$ s to converge. When the power reference is reduced to 0.5 p.u., $\Delta u_{\mathrm{c}} = 100$ V, which also reduced to half of the unit power condition. Similarly, the theoretical voltage balancing time for $S_{\mathrm{n}} = 1.0$ p.u., 0.5 p.u., and 0.25 p.u. for the simulation case can be calculated as 0.02 s, 0.04 s, and 0.08 s, respectively.

B. Steady-State Performance Evaluation

Compared with conventional CPS-PWM, carrier reallocated CPS-PWM usually has a higher switching loss. Fig. 8 gives the steady-state waveforms of MMC under PI-based CPS-PWM [8], carrier reallocated CPS-PWM [14] and proposed method. When their output current have almost the same THD, method in [14] has a 16% larger switching frequency. With proposed inherent switching reallocation process, the switching frequency is greatly reduced to the same as PI-based CPS-PWM [8] and it is smaller than method in [14]. It reveals that, different from existing methods based on carrier reallocation, the proposed CPS-PWM is effective in preventing additional switchings.

To validate the superior voltage balancing accuracy of proposed method, simulation with unequal capacitance under different methods are operated as shown in Fig. 9. In the simulation,

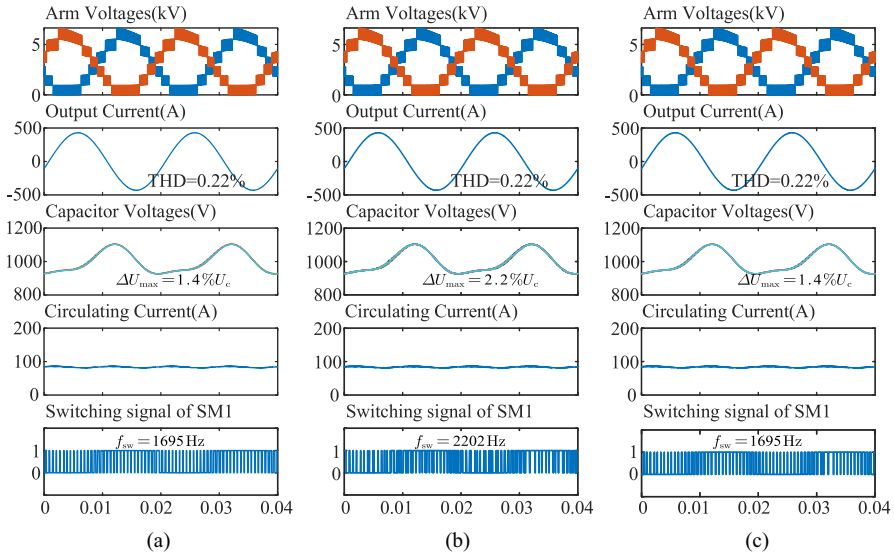

Fig. 8. Simulation waveforms of MMCs under (a) PI-based CPS-PWM [8], (b) carrier reallocated CPS-PWM [14], and (c) proposed method.

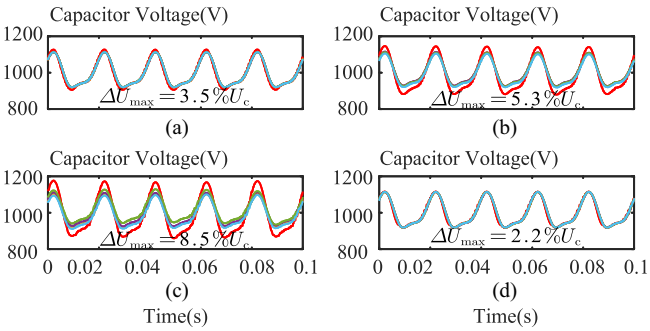

Fig. 9. Simulation waveforms of SM capacitor voltages in steady-state with different methods, (a) method in [8], (b) method in [13], (c) method in [14], and (d) proposed method.

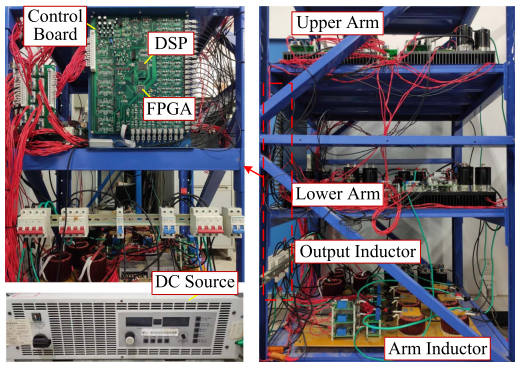

Fig. 10. Photograph of the laboratory prototype of the single phase MMC.

the capacitance of SM1 is set to 0.6 p.u. and that of other SMs remain 1.0 p.u. Eventually voltage deviation is apparent in Fig. 9(a)–(c) with existing methods. By contrast, adopting proposed CPS-PWM method, even with significant difference in capacitance, the capacitor voltages are balanced well in Fig. 9(d).

IV. Experimental Verification

A laboratory prototype of a single-phase MMC with four SMs per arm is established as shown in Fig. 10 to verify the proposed method. A digital signal processor (TMS320F28335) and an FPGA (EP4CE10E22C8) are used for receiving sampling data, data processing, and switching signal generation. The main parameters are summarized in Table I. Results of comparative experiments are shown in Figs. 6–9, where $u_{can1} \sim u_{can6}$, u_{an}, i_{sa}, i_{ca} are the capacitor voltages, arm voltage, output current and circulating current. The main difference from simulation lies in the nonidentical control implementation (including control delay, dead time of driving signals, measurement errors, etc.) and number of SMs per arm.

A. Dynamic Performance Evaluation

Fig. 11(a), (d), and (g) give the experimental results of dynamic response of PI-based CPS-PWM method in [8]. The balancing time increases significantly as output power decreases. In Fig. 11(b), (e), and (h), the method in [13] shows certain robustness against output power. However, the energy fluctuates significantly during the initial period of applying balancing control. When the parameters of method in [13] are set to get a fast convergence speed, there is certain sacrifice in other control loops, so the design of those parameters is complicated and hard. With proposed CPS-PWM method, shown in Fig. 11(c), (f), and (g), the converge time is much smaller than other methods and it is also robust against output power change. The detailed statistic results for different methods are listed in Table III.

Similar calculation for capacitor voltage balancing time can be computed and $\Delta u_c = 10$ V with the experimental

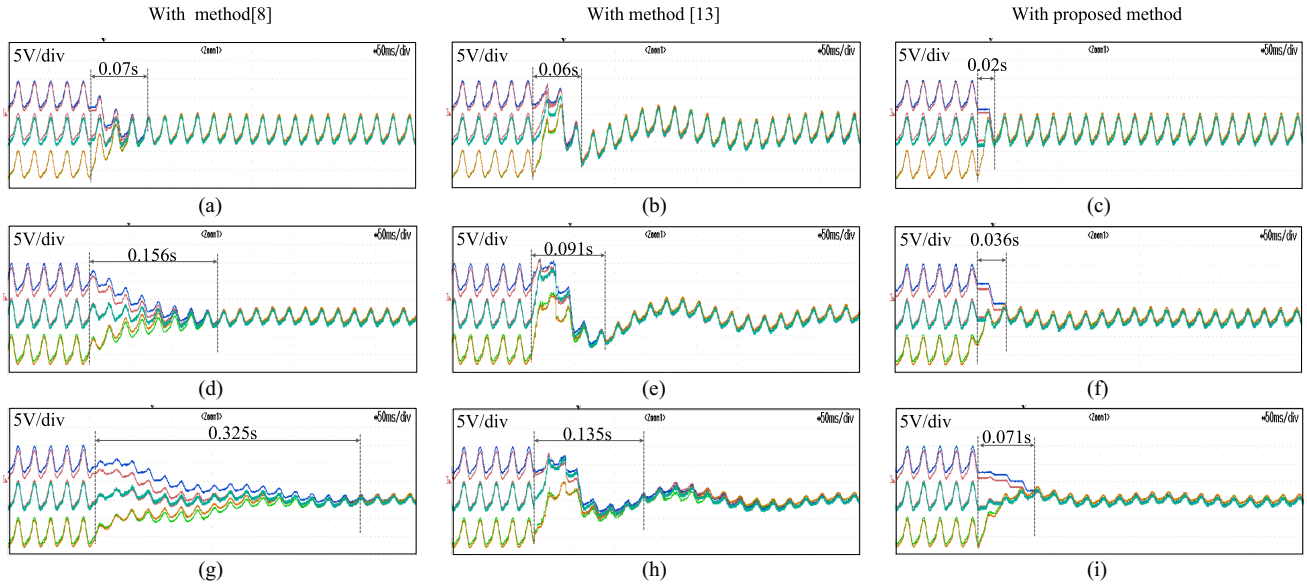

Fig. 11. Experimental waveforms of capacitor voltage in dynamic process with different method. (a)–(c) S = 1.0 p.u., (d)–(f) S = 0.5 p.u., (g)–(i) S = 0.25 p.u.

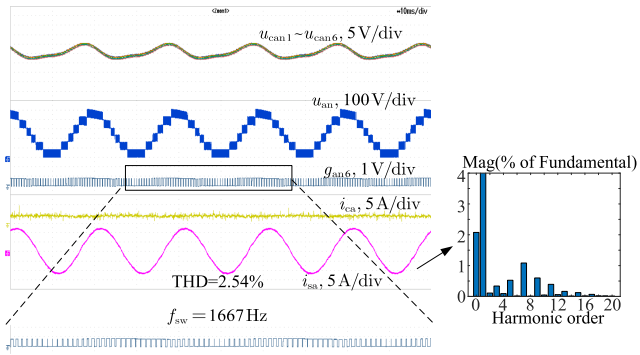

Fig. 12. Experimental waveforms of MMC under equal SM capacitance with method in [8].

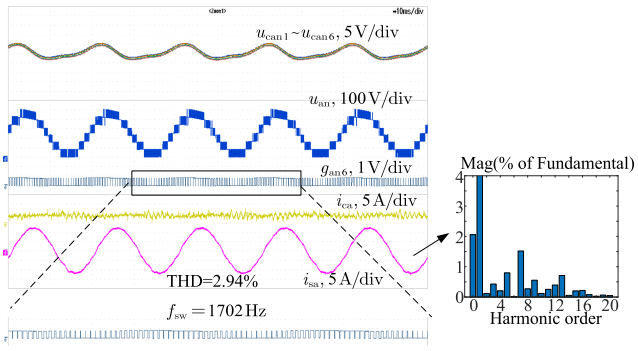

Fig. 13. Experimental waveforms of MMC under equal SM capacitance with method in [13].

parameters. Then, the theoretical capacitor voltage balancing time is 0.02 s, 0.04 s, and 0.08 s, respectively, for S = 1.0 p.u., 0.5 p.u., and 0.25 p.u., which is verified by the experiment results.

B. Steady-State Performance Under Unequal Capacitance

Figs. 12–14 show the steady-state waveforms under method in [8], method in [13] the proposed inherent switching reallocated CPS-PWM. When they have almost the same THD for output current, switching frequency under these methods are also close. Fig. 15 gives the experimental results of different methods under unequal capacitance, it is worth noting that the SM1 capacitance is set to 1.5 mF, while other SMs maintain 2.0 mF. Under PI-based balancing control for CPS-PWM [8], the difference of SM capacitance have strong effect on the voltage balancing which results in relatively large amplitude difference near the voltage peaks and valleys. With improved balancing control [13], the amplitude difference is reduced compared to PI-based method but the voltage deviation is still

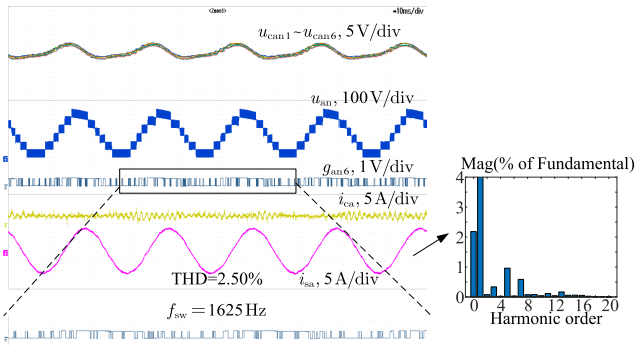

Fig. 14. Experimental waveforms of MMC under equal SM capacitance with proposed method.

large. Comparing with the steady-state waveforms under equal capacitance, the circulating current in Fig. 15(b) exhibits more severe fluctuations. Under proposed CPS-PWM, SM capacitance differences have negligible influence on the capacitor voltage balancing which indicates that higher balancing control accuracy has been achieved.

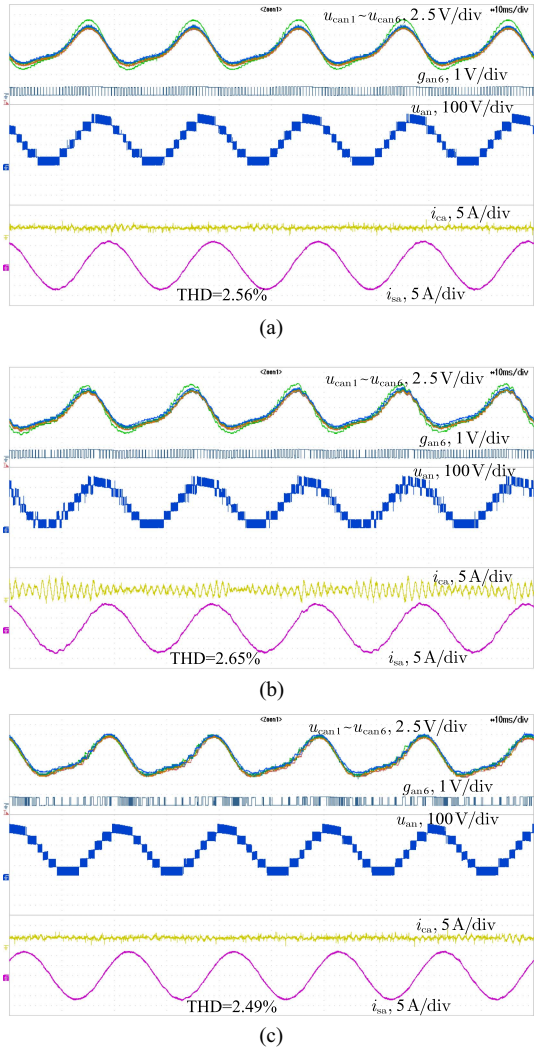

Fig. 15. Experiment waveforms of MMC under unequal SM capacitance with different methods. (a) method in [8], (b) method in [13], and (c) proposed method.

V. Conclusion

An inherent switching reallocated CPS-PWM method for MMC is proposed in this article. Compared to other carrier reallocation based methods, the proposed method groups SMs and carriers into bypassing and inserting group for each, avoiding additional switching actions. Besides, the sorting basis (carrier average values and SM capacitor voltages) in the proposed method are intuitive and involve negligible calculations. Therefore, the inherent switching realloacted CPS-PWM mainly requires logical computations, enabling full implementation on FPGA, realizing a higher reallocation frequency to the same sampling frequency. The analysis, simulations, and experiments demonstrate the features and contributions of proposed inherent switching reallocated CPS-PWM as follows.

1) The proposed method has faster convergence speed than other CPS-PWM methods in capacitor voltage balancing, which also maintains robust performance across a wide power range.
2) The proposed method surpasses other CPS-PWM methods in balancing performance under unequal SM capacitances.
3) The proposed method has superior accuracy in capacitor voltage balancing compared to other carrier reallocation-based methods.
4) The proposed method exhibits lower switching losses compared to other carrier reallocation based methods.
5) The proposed method operates independently of MMC control loops, enabling seamless integration with other strategies to further enhance the capacitor voltage balancing ability.

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