Improved Single DC Source Hybrid Neutral Point Clamped Converter With 13 Levels

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***Abstract*—In this article, a 13-level circuit topology is proposed, which features a single dc source, extended linear modulation range, and a high ratio of output voltage levels to semiconductor devices. The proposed converter, which consists of a series-connected floating H-bridge (FHB) supplementing a five-level active neutral point clamped converter (5L-ANPC), can generate 13 pole voltage levels in the normal modulation region and 15 levels in the extended modulation region. The key performance improvements offered by the proposed topology are enhanced power quality, reduced losses, and increased power density. Whereas existing schemes with a similar circuit structure regulate the FHB to one-eighth of the dc-link voltage and only achieve nine levels, the proposed joint-phase redundancy balancing approach regulates the FHB stage to one-twelfth of the total dc-link voltage on a switching-frequency basis, thereby increasing output power quality while reducing the converter's cost and size without the need for multiple isolated supplies. Furthermore, the proposed modulation scheme also allows for a switching frequency reduction of the higher voltage blocking 5L-ANPC stage by shifting the high-frequency switching to the low voltage blocking FHB stage, thus reducing losses. This work also evaluates operation in the topology's extended linear modulation range, which is shown to be increased to 0.612 times the dc-link voltage (modulation index, $M = 1.223$) without limitations on load power factors, compared to the typical limit of to 0.577 times the dc-link voltage ($M = 1.154$) for nonboosting topologies such as 3L-ANPC and 5L-ANPC. The proposed converter uses boosting states enabled by the FHB in this extended modulation region, which increases the number of output levels to 15. The effectiveness of the proposed topology and capacitor balancing scheme is validated using experimental and analytical results. Based on experimental and analytical results, the proposed topology is shown to have improved power quality, efficiency, size, and weight relative to the existing solutions.**

***Index Terms*—Active neutral point clamped (ANPC), cascaded H-bridge, flying capacitor (FC), joint-phase redundancy, medium voltage AC (MVAC), medium voltage DC (MVDC), model predictive control (MPC), motor drive, space vector (SV).**

I. Introduction

MULTILEVEL converter topologies are indispensable for medium and high voltage conversion applications, such as those required in transportation electrification, renewable energy integration, and power distribution. The most valuable features of multilevel converter typologies include the reduction of device voltage ratings, improved power quality, reduced switching loss, and low electromagnetic interference. Such factors are vital in meeting system requirements while limiting cost, size, and losses.

A popular medium or high-voltage three-phase multilevel converter solution for the applications mentioned above is the three-level (3L) active neutral point clamped (ANPC) converter [1], [2], [3], [4]. The success of the ANPC is due to its compactness relative to alternative designs; ANPC does not require isolated power supplies unlike cascaded H-bridge (CHB) converters, and ANPC requires fewer and smaller passive power devices compared to flying capacitor converter (FCC) [5], [6], [7] and modular multilevel converter (MMC) [7], [8], [9], [10].

Several improvements to the 3L-ANPC converter have been proposed in the literature; for instance, the 5L-ANPC converter, which adds a flying capacitor (FC) stage to the 3L-ANPC topology, has found widespread success [11], [12]. Other proposed improvements to the 3L-ANPC are the addition of floating H-bridge (FHB) converters connected in series with the output of the 3L-ANPC to form a five-level (5L) converter [13]. These FHB stages do not use isolated supplies but regulate capacitor voltages by controlling reactive power flow into the FHB [14]. A nine-level (9L) ANPC topology using both an FC stage and an FHB stage regulated to one-eighth the dc-link voltage, referred to here as the 9L-ANPC, has also been proposed [15], [16], [17], [18]. In each case, per-phase redundancy balances the FC and FHB capacitors, allowing for high-frequency capacitor regulation without impacting the output pole voltage. Previous works have shown that model predictive control (MPC) is well-suited for the selection of redundant states due to the ease at which proper state selection can be made while considering multiple performance objectives [19], [20], [21], [22]. Isolated power supplies have also been proposed for the series-connected H-bridge stage to avoid capacitor regulation and to achieve 11 output voltage levels [23]; however, isolated power supplies add complexity, size, and losses to a design and therefore are preferably avoided.

Inclusion of a series-connected stage can further improve converter power quality and efficiency when using common-mode voltage to increase the number of output voltage levels. For instance, a 3L-ANPC converter with a single FHB will typically achieve five output voltage levels with an FHB voltage

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of a quarter of the dc-link voltage [24], however, when taking advantage of common-mode voltages, the FHB stage can be regulated to a sixth of the dc-link to create a seven-level converter, thereby reducing the output voltage step size and reducing device switching energy [5], [13]. This approach of using common mode voltage (i.e., joint-phase redundancies) to achieve additional output voltage has been previously proposed for other topologies, however, regulation has only been achieved with low-frequency control of common mode voltage [24], [25], [26], [27]. In addition, the series-connected stages can increase the linear modulation limit over that of the base converter alone [23], [28], [29]; however, this increase in modulation has yet to be applied to the hybrid ANPC converter without the use of isolated supplies.

This article proposes an improved hybrid neutral point converter topology with a 13-level (13L) output and low voltage FHB (one-twelfth of the dc-link voltage), which substantially increases performance over other topologies within its class. The salient features of the proposed topology and associated control scheme are as follows.

1) A low voltage ($V_{dc}/12$) FHB stage is connected in series with a 5L-ANPC to generate a 13-level pole-voltage waveform with only 12 switches per phase and without the use of isolated power supplies.
2) The FC and FHB stages are regulated to their nominal voltages of $V_{dc}/4$ and $V_{dc}/12$, respectively, on a switching-frequency basis using joint-phase redundancy while operating up to $M = 1.154$, thus keeping required capacitor sizes small. The FHB capacitors can only be balanced using joint-phase redundancies, as there are insufficient per-phase redundancies to regulate the FHB to this reduced voltage.
3) The modulation approach capitalizes on the proposed converter's joint-phase redundancies to minimize switching losses by modulating the highest voltage-blocking devices at line frequency and modulating the lowest voltage-blocking devices switch at the highest frequency while regulating floating capacitor and midpoint voltages.
4) The proposed topology can operate in an extended linear modulation region utilizing its series-connected FHB, specifically up to $M = 1.223$, irrespective of the power factor, as compared to the $M = 1.154$ limit typical of converters without boosting capability such as 5L-ANPC. Operation in extended linear modulation uses 15 output pole voltage levels.

II. Circuit Topology and SVS

A. Power Circuit

The proposed topology consists of a 5L-ANPC stage and a series-connected FHB stage, as shown in Fig. 1. The input to the converter uses a single dc source. A midpoint is formed internally to the converter via the dc-link capacitors C_{dc1} and C_{dc2} of equal capacitance C_{dc}. The objective of the 5L-ANPC stage is to generate the fundamental component of the output waveform, while the FHB stage improves output power quality. This configuration allows the 5L-ANPC stage to have a reduced

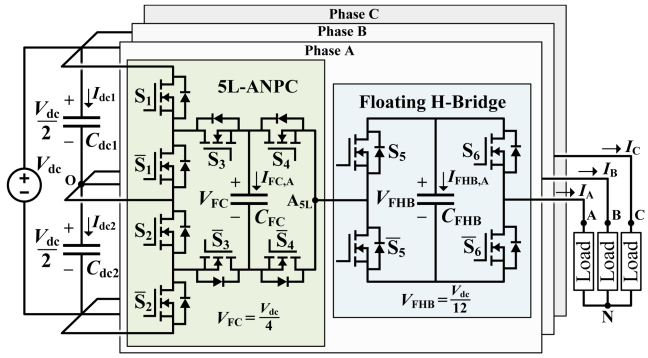

Fig. 1. Power circuit topology of the proposed 13L-ANPC.

TABLE I
Switching States of 5L-ANPC Stage of Phase Leg X

$S_{5\text{L-ANPC},X}$	$V_{X5\text{L}O}$	Switch states S_1	S_2	S_3	S_4	Capacitor current I_{dc1}	I_{dc2}	$I_{FC,X}$	Period used
-1	$-V_{dc}/2$	0	0	0	0	0	$+I_X$	0	$V_{XN} \leq 0$
$-½$	$-V_{dc}/4$	0	0	1	0	0	0	$+I_X$	$V_{XN} \leq 0$
$-½$	$-V_{dc}/4$	0	0	0	1	0	$+I_X$	$-I_X$	$V_{XN} \leq 0$
0	0	0	0	1	1	0	0	0	$V_{XN} \leq 0$
0	0	1	1	0	0	0	0	0	$0 \leq V_{XN}$
$+½$	$V_{dc}/4$	1	1	1	0	$-I_X$	0	$+I_X$	$0 \leq V_{XN}$
$+½$	$V_{dc}/4$	1	1	0	1	0	0	$-I_X$	$0 \leq V_{XN}$
$+1$	$V_{dc}/2$	1	1	1	1	$-I_X$	0	0	$0 \leq V_{XN}$

switching frequency to minimize losses. The 5L-ANPC stage is a hybrid combination of a 3L-ANPC converter and a 3L-FC converter. The switches selecting the dc-link capacitor (S_1 and S_2) block $V_{dc}/2$. These higher voltage blocking switches have line frequency switching, which reduces the switching loss of the converter. Therefore, the design of S_1 and S_2 should prioritize low on-resistance because switching losses will be negligible relative to conduction losses. As in a typical 5L-ANPC, the FC voltage V_{FC} is regulated to $V_{dc}/4$, thus, switches S_3 and S_4 block $V_{dc}/4$. The switching states of the 5L-ANPC stage of the converter are summarized in Table I. The table also marks the polarity of the phase output current I_X sunk by the capacitor, where X denotes separate phase legs of the converter (where $X \in \{\text{A}, \text{B}, \text{C}\}$). There are five output voltage states ($S_{5\text{L-ANPC},X}$) of the 5L-ANPC stage. Redundancies of $S_{5\text{L-ANPC},X} = 0$ enable S_1 and S_2 to be modulated at line frequency because S_1 remains on for the positive half cycle of the output voltage and S_2 remains on for the negative half cycle of the output voltage, as indicated by the "period used" column. Redundancies of $S_{5\text{L-ANPC},X} = \pm 1/2$ are used to regulate the voltage of C_{FC}. Further details regarding capacitor regulation are discussed in Section III.

The second stage of the proposed converter is a series-connected H-bridge module. The FHB capacitor (C_{FHB}) has no external power supply, similar to the FC stage. The controller regulates the capacitor voltage of the FHB stage to $V_{dc}/12$; hence, the blocking voltage of S_5 and S_6 is $V_{dc}/12$. The switching states of the FHB stage are shown in Table II. The three output voltage states of the FHB stage $S_{FHB,X}$ either bypass, add, or subtract the FHB capacitor voltage V_{FHB} to the output pole voltage V_{XO} of the proposed converter. Therefore, for each of

TABLE II
SWITCHING STATES OF FHB STAGE OF PHASE LEG X

$S_{\text{FHB},X}$	$V_{XX_{5L}}$	Switch states S_5	S_6	Capacitor current $I_{\text{FHB},X}$
−1	$-V_{\text{dc}}/12$	1	0	$+I_X$
0	0	1	1	0
0	0	0	0	0
+1	$V_{\text{dc}}/12$	0	1	$-I_X$

TABLE III
SWITCHING STATES OF PROPOSED CONVERTER OF PHASE LEG X

	Switch states						Capacitor current				Period
V_{XO}	S_1	S_2	S_3	S_4	S_5	S_6	I_{dc1}	I_{dc2}	$I_{\text{FC},X}$	$I_{\text{FHB},X}$	used
$-7V_{\text{dc}}/12$	0	0	0	0	1	0	0	$+I_X$	0	$+I_X$	$V_{XN} \le 0$
$-V_{\text{dc}}/2$	0	0	0	0	$*$	$*$	0	$+I_X$	0	0	$V_{XN} \le 0$
$-5V_{\text{dc}}/12$	0	0	0	0	0	1	0	$+I_X$	0	$-I_X$	$V_{XN} \le 0$
$-V_{\text{dc}}/3$	0	0	1	0	1	0	0	0	$+I_X$	$+I_X$	$V_{XN} \le 0$
$-V_{\text{dc}}/3$	0	0	0	1	1	0	0	$+I_X$	$-I_X$	$+I_X$	$V_{XN} \le 0$
$-V_{\text{dc}}/4$	0	0	1	0	$*$	$*$	0	0	$+I_X$	0	$V_{XN} \le 0$
$-V_{\text{dc}}/4$	0	0	0	1	$*$	$*$	0	$+I_X$	$-I_X$	0	$V_{XN} \le 0$
$-V_{\text{dc}}/6$	0	0	1	0	0	1	0	0	$+I_X$	$-I_X$	$V_{XN} \le 0$
$-V_{\text{dc}}/6$	0	0	0	1	0	1	0	$+I_X$	$-I_X$	$-I_X$	$V_{XN} \le 0$
$-V_{\text{dc}}/12$	0	0	1	1	1	0	0	0	0	$+I_X$	$V_{XN} \le 0$
0	0	0	1	1	$*$	$*$	0	0	0	0	$V_{XN} \le 0$
$+V_{\text{dc}}/12$	0	0	1	1	0	1	0	0	0	$-I_X$	$V_{XN} \le 0$
$-V_{\text{dc}}/12$	1	1	0	0	1	0	0	0	0	$+I_X$	$0 \le V_{XN}$
0	1	1	0	0	$*$	$*$	0	0	0	0	$0 \le V_{XN}$
$+V_{\text{dc}}/12$	1	1	0	0	0	1	0	0	0	$-I_X$	$0 \le V_{XN}$
$+V_{\text{dc}}/6$	1	1	1	0	1	0	$+I_X$	0	$+I_X$	$+I_X$	$0 \le V_{XN}$
$+V_{\text{dc}}/6$	1	1	0	1	1	0	0	0	$-I_X$	$+I_X$	$0 \le V_{XN}$
$+V_{\text{dc}}/4$	1	1	1	0	$*$	$*$	$+I_X$	0	$+I_X$	0	$0 \le V_{XN}$
$+V_{\text{dc}}/4$	1	1	0	1	$*$	$*$	0	0	$-I_X$	0	$0 \le V_{XN}$
$+V_{\text{dc}}/3$	1	1	1	0	0	1	$+I_X$	0	$+I_X$	$-I_X$	$0 \le V_{XN}$
$+V_{\text{dc}}/3$	1	1	0	1	0	1	0	0	$-I_X$	$-I_X$	$0 \le V_{XN}$
$+5V_{\text{dc}}/12$	1	1	1	1	1	0	$+I_X$	0	0	$+I_X$	$0 \le V_{XN}$
$+V_{\text{dc}}/2$	1	1	1	1	$*$	$*$	$+I_X$	0	0	0	$0 \le V_{XN}$
$+7V_{\text{dc}}/12$	1	1	1	1	0	1	$+I_X$	0	0	$-I_X$	$0 \le V_{XN}$

the five voltage levels of the first stage of the proposed converter, an additional two voltage levels can be generated, creating 15 distinct voltage levels.

The output pole voltage levels of the proposed converter are shown in Table III. The symbol $*$ marks that the FHB stage bypasses, i.e., S_5 and S_6, are either both on or both off. Note that there are insufficient redundancies in the pole voltages to regulate the FHB capacitor; for instance, for $V_{XO} = -V_{\text{dc}}/3$, the FHB current is always equal to the phase output current so will continually charge if the phase current is positive and continually discharge if it is negative.

Prior works using the proposed circuit structure (5L-ANPC with a series-connected FHB) regulate the FHB stage to $V_{\text{dc}}/8$ to allow for complete per-phase redundancy when $|V_{XO}| < V_{\text{dc}}/2$, i.e., all output pole voltage, which use the FHB capacitor can either pass positive or negative phase current to the FHB capacitor. However, this will only generate 11 unique output poles voltages [15], [16], [17], [18] compared to the 15 achieved in the proposed topology.

Capacitor regulation in this work instead uses a joint-phase redundancy scheme to regulate the FHB capacitor voltage instead of per-phase redundancy, as detailed in Section III-B. Joint-phase redundancy can regulate the FHB capacitor to $V_{\text{dc}}/12$, thereby increasing the number of voltage levels and, therefore, power quality while simultaneously lowering device-blocking voltages, which decreases size and semiconductor losses as shown in Section IV-C.

The proposed converter can also generate output voltages greater than the input voltage. Specifically, the converter may output $V_{XO} = \pm 7V_{\text{dc}}/12$, as shown in Table III. These additional voltage levels are used in Section III-C to extend the linear modulation range of the converter, thus increasing the power rating of the converter.

Details regarding the modulation of the proposed converter are best explained using space vector structures (SVSs); therefore, in the following section, the generation of the SVS for the proposed converters is described.

B. SVS Generation

It can be seen from Table I that the 5L-ANPC stage generates five distinct voltage levels across nodes $X_{5\text{L}}$ and O ($V_{X_{5\text{L}}\text{O}}$) marked in Fig. 1. These five distinct voltages with a resolution of $V_{\text{dc}}/4$ will result in the generation of a 5L hexagonal SVS of circumradius V_{dc} and a resolution of $V_{\text{dc}}/4$. For all the nonzero distinct voltage levels in $V_{X_{5\text{L}}\text{O}}$, there is at least one redundancy that draws power from the dc-link, as shown by the dc-link capacitor current in Table I. This ensures that active power can be drawn from the dc source for any active space vector (SV) location in the 5L SVS. Using this feature, the 5L-ANPC stage generates the fundamental component of the output waveform, which is responsible for the active power delivered to the load. Thus, the FHB stage only provides reactive power and increases the converter output power quality without relying on isolated supplies, which would otherwise increase converter cost, losses, and size.

The proposed 13-level SVS is obtained by the superposition of the 5L SVS of circumradius V_{dc} generated by the ANPC stage and the SVS of the FHB stage, as shown in Fig. 2. The FHB stage generates 3-level hexagonal SVS of circumradius $V_{\text{dc}}/6$ and a resolution of $V_{\text{dc}}/12$ using the three distinct voltage levels across voltage nodes V_X and $V_{X_{5\text{L}}}$, as shown in Table II. Assuming stiff regulation of the capacitor voltages, the output voltage of the converter in the stationary orthogonal reference frame ($\alpha\beta\gamma$) used for SV analysis can be written as in (1). Here, $S_{\text{5L-ANPC},X}$ and $S_{\text{FHB},X}$ are the switching states of the 5L-ANPC stage and the FHB stage, as shown in Tables I and II, respectively. Similar to the superposition technique used in linear circuits, to independently analyze the SV generated by one stage, the switching states of the other stages are forced to zero. That is, if 5L-ANPC SV is being analyzed, $S_{\text{FHB},X}$ ($X \in \{\text{A}, \text{B}, \text{C}\}$) is substituted as zero in (1)

$$\begin{bmatrix} V_{\alpha_{\text{out}}} \\ V_{\beta_{\text{out}}} \\ V_{\gamma_{\text{out}}} \end{bmatrix} = \frac{V_{\text{dc}}}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & \frac{1}{6} & -\frac{1}{12} & -\frac{1}{12} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 & \frac{\sqrt{3}}{12} & -\frac{\sqrt{3}}{12} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{12} & \frac{1}{12} & \frac{1}{12} \end{bmatrix} \begin{bmatrix} S_{\text{5L-ANPC},A} \\ S_{\text{5L-ANPC},B} \\ S_{\text{5L-ANPC},C} \\ S_{\text{FHB},A} \\ S_{\text{FHB},B} \\ S_{\text{FHB},C} \end{bmatrix}. \tag{1}$$

TABLE IV
5L-ANPC STAGE STATES FOR THE SVS SHOWN IN FIG. 2(A)

	0	**1_1**	**1_2**	**2_1**	**2_2**	**3_1**	**3_2**	**3_3**	**4_1**	**4_2**	**4_3**	**5_1**	**5_2**	**5_3**	**6_1**	**6_2**	**7_1**	**7_2**	**8_1**	**8_2**	**9_1**	**9_2**	**10**	**11**	**12**	**13**	**14**
$S_{5\text{L-ANPC,A}}$	0	+½	0	0	+½	+½	+1	0	+½	+1	0	0	+½	+1	+½	+1	+½	+1	+½	+1	+½	+1	+1	+1	+1	+1	+1
$S_{5\text{L-ANPC,B}}$	0	0	−½	0	+½	0	+½	−½	−½	0	−1	0	+½	+1	−½	0	0	+½	−1	−½	+½	+1	0	−½	+½	−1	+1
$S_{5\text{L-ANPC,C}}$	0	0	−½	−½	0	−½	0	−1	−½	0	−1	−1	−½	0	−1	−½	−1	−½	−1	−½	−1	−½	−1	−1	−1	−1	−1

TABLE V
FHB STAGE STATES FOR THE SVS SHOWN IN FIG. 2(B)

	a_1	**a_2**	**a_3**	**b_1**	**b_2**	**c_1**	**c_2**	**d_1**	**d_2**	**e_1**	**e_2**	**f_1**	**f_2**	**g_1**	**g_2**	**h**	**i**	**j**	**k**	**l**	**m**	**n**	**o**	**p**	**q**	**r**	**s**
$S_{\text{FHB,A}}$	0	−1	+1	+1	0	0	+1	−1	0	−1	0	0	−1	0	+1	+1	0	−1	−1	0	+1	+1	+1	−1	−1	−1	+1
$S_{\text{FHB,B}}$	0	−1	+1	0	−1	0	+1	0	+1	0	+1	0	−1	−1	0	0	+1	+1	0	−1	−1	−1	+1	+1	+1	−1	−1
$S_{\text{FHB,C}}$	0	−1	+1	0	−1	−1	0	−1	0	0	+1	+1	0	0	+1	−1	−1	0	+1	+1	0	−1	−1	−1	+1	+1	+1

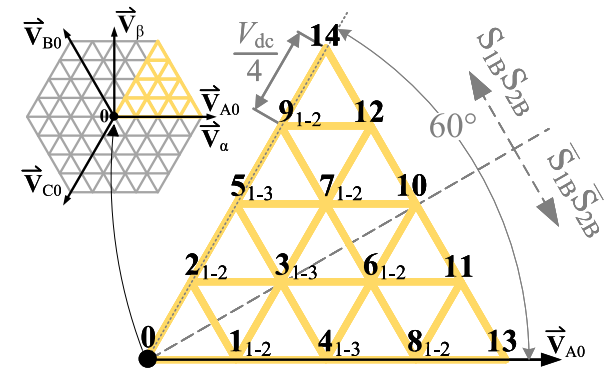

Fig. 2. Derivation of the SVS for the proposed 13L-ANPC. (a) 5L-ANPC SVS. (b) Resultant SVS by the addition of the FHB SVS to the 5L-ANPC SVS.

Fig. 2(a) shows the SVS for the 5L-ANPC stage of the converter, notated with $\vec{0}$–$\vec{14}$ for the possible output vectors within the first sector of the SVS, i.e., in the first 60° of the output waveform. Due to three-phase and half-wave symmetry, this sector is representative of the other sectors. Table IV shows the output states of the 5L-ANPC to achieve these vectors, with joint-phase redundancies shown using subscripts. In addition to the per-phase redundancies (see Table I), there are more redundancies for the same SV using joint-phase redundancy (shown in Table IV). These additional redundancies are used in Section III-D to balance the midpoint of the dc-link.

Similarly, Fig. 2(b) shows the SVS of the FHB stage, with the SVs notated with $\vec{a}$–$\vec{s}$. Table V summarizes the corresponding switching states of the FHB stage, with FHB stage joint-phase redundancies marked with subscripts, i.e., $\vec{b}_1$ and $\vec{b}_2$ generate the same SV point, however, have different pole voltages and common mode voltage. In the FHB stage SVS, the zero vector ($\vec{a}$) has three redundancies, the short vectors of magnitude $V_{dc}/12$ ($\vec{b}$–$\vec{g}$) have two redundancies each, and both the intermediate of magnitude $\sqrt{3}V_{dc}/12$ ($\vec{h}$–$\vec{m}$) and long vectors of magnitude $V_{dc}/6$ ($\vec{n}$–$\vec{s}$) do not have redundancies.

In Fig. 2(b), the SVS of the FHB stage is superimposed onto the first sector of the 5L-ANPC SVS, thus creating the SVS for the first sector of the proposed 13L-ANPC converter. It can be seen from the resultant SVS obtained from superposition that there are additional overlaps of SV locations, leading to increased redundancies to obtain the same output voltage.

The overlapping SV points shown in Fig. 2(b) from the superposition of the 5L-ANPC SVS and FHB SVS enable the FHB to be balanced to $V_{dc}/12$ on a high-frequency basis. Without these joint-phase overlaps, the FHB could not be regulated to $V_{dc}/12$. By achieving an FHB voltage $V_{dc}/12$ rather than the traditional $V_{dc}/8$ value, the circuit configuration is improved by increasing the number of output levels for the same number of switches, which increases power quality, while in the meantime reducing the FHB capacitor and switch voltage ratings, thus increasing power density and reducing cost. The specifics of how the SVS overlaps enable $V_{dc}/12$ FHB capacitor regulation are discussed in the next section.

III. CAPACITOR REGULATION

Proper operation of the proposed 13L-ANPC hybrid converter relies on regulating the capacitors in the power circuit without the use of external power supplies. The capacitors in the topology can be grouped into three types based on their position on the power circuit, namely: the FC capacitors (C_{FC}), the dc-link midpoint forming capacitors (C_{dc1} and C_{dc2}), and the FHB capacitors (C_{FHB}). First, in Section III-A, the regulation of the FC voltages and midpoint voltage (i.e., dc-link capacitor voltages) is discussed. The discussion regarding FHB capacitor regulation is split into two sections; Section III-B, discusses the joint-phase redundancy regulation of the FHB capacitor to $V_{dc}/12$ in the typical modulation range when $M \leq 1.154$. Section III-C then

covers FHB capacitor regulation in the extended modulation range.

A. Balancing of 5L-ANPC Stage Capacitors

Regulation of C_{FC} capacitor to $V_{\text{dc}}/4$ voltage using per-phase redundancy balancing can be found throughout literature [11], [30], [31]. In summary of the approach, V_{FC} is regulated by selecting between the two redundancies available whenever the FC is in the conduction path (i.e. $S_{\text{5L-ANPC},X} = \pm 1/2$), e.g., redundancies in $S_{\text{5L-ANPC},X} = 1/2$ takes opposing currents through the FC capacitor per Table I. If the phase X FC capacitor (where $X \in \{\text{A}, \text{B}, \text{C}\}$) is overcharged and phase current I_X is positive, the redundancy where $I_{\text{FC},X} = -I_X$ is selected. This will result in a negative current flowing through $C_{\text{FC},X}$, leading to a reduction in the overcharged capacitor voltage. This is similarly the case where $S_{\text{5L-ANPC},X} = -1/2$. States $S_{\text{5L-ANPC},X} = \{-1, 0, \text{or } 1\}$ leave V_{FC} undisturbed, therefore, neither impacts nor is impacted by FC regulation. Therefore, per-phase redundancies in the 5L-ANPC enable high-frequency regulation of the FC voltage, regardless of the output voltage of the proposed converter, thus keeping the required FC capacitance to a minimum.

The worst-case FC capacitor ripple is, thus, determined by FC capacitance, maximum output current I_{pk} and the longest duration between converter switching state changes, i.e., the entirety of a switching period T_{sw}, as shown in the following equation:

$$\left| V_{\text{FC}} - \frac{V_{\text{dc}}}{4} \right| < \frac{T_{\text{sw}} I_{\text{pk}}}{C_{\text{FC}}}. \tag{2}$$

The midpoint voltage of the 5L-ANPC stage must also be regulated to ensure proper output voltage and power quality. Regulation of the midpoint voltage of the proposed topology uses common-mode voltage as the per-phase redundancies shown in Table I are used to regulate the FC and to line-frequency modulate S_1 and S_2, similar to 3L-ANPC and 5L-ANPC converter [12], [32]. The available redundancies are used to regulate the midpoint voltage because the current is drawn from the dc-link capacitors based on $S_{\text{5L-ANPC},X}$, as marked in Table I. The regulation of the dc-link midpoint voltage is dependent on the regulation action of the FC capacitor because dc-link capacitor current draw depends on the per-phase redundancy used in the $S_{\text{5L-ANPC},X} = \pm 1/2$ output state. Section III-D discusses the method to manage this. The selection of dc-link capacitance in the proposed converter is the same as in other neutral-point-clamped topologies [3].

B. Regulation of V_{FHB} in the Typical Modulation Region

The charge balancing of C_{FHB} is analyzed for SV points $\vec{V_{\text{ex.1}}}$–$\vec{V_{\text{ex.7}}}$ in Fig. 2(b) describes the balancing of FHB capacitor using joint-phase redundancies. The abovementioned example SV points cover all the possible scenarios for balancing of FHB capacitor in the entire resultant SVS. For a nominal voltage of $V_{\text{dc}}/12$ in the FHB stage, every SV point within the hexagon of circumradius V_{dc} there exists at least 3 joint-phase redundancy (see $\vec{V_{\text{ex.1}}}$–$\vec{V_{\text{ex.3}}}$ in Fig. 2(b), and will be explained in-depth in this section). This region of operation is referred to as the "typical modulation region," as this is the modulation region for a conventional 3-phase inverter without boosting capabilities, such as 3L-ANPC or 5L-ANPC. The typical linear modulation limit is $M = 1.154$, or equivalently $|\vec{V}^{\alpha\beta}| = 0.866 V_{\text{dc}}$ if the magnitudes of the modulation index M and desired SV voltage $\vec{V}^{\alpha\beta}$ have magnitudes according to the following equation:

$$\frac{1}{2} V_{\text{dc}} M = \frac{2}{3} |\vec{V}^{\alpha\beta}| = |V_{X\text{N}}|. \tag{3}$$

For any SV point outside the normal modulation region, i.e., SV points outside the hexagon of circumradius V_{dc}, the joint-phase redundancies reduce to two or fewer [see $\vec{V_{\text{ex.4}}}$–$\vec{V_{\text{ex.7}}}$ in Fig. 2(b)]. This region is referred to as the "extended modulation region" as this region is obtained by additional levels above $V_{\text{dc}}/2$ obtained from the FHB stage. The extended modulation region is discussed in Section III-C.

SV points within the typical modulation region have three joint-phase redundancies and are the same, in principle, as either of the example vectors $\vec{V_{\text{ex.1}}}$–$\vec{V_{\text{ex.3}}}$ in Fig. 2(b). Specifically, each SV point obtains its three redundancies as follows.

1) As in $\vec{V_{\text{ex.1}}}$, where a single SV from 5L-ANPC SVS is used along with either of the three zero vectors from the FHB SVS; i.e., vectors $\vec{a_1}$–$\vec{a_3}$. For $\vec{V_{\text{ex.1}}}$, $\vec{7_1}$–$\vec{7_2}$ is used along with vectors $\vec{a_1}$–$\vec{a_3}$.
2) As in $\vec{V_{\text{ex.2}}}$, where either an SV from 5L-ANPC SVS is used with either of the two short redundant vectors of the FHB stage; i.e., vectors $\vec{b_1}, \vec{b_2}$ or $\vec{c_1}, \vec{c_2}$ ... or $\vec{g_1}, \vec{g_2}$; or a different SV from 5L-ANPC SVS is used with a long vector of the FHB stage; i.e., vectors $\vec{n}$–$\vec{s}$. For $\vec{V_{\text{ex.2}}}$, $\vec{7_1}$–$\vec{7_2}$ is used along with either $\vec{c_1}$ or $\vec{c_2}$, or $\vec{12}$ is used along with $\vec{r}$.
3) As in $\vec{V_{\text{ex.3}}}$, where three different SV from 5L-ANPC SVS is used along with three different intermediate magnitude vectors of the FHB stage; i.e., vectors $\vec{h}$–$\vec{m}$. For $\vec{V_{\text{ex.3}}}$, $\vec{7_1}$–$\vec{7_2}$ is used along with $\vec{h}$, $\vec{12}$ is used along with $\vec{l}$, and vector $\vec{10}$ is used along with $\vec{j}$.

The capability of each of the abovementioned SV points to be balanced can be represented by finding the natural-number ($\mathbb{N}$) nullspace of the matrix containing the redundant switching states (RSSs) (A_V, formed from the columns of Table V) of a desired output vector $\vec{V}$ [e.g., $\vec{V_{\text{ex.1}}}$ in Fig. 2(b)]. This nullspace solution represents the different ways the redundancies may be used that have a net-zero effect on capacitor voltage. This will be apparent when applied to the example vectors $\vec{V_{\text{ex.1}}}$–$\vec{V_{\text{ex.3}}}$ marked in Fig. 2(b). The $\mathbb{N}$ nullspace approach is mathematically shown as

$$\text{Null}(A_V^{\text{T}}) = \left\{ \vec{x}_V \in \mathbb{N}^n \middle| A_V^{\text{T}} \tilde{x}_V = \tilde{0} \right\} \tag{4}$$

where $\vec{x}_V$ is a vector making up the nullspace, i.e., a solution to modulate the proposed topology. Each $\vec{x}_V$ is in $\mathbb{N}^n$ space due to n redundant vectors. Strictly, there is always the trivial zero solution to the nullspace; however, in this application, the zero solution, i.e., $\vec{x}_V = \vec{0}$, is ignored. It is sufficient to find one nonzero $\vec{x}_V$ for each vector point to prove that the capacitors may be regulated on a switching-frequency basis.

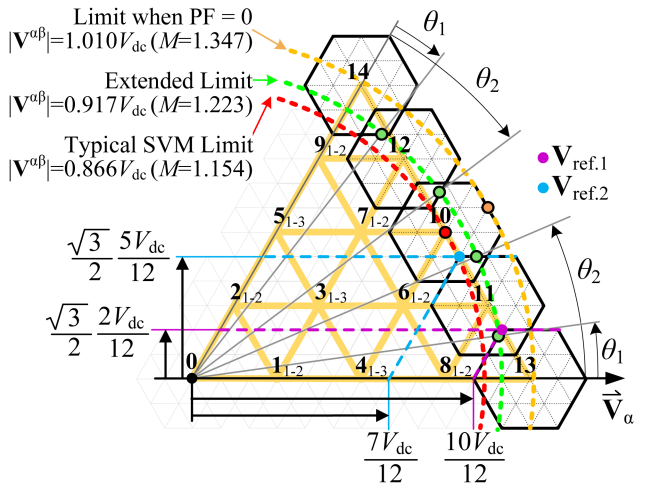

Fig. 3. SVS of the proposed 13L converter, showing typical SVM limit ($M = 1.154$), the derivation of extended linear modulation limit ($M = 1.223$) based on additional levels generated by the FHB stage, and the maximum modulation limit ($M = 1.347$) when the power factor is zero.

Vector $\vec{V_{ex.1}}$ can be achieved with redundant vectors $\vec{a_1}$ to $\vec{a_3}$ of the FHB stage. Therefore, as seen from (5), a solution to maintain capacitor voltage is to exclusively use the noncharging state ($\vec{a_1}$) and not to apply states $\vec{a_2}$ and $\vec{a_3}$. Alternatively, states $\vec{a_2}$ and $\vec{a_3}$ may be used alternating to maintain a net-zero change in capacitor voltages

$$A_{V_{ex.1}} = \begin{bmatrix} \tilde{a_1} \\ \tilde{a_2} \\ \tilde{a_3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & -1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \Rightarrow \vec{x}_{V_{ex.1}} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix}. \tag{5}$$

Balancing at $\vec{V_{ex.2}}$ is achieved with redundant vectors $\vec{c_1}$, $\vec{c_2}$, and $\vec{r}$ of the FHB stage. If each of these states is used an equal number of times, then a net-zero capacitor change can be maintained

$$A_{V_{ex.2}} = \begin{bmatrix} \tilde{c_1} \\ \tilde{c_2} \\ \tilde{r} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1 \\ 1 & 1 & 0 \\ -1 & -1 & 1 \end{bmatrix} \Rightarrow \vec{x}_{V_{ex.2}} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}. \tag{6}$$

Similarly, balancing at $\vec{V_{ex.3}}$ is achieved with redundant vectors $\vec{h}$, $\vec{l}$, and $\vec{j}$ of the FHB stage. Also, in this case, if each state is used an equal number of times, then a net-zero capacitor charge can be maintained

$$A_{V_{ex.3}} = \begin{bmatrix} \tilde{h} \\ \tilde{l} \\ \tilde{j} \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ 0 & -1 & 1 \\ -1 & 1 & 0 \end{bmatrix} \Rightarrow \vec{x}_{V_{ex.3}} = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}. \tag{7}$$

This analysis shows that the FHB capacitors can be regulated to $V_{dc}/12$ on a switching-frequency basis. In summary, the example vectors $V_{ex.1}$–$V_{ex.3}$, which are representative of the entire normal modulation region, are shown to offer sufficient joint-phase redundancies to control the polarity of FHB capacitor current, thus keeping the FHB capacitor voltage regulated to $V_{dc}/12$. A further implication of this analysis is that worst-case capacitor voltage deviation would occur only for one switching cycle; specifically, if the capacitor were initially at its nominal value, the output current is at its peak value I_{pk}, and the duty cycle is such that one state is used for the entire switching period T_{sw}. The worst-case FHB capacitor error is shown in (8). This is the worst-case value because, in practice, depending on the power factor and modulation index, the ripple will be lower than this worst-case value

$$\left| V_{FHB} - \frac{V_{dc}}{12} \right| < \frac{T_{sw} I_{pk}}{C_{FHB}}. \tag{8}$$

C. Regulation of V_{FHB} in the Extended Modulation Region

Topologies with series-connected stages can produce extended pole voltages beyond that possible with the base stage alone [33], [34] thereby enabling operation in the extended modulation region and, therefore, increased linear modulations, i.e., $M > 1.154$. When an external power source supplies these series-connected stages, operation in this extended modulation range is only limited by the maximum output voltage that can be established [23]. However, in the proposed topology, the series-connected stage is not supplied by an external supply so operation in the extended modulation range is more nuanced [35], [36].

Vectors $\vec{V_{ex.4}}$–$\vec{V_{ex.7}}$ marked in Fig. 2(b) exemplify the vectors found in the proposed 13L-ANPC hybrid that are due to the boosting capability of the topology and, hence, reside outside the typical modulation region. In these cases, there are insufficient per-phase and joint-phase redundancies to regulate the FHB capacitors, i.e., no nonzero solutions exist to (4). Thus, when operating in the extended modulation range, the capacitor charge balancing must occur on a line-frequency basis instead of the switching-frequency basis achieved in the typical modulation region.

The extended linear modulation range of the proposed converter is limited by two factors. First, all output real power must be supplied by the 5L-ANPC stage of the converter because the FHB does not include an isolated supply and thus can only supply reactive power. Second, linear modulation must be preserved to maintain power quality performance. Thus, due to the power constraint, the extended modulation limit for an arbitrary power factor is limited by the unity power factor case due to the power constraint.

Maximum output power of the 5L-ANPC is achieved by selecting the highest magnitude 5L-ANPC SV [see Fig. 2(a)] for any joint-phase redundancies in the 13L-ANPC [see Fig. 2(b)]. For example, to modulate $V_{ex.4}$ in Fig. 2(b), redundancy $\vec{12}$ from the 5L-ANPC and $\vec{m}$ from the FHB should be used rather than $\vec{10}$ from the 5L-ANPC and $\vec{i}$ from the FHB because the magnitude of $\vec{12}$ is greater than $\vec{10}$ for the 5L-ANPC stage, therefore, more power will be supplied by the 5L-ANPC stage. The resulting maximum fundamental output of the 5L-ANPC stage ($\vec{V}^{\alpha\beta,\max}_{5L\text{-}ANPC}$) is a staircase waveform, as mathematically shown in (9). Due to three-phase and quarter-wave symmetries, only two firing angles, θ_1 and θ_2, are required to define this waveform. Fig. 3

shows the definitions of θ_1 and θ_2

$$\vec{V}_{\text{5L-ANPC}}^{\alpha\beta,\max} = V_{\text{dc}} \begin{cases} 1 & -\theta_1 \le \theta < \theta_1 \\ \frac{7}{8} + j\frac{\sqrt{3}}{8} & \theta_1 \le \theta < \theta_2 \\ \frac{3}{4} + j\frac{\sqrt{3}}{4} & \theta_2 \le \theta < 60^\circ - \theta_2 \\ \frac{5}{8} + j\frac{3\sqrt{3}}{8} & 60^\circ - \theta_2 \le \theta < 60^\circ - \theta_1 \\ \frac{1}{2} + j\frac{\sqrt{3}}{2} & 60^\circ - \theta_1 \le \theta < 60^\circ + \theta_1 \\ \frac{1}{4} + j\frac{\sqrt{3}}{3} & 60^\circ + \theta_1 \le \theta < 60^\circ + \theta_2 \\ j\frac{\sqrt{3}}{2} & 60^\circ + \theta_2 \le \theta < 120^\circ - \theta_2 \\ \vdots & \vdots \end{cases}. \tag{9}$$

The values for θ_1 and θ_2 are calculated to maximize the output fundamental while preserving power quality, i.e., maintaining linear modulation. For this, the reference vectors $\vec{V}_{\text{ref.1}}$ and $\vec{V}_{\text{ref.2}}$ in Fig. 3 are used. These reference vectors represent the extrema of two 5L-ANPC output SV vector modulation ranges. For instance, $\vec{V}_{\text{ref.1}}$ is the furthest vector that can be achieved from the 5L-ANPC SV $\vec{13}$; when $\vec{V}^{\alpha\beta}$ is outside the 3-level SVS of circumradius $V_{\text{dc}}/6$ superimposed on $\vec{13}$, $\vec{13}$ cannot be used. Thus, firing angle θ_1 is calculated by the relation between $\vec{V}^{\alpha\beta}$ and $\vec{V}_{\text{ref.1}}$. If the magnitude of $\vec{V}^{\alpha\beta}$ is greater than that of $\vec{V}_{\text{ref.1}}$, then θ_1 occurs at the intersection of $\vec{V}^{\alpha\beta}(\theta)$ and a line projected 0° from $\vec{V}_{\text{ref.1}}$. Otherwise, θ_1 occurs at the intersection of $\vec{V}^{\alpha\beta}(\theta)$ and a line projected 240° from $\vec{V}_{\text{ref.1}}$. These projected lines are marked in Fig. 3. The firing angle θ_1 is, therefore, calculated as shown (10), where the magnitude of $\vec{V}_{\text{ref.1}}$ is calculated as in (11)

$$\theta_1 = \begin{cases} \text{asin}\left(\frac{2}{12}\frac{\sqrt{3}}{2}\frac{V_{\text{dc}}}{|\vec{V}^{\alpha\beta}|}\right) & |\vec{V}^{\alpha\beta}| \ge \left|\vec{V}_{\text{ref.1}}\right| \\ \text{acos}\left(\frac{10}{12}\frac{\sqrt{3}}{2}\frac{V_{\text{dc}}}{|\vec{V}^{\alpha\beta}|}\right) - \frac{\pi}{6} & |\vec{V}^{\alpha\beta}| < \left|\vec{V}_{\text{ref.1}}\right| \end{cases} \tag{10}$$

$$\left|\vec{V}_{\text{ref.1}}\right| = \sqrt{\left(\frac{2}{12}\frac{\sqrt{3}}{2}V_{\text{dc}}\right)^2 + \left(\frac{11}{12}V_{\text{dc}}\right)^2}. \tag{11}$$

The calculation of θ_2 is similar to θ_1. Using the intersection between $\vec{V}^{\alpha\beta}(\theta)$ and the same projections (0° and 240°) from $\vec{V}_{\text{ref.2}}$, θ_2 can be calculated according to (12) and (13)

$$\theta_2 = \begin{cases} \text{asin}\left(\frac{5}{12}\frac{\sqrt{3}}{2}\frac{V_{\text{dc}}}{|\vec{V}^{\alpha\beta}|}\right) & |\vec{V}^{\alpha\beta}| \ge \left|\vec{V}_{\text{ref.2}}\right| \\ \text{acos}\left(\frac{7}{12}\frac{\sqrt{3}}{2}\frac{V_{\text{dc}}}{|\vec{V}^{\alpha\beta}|}\right) - \frac{\pi}{6} & |\vec{V}^{\alpha\beta}| < \left|\vec{V}_{\text{ref.2}}\right| \end{cases} \tag{12}$$

$$\left|\vec{V}_{\text{ref.2}}\right| = \sqrt{\left(\frac{5}{12}\frac{\sqrt{3}}{2}V_{\text{dc}}\right)^2 + \left(\frac{19}{24}V_{\text{dc}}\right)^2}. \tag{13}$$

Next, the power constraint of the FHB stage is applied by ensuring the 5L-ANPC stage can provide the entire fundamental output component so the FHB stage supplies only reactive power. The actual output magnitude of the 5L-ANPC stage can be reduced by changing the values of θ_1 and θ_2 or by modulating between 5L-ANPC vectors rather than using a staircase waveform used in (9). Thus, if the maximum output of the 5L-ANPC stage $\vec{V}_{\text{5L-ANPC}}^{\alpha\beta,\max}$ meets the constraint shown in (14), then the FHB stage is not required to provide real power. The fundamental magnitude of $\vec{V}_{\text{5L-ANPC}}^{\alpha\beta,\max}$ is calculated from the first coefficient of the Fourier series, as shown in (15). Recall that θ_1 and θ_2 are functions of $|\vec{V}^{\alpha\beta}|$ and, subsequently, $\vec{V}_{\text{5L-ANPC}}^{\alpha\beta,\max}$ is a function of $|\vec{V}^{\alpha\beta}|$. Therefore, the maximum output fundamental may be calculated by applying the (14) constraint to (15). The resulting magnitude is shown in (16), or equivalently $M = 1.223$ based on (3). The firing angles associated with this magnitude are $\theta_1 = 8.1^\circ$ and $\theta_2 = 23.2^\circ$ and are marked in Fig. 3. Thus, the proposed 13L-ANPC converter topology can modulate 5.9% higher than the typical linear modulation limit, regardless of power factor

$$|\vec{V}^{\alpha\beta}| \le |\vec{V}_{\text{5L-ANPC}}^{\alpha\beta,\max}| \tag{14}$$

$$|\vec{V}_{\text{5L-ANPC}}^{\alpha\beta,\max}| = |\frac{1}{2\pi}\int_0^{2\pi}\left(\Re\left\{\vec{V}_{\text{5L-ANPC}}^{\alpha\beta,\max}(\theta)\right\}e^{-j\theta}\right)d\theta| \tag{15}$$

$$|\vec{V}^{\alpha\beta}| = |\vec{V}_{\text{5L-ANPC}}^{\alpha\beta}| = 0.917V_{\text{dc}}. \tag{16}$$

Extended modulation range operation changes the dynamics of the capacitor ripple compared to operation in the typical modulation region. Primarily, capacitor ripple depends on the output frequency f rather than the switching frequency, as was the case for the typical modulation region (8). Depending on operating conditions such as output frequency and switching frequency, the capacitor ripple in the extended modulation range can be greater than the switching frequency ripple calculated in (8). The worst-case capacitor ripple in the extended modulation is shown in (17). This assumes peak current is drawn throughout the period when $\vec{V}_{\text{5L-ANPC}}^{\alpha\beta,\max} = V_{\text{dc}}$, which has the highest current for unity power factors, while simultaneously having the longest duration between firing angles, i.e., $2\theta_1$ or 16.2° when $M = 1.223$. These assumptions create a worst-case calculation because actual operating conditions such as sinusoidal current, noncontinuous FHB conduction, power factors less than unity, and lower modulation indexes will each result in a lower ripple

$$\left|V_{\text{FHB}_{\text{extended}}} - \frac{V_{\text{dc}}}{12}\right| < \frac{16.2^\circ}{360^\circ}\frac{I_{\text{pk}}}{f \cdot C_{\text{FHB}}} = \frac{0.045I_{\text{pk}}}{f \cdot C_{\text{FHB}}}. \tag{17}$$

For lower power factors, the linear modulation limit can be further extended. In the bounding case where the power factor is zero, the modulation index is limited only by maintaining linear modulation. This limit is equal to the radius of the inscribing circle of the resultant converter SVS (see Fig. 3), thus, is calculated as in (18), which is equivalently $M = 1.347$ based on (3). Hence, for a power factor of zero, the proposed converter can achieve modulations 16.7% higher than the typical modulation limit while having linear control over the modulation

$$\left|\vec{V}_{\text{PF=0}}^{\alpha\beta,\max}\right| = \left(V_{\text{dc}} + \frac{1}{6}V_{\text{dc}}\right)\cos\left(\frac{\pi}{6}\right) = 1.010V_{\text{dc}}. \tag{18}$$

D. Control Implementation

The control implementation of the proposed topology uses space vector modulation (SVM) due to its reliance on joint-phase redundancies to regulate the converter's FHB and dc-link midpoint voltages. The SVM algorithm selects the SV points and dwell times to create the desired switching period-averaged SV output. SV selection and dwell time calculations are not specific to this multilevel topology and, thus, can be found in

other texts [37], [38]. Once the required SV points and dwell times are selected, specific switching states that create those SV points must be selected.

Finite control set model predictive control (FCS-MPC) [19], [20], [21], [22] is used to select between the available redundant options. In this technique, first, all available RSS that achieve the desired SV point are calculated from (1) and Table III for joint-phase and per-phase RSS, respectively. Next, the predicted effect of the RSS choice is calculated based on the present and predicted states of the converter (e.g., capacitor voltage, output current). For instance, capacitor voltages are predicted by extrapolating capacitor voltage from their value at the start of the SVM dwell period to the end of the SVM dwell period. Similar predictions are included for any other characteristics used to calculate MPC costs. Then, the score of each RSS choice is calculated based on the predictions of the system states. The RSS with the lowest cost is selected.

The cost function (J) used for the FCS-MPC includes weights (λ) for several predicted performance attributes (19)–(23). The predicted capacitor voltage error is the most heavily weighted performance metric for the proposed topology, as it is critical to the operation of the converter. Additional costs are also included in the FCS-MPC calculation to improve other performance metrics, specifically reducing switching loss and limiting common mode stresses. These additional costs may be readily included in the cost calculation by ignoring predicted FHB capacitor error if it is acceptably low (i.e., using a deadband region). A further advantage of FCS-MPC for this application is that the extended modulation range requires no additional control design. The cost function (19), includes costs for midpoint error J_{NP}, common mode voltage, and for each phase, FHB capacitor voltage error J_{FHB}, FC capacitor voltage error J_{FC}, and switching loss J_{loss}. For voltage errors costs (20)–(22), a deadband voltage (V_{db}) is used to ignore low errors in the predicted voltage, where predictions are denoted with a prime symbol $'$, for example V'_{FHB_X} is the predicted FHB capacitor voltage of phase X (where $X \in \{\mathrm{A},\mathrm{B},\mathrm{C}\}$). The costs related to capacitor voltage errors are squared in (19) to further prioritize capacitors with the most significant error. The common mode voltage stress cost, i.e., $\lambda_\gamma V'_{\gamma_{\mathrm{out}}}$ in (19), is a linear relationship with the γ-axis term of (1). The switching loss cost (23) is proportional to the estimated switching energy of each high-frequency modulating switch, where n denotes a given switch (see Fig. 1), $S_{S_{n,X}}$ and $S'_{S_{n,X}}$ are, respectively, the previous and predicted switch state (either 1 or 0) of a given switch (see Table III), and $V_{S_{n,X}}$ is the blocking voltage of a given switch

$$J = \sum_{X=\mathrm{A},\mathrm{B},\mathrm{C}} \left(J^2_{\mathrm{FHB}_X} + J^2_{\mathrm{FC}_X} + J_{\mathrm{loss}_X}\right) + J^2_{\mathrm{NP}} + \lambda_\gamma V'_{\gamma_{\mathrm{out}}} \tag{19}$$

$$J_{\mathrm{FHB}_X} = \lambda_{\mathrm{FHB}} \begin{cases} 0 & |V'_{\mathrm{FHB}_X} - \frac{V_{\mathrm{dc}}}{12}| < V_{db} \\ |V'_{\mathrm{FHB}_X} - \frac{V_{\mathrm{dc}}}{12}| & \text{otherwise} \end{cases} \tag{20}$$

$$J_{\mathrm{FC}_X} = \lambda_{\mathrm{FC}} \begin{cases} 0 & |V'_{\mathrm{FC}_X} - \frac{V_{\mathrm{dc}}}{4}| < V_{db} \\ |V'_{\mathrm{FC}_X} - \frac{V_{\mathrm{dc}}}{4}| & \text{otherwise} \end{cases} \tag{21}$$

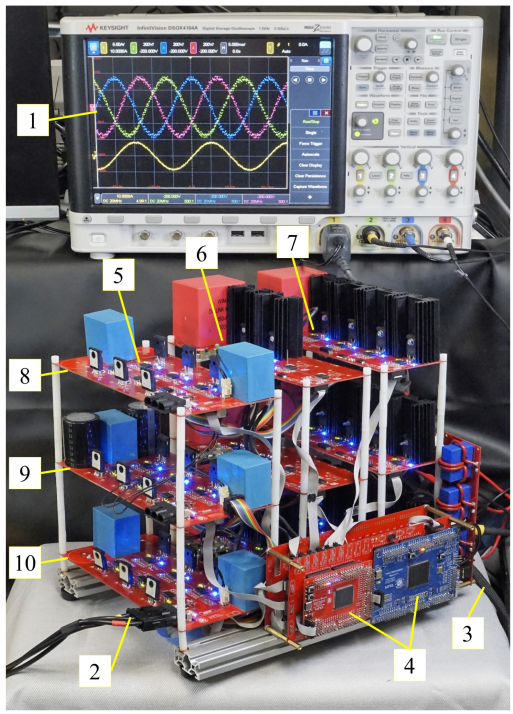

Fig. 4. Photograph of experimental setup marked with 1) output waveforms, 2) DC-connection, 3) AC-connection, 4) controllers, 5) 3L-ANPC stage, 6) FC stage, 7) FHB stage, 8) phase leg A, 9) phase leg B, and 10) phase leg C.

$$J_{\mathrm{NP}} = \lambda_{\mathrm{NP}} \begin{cases} 0 & |V'_{\mathrm{dc1}} - V'_{\mathrm{dc2}}| < V_{db} \\ |V'_{\mathrm{dc1}} - V'_{\mathrm{dc2}}| & \text{otherwise} \end{cases} \tag{22}$$

$$J_{\mathrm{loss}_X} = \lambda_{\mathrm{loss}} \sum_{n=3}^{6} \left(|I_X| V_{S_{n,X}} |S'_{S_{n,X}} - S_{S_{n,X}}|\right). \tag{23}$$

The weight selection in the proposed converter should prioritize capacitor error costs. Each weight for voltage error costs, i.e., λ_{FHB}, λ_{FC}, and λ_{NP}, are of similar magnitude. The switching loss weight λ_{loss} is then set such that J_{loss_X} is at least an order of magnitude lower than the capacitor voltage error costs. Similarly, the common mode voltage weight λ_γ is set to have J_γ an order of magnitude lower than J_{loss_X}. With this weight selection approach, the capacitor voltage balancing is prioritized whenever the predicted error is greater than the deadband voltage, otherwise, loss minimization will be prioritized, with common mode stress being a tie-breaker of similarly lossy options.

Next, in Section IV, the control principles discussed above are applied to a hardware prototype to validate and verify the proposed topology.

IV. Results and Inferences

A. Experimental Setup

Fig. 4 shows the prototype hardware for the proposed 13L-ANPC. This prototype has separate modules for the different converter stages, so can also be operated as either the proposed topology, 3L-ANPC, 5L-ANPC, or 9L-ANPC (i.e., 5L-ANPC

TABLE VI
HARDWARE PARAMETERS OF EXPERIMENTAL SETUP

Parameter	Value
DC input voltage	375 V
Nominal capacitor voltage [$C_{\rm dc}$,$C_{\rm FC}$,$C_{\rm FHB}$]	[187.5, 93.75, 31.25] V
AC load	47 Ω, Star-Connected
SVM carrier period	3 kHz
Split dc-link capacitance $C_{\rm dc}$	1.2 mF (Rating: 320 V)
FC capacitance $C_{\rm FC}$	900 µF (Rating: 160 V)
FHB capacitance $C_{\rm FHB}$	900 µF (Rating: 55 V)
Switch	UJ4C075033K4S
Gate driver	NCV5700-D
Digital signal processor	TMS320F28388S
Field-programmable gate array	LCMX02-7000HE

with a $V_{\rm dc}/4$ FHB stage). The hardware parameters and component selections for the experimental setup are summarized in Table VI. The converter uses a carrier frequency of 3 kHz, i.e., three output SVs are used every 333 μs. Based on this hardware configuration, the peak phase current is 4.61 A at the typical modulation limit ($M = 1.154$), and 4.88 A at the extended modulation limit ($M = 1.223$). According to (8) and (17), the FHB capacitor ripple expected is less than ±1.7 V for $M = 1.154$ and ±4.9 V for $M = 1.223$. The modulation and control are programmed onto the digital signal processor, and a field programmable gate array is then used to generate complementary switching signals with appropriate dead time. The capacitor regulation control is configured as discussed in Section III-D, with the costs included for capacitor voltage errors, midpoint regulation error, switching loss, and common-mode voltage stress. The implemented FCS-MPC uses a deadband voltage V_{db} of ±0.65% $V_{\rm dc}$ (±2.5 V) to allow for switching loss optimization while capacitor voltage errors are low.

B. Experimental Results

Experimental results were obtained from the prototype hardware to validate the operation of the converter. Fig. 5 shows waveforms for the proposed converter operating at the typical modulation limit, i.e., $M = 1.154$, at the rated power (1.5 kW) of this operating point.

Fig. 5(a) shows the output waveforms of the converter and validates the overall operation of the proposed topology. The line voltage (V_{AB}) shows the correct creation of the output SVs to generate high-quality output current without filtering. Fig. 5(b) demonstrates the capacitor regulation of the proposed 13L converter. The maximum capacitor ripple of the FC and FHB capacitors is ±2.5 V, consistent with the deadband voltage selection discussed in Section IV-A. Capacitors are regulated at the switching frequency, thus keeping the required capacitance low.

Experimental results shown in Fig. 5(c) verify that the proposed converter has a favorable distribution of device blocking voltages and switching frequency; $V_{\rm dc}/2$ blocking switches (S_1–S_2) switch once a line-cycle, $V_{\rm dc}/4$ blocking switches (S_3–S_4) have an average switching frequency of 500 Hz, and $V_{\rm dc}/12$ blocking switches (S_5–S_6) have an average switching frequency of 2.2 kHz. Therefore, switching losses are kept low because the higher blocking voltage switches, which have the greatest switching energies, are switched less frequently than lower blocking voltage switches.

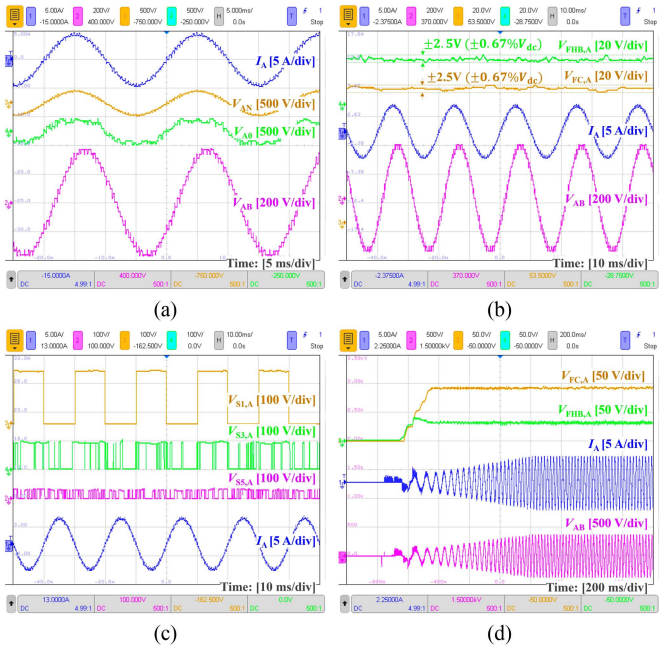

Fig. 5. Experimental waveforms for the proposed converter showing operation at the rated power of the converter within the typical modulation index ($M = 1.154$) (a) steady-state operation, (b) capacitor regulation, (c) semiconductor switching waveforms, and (d) simultaneous frequency-modulation index ramp, keeping a constant Volts/Hz ratio.

The startup and transient performance of the proposed converter is verified in Fig. 5(d). In this experiment, the floating capacitor voltages are initially zero. When the converter is turned on, the output reference is ramped from $M = 0$ to $M = 1.154$ with a constant volt-hertz ratio. Fig. 5(d) shows that before capacitor voltage regulation is complete, the waveform quality is degraded because the operation of the converter is closer to that of a 3L-ANPC converter than the proposed converter's 13-level capability; however, the floating capacitor voltages quickly arrive at their nominal values (less than 200 ms). This transient experiment verifies the proposed converter's ability to regulate capacitor voltages for any output voltage in this modulation range.

Experimental results are also taken at the maximum extended modulation range, at the rated power of this operating point (1.68 kW). Fig. 6(a) shows the increased output voltage, demonstrating that waveform quality is maintained for the higher modulation and current. The capacitor regulation at the maximum extended modulation is shown in Fig. 6(b). This shows the FHB capacitor ripple is ±3.7 V, whereas the calculated from (17) was ±4.9 V. This 24% difference is due to the worst-case assumptions of the extended modulation ripple equation, particularly due to actual operating conditions such as sinusoidal current and noncontinuous FHB conduction. The FC stage capacitor ripple remains low during this operating mode because it is still regulated at the switching frequency. This validates the operation of the proposed converter in the extended linear modulation

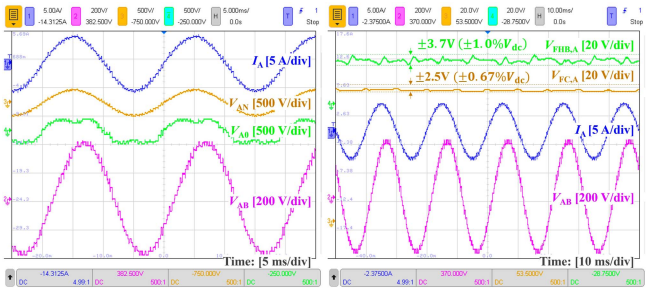

Fig. 6. Experimental waveforms for the proposed 13L-ANPC for the maximum unity power factor modulation ($M = 1.223$) for (a) output voltage and current waveforms and (b) capacitor regulation waveforms.

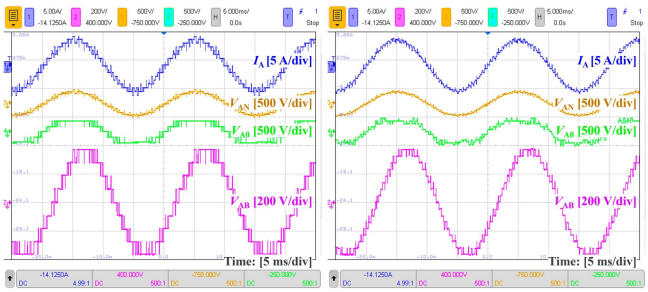

Fig. 7. Experimental output voltage and current waveforms for alternative topologies (a) 5L-ANPC [11] and (b) 9L-ANPC [13].

range, achieving 5.9% higher output voltage than a typical SV modulated converter.

Alternate ANPC converter topologies were also tested to provide a reference point for the performance of the proposed topologies. Each converter tested uses the same capacitances, carrier frequency, supply voltage, load, and control approach. The basic output waveforms for 5L-ANPC and 9L-ANPC are shown in Fig. 7 for $M = 1.154$. These experimental results are used next in Section IV-C to demonstrate the merits of the proposed topology and compare performance between the proposed topology and the reference topologies.

C. Comparison and Discussion

A comparative analysis is conducted to evaluate performance improvements of the proposed topology against the reference designs of 3L-ANPC, 5L-ANPC, and 9L-ANPC. These specific reference topologies because

1) they closely relate to the proposed topology and, therefore, can share the same design for a fair and even comparison;
2) each may be tested on the hardware setup in Section IV;
3) these topologies have been used in prior topology comparisons so serve as a common point of reference, for instance, these topologies have been variously compared with 2L converter, FCC, CHB, MMC, and other hybrid NPC variations [5], [39], [40], [41], [42], [43].

Fig. 8 compares the proposed converter to the reference converter topologies. The modulation index is swept from $M = 0.1$

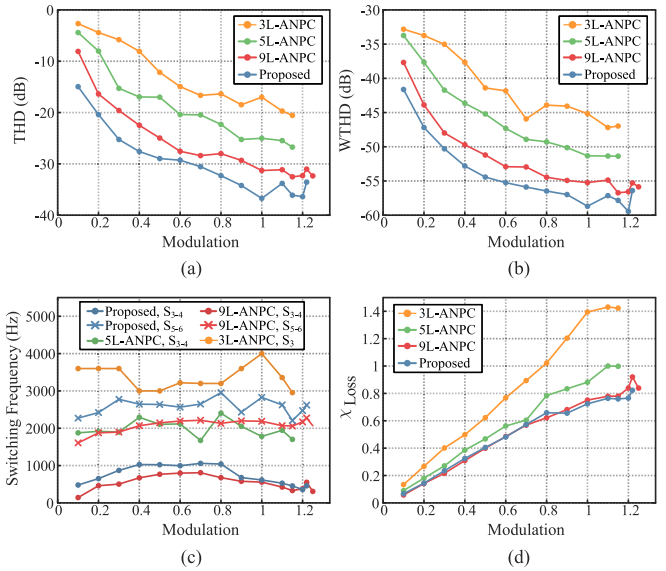

Fig. 8. Converter performance comparison of the proposed converter and alternative designs; 3L-ANPC, 5L-ANPC [11] and 9L-ANPC [13]. Performance metrics shown are (a) total distortion, (b) WTHD, (c) device switching frequencies, and (d) normalized semiconductor loss FOM.

to $M = 1.154$ for the 3L-ANPC and 5L-ANPC. The modulation is swept from $M = 0.1$ to the extended modulation limit (16) for the proposed topology. The extended modulation limit for 9L-ANPC was calculated as $M = 1.255$ using the same approach as in Section III-B. Each test has the same carrier frequency and hardware parameters listed in Table VI, apart from the elimination of components in the cases of 3L-ANPC and 5L-ANPC.

First, power quality is compared in Fig. 8(a) and (b), measured with total harmonic distortion (THD) and weighted total harmonic distortion (WTHD) of the output line voltages (24). This demonstrates the substantially improved power quality of the proposed topology compared to 9L-ANPC and other reference topologies. In addition, it demonstrates that capacitor regulation accuracy is sufficient to avoid negative impacts on waveform quality

$$\{\text{THD}, \text{WTHD}\} = \left\{ \sqrt{\sum_{n=2}^{120} \frac{V_{AB_n}^2}{V_{AB_1}^2}}, \sqrt{\sum_{n=2}^{120} \frac{V_{AB_n}^2}{nV_{AB_1}^2}} \right\}. \quad (24)$$

Fig. 8(c) shows the average device switching frequencies of the converters. Switches S_1–S_2 modulate at line frequency in each of the shown converters, so it is not shown. Relative to 5L-ANPC, the proposed converter substantially reduces the switching frequency of S_3–S_4, greatly reducing switching loss. Relative to 9L-ANPC, the proposed topology has slightly higher device switching frequencies for both converter stages. This is attributed to the 9L-ANPC converter having more redundant switching options than the proposed 13L converter, which the FCS-MPC algorithm uses to reduce switching instances without negatively impacting capacitor regulation. Although there are higher switching frequencies in the proposed converter, the FHB stage has a 33% lower voltage than the 9L-ANPC, which brings

TABLE VII
COMPARISON OF PROPOSED CONVERTER AND REFERENCE TOPOLOGIES

FOM	3L-ANPC	5L-ANPC	9L-ANPC	Proposed
Switches per phase	6	8	12	12
Switch standing voltage	$9.0V_{\rm dc}$	$9.0V_{\rm dc}$	$10.5V_{\rm dc}$	$10.0V_{\rm dc}$
Capacitor standing voltage	$1.0V_{\rm dc}$	$1.75V_{\rm dc}$	$2.125V_{\rm dc}$	$2.0V_{\rm dc}$
Total output voltage levels	3	5	11	15
Maximum modulation	1.154	1.154	1.255	1.223
THD, M=0.5 [dB]	-12	-17	-25	-29
THD, M=1.154 [dB]	-21	-27	-33	-36
Semiconductor loss, $\chi_{\rm loss}$	1.43	1.00	0.92	0.82
Total die area , $\chi_{\rm die}$	0.47	1.00	2.47	2.64
Capacitor size, $\chi_{\rm C}$	0.81	1.00	0.89	0.91
Converter cost, $\chi_{\rm cost}$	0.81	1.00	0.98	1.00
Converter volume, $\chi_{\rm vol}$	0.96	1.00	0.89	0.87

about savings in switching loss and the abovementioned power quality improvement.

Using these results, a loss figure of merit (FOM) [44] is calculated to compare the converters' semiconductor losses. The loss FOM $\chi_{\rm loss}$ shown in (25), is applied to a range of modulation indexes in Fig. 8(d). The $\chi_{\rm loss}$ is dependent on the ith device switching frequency $f_{{\rm sw}_i}$, blocking voltage V_{B_i}, and $I_{{\rm rms}_i}$, which is proportional to M due to the fixed resistive load. The device characteristics $R'_{{\rm on}_i}$ and C'_{Q_i} are based on device blocking voltage and device technology, i.e., S_1–S_2 are assumed to use silicon and the remaining switches are assumed to be silicon carbide [44]

$$\chi_{\rm loss} \propto \frac{1}{P_{\rm rated}} \sum_{i=1}^{N_{\rm sw}} 2I_{{\rm rms}_i} V_{B_i} \sqrt{f_{{\rm sw}_i} R'_{{\rm on}_i} C'_{Q_i}}. \tag{25}$$

Table VII summarizes several figures of merit (FOMs) between the proposed converter and the reference topologies. The first four FOMs relate to the circuit structure of the converters, specifically a count of semiconductor devices, the standing voltage (i.e., summation of blocking voltages) of both the switches and capacitors and the maximum number of output levels. Next, Table VII lists the maximum linear modulation limit for an arbitrary power factor, as calculated in Section III-C. The modulation limit is higher for 9L-ANPC and the proposed topology due to the series-connected FHB stage. The higher modulation limit increases the output power of the converter, assuming a constant resistive load. A series of performance-based FOMs are then shown in Table VII.

First, the THD at two operating points are shown to compare the power quality of the converters. The higher quantity of output levels in the proposed converter gives it superior power quality performance relative to the reference topologies. This power quality improvement can either reduce or eliminate output filtering or enable switching frequency reductions to reduce losses.

Next, the maximum $\chi_{\rm loss}$ from Fig. 8(d) are listed, which demonstrates the low losses of the proposed converter relative to the reference converters. The reduced losses relative to the 3L-ANPC and 5L-ANPC can be attributed to the reductions of switching frequency in higher blocking-voltage devices, i.e., S_3–S_4. The reduced losses relative to the 9L-ANPC are due to the lower FHB stage blocking voltages.

An FOM for semiconductor die area $\chi_{\rm die}$ (26) is calculated using the operating point with the maximum $\chi_{\rm loss}$ [44]. The die area FOM is proportional to the summation of the die area for each switch, scaled by the output power of the converter. This die area FOM relates to the semiconductor cost of the converter.

$$\chi_{\rm die} \propto \frac{1}{P_{\rm rated}} \sum_{i=1}^{N_{\rm sw}} 2I_{\rm rms} V_{B_i} \sqrt{\frac{R'_{{\rm on}_i}}{C'_{Q_i} f_{{\rm sw}_i}}}. \tag{26}$$

A capacitor FOM (χ_C) is used to compare floating capacitor sizes and cost. Capacitor energy density is roughly constant for a given dielectric [45]. Thus, χ_C is proportional to the total capacitor energy as in (27), where the ith capacitor has nominal voltage V_i and capacitance C_i, and $N_{\rm caps}$ is the total number of capacitors including the dc-link capacitors as well as the floating capacitors in three phases of the converter. The total capacitor energy is scaled by the output power rating of the converter. Table VII shows the results of this calculation

$$\chi_C \propto \frac{1}{P_{\rm rated}} \sum_{i=1}^{N_{\rm caps}} \frac{1}{2} C_i V_{C_i}^2. \tag{27}$$

Lastly Table VII includes a cost FOM $\chi_{\rm cost}$ and a volume FOM $\chi_{\rm vol}$ to summarize the overall design of the converters. For these FOMs, a concept inverter is designed by scaling the prototype results up to a dc voltage of 4 kV and an output power rating of 40 $A_{\rm rms}$ when $M = 1.154$. Capacitances are scaled by the required current and acceptable voltage ripple increase. Each design has an equal output frequency, dc-link capacitor size, floating capacitor size, and SVM carrier frequency. Cost and volume are calculated by summing the required components, including semiconductors, capacitors, gate-drive circuitry, and heatsinks. The semiconductor cost is scaled by the required die area using IXBH12N300 IGBT for S_1–S_2 and C2M0045170D SiC MOSFET for the remaining switches. The capacitor cost and volume are scaled by capacitor energy based on DCP4I061509JD4KSSD. The heatsink cost and volume are calculated assuming a 30° C temperature rise based on the 6400BG heatsink, scaling with constant cost per watt and constant volume per watt, and assuming 5L-ANPC achieves 99% efficiency [46], with losses of the 9L-ANPC and the proposed converter calculated based on $\chi_{\rm loss}$. The results are then scaled based on output power and normalized to the results of the 5L-ANPC.

Several conclusions regarding the proposed converter are drawn from Table VII. Primarily, the proposed converter improves power quality, efficiency, and power density relative to alternatives. These performance improvements are at the expense of semiconductor die area; however, as demonstrated by the cost FOM, the increase in semiconductor cost is outweighed by the reduced capacitor size and lower losses. Although the proposed converter requires an additional converter stage relative to the 5L-ANPC, the FHB stage is small because it requires 66% lower blocking voltage and 89% lower capacitor energy compared to the FC stage, i.e., S_3–S_4 and $C_{\rm FC}$, respectively. Furthermore, power quality improvements of the proposed converter will either reduce filtering requirements and, thus, further increase power density or switching frequency may be reduced, thereby

further increasing efficiency. Next, prior works that compare the same reference topologies are used to draw several further conclusions. First, 5L-ANPC and 9L-ANPC are shown to be more power-dense than 2L converter, FCC, and CHB [5], [39] and the 5L-ANPC was shown to be more power-dense than MMC in [8]. Thus, by extension, we may conclude that the proposed converter can achieve power densities greater than FCC, MMC, and CHB. In comparison to single dc source topologies considered in [4], the proposed topology has the fewest switches per output level and capacitors per output level.

V. Conclusion

This article introduced a novel three-phase converter scheme combining the 5L ANPC topology with a series-connected FHB to achieve a multilevel converter with 13 output voltage levels without requiring isolated sources, surpassing existing designs that typically achieve only 9Ls with a similar circuit structure. The key innovation lies in the capacitor voltage regulation approach, which employs joint-phase redundancy, enabling the FHB capacitor voltage to be regulated to one-twelfth of the total dc-link voltage on a switching frequency basis. This approach not only increases the number of output levels, which improves power quality but also increases converter power density due to the reduced-voltage FHB stage voltage. Furthermore, converter efficiency is enhanced by concentrating the highest frequency switching within this low-voltage FHB stage. Furthermore, the FHB stage was shown to enable the linear modulation limit to be extended from 1.154 to 1.223, regardless of power factor, thus enabling greater dc-link utilization. Experimental validations and analytical results demonstrated the superior performance of the proposed topology in terms of power quality, efficiency, and footprint compared to existing solutions. These findings underscore the proposed converter's potential to advance the state-of-the-art in power electronics for enhanced energy conversion systems, including motor drives, active front ends, and three-phase inverter applications.

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