Extendable Multi-Input High Step-Up DC–DC Converter for Multisource Energy Systems

Sohrab Abbasian, *Student Member, IEEE*, Homayon Soltani Gohari, Mohammad Farsijani, *Student Member, IEEE*, Sina Ahmadian, and Tomi Roinila, *Member, IEEE*

***Abstract*—Boosting the output voltage of the energy sources in a multienergy system is often a key factor in ensuring energy source compatibility, improving transmission efficiency, enabling effective power conversion, supporting energy storage, and meeting grid or system standards. This article proposes a multi-input, high step-up dc–dc converter capable of providing a regulated dc link while using different energy sources. Based on a specialized structure that employs coupled inductors (CIs) and voltage multiplier cells, the converter offers an adjustable high voltage gain. A key advantage of the converter is its scalability, which allows for the integration of multiple inputs. The soft-switching operation enhances efficiency, thereby making it suitable for a wide range of applications. The current-fed structure ensures low input current ripple, making it particularly well-suited for renewable energy applications. In addition, reduced current spikes on the switches extend their lifespan and allow for the use of more cost-effective components. The resonant operation of the primary sides of the CIs mitigates reverse recovery issues in the output diode. The operating principle of the proposed converter is analyzed in detail, and losses in different components are studied. Design considerations for the components are provided, and the proposed converter is compared with similar designs to assess its advantages and disadvantages. The proposed multiport converter is modeled, and its control system is designed. Finally, a 550-W prototype is implemented, and experimental results are presented.**

***Index Terms*—Coupled inductor (CI), dc–dc converter, high step-up, multi-input converter, soft switching.**

I. Introduction

RECENT developments in power electronics and the transition toward increased renewable energy integration have led to significant changes in energy production and utilization [1], [2]. For example, electric vehicle (EV) charging stations require the development of more efficient converters to enhance the integration of renewables into these stations. The relatively low output voltage of renewable energy sources (RESs), particularly photovoltaic (PV) panels, necessitates the use of high step-up dc–dc converters in their operation [3], [4]. These converters must maintain the required output voltage levels despite fluctuations in source voltage.

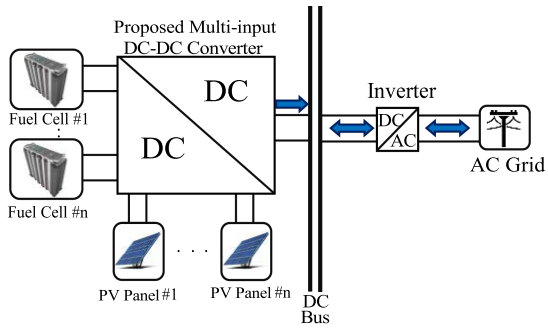

Fig. 1. Schematic of renewable energy-based EV charging station utilizing multi-input high step-up DC–DC converter.

Fig. 1 shows a schematic diagram of a distributed energy system based on PV and battery utilizing a multi-input high step-up dc–dc converter. As the figure illustrates, it is desirable to use multiple PV arrays and batteries, with each source being controlled separately. In conventional systems, a single dc–dc converter is assigned to each PV array and battery. However, modern systems utilize multi-input dc–dc converters, eliminating the need for several single input single output dc–dc converters. In addition, employing multi-input high step-up dc–dc converters simplifies the control system and enhances energy management, provided that the converter can control the inputs independently. Another key advantage of these converters is their ability to accommodate additional inputs as needed by the designer.

Nonisolated multi-input converters are favored in most multi-input systems due to their reduced size and cost. Several voltage-boosting techniques can be employed in such converters. Among these methods, utilizing coupled inductors (CIs) stands out as a simple, straightforward, and reliable approach [5], [6]. However, the most significant challenge with this method is the voltage spikes on the switches caused by the leakage inductance of the CIs. The work in [7] attempted to mitigate these voltage spikes; however, the low voltage ratio of the proposed converter remains a primary drawback.

A crucial consideration in designing converters for RESs is minimizing input current ripple. It is essential for the converter

Received 29 January 2025; revised 8 March 2025; accepted 20 March 2025. Date of publication 24 March 2025; date of current version 30 June 2025. Recommended for publication by Associate Editor M. Wang. *(Corresponding author: Sohrab Abbasian.)*

Sohrab Abbasian and Tomi Roinila are with the Faculty of Electrical Engineering, Tampere University, 33100 Tampere, Finland (e-mail: sohrab.abbasiankasehgari@tuni.fi).

Homayon Soltani Gohari is with the Faculty of Electrical Engineering, K. N. Toosi University of Technology, Tehran 19991, Iran.

Mohammad Farsijani is with the Department of Electrical and Computer Engineering, University of Illinois Chicago, Chicago, IL 60607 USA.

Sina Ahmadian is with the Faculty of Electrical Engineering, Kermanshah University of Technology, Kermanshah 67156, Iran.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3554438.

Digital Object Identifier 10.1109/TPEL.2025.3554438

to have a nonpulsating input current with minimal ripple. The converter in [8] has pulsating input current, which can negatively affect connected RESs. A multi-input high step-up converter introduced in [9] offers zero-voltage switching performance and low input current ripple, making it suitable for RESs. Nevertheless, its efficiency, reliability, cost, and volume may be compromised by the large number of components. Similarly, the multi-input converter discussed in [10] suffers from a high component count due to its cascaded structure. While the presented converter performs well in wind energy systems, its scalability and input current characteristics remain limited.

Recent advancements in bidirectional dc–dc converters have addressed some limitations of traditional unidirectional topologies. For instance, Saadatizadeh et al. [11] proposed a nonisolated bidirectional dc–dc converter with zero voltage switching capabilities, offering improved efficiency and reduced switching losses. However, this topology requires two capacitors in series at the output, necessitating careful balancing, which complicates practical implementation. Similarly, Karimi Hajiabadi et al. [12] introduced a three-port quadratic step-up dc–dc converter with high gain and continuous input current. While this design provides significant advantages in voltage gain and input current characteristics, it employs five switches, increasing system cost and complexity, and lacks the flexibility of adjustable voltage gain through CIs.

Past studies have introduced multiport converters with fewer components, but their voltage levels remain insufficient for effective deployment in renewable energy applications [13], [14].

A high voltage gain with a reasonable duty cycle is crucial for high step-up converters. Operating with a large duty cycle can lead to increased conduction losses and reduced efficiency. This issue limits the utility of the dual-input converters, as shown in [15], [16]. The dual-input dc–dc converter proposed in [1] provides high voltage gain with a low duty cycle, minimizes switch voltage spikes using a passive clamp circuit, and achieves zero current switching (ZCS) performance, along with relatively low switch voltage stress. However, it suffers from discontinuous input current, which increases ripple and reduces efficiency, particularly in PV applications. In addition, its design is limited to two input sources, making it impractical for energy systems that require greater scalability and integration of multiple sources.

To address the limitations of previously introduced converters and meet the demands of multienergy systems, this article presents a CI-based multi-input dc–dc converter with high voltage gain. The use of CIs enables a wide output voltage range, and the converter design allows for the addition of as many input sources as required, with each source being controlled independently. An inductor filter at the input ports ensures reduced input current ripple. To maximize efficiency, the converter switches operate under soft-switching conditions, while the resonant operation of the primary side of the CIs enables ZCS for the output diode. In addition, the energy stored in the leakage inductance is recycled, minimizing current spikes in the switches.

The rest of this article is organized as follows. Section II examines the operation of the proposed converter during each time interval, accompanied by the corresponding theoretical analysis. Section III addresses the study of losses in different parts of the proposed converter, providing valuable insights for heat sink design and guiding component selection. A comprehensive component design guideline is outlined in Section IV. In Section V, the proposed multi-input converter is modeled, and its control system is designed. To assess the converter's advantages and disadvantages, a comparative study is presented in Section VI, where various operational and structural factors are evaluated. Finally, Section VII presents and discusses the experimental results from a 550-W proof-of-concept.

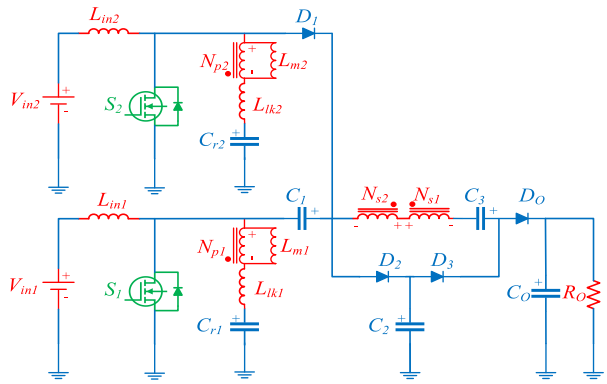

Fig. 2. Schematic of the proposed converter.

II. Proposed Converter; Operating Principles and Analysis

A. Operating Principles

The proposed converter circuit, depicted in Fig. 2, comprises two power switches (S_1, S_2), four diodes (D_1, D_2, D_3, D_O), two inductors (L_{in1} and L_{in2}), two CIs, four capacitors (C_1, C_2, C_3, C_O), and two resonant capacitors (C_{r1}, C_{r2}). The key advantage of the proposed topology is its ability to be extended to accommodate more than two inputs, as demonstrated in Fig. 3. The operation of this converter can be segmented into seven time intervals, with key waveforms shown in Fig. 4. To ensure a straightforward and comprehensible analysis, the following simplifying assumptions are adopted.

1) Ideal inductive and capacitive components: without parasitic elements.
2) Ideal switching components.
3) Negligible variations in capacitor voltages and inductor currents.
4) Continuous conduction mode.

It is important to note that the CIs are modeled using ideal transformers with parallel magnetizing inductors and series leakage inductors. The turn ratios and coupling coefficients of the ideal transformers are assumed to be "$n_i = N_{si}/N_{pi}$" and "$k = \frac{L_m}{L_m+L_k}$", respectively.

Mode 1 [see Fig. 5(a)*]*: At the beginning of this mode, S_1 is turned ON in ZCS condition facilitated by L_{in1} and L_{lk1}. Meanwhile, S_2, which was ON in the previous operating mode, remains ON. In this condition, diode D_O maintains conduction, nevertheless, its current undergoes a gradual decline with a slow decay, as depicted in Fig. 4. In addition, the output capacitor

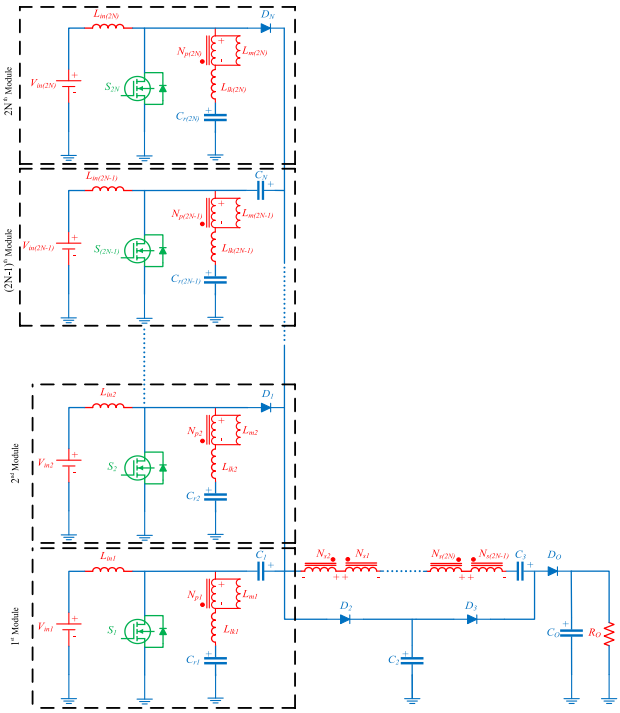

Fig. 3. Schematic of extended version of the proposed converter.

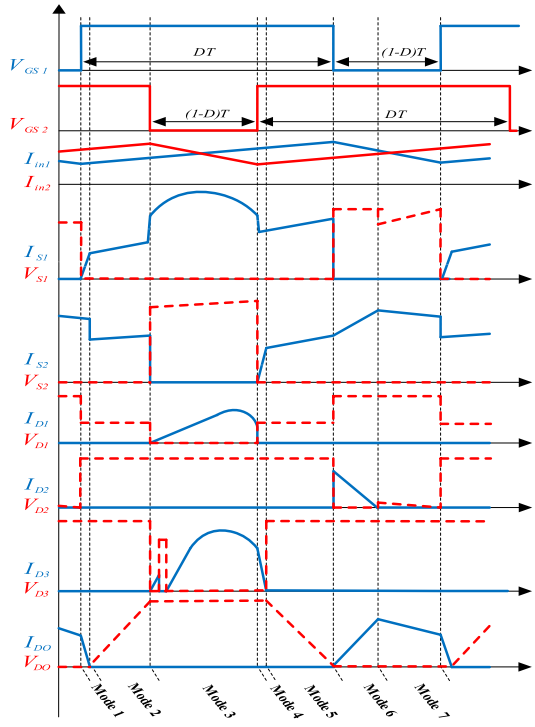

Fig. 4. Key waveforms of the proposed in each time interval.

remains charged. This short-time transient interval concludes once the magnetizing inductor L_{m1} ceases to discharge.

Mode 2 [see Fig. 5(b)*]*: In this time interval, the output diode is turned OFF under ZCS conditions, and both input inductors are charged from their respective sources. This mode behavior can be mathematically represented by the following equations:

$$V_{Lin1}^{D} = V_{in1} \tag{1}$$

$$V_{Lm1}^{D} = \left[\frac{L_{m1}}{L_{m1}+L_{k1}}\right] V_{Cr1} = kV_{Cr1} \tag{2}$$

$$V_{Lk1}^{D} = \left[\frac{L_{k1}}{L_{m1}+L_{k1}}\right] V_{Cr1} = (1-k)V_{Cr1} \tag{3}$$

$$T_{r1} = 2\pi\sqrt{L_{lk1}C_{r1}} \tag{4}$$

$$V_{Lin2}^{D} = V_{in2} \tag{5}$$

$$V_{Lm2}^{D} = \left[\frac{L_{m2}}{L_{m2}+L_{k2}}\right] V_{Cr2} = kV_{Cr2} \tag{6}$$

$$V_{Lk2}^{D} = \left[\frac{L_{k2}}{L_{m2}+L_{k2}}\right] V_{Cr2} = (1-k)V_{Cr2} \tag{7}$$

$$T_{r2} = 2\pi\sqrt{L_{lk2}C_{r2}} \tag{8}$$

$$V_{Lin2}^{D} = V_{in2}. \tag{9}$$

Mode3 [see Fig. 5(c)*]*: This mode initiates when S_2 is turned OFF, and D_1 begins conducting to suppress voltage spikes. In addition, D_3 is turned ON and its current rises gradually with a slow slope, as illustrated in Fig. 4. As a result, capacitors C_1 and C_3 are charged with the energy from L_{in2} and C_2. In this condition following equations can be written:

$$V_{Ns1}^{D} = n_1\, V_{Lm1}^{D} \tag{10}$$

$$V_{Ns2}^{D'} = n_2\, V_{Lm2}^{D'} \tag{11}$$

$$V_{Lin2}^{D'} = V_{in2} - V_{C1} \tag{12}$$

$$V_{Lm2}^{D'} = k(V_{Cr2} - V_{C1}) \tag{13}$$

$$V_{C3} = V_{C2} - V_{NS2}^{D'} + V_{NS1}^{D} - V_{C1}. \tag{14}$$

Mode 4 [see Fig. 5(d)*]*: This short-time mode corresponds to the turning ON process of S_2, which resembles mode 1. As depicted in Fig. 4, the current of S_2 gradually increases in ZCS condition due to the existence of L_{in2} and L_{lk2} in this switch current pass.

Mode 5 [see Fig. 5(e)*]*: In this time interval, which is identical to Mode 2, both switches conduct and input inductors are magnetized. In this condition, stored energy of the output capacitor is transferred to the load.

Mode 6 [see Fig. 5(f)*]*: This mode initiates upon the turning OFF S_1. Capacitors C_1 and C_2, alongside diode D_2, function as a clamp to suppress switch spikes. In this condition, the current direction in the primary sides of the CIs leads to output diode conduction, and the output capacitor is charged. As depicted in Fig. 4, D_2 is turned OFF under the condition of ZCS

$$V_{Ns1}^{D'} = n_1\, V_{Lm1}^{D'} \tag{15}$$

$$V_{Ns2}^{D} = n_2\, V_{Lm2}^{D} \tag{16}$$

$$V_{Lin1}^{D'} = V_{C1} + V_{in1} - V_{C2} \tag{17}$$

$$V_{Lm1}^{D'} = k(V_{cr1} + V_{C1} - V_{C2}) \tag{18}$$

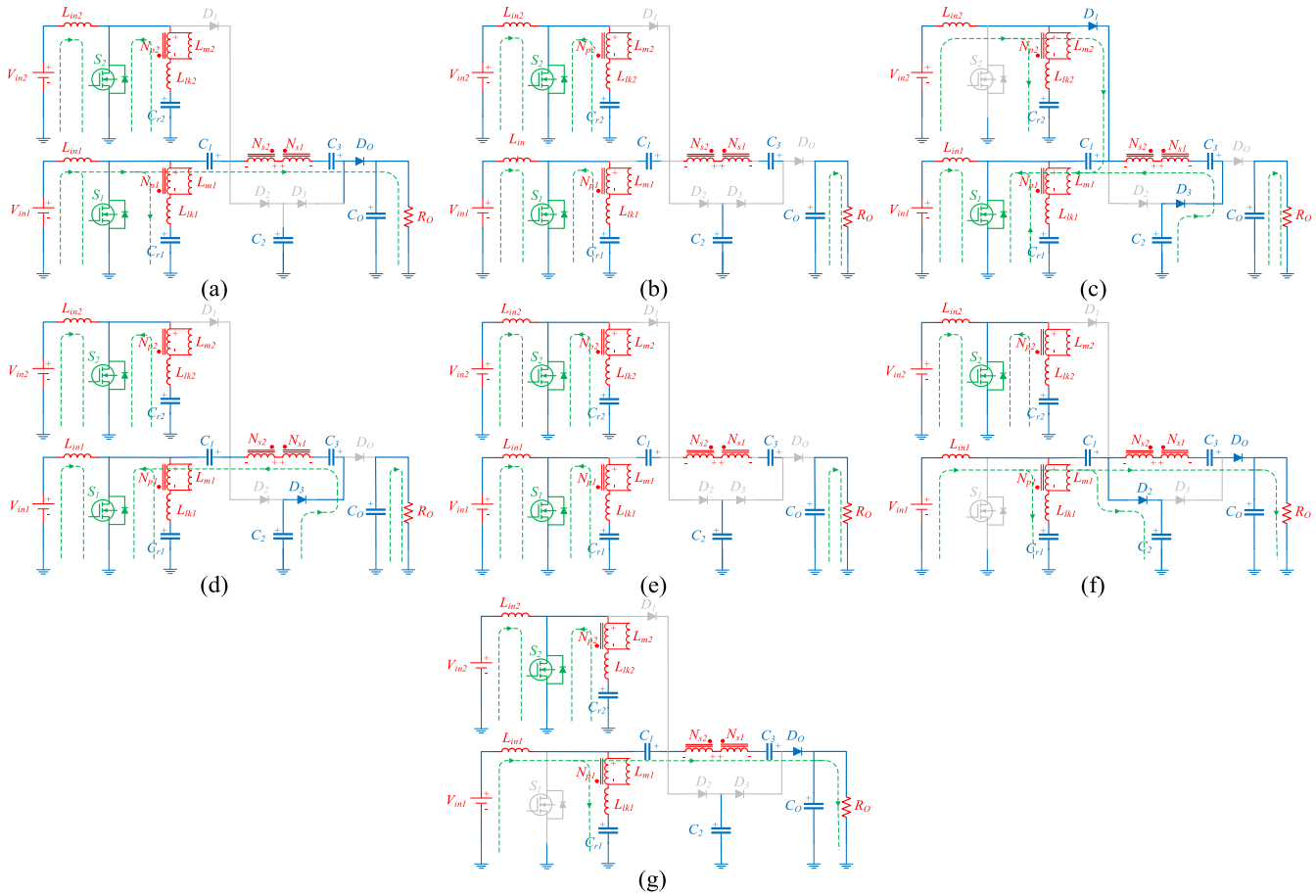

Fig. 5. Current paths and equivalent circuit of the proposed converter in each time interval. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7.

$$V_O = V_{C3} + V_{NS2}^{D} - V_{NS1}^{D'} + V_{C2}. \tag{19}$$

Mode 7 [see Fig. 4(g)*]*: In the operational sequence, once D_2 has completed its role as a clamp circuit, it is subsequently turned OFF, allowing for the output capacitor to be charged via D_1, mirroring the behavior observed in the preceding mode.

B. Steady State Analysis

Through the application of the volt-second equilibrium principle for L_{in2}, as described in (4) and (10), V_{C1} can be derived as

$$\int_0^D V_{Lin2}^{D} + \int_D^1 V_{Lin2}^{D'} = 0 \rightarrow V_{C1} = \frac{V_{in2}}{D'}. \tag{20}$$

Similarly, to V_{C1}, V_{C2} can be obtained by employing (1) and (15) and substituting (17)

$$\int_0^D V_{Lin1}^{D} + \int_D^1 V_{Lin1}^{D'} = 0 \rightarrow V_{C2} = V_{C1} + \frac{V_{in1}}{D'} = \frac{V_{in1} + V_{in2}}{D'}. \tag{21}$$

V_{Cr1} is obtained as follows, based on (18) and (19), and by applying the volt-second equilibrium axiom for L_{m1} from (2) and (16), followed by substituting (18) and (19)

$$\int_0^D V_{Lm1}^{D} + \int_D^1 V_{Lm1}^{D'} = 0 \rightarrow$$

$$\int_0^D kV_{Cr1} + \int_D^1 k(V_{Cr1} + V_{C1} - V_{C2}) = 0 \rightarrow$$

$$V_{Cr1} = D'\,(V_{C2} - V_{C1}) \rightarrow V_{Cr1} = V_{in1}. \tag{22}$$

Similar to V_{Cr1}, V_{Cr2} is obtained by utilizing (5) and (11) and substituting (18)

$$\int_0^D V_{Lm2}^{D} + \int_D^1 V_{Lm2}^{D'} = 0 \rightarrow$$

$$\int_0^D kV_{Cr2} + \int_D^1 k(V_{Cr2} - V_{C1}) = 0 \rightarrow$$

$$V_{Cr2} = D'V_{C1} \rightarrow V_{Cr2} = V_{in2}. \tag{23}$$

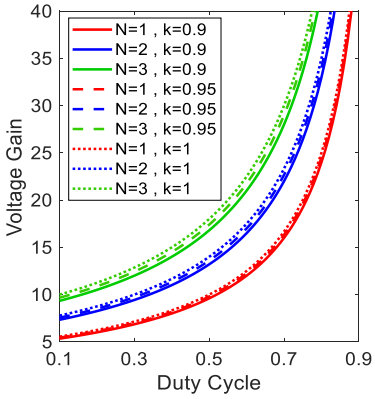

Fig. 6. Output voltage of the proposed converter as a function of duty cycle with different turn ratio and coupling coefficient.

Considering (2), (5), (11), and (16) yields

$$\begin{cases} V_{Lm1}^{D} = kV_{in1} \\ V_{Lm1}^{D'} = -k\frac{D}{D'}V_{in1} \\ V_{Lm2}^{D} = kV_{in2} \\ V_{Lm2}^{D'} = -k\frac{D}{D'}V_{in2} \end{cases}. \tag{24}$$

The combination of equations (8), (9), (13), (14), and (22) results in

$$\begin{cases} V_{Ns1}^{D} = n_1\, kV_{in1} \\ V_{Ns1}^{D'} = -n_1\, k\frac{D}{D'}V_{in1} \\ V_{Ns2}^{D} = n_2\, kV_{in2} \\ V_{Ns2}^{D'} = -n_2 k\frac{D}{D'}V_{in2} \end{cases}. \tag{25}$$

Substituting equations (18), (19), and (23) into (12) yields the value of V_{C3}

$$V_{C3} = \frac{V_{in1}}{D'} + n_2 k\frac{D}{D'}V_{in2} + n_1 kV_{in1}. \tag{26}$$

According to (17), the output voltage can be expressed as a function of the voltage across C_2, C_3, and the secondary sides of the CIs. Hence, using equations (19), (22), and (24) to substitute into (17) yields the value of V_O

$$V_O = (2+n_1k)\frac{V_{in1}}{D'} + (1+n_2k)\frac{V_{in2}}{D'}. \tag{27}$$

Therefore, neglecting the leakage inductance of the CI implies a coupling coefficient k of 1. Consequently, the suggested converter ideal voltage gain can be determined as follows:

$$V_O = (2+n_1)\frac{V_{in1}}{D'} + (1+n_2)\frac{V_{in2}}{D'}. \tag{28}$$

According to (28), the output voltage of the converter is influenced by the input voltage levels, turn ratios, and duty cycle, allowing for a broad range of output voltages to suit various applications. Fig. 6 shows output voltage variations as a function of duty cycle, turn ratio, and coupling coefficient ($n_1 = n_2$).

Based on the equivalent circuit of the converter during various time intervals explained in the previous section, and utilizing the aforementioned equations, the voltage stress of the semiconductors can be determined as

$$V_{S1} = V_{D2} = V_{C2} - V_{C1} = \frac{V_{in1}}{D'} \tag{29}$$

$$V_{S2} = V_{C1} = \frac{V_{in2}}{D'} \tag{30}$$

$$V_{D1} = V_{C2} = \frac{V_{in1} + V_{in2}}{D'} \tag{31}$$

$$V_{D3} = V_{DO} = V_O - V_{C2} = \frac{1+n_1}{D'}V_{in1} + \frac{n_2}{D'}V_{in2}. \tag{32}$$

To determine the current through the converter semiconductors, assume that L_{in1}, L_{in2}, L_{m1}, and L_{m2} are sufficiently large to neglect any current ripple. Applying the ampere-second balance principle to all capacitors, the average currents through all diodes are equal to the output current, I_O. Assuming negligible losses in the converter, the following equations can be derived:

$$I_{in1} = (1+n_2)\frac{I_O}{D'} \tag{33}$$

$$I_{in2} = (2+n_1)\frac{I_O}{D'} \tag{34}$$

$$I_{lm(avg)} = 0. \tag{35}$$

Current stress of the switches and diode are calculated as

$$I_{S1} = I_{S2} = ((2+n_1+n_2)\frac{I_O}{D'} \tag{36}$$

$$I_{D1(\text{peak})} = \frac{2I_O}{D'} \tag{37}$$

$$I_{D2(\text{peak})} = \frac{4I_O}{D'} \tag{38}$$

$$I_{D3(\text{peak})} = I_{DO(\text{peak})} = \frac{I_O}{D'}. \tag{39}$$

III. Loss Analysis

In order to accurately evaluate the performance of the converter, loss analysis of the proposed converter is done in this section. Five categories of the losses accrued in the converter are studied and their values for a 550-W prototype are calculated.

A. Switch Losses

Switch losses include switching and ohmic losses. Due to the soft switching of the converter at the moment the switch is turned ON, its switching losses only include losses during turning OFF. Ohmic losses and switching losses can be calculated as follows:

$$P_{\text{loss(turn off) }S1} = \left(\frac{1}{2} * V_{DS1} * I_{DS1} * t_{\text{turn-off fall time}}\right) * f_s = 1.33\ \text{W} \tag{40}$$

$$P_{\text{loss(turn off)}S2} = \left(\frac{1}{2} * V_{DS2} * I_{DS2} * t_{\text{turn-off fall time}}\right) * f_s = 0.47\ \text{W} \tag{41}$$

$$P_{\text{loss(conduction) }S1} = R_{DS1(\text{on})} \times I_{DS1(\text{RMS})}^2 = 1.34\ \text{W} \tag{42}$$

$$P_{\text{loss(conduction) }S2} = R_{DS1(\text{on})} \times I_{DS2(\text{RMS})}^2 = 0.61\ \text{W} \tag{43}$$

$$P_{\text{loss}(S1,\ S2)} = P_{\text{loss}(S1)} + P_{\text{loss}(S2)} = 3.75\ \text{W} \tag{44}$$

where R_{DS} of the MOSFET typically is about 4.5 mΩ.

B. Diode Losses

Ohmic and reverse recovery losses of the diodes in this topology are ignorable and the main losses of the diodes are related to the voltage drop of the diodes. Hence, value of the diodes losses can be calculated as

$$P_{\text{loss(diodes)}} = V_{\text{forward diode}} \times I_{D(\text{average})} = 3.36\ \text{W}. \quad (45)$$

C. Capacitor Ohmic Loss

In order to calculate the internal resistance loss of capacitors, the following equation can be considered:

$$P_{\text{loss(capacitor)}} = \text{ESR} \times I^2_{\text{COUT(RMS)}} = 0.1 * 2^2 = 0.4\ \text{W}. \quad (46)$$

Only C_4 is considered with ESR $= 50\ \text{m}\Omega$ and the rest of capacitors have a small ESR due to their material (MKT).

D. Input Inductors Losses

Each inductor has two losses, magnetic loss, and ohmic loss. For the T131-26 iron powder core at 100 kHz magnetic loss is approximately equal to 1.23 W and conduction loss of the first and second inductors are equal to 1.58 W and 0.94 W, respectively

$$P_{\text{loss(Input inductor1)}} = P_{\text{loss(magnetic)}} + P_{\text{loss(conduction)}} = 3.48\ \text{W} \quad (47)$$

$$P_{\text{loss(Input inductor2)}} = P_{\text{loss(magnetic)}} + P_{\text{loss(conduction)}} = 2.67\ \text{W}. \quad (48)$$

E. CI Losses

The same as input inductors, the CIs have magnetic and ohmic losses. The core loss is 1.15 W when the switching frequency is 100 kHz for the ETD39 ferrite core, and conduction loss is equal 0.32 W for each CI. So, the core losses can be calculated as

$$P_{\text{loss(cores)}} = P_{\text{loss(core1)}} + P_{\text{loss(core2)}} = 2.94\ \text{W}. \quad (49)$$

According to the accomplished loss calculations, the efficiency of topology can be calculated as follows:

$$\eta = \frac{P_O}{P_O + P_{\text{loss}}} = \frac{550}{550 + 16.6} = 97.07\%. \quad (50)$$

Fig. 7 illustrates the power losses in various components, derived from experimental data. In addition, the variation in converter efficiency as a function of duty cycle is presented in Fig. 8 to analyze power losses under different operating conditions. Finally, Fig. 9 compares the efficiency of the proposed converter with recently introduced topologies in the literature, including those in [1], [9], and [17], [18], to evaluate its performance.

IV. Design Consideration

To achieve optimal performance and resonance, it is essential to design the converter components based on the rated voltage and current, as well as the allowable ripple values for current in inductors and voltage in capacitors.

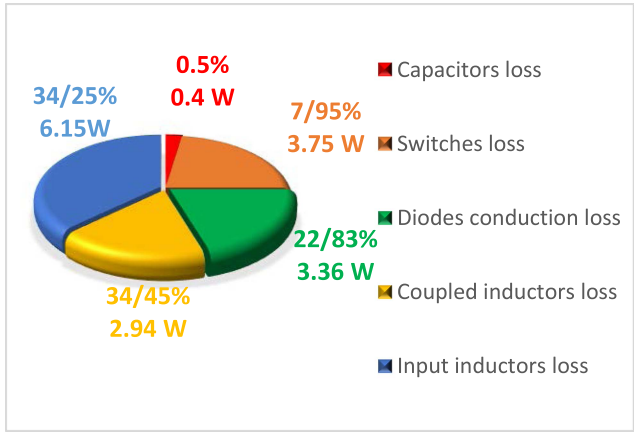

Fig. 7. Power loss distribution of the prototype.

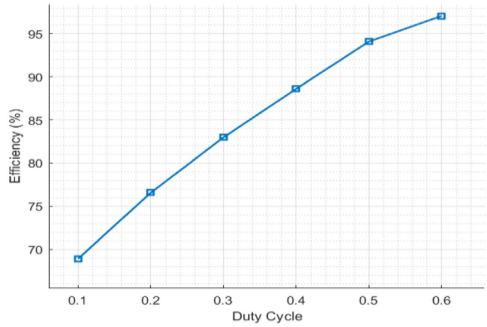

Fig. 8. Proposed converter efficiency as a function of duty cycle.

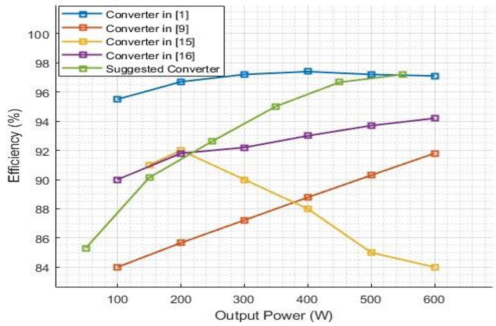

Fig. 9. Proposed converter efficiency comparison.

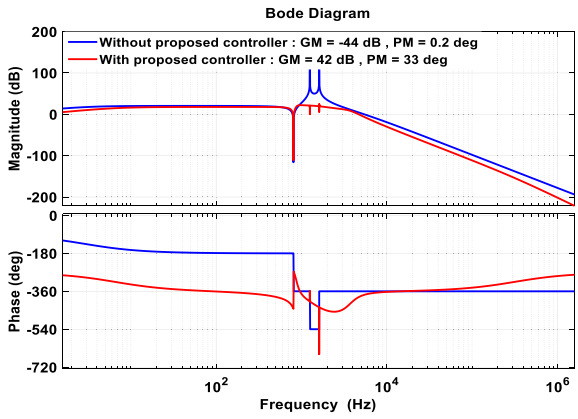

Fig. 10. Bode diagrams of G_{vg1} without control and with control ($\frac{G_{Vg1}}{1+T}$ which is named Closed Loop G_{vg1} on the figure).

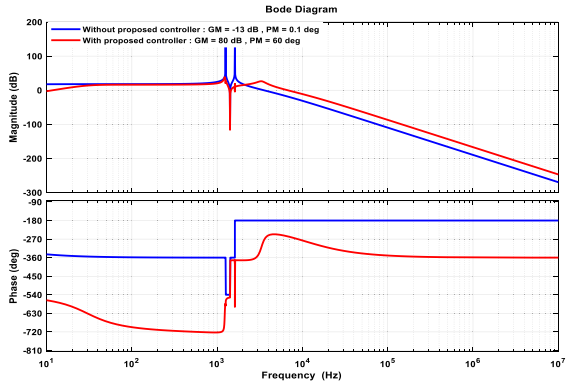

Fig. 11. Bode diagrams of G_{vg2} without control and with control ($\frac{G_{Vg2}}{1+T}$ which is named Closed Loop G_{vg2} on the figure).

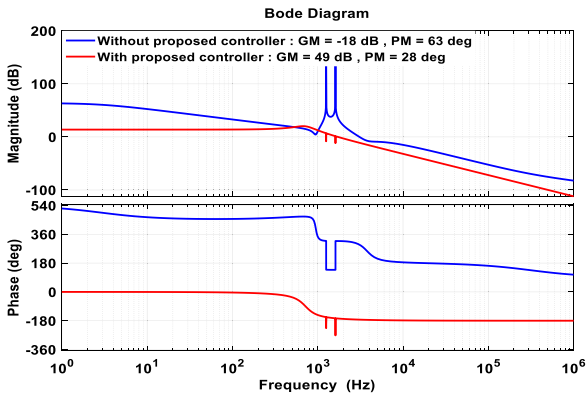

Fig. 12. Bode diagrams of G_{vd1} without control and with control ($\frac{G_{vd1}}{1+T}$ which is named Closed Loop $G_{I1\,d1}$ on the figure).

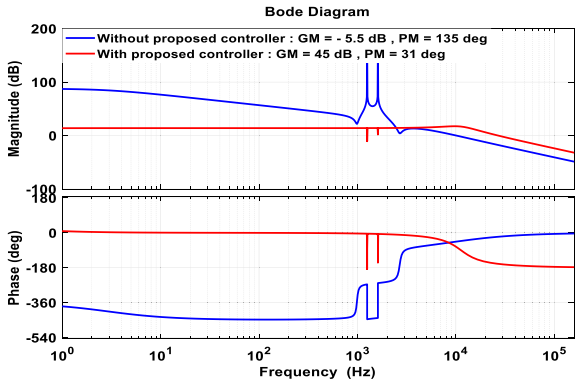

Fig. 13. Bode diagrams of G_{vd2} without control and with control ($\frac{G_{vd2}}{1+T}$ which is named Closed Loop $G_{I2\,d2}$ on the figure).

A. *Input Filter Design* (L_{in1} *and* L_{in2})

By assuming 15% input current ripple, the size of input inductor is obtained from the following equation:

$$L_{in1} = \frac{V_{in1}D}{\Delta I_{in1} f_s} \rightarrow L_{Lin1} > \frac{V_{in1}D}{0.15 I_{in1} f_s} \rightarrow L_{in1} > 64\ \mu\text{H} \tag{51}$$

$$L_{in2} = \frac{V_{in2}D}{\Delta I_{in2} f_s} \rightarrow L_{Lin2} > \frac{V_{in2}D}{0.15 I_{in2} f_s} \rightarrow L_{in2} > 60\ \mu\text{H}. \tag{52}$$

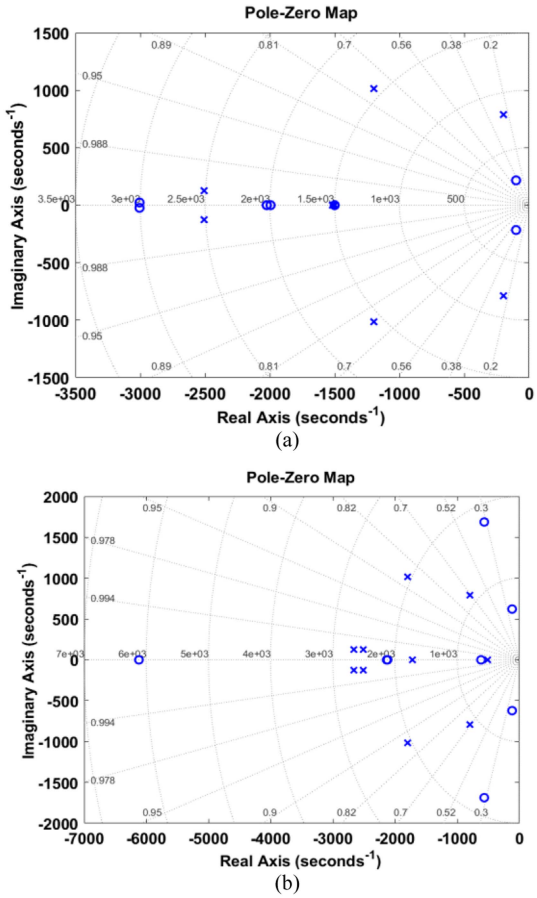

Fig. 14. Pole-zero mapping of the control-to-output transfer function. (a) *Gvd1*. (b) *Gvd2*.

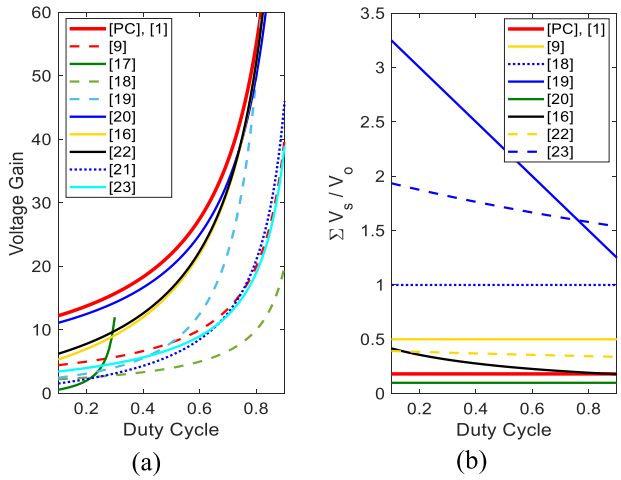

Fig. 15. Comparison of the proposed converter with similar one from (a) voltage gain point of view and (b) switch voltage stress point of view.

B. *Capacitors Design*

The following equations are used to calculate the size of capacitors by assuming 2.5% voltage ripple for C_1, C_2, C_3, and

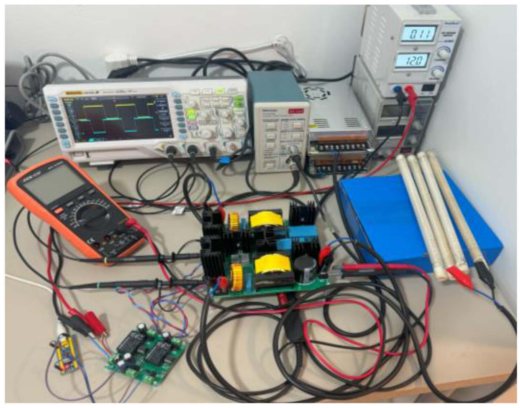

Fig. 16. Implemented prototype.

0.02% voltage ripple for C_O and assumed capacitors average current equal to I_O

$$C_1 = \frac{P_O}{V_O \Delta V_{C1} f_s} \rightarrow C_1 > \frac{P_O D'}{V_O 0.025 V_{in2} f_s} \rightarrow$$
$$C_1 > 12.43\ \mu\text{F} \tag{53}$$

$$C_2 = \frac{P_O}{V_O \Delta V_{C2} f_s} \rightarrow C_2 > \frac{P_O D'}{V_O 0.025 (V_{in1} + V_{in2}) f_s} \rightarrow$$
$$C_2 > 8.23\ \mu\text{F} \tag{54}$$

$$C_3 = \frac{P_O}{V_O \Delta V_{C3} f_s} \rightarrow$$
$$C_3 > \frac{P_O D'}{V_O 0.025 (V_{in1} + n_1 D' V_{in1} + n_2 D V_{in2}) f_s} \rightarrow$$
$$C_3 > 3.15\ \mu\text{F} \tag{55}$$

$$C_O = \frac{P_O}{V_O \Delta V_{C6} f_s} \rightarrow C_6 > \frac{P_O}{V_O 0.0002 V_O f_s} \rightarrow$$
$$C_6 > 178.05\ \mu\text{F}. \tag{56}$$

C. CI Magnetizing Inductance Design (L_{m1} and L_{m2})

By assuming 2 A current ripple for each magnetic inductance, the amount of the magnetic inductance is obtained from the following equations:

$$L_{m1} = \frac{V_{in1} D}{\Delta I_{Lm1} f_s} \rightarrow L_{m1} > \frac{V_{in1} D}{2 f_s} \rightarrow L_{Lm1} > 72\ \mu\text{H} \tag{57}$$

$$L_{m2} = \frac{V_{in2} D}{\Delta I_{Lm2} f_s} \rightarrow L_{m2} > \frac{V_{in2} D}{2 f_s} \rightarrow L_{Lm2} > 54\ \mu\text{H}. \tag{58}$$

D. Design of Resonance Components

To calculate the values of C_{r1} and C_{r2} (resonance capacitors) and the leakage inductances L_{lk1} and L_{lk2} of the CI, the components are designed to operate in boundary resonance mode. This design approach helps reduce output diode switching losses and mitigates reverse recovery issues. In addition, the leakage inductances of the CI depend on the winding configuration. Consequently, the following equation is derived:

$$\pi \sqrt{L_{lk1} C_{r1}} \leq D T_s \rightarrow C_{r1} \leq \frac{D^2}{\pi^2 L_{lk1} f_s^2} \rightarrow C_{r1} \leq 1.02\ \mu\text{F} \tag{59}$$

$$\pi \sqrt{L_{lk2} C_{r2}} \leq D T_s \rightarrow C_{r2} \leq \frac{D^2}{\pi^2 L_{lk2} f_s^2} \rightarrow C_{r2} \leq 1.02\ \mu\text{F}. \tag{60}$$

V. Control and Modeling

The proposed converter includes six capacitors, two inductors, and two CIs, resulting in a total of ten state variables, as indicated in the following equation:

$$X = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \\ x_{10} \end{bmatrix} \Rightarrow \begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3\_1} \\ I_{L3\_2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{bmatrix} \begin{bmatrix} I_{Lin-1} \\ I_{Lin-2} \\ I_{Lm-1} \\ I_{Lm-2} \\ V_{Cr-1} \\ V_{Cr-2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{Co} \end{bmatrix}. \tag{61}$$

After establishing the state-space model, transfer functions are derived. The first transfer function relates input voltage to output voltage, illustrating how input changes influence the output. Accordingly, the transfer function from input voltages to output voltage ($G_{vg1} = (V_O/V_{in\text{-}1})$ and $G_{vg2} = (V_O/V_{in\text{-}2})$) can be written as (62)–(65) shown at the bottom of the next page.

The second transfer function relates the duty cycle to the output voltage, highlighting the control pathway through which the converter operates. Similarly, the transfer function from duty cycle to output voltage can be obtained as (64) and (65). Finally, using the obtained the formulas, controller of the proposed converter for each input can be designed as

$$G_{c1} = \frac{10}{s} * \frac{\left(1 + \frac{s}{1000}\right)\left(1 + \frac{s}{1500}\right)}{\left(1 + \frac{s}{40000}\right)\left(1 + \frac{s}{45000}\right)} \tag{66}$$

$$G_{c2} = \frac{20}{s} * \frac{\left(1 + \frac{s}{2000}\right)\left(1 + \frac{s}{2000}\right)}{\left(1 + \frac{s}{50000}\right)\left(1 + \frac{s}{52000}\right)}. \tag{67}$$

The Bode plots (see Figs. 10–13) are analyzed to assess the system gain margin and phase margin before and after applying the control system. The controller enhances the phase margin and modifies the gain crossover frequency, resulting in greater stability and dynamic performance. These enhancements are clearly demonstrated by comparing the Bode diagrams before and after applying the controller, showcasing the control strategy effectiveness in achieving the desired converter performance.

In Fig. 14(a) and (b), the pole-zero plots of the transfer functions G_{vd1} and G_{vd2} are presented. As observed, all poles and zeros are located in the left half-plane, indicating the proper functioning and stability of the controller. The presence of poles

TABLE I
COMPARATIVE STUDY OF THE PROPOSED CONVERTER

Converter	No. of S/D/C/L+CI	Soft Switching	ICR	CF/VF	Extendable	Voltage Gain	Voltage Stress of Switches
[1]	2/5/4/0+2^{2W}	Yes	High	VF	No	$\frac{3+2N}{1-D}$	$\frac{2}{3+2N}$
[9]	2/8/6/2+0	Yes	Low	CF	No	$\frac{4}{1-D}$	0.5
[16]	2/4/5/2+1^{2W}	No	Low	CF	No	$\frac{4+2ND}{1-D}$	$\frac{1}{4+2ND}$
[17]	4/2/1/1+0	No	High	VF	No	$\frac{4D}{1-3D}$	---
[18]	2/8/5/2+0	Yes	Low	CF	No	$\frac{2}{1-D}$	$\frac{2}{1-D}$
[19]	4/5/4/4+0	No	Low	CF	No	$\frac{2}{(1-D)^2}$	$\frac{7-5D}{2}$
[20]	2/4/4/1+1^{2W}	No	Low	CF	No	$\frac{2+2N}{1-D}$	$\frac{1}{2+2N}$
[21]	4/4/2/0+2^{3W}	Yes	High	VF	No	$\frac{1+ND}{1-D}$	---
[22]	3/5/4/1+1^{2W}	No	High	VF	No	$\frac{(1+N+D)(1+D)}{1-D}$	$\frac{2}{(1+N+D)}$
[23]	5/5/5/4+0	No	High	VF	No	$\frac{3+D}{1-D}$	$\frac{6(1-D)}{3-2D-D^2}$
PC	2/4/4/2+2^{W}	Yes	Low	CF	Yes	$\frac{3+2N}{1-D}$	$\frac{2}{3+2N}$

(S: Switches, D: Diodes, C: Capacitors, L: Inductors, CI: Coupled Inductors, ICR: Input Current Ripple, CF: Current Fed, VF: Voltage Fed , PC: Proposed Converter)

in this region ensures that the system quickly reaches a steady state without significant oscillations. In addition, the placement of zeros influences the system's frequency response, and adjusting their positions allows for performance optimization. These characteristics confirm that the controlled system is not only stable but also capable of effectively handling disturbances and load variations.

VI. COMPARATIVE STUDY

After introducing a new converter and conducting a theoretical analysis, it is imperative to compare it with similar recently introduced converters from various perspectives to ascertain its strengths and weaknesses. It should be noted that, for a fair comparison, multi-input converters are selected, and their two-input versions are considered.

The first crucial factor is the component count, which directly impacts the converter cost, volume, reliability, efficiency, and the complexity of its control system. Power switches, diodes, capacitors, inductors, and CIs constitute the main components of the power circuit in converters, all of which are analyzed in Table I. As shown, the proposed converter has the fewest switches, capacitors, and diodes.

$$G_{Vg1}=\frac{(1.985e18\ s^6)+(3.868e07\ s^5)-(9.901e26\ s^4)-(3.287e14\ s^3)-(2.666e34\ s^2)\ -(4.689e22\ s)-4.576e10}{(s^{10})+(18.18\ s^9)-(1.088e09\ s^8)-(1.979e10\ s^7)+(1.96e17\ s^6)+(3.564e18\ s^5)+(5.746e25\ s^4)+(1.045e27\ s^3)+(2.539e33\ s^2)+(\ 4.616e34\ s)-4.4980e+09} \tag{62}$$

$$G_{Vg2}=\frac{(-5.105e17\ s^6)\ +(1.347e05\ s^5)\ +(2.095e26\ s^4)\ -(3.433e13\ s^3)\ +(1.98e34\ s^2)\ -(1.547e22\ s)\ +\ 6.5e08}{(s^{10})+(18.18\ s^9)-(1.088e09\ s^8)-(1.979e10\ s^7)+(1.96e17\ s^6)+(3.564e18\ s^5)+(5.746e25\ s^4)+(1.045e27\ s^3)+(2.539e33\ s^2)+(4.616e34\ s)+8.585e+07} \tag{63}$$

$$G_{vd1}=\frac{(-454.5\ s^9)\ +(9.091e08\ s^8)\ -(5.149e12\ s^7)\ -(3.526e16\ s^6)+(\ 4.917e21\ s^5)\ -(\ 2.589e26\ s^4)-(1.671e30\ s^3)-(8.04e33\ s^2)\ -(7.04e37\ s)\ +\ 2.399e26}{(s^{10})\ +(18.18\ s^9)\ -(1.088e09\ s^8)-(1.979e10\ s^7)\ +(1.96e17\ s^6)\ +(3.564e18\ s^5)\ +(5.746e25\ s^4)+(1.045e27\ s^3)+(2.539e33\ s^2)\ +(4.616e34\ s)} \tag{64}$$

$$G_{vd2}=\frac{(-3.636e09\ s^8)\ -(2.278e14\ s^7)\ +(1.411e17\ s^6)\ +(\ 3.074e22\ s^5)\ +(6.311e26\ s^4)\ +(3.036e31\ s^3)+(3.216e34\ s^2)+(\ 1.108e39\ s)\ -(\ 2.53e27)}{(s^{10})\ +(18.18\ s^9)\ -(1.088e09\ s^8)\ -(1.979e10\ s^7)\ +(1.96e17\ s^6)\ +(3.564e18\ s^5)\ +(5.746e25\ s^4)+(1.045e27\ s^3)+(2.539e33\ s^2)\ +(4.616e34\ s)}. \tag{65}$$

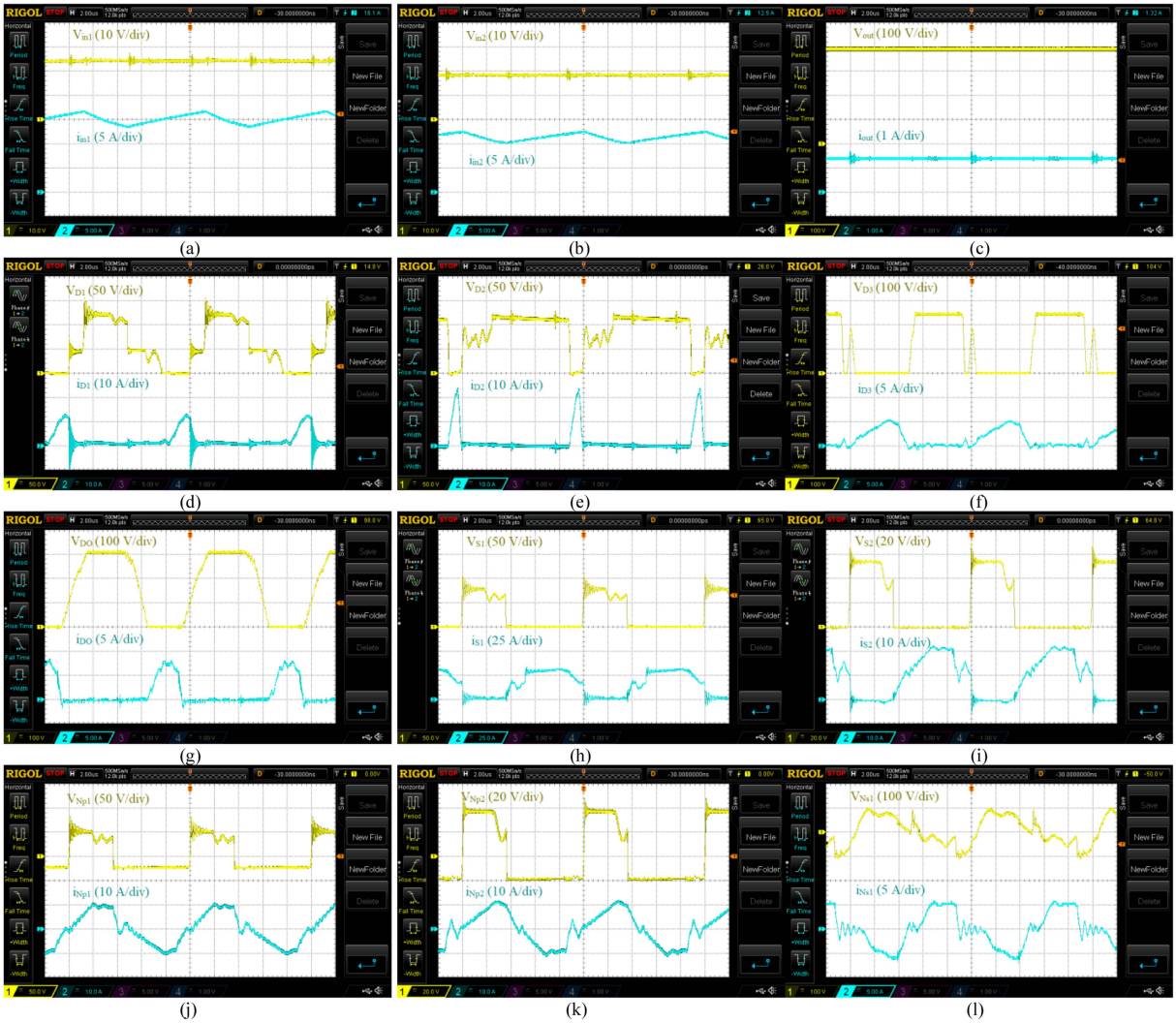

Fig. 17. Experimental results. (a) Input#1 voltage/current. (b) Input#2 voltage/current. (c) Output voltage/current. (d) Voltage/current of first diode. (e) Voltage/current of the second diode. (f) Voltage/current of the third diode. (g) Voltage/current of the output diode. (h) Voltage/current of first switch. (i) Voltage/current of the second switch. (j) Voltage/current of the primary of the first CI. (k) Voltage/current of the secondary of the first CI. (l) Voltage/current of the primary of the second CI.

TABLE II
PROTOTYPE CHARACTERISTICS

Parameters/Components	Value/Description
S_1, S_2	FDP045N10A 100 V, 164 A 4.5 mΩ on-resistance
D_1, D_2 D_3, D_O	MBR20200CT schottky diode, V_F=0.55 V MBR30300CT schottky diode,V_F=0.65 V
CI 1 and 2 L_{m1}, L_{m2}	Turns ratio: 2.3 (Ns / Np = 57:25) Core: ETD 39/20/13 ferrite core Magnetizing inductance: 72 μH Leakage inductance: 3.6 μH
L_{in1}, L_{in2}	Number of windings turns: 29 Core: T131-26 100 μH, 18 A
C_{r1}, C_{r2} C_1 C_2, C_3 C_O	1 μF, 100 V (MKT) 20 μF, 100 V (MKT) 15 μF, 250 V 220 μF, 400 V
Switching Frequency	100 kHz
Output Power	550 W

Soft-switching performance is the next evaluation factor that affects the converter's efficiency and cooling system. As explained in Section II, the proposed converter exhibits ZCS performance for both the switches and the output diode. The quality of the input current and the structure of the input port of the converter have a direct effect on the performance of the RESs and the power extraction process from them. The proposed converter offers ideal conditions, with continuous input current exhibiting minimal ripple and a current-fed structure for the input port.

In the context of multi-input converters, the extendable structure feature provides designers with the flexibility to add numerous input sources. The proposed converter is capable of extension, and the addition of input sources does not affect the others.

The final two assessment criteria are voltage gain and voltage stress on the switches. Voltage gain, being the most critical feature of high step-up dc–dc converters, significantly influences converter performance. The larger the voltage gain, the smaller

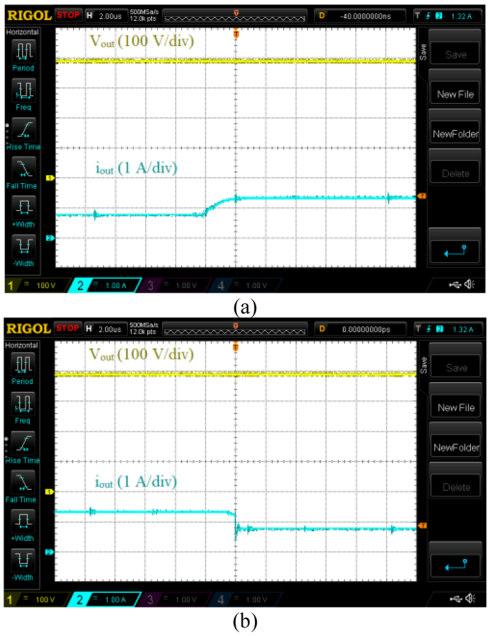

Fig. 18. Experimental results of output voltage and current under condition of load changing. (a) From 320 to 550 W. (b) From 550 to 320 W.

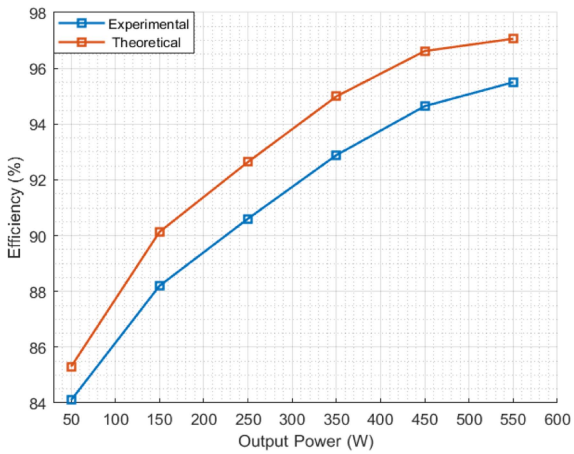

Fig. 19. Theoretical and experimental efficiency of the implemented prototype as a function of output power.

the duty cycle required to achieve the desired output voltage level, resulting in reduced conduction losses. As shown in Fig. 15(a), the proposed converter benefits from a larger voltage gain compared to the studied converters. It should be noted that the voltage gain waveforms of the converters are plotted assuming $Vin_1 = Vin_2$.

The cumulative voltage stress on the switches is plotted in Fig. 15(b). As shown, the value of this factor is 0.18 for the proposed converter, which is lower than most of the studied converters except for [20]. Although [20] has lower voltage stress, its voltage gain is less than that of the proposed converter.

After conducting a comprehensive comparison study, it is evident that the proposed converter and [1] exhibit superior performance and characteristics when compared to alternative converters. The converter introduced in [1] exhibits characteristics closest to the proposed converter. It boasts an almost identical component count, soft-switching performance, voltage gain, and voltage stress. However, its significant drawback is the inability to be extended.

VII. Experimental Results

A 550-W prototype of the proposed converter, illustrated in Fig. 16 and characterized in Table II, was tested to validate the theoretical analysis. The dimensions of the implemented converter is $16\times16\times10$ cm^3 and its power density is 214.84 W/L. Fig. 16(a)–(l) illustrates the experimental results for the proposed converter with duty cycles $D = 0.6$ and turn ratios $n_1 = n_2 = 2.3$. With input voltages of 18 V and 24 V shown in Fig. 17(a) and (b), the resulting output voltage is approximately 390 V, as depicted in Fig. 17(c), confirming the accuracy of the voltage gain formula (28). As can be seen, output voltage ripple is very small that is a result of designing value of the capacitor C_O using (56). The input current waveforms shown in Fig. 17(a) and (b) highlight a key advantage of the proposed design: reduced input current ripple, achieved through the current-fed structure. Fig. 17(d)–(g) illustrates the current and voltage waveforms of diodes D_1–D_3 and D_O, providing an explanation of the converter performance during each time interval. Fig. 17(f)–(g) shows the soft switching performance of diodes D_3 and D_O, which achieve ZCS during both turn-ON and turn-OFF, effectively resolving reverse recovery issues, especially for diode D_O. Moreover, the voltage and current stress of the diodes D_1, D_2, D_3, and D_O are 115 V–14A, 80 V–24 A, 260 V–5 A, and 260 V–8 A, respectively, which validate theoretical analysis accomplished in (31)–(32) and (37)–(39). Due to input and leakage inductances, both switches (S_1 and S_2) demonstrate ZCS during turn-ON, as shown in Fig. 17(h)–(i). In addition, according to the figures, the drain-source voltages and currents of S_1 and S_2 are approximately 75 V–32 A and 52 V–22 A, respectively, which validate (29)–(30). The low imposed voltages on the switches in comparison to the output voltage provides the chance to select low-cost MOSFETs. Finally, Fig. 17(j)–(l) shows the current and voltage waveforms for the primary and secondary windings of the CI. Moreover, to investigate converter performance under load changing condition, output voltage and current are shown in Fig. 18 during load changing from 320 to 550 W and vice versa. Finally, theoretical and experimemntal efficiency of the implemented prototype as a function of output power are illustrated in Fig. 19.

VIII. Conclusion

In this article, a multi-input high step-up dc–dc converter is proposed, effectively addressing the challenges associated with boosting output voltage in multienergy systems. Through the integration of CIs, voltage multiplier cells, and a current-fed structure, the converter achieves high voltage gain, low input current ripple, and enhanced efficiency, making it an ideal candidate for renewable energy applications. The soft-switching operation not only improves efficiency but also prolongs the lifespan of the switches and reduces overall cost.

Moreover, the resonant operation mitigates reverse recovery issues in the output diode, contributing to the converter's robust

performance. A detailed analysis of the converter's operating principles, component losses, and design considerations is provided, and the comparative study validates its superiority over similar designs. The successful implementation of a 550-W prototype, supported by experimental results, demonstrates the practical viability of the proposed converter.

To further enhance the proposed converter and expand its practical applications, several future directions are suggested. First, achieving full soft-switching within the proposed topology can improve efficiency and reduce switching losses. In addition, developing a robust controller based on energy awareness of the inputs will enhance the system's adaptability and performance under varying operating conditions. Finally, designing a higher voltage gain configuration based on the proposed topology will further increase its applicability in high-power and high-voltage scenarios, making it more suitable for industrial and renewable energy applications.

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