Letters

Dual-NMOS GaN Gate Driver With Active Bootstrap and Infinite-CMTI Level Shifter for Configurable d*V/dt* and MHz Operation

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***Abstract*—This letter proposes a novel dual-NMOS gallium-nitride gate driver integrating an active bootstrap (BST) and a high common-mode transient immunity (CMTI) capacitive level shifter (LS). Compared to conventional PMOS-based BST circuits requiring extra LSs, the proposed design utilizes bidirectional NMOS BST switch pairs with dedicated ON-OFF control circuit, providing reliable floating gate voltage with reduced on-chip area. The capacitive LS achieves theoretically infinite CMTI by isolating differential-mode logic signals from common-mode noise through current-mirror-based edge-detection and noise isolation. Furthermore, the dual-NMOS high-side buffer enables continuously adjustable *dV/dt* via adaptive Miller plateau detection and configurable gate charging currents, reducing switching losses and voltage spikes versus fixed gate-resistor drivers. Experimental results demonstrate a peak efficiency of 91.8% in a 12-to-1.8 V conversion and 4.6% efficiency improvement under 48 V input and 2 MHz switching frequency, validating its potential for high-frequency, high-density power applications such as automotive dc–dc converters.**

***Index Terms*—Active bootstrap (BST), configurable *dv/dt* control, dual-NMOS driver, gallium-nitride (GAN) power devices, high common-mode transient immunity (CMTI) level shifter (LS), low switching loss.**

I. Introduction

GALLIUM-NITRIDE (GaN) power devices are widely adopted in high-frequency switching (F_{SW}) converters and high-conversion-ratio applications due to their superior figure of merit ($R_{DS,\ ON} \times Q_G$), offering significant advantages in consumer electronics, automotive systems, and data center power supplies [1], [2], [3]. However, conventional silicon (Si) MOSFET gate drivers face critical challenges when driving GaN high-electron-mobility transistors (HEMTs), particularly under high *dV/dt* and high common-mode transient immunity (CMTI) noise conditions [4], [5], [6], which may introduce reliability issues and efficiency degradation due to the unique device characteristics of GaN and high F_{SW} operation. As illustrated in Fig. 1, three key limitations hinder the full utilization of the device's excellent performance in high-voltage (HV) high-speed half-bridge buck converters.

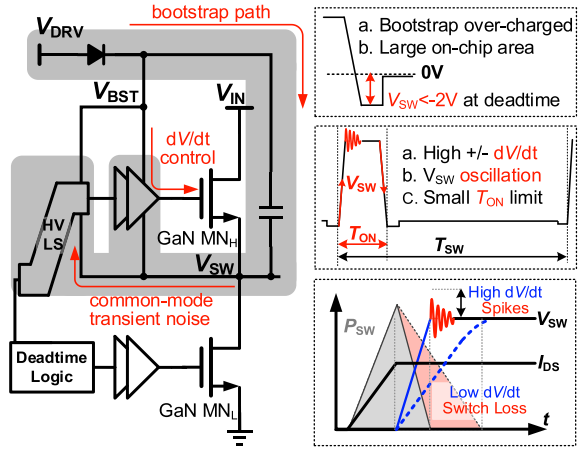

Fig. 1. Illustration of main design challenges in HV high-speed GaN gate drivers.

Bootstrap (BST) Circuit Reliability: GaN HEMTs lack body diodes, causing negative V_{SW} during deadtime and potential gate overvoltage. Conventional HV diode-based BST circuits require either a PMOS or NMOS switch along with additional level shifters (LS), which occupy excessive silicon area [7], [8].

CMTI Limitations: High F_{SW} results in high $\pm dV/dt$ slew rates (SR), switch node oscillations, and a limited high-side switch-on time. Consequently, there are increased requirements for higher CMTI and reliability for the HV LS.

Switching Loss-Oscillation Tradeoff: Conventional fixed gate-resistor drivers either induce voltage spikes at high *dV/dt* or switching losses at low *dV/dt*, limiting efficiency in wide-input-range applications. Some designs use digital or adaptive-slope gate drivers for ringing suppression, but these often occupy significant chip area and have limited adjustment ranges [9], [10].

To address these issues, this letter proposes a dual-NMOS GaN gate driver with three key innovations.

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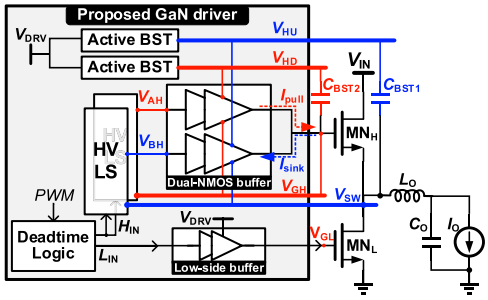


Fig. 2. Block diagram of proposed GaN gate driver in half-bridge topology.

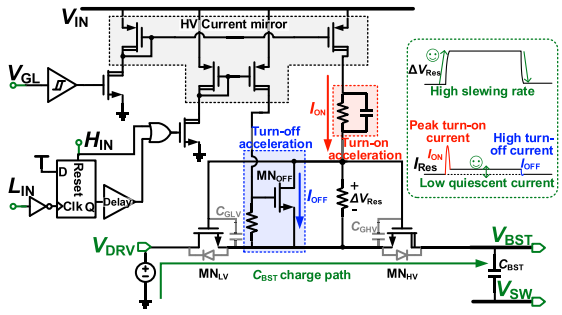


Fig. 3. Proposed active HV NMOS bootstrap circuit with switching transient acceleration.

1) An active BST circuit utilizing bidirectional NMOS switches and transient acceleration on-off control, reducing on-chip area compared to PMOS-based designs.
2) A capacitive LS with current-mirror-based edge detection, achieving infinite CMTI by isolating differential-mode signals from common-mode noise theoretically.
3) A dual-NMOS high-side buffer featuring adaptive Miller plateau (MP) detection and continuously adjustable *dV/dt* with a range of 14.75 times at a 40 V input designed for low switching losses and reduced voltage spikes.

Experimental results validate a peak efficiency of 91.8% at 12 to-1.8 V conversion and efficiency improvement of 4.6% under 48 V input at 2 MHz, highlighting its applicability in high-density automotive and server power modules.

II. Proposed Half-Bridge Driver

The architecture of the proposed GaN half-bridge driver is illustrated in Fig. 2. The input pulsewidth modulation signal is processed by a deadtime logic circuit to generate complementary high-side $H_{\rm IN}$ and low-side $L_{\rm IN}$ control signals. These signals are fed into the HV LS and low-side buffer, respectively. The high-side driver employs a dual-NMOS buffer operating in two floating domains referenced to $V_{\rm GH}$ (high-side gate voltage) and $V_{\rm SW}$ (switch node voltage). The low-side buffer incorporates a delay compensation corresponding to the high-side signals path. This architecture integrates three key innovations: an active BST circuit for reliable gate voltage generation, a capacitive LS with theoretically infinite CMTI, and a dual-NMOS buffer enabling configurable *dV/dt* control.

A. HV-Switch Active Bootstrap

Fig. 3 shows the proposed active BST circuit, which employs a pair of common-source NMOS, $\rm MN_{LV}$, and $\rm MN_{HV}$ as bidirectional isolation switches to block the reverse charging path when negative $V_{\rm SW}$ occurs during deadtime. These two switches are controlled by one floating control circuit, consuming less area than PMOS switches. The gate control voltage $\Delta V_{\rm Res}$ is generated by the current drop across the resistor from a HV current mirror. The switches are both turned ON and maintain high voltage level when $V_{\rm GL}$ is "1." When the switches need to be turned OFF, the current is terminated and the charges on the parasitic gate-source capacitors, $C_{\rm GLV}$ and $C_{\rm GHV}$, are dissipated by the resistor, then $\Delta V_{\rm Res}$ keeps low.

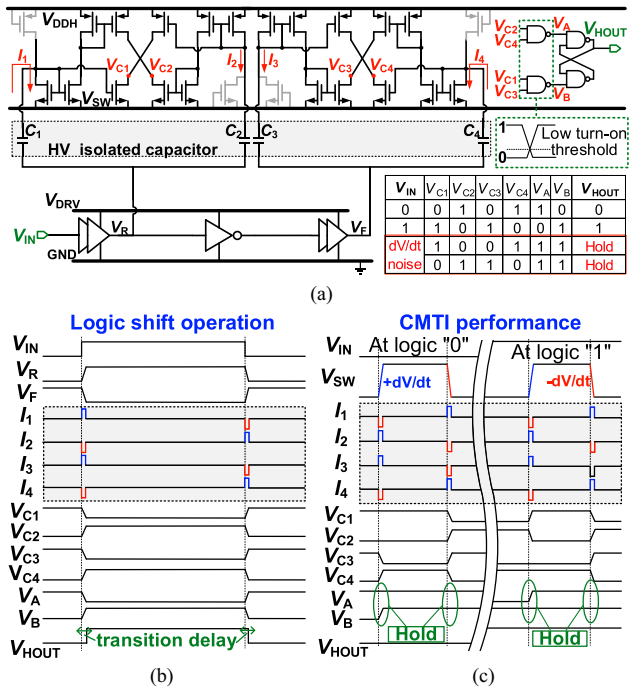


Fig. 4. (a) Proposed capacitive level shifter with operation waveform. (b) Logic shift. (c) CMTI performance.

However, the switching speed of this ON-OFF control scheme cannot be traded off against the power consumption on the resistor, so the acceleration circuits are introduced. During turn-OFF, an additional $\rm MN_{OFF}$ with small size is activated by the logic input signals $H_{\rm IN}$ and $L_{\rm IN}$, and pulls down $\Delta V_{\rm Res}$ speedy. Meanwhile, the resistor-capacitor parallel network is in series with the current path, which generates a large transient current to turn ON the switches rapidly and deactivate in steady state with low quiescent current. The acceleration circuits achieve high switching speed at low quiescent current. Proposed bi-directional NMOS BST switch can generate reliable gate voltage with 35% lower on-chip area compare with PMOS design.

B. High CMTI Level Shifter

The proposed highly reliable capacitive HV LS is illustrated in Fig. 4(a), showing reduced propagation delay and chip area compared to conventional isolated LDMOS-based LSs. The LV

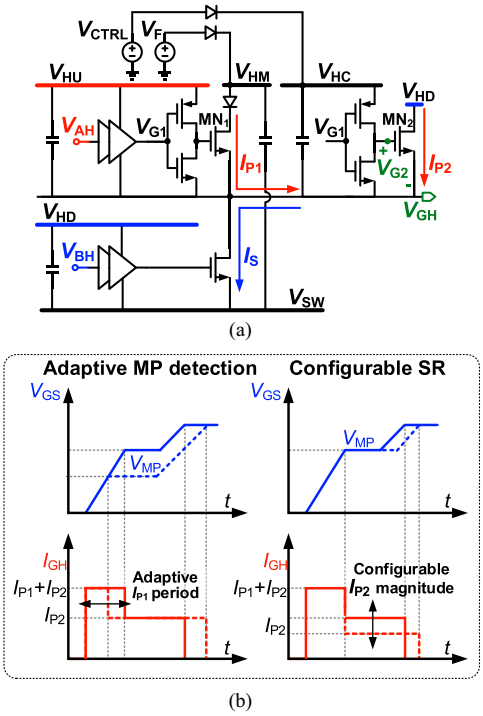


Fig. 5. (a) High-side dual-NMOS buffer. (b) Adaptive MP detection and configurable SR charging waveform.

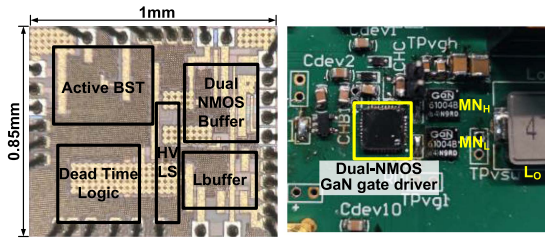


Fig. 6. Die micrograph of the proposed dual-NMOS GaN gate driver and half-bridge converter.

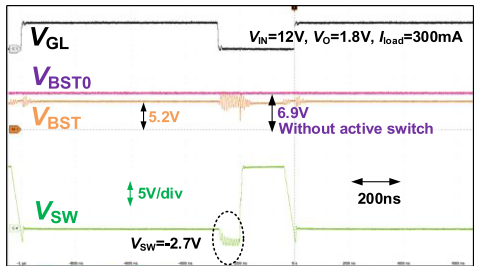


Fig. 7. Waveform of bootstrap voltage W and W/O active switch.

signals, V_R and V_F, which have steep transition edges and opposite phase, generate large transient currents through isolated capacitor $C_{1\text{-}4}$ to the floating HV domain. The floating N-type and P-type current mirrors duplicate the relative positive current to the subsequent stage while blocking up the negative current in $I_{1\text{-}4}$. This technique completely separates the useful differential mode transition signals from the interference of common mode noise through combinational logic, theoretically achieving infinite CMTI. The output V_{HOUT} is represented as a logic "hold" after the RS flip-flop blanking while *dV/dt* disturbance occurs, as shown in Fig. 4(c). Meanwhile, the NAND gates are designed with low asymmetrical turn-ON thresholds to enhance noise immunity. The minimum propagation delay is achieved by utilizing high-bandwidth current mirrors and a minimal stage of combinational logic gates. Additionally, due to the use of edge triggering method, there is no minimum input signal width limitation or mismatch concerns about layout or process in proposed LS, in contrast to the conventional designs.

C. Dual-NMOS Buffer

Fig. 5 demonstrates the proposed high-side dual-NMOS buffer with adaptive MP detection and configurable SR. Two power NMOSs, MN_1 and MN_2, provide pull-up currents while V_{GH} rising. The larger size MN_1 provides high current I_{P1} before the MP stage, rapidly pulling up V_{GH} to reduce switching loss. MN_2 provides a configurable current I_{P2} for *dV/dt* regulation at V_{SW} rising stage.

The basic principle of adaptive MP detection is derived from the phenomenon, which was described in [6]: Since GaN FETs MN_L do not have body diode, reverse current generates a negative voltage $-V_{\mathrm{FW}}$ during deadtime. Since MN_H and MN_L are identical at same the load current (I_L), and if channel length modulation effect and drain–source asymmetry can be ignored, the voltage MN_L during deadtime emulates MN_H at the MP stage, leading to

$$V_{\mathrm{MP}} = V_{\mathrm{FW}}. \tag{1}$$

Based on this analysis, we propose the voltage emulation technique for two floating voltage supply paths. Before the MP stage, MN_1 provides the primary driving current I_{P1} with the floating drain voltage V_{HM} generated by the negative voltage $-V_{\mathrm{FW}}$, while diode's forward voltage drop is compensated by a LV source V_F. Thus, the charging current I_{P1} adaptively shuts down while

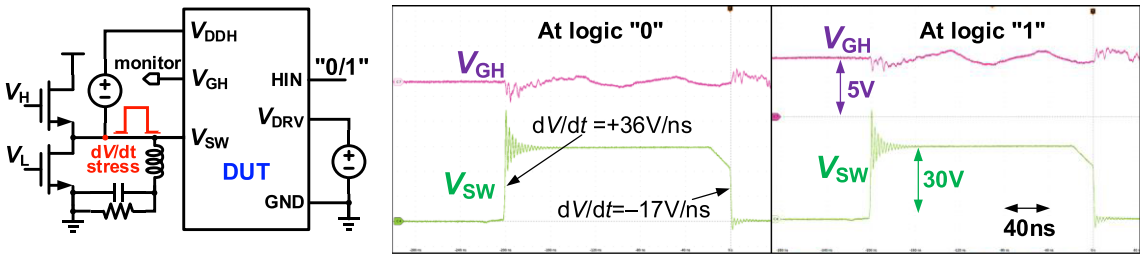
$$V_{\mathrm{GH}} = V_{\mathrm{HM}} = V_{\mathrm{MP}}. \tag{2}$$

Similarly, during MP stage, the external configurable LV voltage source V_{CTRL} is transferred to the floating V_{HC}, which acts as the gate voltage of MN_2, V_{G2}. Thus, the gate charging current I_{P2} controlled by V_{CTRL} can be written as

$$I_{P2} = \frac{1}{2}\frac{W}{L}\mu_n C_{OX}(V_{\mathrm{CTRL}} - V_{TH})^2. \tag{3}$$

The *dV/dt* of switching node is proportional to the driving current I_{P2} and is regulated accordingly.

The operation waveforms are shown in Fig. 5(b), the proposed dual-NMOS output buffer realizes a high *dI/dt* and configurable *dV/dt* condition. Compared with the conventional PMOS gate resistor or segmented driver [12], this scheme is the most direct and efficient method, reducing the switching losses and voltage spikes with less on-chip area at the same driving current.



(a) (b) (c)

Fig. 8. HV level shifter CMTI performance evaluation. (a) Measurement setup. (b) Waveform at logic "0." (c) Waveform at logic "1."

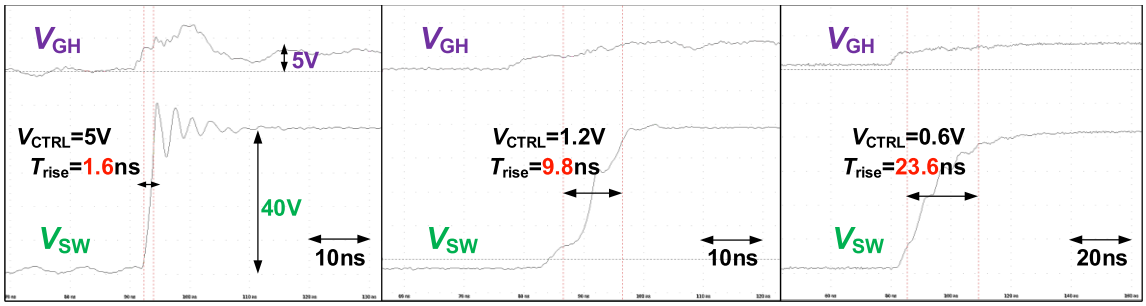


Fig. 9. Measured waveforms of MN_H gate–source voltage V_{GH} and switch node voltage V_{SW} with dV/dt control by V_{CTRL}.

III. Experiment Verification

The proposed GaN driver was fabricated in a 0.18-μm BCD process, occupying a silicon area of 0.85 mm^2. A test PCB of half-bridge converter was designed to validate the driver's performance under high-frequency conditions, as presented in Fig. 6. The measured waveforms of active BST circuit are presented in Fig. 7. The voltage V_{BST0} without active switches reaches 6.9 V while V_{SW} is –2.7 V during deadtime, exceeding the safe operating voltage of GaN gate terminals. In contrast, the proposed active BST circuit stabilizes V_{BST} at 5.2 V, preventing the gate overvoltage effectively.

To validate the CMTI performance of the proposed HVLS, a dedicated half-bridge test circuit, as shown in Fig. 8(a) is employed to generate *dV/dt* stress for the DUT. When V_H become high, the switching node voltage V_{SW} rises rapidly, producing positive *dV/dt* at rising edge. After V_H become low, the circuit enters deadtime state, and V_{SW} is pulled down by the inductor current slowly. When V_L becomes high, V_{SW} drops rapidly, producing negative *dV/dt* at this steep falling edge. When a *dV/dt* stress of +36 V/ns and –17 V/ns is applied to V_{SW}, the high-side gate voltage V_{GH} remains stable without latch-up or logic errors. The results are illustrated in Fig. 8(b) for logic "0" and Fig. 8(c) for logic "1." This comprehensive test validates the CMTI performance of proposed LS across all operational scenarios. In contrast to some prior arts, which HVLS were tested only under specific phase conditions, these designs could not validate output reliability under V_{SW} oscillation.

The *dV/dt* adjustability of the dual-NMOS buffer was tested by varying the external control voltage V_{CTRL}. As shown in Fig. 9, the rise time of V_{SW} can be adjusted from 1.6 ns (*dV/dt* = 25 V/ns) to 23.6 ns (*dV/dt* = 1.7 V/ns), corresponding to approximately 20% reduction in voltage spikes. The proposed gate control method is continuous and configurable because the regulation voltage V_{CTRL} is consecutive, in contrast to other designs with discrete *dV/dt* adjustment steps. The statistical measured efficiency is presented in Fig. 10. The proposed dual-NMOS GaN gate driver can significantly reduce switching losses and achieve a peak efficiency at 12-to-1.8 V conversion and efficiency improvement of 4.6% under 48 V input at 2 MHz switching frequency.

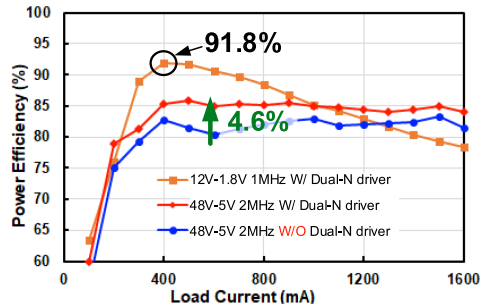


Fig. 10. Measured efficiency.

The comparison between the proposed dual-NMOS GaN driver and state-of-the-art designs is given in Table I. The on-chip driver parts include overvoltage protection BST, high-CMTI level-shifter and high-side buffer for *dV/dt* control. Compared to other GaN high-speed driver techniques typically address only one or two of those parts, the proposed driver design is more comprehensive, requiring fewer off-chip components, avoiding

TABLE I
COMPARISON WITH PREVIOUS WORKS

Design		ISSCC' 21[11]	CICC' 22[7]	JSSC' 21[8]	TIE' 23[4]	TIE' 20[12]	This article
Process		0.5 μm SOI	0.5 μm HV	0.35 μm BCD	0.5 μm SOI	0.18 μm BCD	0.18 μm BCD
V_{IN} [V]		600	3-48	3-40	400	3-18	12-48
F_{SW} [MHz]		1	0.5-10	10-30	1	2-10	2
V_{SW} Rising time @V_{IN}		28 ns @400 V	3.9 ns @44 V	(1.5 & 1.2) ns @40 V	9 ns# @400 V	16 ns @18 V	(1.6 to 23.6) ns @40 V
CMTI [V/ns]	Measured	N.A.	+20.6	N.A.	+100	N.A.	+36 & -17
	Theoretically*	N.A.	Infinite	N.A.	N.A.	N.A.	Infinite
On-chip Driver Parts	Bootstrap	×	○	○	×	○	○
	Level Shifter	×	○	×	○	○	○
	H-Buffer	○	×	×	○	×	○
Off-chip Components		2×R_{gate} 1×D_{BST} 1×C_{BST}	2×R_{gate} 1×C_{BST}	2×R_{gate}	2×R_{gate} 1×D_{BST} 1×C_{BST}	2×R_{gate} 1×C_{BST}	1×C_{BST}
Peak EFF [%]		N.A.	90.1	90.7	N.A.	91.58	91.8
Chip Area [mm^2]		1.8#	2.045	0.48	4.15	2.72	0.85

* From post simulation # Estimated from testing results

discrete gate resistor and BST diode. This significantly reduces the whole power module complexity and enhances application adaptability.

IV. CONCLUSION

This letter presents a dual-NMOS GaN gate driver integrating an active BST circuit and a high CMTI LS. The BST circuit replaces conventional PMOS switches with NMOS-based bidirectional switches and dedicated control circuits, eliminating large-area PMOS devices and additional LSs. The capacitive LS isolates differential-mode logic signals from common-mode noise, achieving theoretically infinite CMTI. Additionally, the dual-NMOS buffer enables adaptive MP detection and continuously adjustable *dV/dt* control, significantly reducing switching losses and oscillations. Experimental results validate a peak efficiency of a 91.8% and efficiency improvement of 4.6% under HV high-frequency conditions, demonstrating its potential for advanced power applications.

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