

Cubic Synchronous Bidirectional DC–DC Battery Charger Converter With Common-Ground and High Voltage Gain Ratio Features

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Abstract—This article presents a novel bidirectional dc–dc converter with a cubic voltage gain ratio, designed to address the limitations of existing converter topologies and enhance performance in dc microgrid applications. The proposed converter features a common ground connection, wide and high voltage gain range, and improved semiconductor utilization. Key contributions of this work include achieving the highest voltage gain ratio compared to existing bidirectional converters, reducing total current stress on semiconductor devices, and implementing zero voltage switching to minimize switching losses. A prototype of the converter was constructed and tested with a 40 V Nickel-cadmium battery with the dc source voltage of 400 V. The experimental results closely aligning with theoretical predictions, confirming the converter's practical viability. The converter exhibits the capability for battery charging/discharging and demonstrates a peak efficiency of 97.6% and 96.33% in the step-down and the step-up mode of operation, respectively.

Index Terms—Bidirectional dc–dc converter, cubic voltage gain, nonisolated, synchronous (Syn.) operation, wide range voltage gain.

I. INTRODUCTION

DEVELOPMENT and optimization of bidirectional dc–dc converters are essential for applications, such as renewable energy systems, electric vehicles (EVs), and energy storage systems (ESS). The vehicle-to-grid concept leverages the substantial energy storage capacity of EVs to support renewable energy integration. Battery ESS are ideally charged during low demand or high renewable generation periods, and are available to provide reserve energy to the grid for frequency support and mitigating sudden load changes [1]. ESS-to-grid also offers longer-term benefits, such as peak shaving and valley filling [2].

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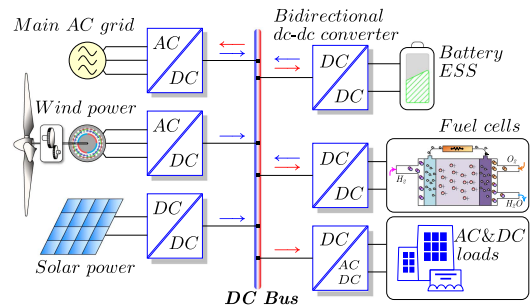


Fig. 1. ESS in a DC microgrid.

Conversely, grid-to-ESS involves charging ESSs using excess grid energy during off-peak times or high renewable generation, enhancing overall power system efficiency and reliability by enabling ESSs to function as both energy consumers and distributed energy resources [3].

As illustrated in Fig. 1, the primary challenge in integrating an energy storage device with a dc microgrid or bus lies in the voltage mismatch. Energy storage devices typically operate at low voltages (LV) (e.g., 24–48 V), while dc buses or grid-connected systems often require much higher operating voltages (e.g., 200–400 V) [4], [5]. A bidirectional dc–dc converter bridges this gap, enabling efficient energy transfer in both charging and discharging modes, while also maintaining stable voltage regulation.

One of the primary requirements for the dc–dc converter in a bidirectional battery charging system is to provide a common ground connection between the LV side and the high-voltage (HV) side. This common ground connection ensures proper operation and safety by maintaining a consistent reference point for both voltage levels. Existing designs, such as those referenced in [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], and [21], often encounter issues like the absence of a common ground between input and output terminals, leading to potential operational inefficiencies and increased complexity in system integration.

Furthermore, synchronous (Syn.) operation of bidirectional converters is essential for reducing losses typically associated with the body diode of switches and enabling zero voltage switching (ZVS) of complementary switches. This significantly

improves overall efficiency. However, certain converters, including those referenced in [10], [13], [14], [15], [16], [18], [19], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], and [32], lack the capability for Syn. operation. This limitation hinders their ability to minimize these losses and achieve ZVS, thereby affecting their overall performance and efficiency.

Maintaining a continuous current on the battery side can extend the battery's lifespan because discontinuous current can reduce the number of charging cycles and subject the battery to large peak currents. These large peak currents can cause stress and damage to the battery, leading to a shorter overall lifespan. As mentioned in [9], [12], [16], [19], and [33], converters exhibit discontinuous current flow on the battery side, which can negatively impact the lifespan of the battery pack.

It is expected from a bidirectional converter to cover the entire range of voltage gain ratios, from 0 to 1 during charging mode and from 1 to a reasonable value during discharging mode. This capability ensures the converter can effectively operate in various charging and discharging scenarios, accommodating different voltage levels and power requirements. Converters referenced in [6], [7], [14], [34], [18], [19], [20], [21], [22], [23], [30], [31], [33], [34], and [35] do not cover the entire range of voltage gain ratios, which limits their applicability in various scenarios.

The topologies described in [36], [37], and [38] lack a common ground between the input and output terminals, making them less suitable for practical applications. In addition, they exhibit low and limited voltage gain ratios, reducing their utility in scenarios that demand a high or flexible voltage range. The converter presented in [39] has a very LV gain ratio, requiring an excessively large duty cycle to achieve HV on the HV terminal. This operational constraint limits its efficiency and practicality. While the design in [40] benefits from low current ripple on the LV side, it lacks ZVS, which is critical for improving efficiency and minimizing switching losses. The converters proposed in [41], [42], [43], [44], [45], and [46] also demonstrate limited voltage gain capabilities in both directions. This narrow voltage gain range significantly restricts their applicability in systems requiring a wide operational voltage range. Several studies have explored coupled inductor and interleaved structures to reduce current ripple at the LV side of bidirectional dc–dc converters; however, they often face limitations in voltage gain or complexity. The converter in [47] employs a coupled inductor to minimize current ripple, improving upon [48]; however, its voltage gain is limited, restricting its applicability in high step-up scenarios. Similarly, the design in [49] combines a coupled inductor with an interleaved structure to further suppress current ripple, yet there is still room for voltage gain enhancement. Bahrami et al. [50] proposed an interleaved coupled inductor structure with six switches, achieving better current ripple performance, though the voltage gain ratio could still be improved. Meanwhile, the converter in [51] features an extendable bidirectional topology with coupled inductors and soft switching, enhancing efficiency but at the cost of increased circuit complexity. While these approaches effectively reduce ripple, they either suffer from limited voltage gain or increased design complexity. The converter in [52] introduces a wide-range voltage gain topology with reduced current ripple at the LV side by incorporating a

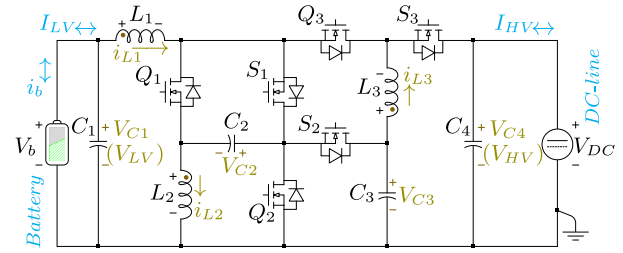


Fig. 2. Proposed bidirectional DC–DC converter.

capacitor loop in the structure; however, its voltage gain can still be further improved.

Recently, a number of new HV gain bidirectional dc–dc converters have been presented in [9], [10], [11], [12], [24], [25], [26], [27], [28], [29], [53], [54], and [55]. Although these converters achieve HV gain and are not limited by their voltage range, there is still room for improving their voltage gain ratio.

Considering the limitations of existing converter topologies, there is a need to develop an improved bidirectional converter with a common ground that has no voltage gain restrictions, is simple, and has enhanced semiconductor utilization. This article proposes such a step-down/step-up bidirectional converter with a cubic voltage gain ratio, suitable for use as the interface converter in discharging and charging applications. The circuit features a wide and HV gain range, enabling dynamic matching between the battery voltage and the constant dc-link voltage.

The presence of a common ground between the input and output terminals avoids additional dv/dt issues, which is beneficial for the operation of the proposed converter. It also offers a wide HV gain range and low current stress on semiconductor devices. A comparative analysis between the proposed converter and its main competitors was conducted, focusing on the normalized total voltage of semiconductor devices (TVS) and the normalized total current of semiconductor devices (TCS). The results indicate that the proposed converter has acceptable TVS and TCS values compared to the most recent bidirectional dc–dc converters. Consequently, the proposed converter can use power switches with lower rated power, improving efficiency. In summary, the proposed converter provides the highest wide voltage gain ratio compared to all previously published bidirectional dc–dc converters. In addition, a dead-beat current controller is adopted for direct battery current regulation, offering accurate, fast, and smooth operation under different states of charge (SoC).

The rest of this article is organized as follows. The proposed common ground bidirectional dc–dc converter is presented in Section II. In this section, the practical considerations and design calculations for the proposed converter is investigated. The proposed controller description is given in Section III. A comprehensive comparative study with the state-of-the-art is presented in Section IV, and the experimental verification is provided in Section V. Finally, Section VI concludes this article.

II. PROPOSED BATTERY CHARGER CONVERTER OPERATION ANALYSIS

Fig. 2 shows the proposed bidirectional dc–dc converter. It consists of six switches $Q_{1,2,3}$ and $S_{1,2,3}$, three inductors $L_{1,2,3}$,

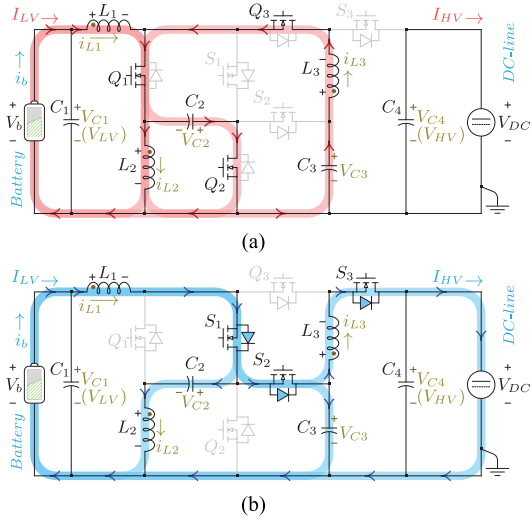


Fig. 3. Equivalent circuit of the proposed bidirectional DC-DC converter during the step-up. (a) Stage-I. (b) Stage-II.

and four capacitors $C_{1,2,3,4}$. The battery is installed on the LV side, and the dc line is connected to the HV side. Therefore, based on the direction of power flow, one can analyze the performance of the proposed converter in both step-up and step-down modes.

A. Step-Up (discharging) Operation Mode

In the step-up operation mode, the battery is discharged to the dc link source. This means that energy is transferred from the lower voltage battery to the HV dc link, thereby decreasing the battery's charge. The converter steps up the voltage from the battery's lower level to the higher level required by the dc link.

In the first stage, as depicted in Fig. 3(a), the switches Q_1 , Q_2 , and Q_3 are activated. In this stage, the body diodes of S_1 , S_2 , and S_3 , are in a reverse-biased state. During this stage as shown in Fig. 4(a) from t_0 to t_1 , inductor L_1 is charged in parallel through switches Q_1 and Q_2 via the battery source V_b and capacitor C_2 , and inductor L_2 is discharged through switch Q_1 to L_1 . Inductor L_3 also receives charge from capacitors C_2 and C_3 through switches Q_2 and Q_3 .

The corresponding steady-state equations are provided below:

$$\begin{cases} v_{L1} = V_{LV} + V_{C2} \\ v_{L2} = -V_{C2} \\ v_{L3} = V_{C2} + V_{C3} \end{cases}, \begin{cases} i_{C2} = -i_{L1} + i_{L2} - i_{L3} \\ i_{C3} = -i_{L3} \\ i_{C4} = -i_{HV}. \end{cases} \quad (1)$$

In the second stage, as depicted in Fig. 3(b), the switches Q_1 , Q_2 , and Q_3 are turned OFF. In addition, the body diodes of S_1 , S_2 , and S_3 become forward biased during a dead time of δT_s from t_1 to t_2 . After the dead time, the switches S_1 , S_2 , and S_3 are activated by gate signals. This methodology ensures that the switches S_1 , S_2 , and S_3 turn ON in ZVS mode as shown in Fig. 4(a) from t_2 to t_3 . During this stage, from t_1 to T_s , inductor L_1 and the battery source discharge through C_2 and L_2 via S_1 and through capacitor C_3 via S_1 and S_2 . Energy from inductors L_1 and L_3 is released to capacitor C_4 and the output dc side via S_1 , S_2 , and S_3 . During the interval from t_3 to T_s , switches S_1 ,

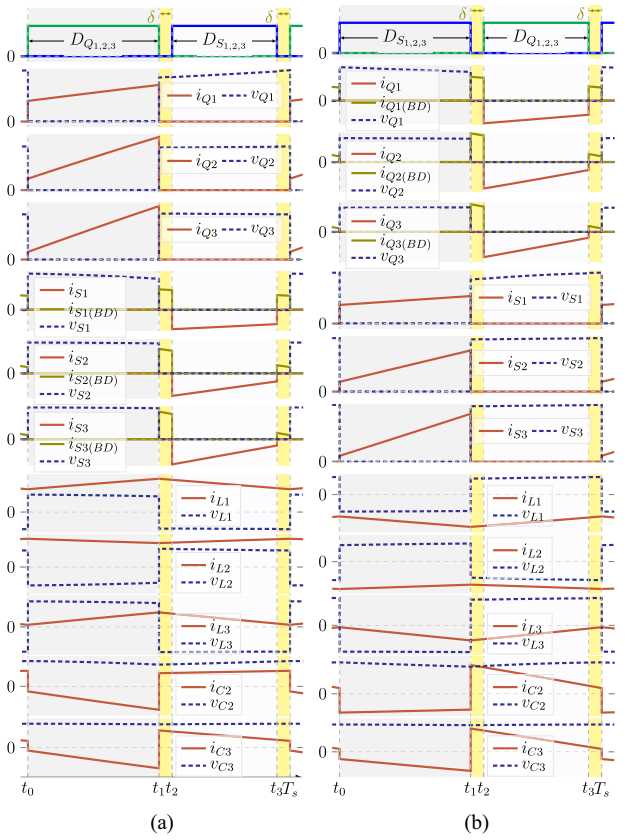


Fig. 4. Typical waveforms of (a) step-up and (b) step-down modes.

S_2 , and S_3 are turned OFF in ZVS mode while the body diodes are conducting.

The equations representing the steady-state conditions are provided below:

$$\begin{cases} v_{L1} = V_{LV} - V_{C3} \\ v_{L2} = -V_{C2} + V_{C3} \\ v_{L3} = V_{C3} - V_{HV} \end{cases}, \begin{cases} i_{C2} = i_{L2} \\ i_{C3} = i_{L1} - i_{L2} - i_{L3} \\ i_{C4} = i_{L3} - i_{HV}. \end{cases} \quad (2)$$

Applying the volt-second balance principle to the inductors for the step-up mode

$$\begin{cases} \overline{V_{L1}} = DT_s(V_{LV} + V_{C2}) + (1 - D)T_s(V_{LV} - V_{C3}) = 0 \\ \overline{V_{L2}} = DT_s(-V_{C2}) + (1 - D)T_s(-V_{C2} + V_{C3}) = 0 \\ \overline{V_{L3}} = DT_s(V_{C2} + V_{C3}) + (1 - D)T_s(V_{C3} - V_{HV}) = 0 \end{cases} \quad (3)$$

where D is the duty cycle of switches Q_1 , Q_2 , and Q_3 .

Therefore, the voltages across capacitors C_2 and C_3 are

$$V_{C2} = \frac{1}{1 - D} V_{LV}, \quad V_{C3} = \frac{1}{(1 - D)^2} V_{LV}. \quad (4)$$

Finally, the voltage gain ratio of the proposed converter in step-up mode is

$$M_{\text{step-up}} = \frac{V_{HV}}{V_{LV}} = \frac{1 + D - D^2}{(1 - D)^3}. \quad (5)$$

TABLE I
 VOLTAGE AND CURRENT OF SWITCHES IN STEP-UP MODE

Switch	Voltage	Current
Q_1	V_{C2}	$i_{L1} + i_{L3}$
Q_2	V_{C3}	$i_{L1} - i_{L2} + i_{L3}$
Q_3	$V_{HV} - V_{C3}$	i_{L3}
S_1	V_{C2}	i_{L1}
S_2	V_{C3}	$i_{L1} - i_{L2}$
S_3	$V_{C2} + V_{HV}$	i_{L3}

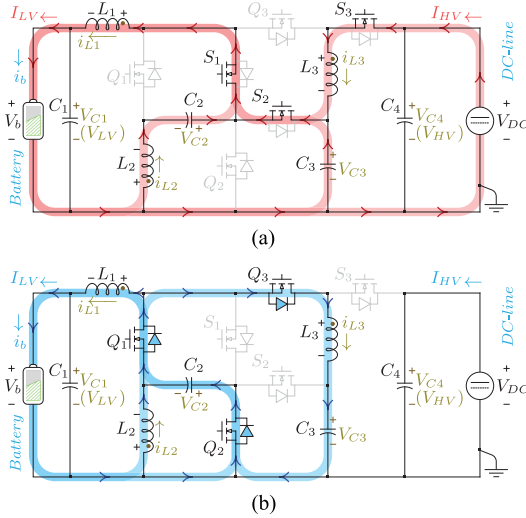


Fig. 5. Equivalent circuit of the proposed bidirectional DC-DC converter during the step-down (a) stage-I and (b) stage-II.

Applying the amp-second balance principle to the capacitors for the step-up mode

$$\begin{cases} \overline{I_{C2}} = DT_s(-I_{L1} + I_{L2} - I_{L3}) + (1-D)T_s(I_{L2}) = 0 \\ \overline{I_{C3}} = DT_s(-I_{L3}) + (1-D)T_s(I_{L1} - I_{L2} - I_{L3}) = 0 \\ \overline{I_{C4}} = DT_s(-I_{HV}) + (1-D)T_s(I_{L3} - I_{HV}) = 0. \end{cases} \quad (6)$$

Therefore, the current through inductors L_1 , L_2 , and L_3 are

$$I_{L1} = \frac{1+D-D^2}{(1-D)^3} I_{HV}, I_{L2} = \frac{2D-D^2}{(1-D)^3} I_{HV}, I_{L3} = \frac{I_{HV}}{1-D}. \quad (7)$$

Table I provides the ON-state current and OFF-state voltage of the switches for the step-up mode.

B. Step-Down (charging) Operation Mode

In the step-down operation mode, the system charges the battery using the dc-link source. This process involves transferring energy from the HV dc link to the battery, which operates at a lower voltage.

In the first stage of this mode, illustrated in Fig. 5(a), switches S_1 , S_2 , and S_3 are activated. At this stage, the body diodes of Q_1 , Q_2 , and Q_3 are in a reverse-biased. During this phase, as depicted in Fig. 4(b) from t_0 to t_1 , inductors L_1 and L_3 are charged through switches S_1 , S_2 , and S_3 via the dc source of V_{DC} and the battery is charging. In addition, inductor L_1 is charged by capacitor C_3 via switches S_1 and S_2 , and it the released energy stored from capacitor C_2 and inductor L_2 through switch S_1 .

The corresponding steady-state equations are provided below:

$$\begin{cases} v_{L1} = V_{C3} - V_{LV} \\ v_{L2} = V_{C2} - V_{C3} \\ v_{L3} = V_{HV} - V_{C3} \end{cases}, \begin{cases} i_{C2} = -i_{L2} \\ i_{C3} = -i_{L1} + i_{L2} + i_{L3} \\ i_{C4} = -i_{L3} + i_{HV}. \end{cases} \quad (8)$$

In the second stage, depicted in Fig. 5(b), switches S_1 , S_2 , and S_3 are switched OFF. Moreover, the body diodes Q_1 , Q_2 , and Q_3 become forward biased. Following a dead time of δT_s from t_1 to t_2 , switches Q_1 , Q_2 , and Q_3 are activated by gate signals. This approach ensures that switches Q_1 , Q_2 , and Q_3 turn ON in ZVS mode, as depicted in Fig. 4(b) from t_2 to t_3 . During this stage, inductor L_1 discharges through the battery and C_2 via Q_1 and Q_2 , and discharges into L_2 via Q_1 . Energy from inductor L_3 is released to capacitors C_2 and C_3 via Q_1 , Q_2 , and Q_3 . From t_3 to T_s , switches Q_1 , Q_2 , and Q_3 are turned OFF in ZVS mode while their body diodes are conducting.

The equations representing the steady-state conditions are provided below:

$$\begin{cases} v_{L1} = -V_{C2} - V_{LV} \\ v_{L2} = V_{C2} \\ v_{L3} = -V_{C2} - V_{C3} \end{cases}, \begin{cases} i_{C2} = i_{L1} - i_{L2} + i_{L3} \\ i_{C3} = i_{L3} \\ i_{C4} = i_{HV}. \end{cases} \quad (9)$$

Applying the volt-second balance principle to the inductors for the step-down mode

$$\begin{cases} \overline{V_{L1}} = DT_s(V_{C3} - V_{LV}) + (1-D)T_s(-V_{LV} - V_{C2}) = 0 \\ \overline{V_{L2}} = DT_s(V_{C2} - V_{C3}) + (1-D)T_s(V_{C2}) = 0 \\ \overline{V_{L3}} = DT_s(V_{HV} - V_{C3}) + (1-D)T_s(-V_{C2} - V_{C3}) = 0. \end{cases} \quad (10)$$

Therefore, the voltages across capacitors C_2 and C_3 are

$$V_{C2} = \frac{D^2}{1+D-D^2} V_{HV}, V_{C3} = \frac{D}{1+D-D^2} V_{HV} \quad (11)$$

Finally the voltage gain ratio of the proposed converter in step-down mode is:

$$M_{\text{step-down}} = \frac{V_{LV}}{V_{HV}} = \frac{D^3}{1+D-D^2}. \quad (12)$$

Applying the amp-second balance principle to the capacitors for the step-down mode

$$\begin{cases} \overline{I_{C2}} = DT_s(-I_{L2}) + (1-D)T_s(I_{L1} - I_{L2} + I_{L3}) \\ \overline{I_{C3}} = DT_s(-I_{L1} + I_{L2} + I_{L3}) + (1-D)T_s(I_{L3}) \\ \overline{I_{C4}} = DT_s(-I_{L3} + I_{HV}) + (1-D)T_s(I_{HV}). \end{cases} \quad (13)$$

Therefore, the current through inductors L_1 , L_2 , and L_3 are

$$I_{L1} = I_{LV}, I_{L2} = \frac{(1-D^2)I_{LV}}{1+D-D^2}, I_{L3} = \frac{D^2 I_{LV}}{1+D-D^2}. \quad (14)$$

Table II provides the ON-state current and OFF-state voltage of the switches for the step-down mode.

C. Design Considerations

By choosing a switching frequency (f_s), the voltage ripples of capacitors (Δv_{C1} , Δv_{C2} , Δv_{C3} , and Δv_{C4}) and current ripples of inductors (Δi_{L1} , Δi_{L2} , and Δi_{L3}), the values of the passive

TABLE II
VOLTAGE AND CURRENT OF SWITCHES IN STEP-DOWN MODE

Switch	Voltage	Current
Q_1	V_{C2}	$i_{L1} + i_{L3}$
Q_2	V_{C3}	$i_{L1} - i_{L2} + i_{L3}$
Q_3	$V_{HV} - V_{C3}$	i_{L3}
S_1	V_{C2}	i_{L1}
S_2	V_{C3}	$i_{L1} - i_{L2}$
S_3	$V_{C2} + V_{HV}$	i_{L3}

components can be calculated as follows:

$$\begin{aligned}
 \text{Step - up : } & \begin{cases} L_1 \geq \frac{D(2-D)V_{LV}}{f_s(1-D)\Delta i_{L1}} \\ L_2 \geq \frac{DV_{LV}}{f_s(1-D)\Delta i_{L2}} \\ L_3 \geq \frac{D(2-D)V_{LV}}{f_s(1-D)^2\Delta i_{L3}} \end{cases}, \\
 & \begin{cases} C_2 \geq \frac{D(2-D)I_{HV}}{f_s(1-D)^2\Delta v_{C2}} \\ C_3 \geq \frac{DI_{HV}}{f_s(1-D)\Delta v_{C3}} \\ C_4 \geq \frac{DI_{HV}}{f_s\Delta v_{C4}} \end{cases} \quad (15) \\
 \text{Step - down : } & \begin{cases} L_1 \geq \frac{(1-D^2)V_{LV}}{f_s D \Delta i_{L1}} \\ L_2 \geq \frac{f_s \Delta i_{L2}}{(1+D)V_{LV}} \\ L_3 \geq \frac{(1+D)V_{LV}}{f_s D \Delta i_{L3}} \end{cases}, \begin{cases} C_1 \geq \frac{\Delta i_{L1}}{8\Delta v_{C1} f_s} \\ C_2 \geq \frac{(1-D^2)I_{HV}}{f_s D^2 \Delta v_{C2}} \\ C_3 \geq \frac{(1-D)I_{HV}}{f_s D \Delta v_{C3}} \end{cases}. \quad (16)
 \end{aligned}$$

From the above equations and considering the following parameters: $V_{LV} = 40$ V, $V_{HV} = 400$ V, $D = 0.5$, $f_s = 20$ kHz, $P = 500$ W, $\Delta i_{L1} = 1$ A, $\Delta i_{L2} = 5$ A, $\Delta i_{L3} = 4$ A, $\Delta v_{C1} = 0.6$ V, $\Delta v_{C2} = 25$ V, $\Delta v_{C3} = 8$ V, and $\Delta v_{C4} = 0.03$ V, the minimum values of the passive components are calculated as follows: $L_1 = 3$ mH, $L_2 = 0.4$ mH, $L_3 = 1.5$ mH, $C_1 = 10$ μ F, $C_{2,3} = 8$ μ F, and $C_4 = 1000$ μ F.

III. RCG AND DEADBEAT BATTERY CURRENT CONTROL SYSTEM DESIGN

The control system is based on a two-loop deadbeat controller, which includes the inner control of the battery or LV side current and outer LV voltage control loop. The control strategy of the proposed converter involves the regulation of both current and voltage on the LV side, corresponding to battery current during constant current (CC) mode and battery voltage during constant voltage (CV) mode. The comprehensive diagram of the control system is depicted in Fig. 6.

The charging process begins with the charger assessing the battery voltage against a precharge threshold. If the voltage is below this threshold, indicating deep discharge, the charger initiates trickle charging. This involves charging the battery at a low rate, typically 10% of its full charging capacity. This slow charging method is employed to prevent damage from high surge currents. Trickle charging continues until the battery

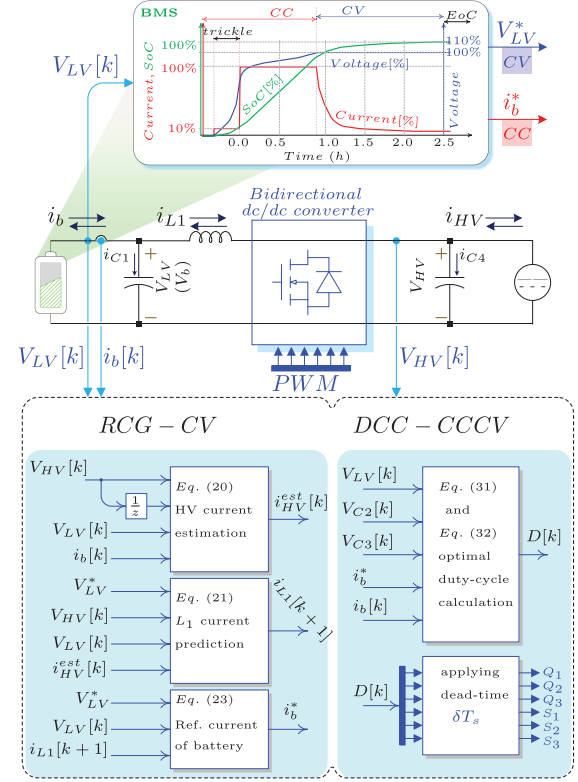


Fig. 6. Proposed RCG and control system.

voltage reaches its minimum charging voltage, typically 60% of cell voltage. Failure to reach this voltage level may indicate potential battery damage. Once the battery voltage surpasses the precharge threshold, the charger transitions to normal charging mode, delivering the full charge current. Charging starts in CC mode, during which the cell voltage steadily rises until it reaches the CV threshold. Upon reaching the CV threshold, the charger switches to CV mode. Here, the charging current gradually decreases to maintain a steady voltage as the battery approaches full charge. Eventually, the charge current reduces to a very low level. The charger monitors the current flow, and when it drops to 10% of the full charging rate, signaling the end of charge (EoC) stage, the charger ceases charging, ensuring the battery is fully charged and protected from overcharging.

For the proposed converter, a digital deadbeat current control (DCC) approach is employed for bidirectional operation. The LV-side voltage reference (V_{LV}^* or V_{bat}^*) is typically set to the full-charge voltage of the battery. When the battery is not fully charged, the LV-side current reference (I_{LV}^* or I_b^*) is determined accordingly in reference current generation (RCG) loop.

A. RCG Loop

In the CV mode, to generate the reference of battery current, we start by considering battery side power equals to HV side power

$$P_{\text{battery}} = P_{HV} \quad (17)$$

$$\begin{cases} V_{LV}I_b = V_{HV}(i_{HV} + i_{C4}); & \text{dis.} \\ V_{LV}I_b = V_{HV}(i_{HV} - i_{C4}); & \text{char.} \end{cases} \quad (18)$$

Therefore, the HV side current is

$$\begin{cases} i_{HV}(t) = \frac{V_{LV}(t)}{V_{HV}(t)}I_b(t) - C_4 \frac{dv_{C4}}{dt}; & \text{dis.} \\ i_{HV}(t) = \frac{V_{LV}(t)}{V_{HV}(t)}I_b(t) + C_4 \frac{dv_{C4}}{dt}; & \text{char.} \end{cases} \quad (19)$$

From discrete backward Euler method the estimated value of the HV side current is

$$\begin{cases} i_{HV}^{\text{est}}[k] = \frac{V_{LV}[k]}{V_{HV}[k]}I_b[k] - \frac{C_4}{T_s}(V_{HV}[k] - V_{HV}[k-1]) \\ \text{dis.} \\ i_{HV}^{\text{est}}[k] = \frac{V_{LV}[k]}{V_{HV}[k]}I_b[k] + \frac{C_4}{T_s}(V_{HV}[k] - V_{HV}[k-1]) \\ \text{char.} \end{cases} \quad (20)$$

In [56], the determination of the reference current for the inner loop involves the utilization of the power balance equation. To enhance the transient response of the output voltage, an additional term, proportional to the voltage error between reference voltage and actual, i.e., $V_{LV}^* - V_{LV}$, is incorporated. Consequently, the expression for the predicted value of L_1 current (i_{L1}^*) is as follows:

$$i_{L1}[k+1] = \frac{V_{HV}[k]}{V_{LV}[k]} \times i_{HV}^{\text{est}}[k] + h(V_{LV}^* - V_{LV}[k]) \quad (21)$$

with $h \in \mathbb{R}^+$.

By applying KCL in the LV side, the battery side current is

$$\begin{cases} i_b(t) = i_{L1}(t) + C_1 \frac{dV_{LV}}{dt}; & \text{dis.} \\ i_b(t) = i_{L1}(t) - C_1 \frac{dV_{LV}}{dt}; & \text{char.} \end{cases} \quad (22)$$

One can assume that the error between the reference battery or LV side voltage (V_{LV}^*) and the predicted voltage ($V_{LV}[k+1]$) is zero. This assumption serves as the basis for determining the duty cycle required to achieve precise alignment between the reference and predicted voltages, ensuring effective control and regulation within the converter. Finally, the expression for the reference battery current (i_b^*) is predicted as follows:

$$\begin{cases} i_b^* = i_{L1}[k+1] + (V_{LV}^* - V_{LV}[k]) \frac{C_1}{T_s}; & \text{dis.} \\ i_b^* = i_{L1}[k+1] - (V_{LV}^* - V_{LV}[k]) \frac{C_1}{T_s}; & \text{char.} \end{cases} \quad (23)$$

B. DCC in CCCV Mode

When determining the reference battery side current, it is set to 100% of the battery's full charging capacity during CC periods. During CV periods, the reference current is obtained from the RCG loop. To ensure that the battery current does not exceed a certain limit, the RCG is employed. This controller includes a limiter, which caps the output of controller, setting the battery current reference (i_b^*) to the upper limit value defined by the limiter.

During the first and second stage of step-up operation mode, when $Q_{1,2,3}$ are ON and OFF, the voltage across the inductor L_1 can be determined as

$$\begin{cases} v_{L1} = L_1 \frac{di_{L1}}{dt} = V_{LV} + V_{C2}; & 0 \leq t \leq DT_s \\ v_{L1} = L_1 \frac{di_{L1}}{dt} = V_{LV} - V_{C3}; & DT_s \leq t \leq T_s. \end{cases} \quad (24)$$

Similarly, during the first and second stage of step-down operation mode, when $S_{1,2,3}$ are ON and OFF, the voltage across the inductor L_1 can be determined as

$$\begin{cases} v_{L1} = L_1 \frac{di_{L1}}{dt} = -V_{LV} + V_{C3}; & 0 \leq t \leq DT_s \\ v_{L1} = L_1 \frac{di_{L1}}{dt} = -V_{LV} - V_{C2}; & DT_s \leq t \leq T_s. \end{cases} \quad (25)$$

The slope of inductor current during step-up (step-down) mode and when the switches are ON and OFF are as follows:

$$\begin{aligned} \delta_{Q_{1,2,3,ON}} &= \frac{di_{L1}}{dt} = \frac{V_{LV} + V_{C2}}{L_1}, \\ \delta_{S_{1,2,3,ON}} &= \frac{di_{L1}}{dt} = \frac{-V_{LV} + V_{C3}}{L_1} \end{aligned} \quad (26)$$

$$\begin{aligned} \delta_{Q_{1,2,3,OFF}} &= \frac{di_{L1}}{dt} = \frac{V_{LV} - V_{C3}}{L_1}, \\ \delta_{S_{1,2,3,OFF}} &= \frac{di_{L1}}{dt} = \frac{-V_{LV} - V_{C2}}{L_1}. \end{aligned} \quad (27)$$

Applying the Euler prediction rule [57], [58], [59], the next step in forecasting the inductor current involves leveraging the current state information and utilizing the established relationships between the system variables. By considering the instantaneous conditions, including the state of switches, along with the measured values of V_{LV} and $V_{C2,3}$, and the currents through the inductor L_1 , the prediction algorithm computes the predicted value of the inductor current in the subsequent time step

$$\begin{cases} i_{L1}[k+1] = i_{L1}[k] + \delta_{Q_{1,2,3,ON}}DT_s + \delta_{Q_{1,2,3,OFF}}(1-D)T_s \\ i_{L1}[k+1] = i_{L1}[k] + \delta_{S_{1,2,3,ON}}DT_s + \delta_{S_{1,2,3,OFF}}(1-D)T_s. \end{cases} \quad (28)$$

Therefore, from (22), the predicted value of battery current during step-up mode can be obtained as

$$\begin{aligned} i_b[k+1] &= i_b[k] + \frac{C_1}{T_s} \{V_{LV}[k+1] - 2V_{LV}[k] + V_{LV}[k-1]\} \\ &+ \frac{V_{LV}[k] + V_{C2}[k]}{L_1} D[k]T_s + \frac{V_{LV}[k] - V_{C3}[k]}{L_1} (1-D[k])T_s. \end{aligned} \quad (29)$$

Similarly, during the step-down mode, the predicted battery current is

$$\begin{aligned} i_b[k+1] &= i_b[k] - \frac{C_1}{T_s} \{V_{LV}[k+1] - 2V_{LV}[k] + V_{LV}[k-1]\} \\ &- \frac{V_{LV}[k] - V_{C3}[k]}{L_1} D[k]T_s - \frac{V_{LV}[k] + V_{C2}[k]}{L_1} (1-D[k])T_s. \end{aligned} \quad (30)$$

Finally, by minimizing the error between the reference battery current (i_b^*) and the predicted battery current ($i_b[k+1]$), one

can determine the optimal duty cycle during step-up and step-down as (31) and (32) are shown at the bottom of the next page, respectively, [60], [61], [62], [63], [64], [65].

C. Stability of the Proposed Controller

The discrete-time model of the proposed system is formulated using the backward difference method. This approach captures the system dynamics within a discrete-time framework, and the resulting model is expressed as follows:

$$\begin{aligned}
 i_{L1}[k] &= \frac{T_s \left\{ u[k]v_{C2}[k] - (1 - u[k])v_{C3}[k] + V_{LV}[k] \right\}}{L_1(z - 1)} \\
 i_{L2}[k] &= \frac{T_s \left\{ -v_{C2}[k] + (1 - u[k])v_{C3}[k] \right\}}{L_2(z - 1)} \\
 i_{L3}[k] &= \frac{T_s \left\{ u[k]v_{C2}[k] + v_{C3}[k] - (1 - u[k])v_{C4}[k] \right\}}{L_3(z - 1)} \\
 v_{C2}[k] &= \frac{T_s \left\{ -u[k]i_{L1}[k] + i_{L2}[k] - u[k]i_{L3}[k] \right\}}{C_2(z - 1)} \\
 v_{C3}[k] &= \frac{T_s \left\{ (1 - u[k])i_{L1}[k] - (1 - u[k])i_{L2}[k] - i_{L3}[k] \right\}}{C_3(z - 1)} \\
 v_{C4}[k] &= \frac{T_s \left\{ (1 - u[k])i_{L3}[k] - v_{C4}[k]/R \right\}}{C_4(z - 1)}. \quad (33)
 \end{aligned}$$

Considering the CV at the LV side during the sampling period, where $V_{LV}[k + 1] = V_{LV}[k] = V_{LV}[k - 1]$, in (23) and (31), the control command is derived as

$$u[k] = \frac{L_1(i_b^* - i_b[k])}{(V_{C2} + V_{C3})T_s} - \frac{V_{LV}[k] - V_{C3}[k]}{V_{C2} + V_{C3}}. \quad (34)$$

From (34), the accuracy of the modulation function $u[k]$ is influenced by the LV-side equivalent inductance L_1 . A mismatch in the inductance parameter affects the control accuracy of the current loop and may even result in system instability. The structure of the current loop of the proposed scheme is illustrated in Fig. 7, where $G_c(z)$ and $G_p(z)$ represent the controller and converter models, respectively. Let L_m denote the inductance value used in the proposed scheme, and λ represent the inductance parameter mismatch ratio, defined as $L_m = \lambda L_1$

$$u[k] = \frac{\frac{L_m}{T_s}(i_{L1}[k + 1] - i_{L1}[k]) - V_{LV}[k] + v_{C3}[k]}{v_{C2}[k] + v_{C3}[k]}. \quad (35)$$

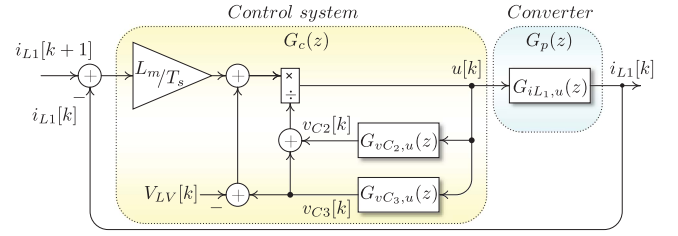


Fig. 7. Block diagram of the inner-loop control system.

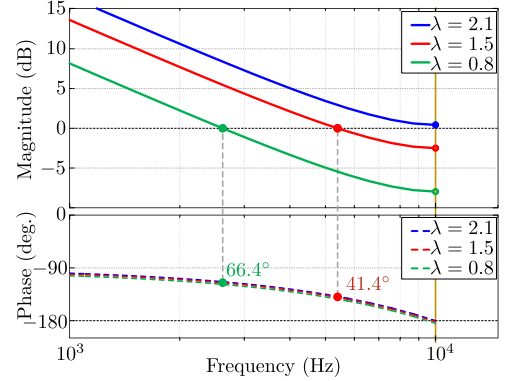


Fig. 8. Bode diagram of $G_o(z)$ for different λ ($\lambda = 2.1, 1.5, 0.8$).

Based on (33) and (35), $G_p(z)$ and $G_c(z)$ are derived as follows:

$$G_c(z) = \frac{u[k]}{i_{L1}[k + 1] - i_{L1}[k]}, \quad G_p(z) = \frac{i_{L1}[k]}{u[k]}. \quad (36)$$

The z -domain open-loop transfer function of the current loop can be derived as [66], [67], [68], [69]

$$G_o(z) = G_c(z) \cdot G_p(z) = \frac{\lambda}{z - 1}. \quad (37)$$

From (37), the z -domain closed-loop transfer function $G(z)$ of the current loop can be derived as

$$G(z) = \frac{\lambda}{z - 1 + \lambda}. \quad (38)$$

Thus, the characteristic equation of the closed-loop system is derived as

$$z - 1 + \lambda = 0. \quad (39)$$

According to *Routh's* stability criterion, the system remains stable within the range $0 < \lambda < 2$.

The dynamic characteristics of the current control loop are evaluated through the Bode plot of the open-loop transfer function, $G_o(z)$, as shown in Fig. 8. The analysis highlights that for the parameter range $0 < \lambda < 2$, the phase margin remains

$$D[k] = \frac{L_1(i_b^* - i_b[k] - \frac{C_1}{T_s}\{V_{LV}[k + 1] - 2V_{LV}[k] + V_{LV}[k - 1]\})}{(V_{C2} + V_{C3})T_s} - \frac{V_{LV}[k] - V_{C3}[k]}{V_{C2} + V_{C3}} \quad (31)$$

$$D[k] = \frac{L_1(i_b^* - i_b[k] + \frac{C_1}{T_s}\{V_{LV}[k + 1] - 2V_{LV}[k] + V_{LV}[k - 1]\})}{(V_{C2} + V_{C3})T_s} - \frac{V_{LV}[k] - V_{C3}[k]}{V_{C2} + V_{C3}}. \quad (32)$$

consistently positive. This observation confirms that the current control loop maintains stable operation within the specified range, ensuring reliable system performance.

IV. COMPARATIVE STUDY

Table III provides general information on the characteristics of the main recent bidirectional dc–dc converters along with the proposed converter. Certain structures, such as those referenced in [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], and [21], encounter challenges due to a lack of common ground between input and output terminals. The converters referenced in [10], [13], [14], [15], [16], [18], [19], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], and [32] are incapable of Syn. operation. This inability limits their capacity to minimize losses typically associated with the body diode of switches. In addition, converters in [9], [12], [16], [19], and [33] exhibit discontinuous current flow at the battery side. This discontinuity can have adverse effects on the longevity of the EV battery pack.

In Fig. 9, we compare the voltage gain ratio of the proposed converter during the step-up mode with other bidirectional dc–dc converters. The findings show that the proposed converter achieves the highest wide voltage gain ratio compared to those converters in Table III. However, it is worth noting that the converters, such as the converter presented in [7], demonstrates a higher voltage gain ratio for gains below 10. Nonetheless, it is inactive for voltage gains lower than 3. Consequently, the proposed converter presents the widest range of voltage gain in the step-up mode compared to other structures. In addition, as demonstrated in Fig. 9, the quadratic voltage gain converters in [24], [25], [26], [27], and [55] and the converters in [28] and [29] emerge as primary competitors to the proposed converter in terms of voltage gain during step-up mode.

In the same vein, in the step-down mode (as illustrated in Fig. 10), the converter we propose demonstrates the lowest voltage gain ratio compared to all other bidirectional converters, and this ratio remains unrestricted.

Moreover, a comparative analysis can be conducted between the proposed converter and its main competitors cited in [16], [25], [28], [27], [29], and [55], focusing on the normalized TVS devices (TVS/V_{HV}) and the normalized TCS devices (TCS/I_{HV}), as depicted in Fig. 11 and Table IV. Although converters, such as those in [38], [46], and [48], achieve HV gain, they also exhibit high switch current stress, particularly at the LV side. This can impact efficiency and reliability, especially under dynamic conditions.

As a result, it is observed that the proposed converter demonstrates a lower TVS compared to the converter in [16] and marginally lower than the converter in [29]. Furthermore, the TCS of the proposed converter is lower than that of the main competitors mentioned in [16], [25], [27], [28], and [29] during step-down operation. This indicates that the proposed converter has a lower current stress on its semiconductor devices. Lower current stress can reduce thermal losses and improve the overall efficiency of the converter, as well as extend the lifespan of the semiconductor devices by reducing the likelihood of thermal

TABLE III
COMPARISON AMONG MAIN BIDIRECTIONAL DC–DC CONVERTERS

Ref.	Number of Elements Utilised†:	Conducting Semi. at 1 and 2:	CG? Syn.? CBC?‡	$M_{step-up}$, Ideal Voltage Gain range:	$M_{step-down}$, Ideal Voltage Gain range:
Proposed	6 S	3, 3	✓	$\frac{1+D-D^2}{(1-D)^3}$	$\frac{D^3}{1+D-D^2}$
	3 L, 4 C	3, 3	✓	$1-\infty$	$0-1$
			✓		
[53]	4 S	2, 2	✓	$\frac{1}{1-D}$	D ,
	1 L, 3 C	2, 2	✓	$1-\infty$	$0-1$
			✓		
[22]	4 S	2, 2	✓	$\frac{2}{1-D}$	$\frac{D}{2}$,
	1 L, 4 C	2, 2	×	$2-\infty$	$0-0.5$
			✓		
[6]	5 S	2, 2	×	$\frac{2}{1-D}$	$\frac{D}{2}$,
	2 L, 4 C	3, 3	✓	$2-\infty$	$0-0.5$
			✓		
[8]	3 S	1, 2	×	$\frac{0.5D}{1-D}$	$\frac{2D}{1-D}$,
	2 L, 4 C	2, 1	✓	$0-\infty$	$0-\infty$
			✓		
[23]	8 S	4, 3	✓	$\frac{3}{1-D}$	$\frac{D}{3}$,
	3 L, 6 C	4, 5	×	$3-\infty$	$0-1/3$
			✓		
[9]	3 S	2, 1	×	$\frac{1+D}{1-D}$	$\frac{D}{(2-D)}$,
	2 L, 2 C	1, 2	✓	$1-\infty$	$0-1$
			×		
[10]	3 S	2, 1	×	$\frac{1+D}{1-D}$	$\frac{D}{2-D}$,
	2 L, 4 C	2, 1	×	$1-\infty$	$0-1$
			✓		
[54]	3 S	1, 2	✓	$\frac{1+D}{1-D}$	$\frac{D}{(2-D)}$,
	2 L, 4 C	2, 1	✓	$1-\infty$	$0-1$
			✓		
[11]	3 S, 2 D	1, 2	×	$\frac{1+D}{1-D}$	$\frac{D}{(2-D)}$,
	3 L, 5 C	2, 1	✓	$1-\infty$	$0-1$
			✓		
[12]	4 S	2, 2	×	$\frac{1+D}{1-D}$	$\frac{D}{2-D}$,
	2 L, 4 C	2, 2	✓	$1-\infty$	$0-1$
			×		
[7]	6 S	3, 3	×	$\frac{3-D}{(1-D)^2}$	$\frac{D^2}{(2+D)}$,
	2 L, 5 C	3, 3	✓	$2-\infty$	$0-0.5$
			✓		
[55]	4 S	2, 2	✓	$\frac{1}{(1-D)^2}$	D^2 ,
	2 L, 3 C	2, 2	✓	$1-\infty$	$0-1$
			✓		
[24]	4 S, 2 D	3, 3	✓	$\frac{1}{(1-D)^2}$	D^2 ,
	2 L, 3 C	3, 2	×	$1-\infty$	$0-1$
			✓		
[25]	3 S, 2 D	2, 2	✓	$\frac{1}{(1-D)^2}$	D^2 ,
	2 L, 3 C	2, 2	×	$1-\infty$	$0-1$
			✓		
[26]	4 S	2, 2	✓	$\frac{1}{(1-D)^2}$	D^2 ,
	2 L, 3 C	2, 2	×	$1-\infty$	$0-1$
			✓		
[27]	4 S	2, 2	✓	$\frac{1}{(1-D)^2}$	D^2 ,
	2 L, 3 C	2, 2	×	$1-\infty$	$0-1$
			✓		
[28]	5 S	3, 2	✓	$\frac{1+D}{(1-D)^2}$	$\frac{D^2}{2-D}$,
	2 L, 4 C	2, 3	×	$1-\infty$	$0-1$
			✓		
[29]	4 S, 2 D	2, 3	✓	$\frac{1+D}{(1-D)^2}$	$\frac{D^2}{2-D}$,
	3 L, 5 C	3, 2	×	$1-\infty$	$0-1$
			✓		

TABLE III
(CONTINUED)

Ref.	Number of Elements Utilised†:	Conducting Semi. at 1 and 2:	CG? Syn.? CBC?	$M_{step-up}$, Ideal Voltage Gain range:	$M_{step-down}$, Ideal Voltage Gain range:
[13]	3 S 2 L, 4 C	2, 1 1, 2	× × ✓	$\frac{2D}{1-D}$, 0 – ∞	$\frac{D}{2(1-D)}$, 0 – ∞
[30]	5 S 2 L, 4 C	2, 3 3, 2	✓ × ✓	$\frac{1+D}{D(1-D)}$, 5.83 – ∞	$\frac{D(1-D)}{1+D}$, 0 – 0.17
[14]	7 S 2 L, 6 C	3, 4 4, 3	× × ✓	$\frac{3+D}{(1-D)^2}$, 3 – ∞	$\frac{D^2}{4-D}$, 0 – 1/3
[34]	5 S 3 L, 5 C	3, 2 2, 3	× ✓ ✓	$\frac{2-D}{(1-D)^2}$, 2 – ∞	$\frac{D^2}{1+D}$, 0 – 0.5
[33]	5 S 2 L, 4 C	3, 2 2, 3	✓ ✓ ×	$\frac{2-D}{(1-D)^2}$, 2 – ∞	$\frac{D^2}{1+D}$, 0 – 0.5
[15]	4 S 3 L, 6 C	1, 3 3, 1	× × ✓	$\frac{1+2D}{1-D}$, 1 – ∞	$\frac{D}{3-2D}$, 0 – 1
[16]	4 S 2 L, 3 C	2, 2 2, 2	× × ×	$\frac{D(2-D)}{(1-D)^2}$, 0 – ∞	$\frac{D^2}{1-D^2}$, 0 – ∞
[17]	6 S 2 L, 5 C	2, 3 3, 2	× ✓ ✓	$\frac{4}{1-D}$, 4 – ∞	$\frac{D}{4}$, 0 – 1/4
[31]	3 S 2 L, 4 C	2, 1 2, 1	✓ × ✓	$\frac{2-D}{1-D}$, 2 – ∞	$\frac{1-D}{2-D}$, 0 – 1/2
[35]	3 S 2 L, 5 C	1, 2 2, 1	✓ ✓ ✓	$\frac{2-D}{1-D}$, 2 – ∞	$\frac{D}{1+D}$, 0 – 1/2
[18]	6 S, 1 D 2 L, 6 C	3, 3 3, 3	× × ✓	$\frac{2}{1-2D}$, 2 – ∞	$\frac{D^2}{1+D}$, 0 – 1/2
[32]	4 S 3 L, 4 C	2, 2 2, 2	✓ × ✓	$\frac{D^2}{(1-D)^2}$, 0 – ∞	$\frac{D^2}{(1-D)^2}$, 0 – ∞
[19]	5 S 2 L, 4 C	2, 3 3, 2	× × ×	$\frac{3+D}{1-D}$, 3 – ∞	$\frac{D}{(4-D)}$, 0 – 1/3
[20]	5 S 2 L, 6 C	2, 5 5, 2	× ✓ ✓	$\frac{2+D}{1-D}$, 2 – ∞	$\frac{D}{(3-D)}$, 0 – 0.5
[21]	5 S 3 L, 5 C	3, 2 2, 3	× ✓ ✓	$\frac{2+D}{1-D}$, 2 – ∞	$\frac{D}{3-D}$, 0 – 1/3
[41]	5 S 3 L, 5 C	2, 3 3, 2	✓ ✓ ✓	$\frac{3-3D+D^3}{(1-D)^2}$, 3 – ∞	$\frac{D^2}{1+D+D^2}$, 0 – 1/3
[36]	6 S 2 L, 4 C	2, 2 2, 2	× ✓ ✓	$\frac{4}{1-D}$, 4 – ∞	$\frac{D}{4}$, 0 – 1/4
[38]	4 S 3 L, 4 C	2, 2 2, 2	× × ✓	$\frac{1+3D}{1-D}$, 1 – ∞	$\frac{D}{4-3D}$, 0 – 1
[39]	2 S, 2 D 3 L, 4 C	2, 2 2, 2	✓ ✓ ✓	$\frac{1}{1-D}$, 1 – ∞	$\frac{D}{D}$, 0 – 1

TABLE III
(CONTINUED)

Ref.	Number of Elements Utilised†:	Conducting Semi. at 1 and 2:	CG? Syn.? CBC?	$M_{step-up}$, Ideal Voltage Gain range:	$M_{step-down}$, Ideal Voltage Gain range:
[40]	4 S 3 L, 4 C	2, 2 2, 2	✓ × ✓	$\frac{1-D+D^2}{(1-D)^2}$, 1 – ∞	$\frac{D^2}{1-D+D^2}$, 0 – 1
[42]	4 S 2 L, 4 C	2, 2 2, 2	✓ ✓ ✓	$\frac{2}{1-D}$, 2 – ∞	$\frac{D}{2}$, 0 – 1/2
[37]	3 S 1 L, 3 C	2, 2 2, 2	× × ×	$\frac{2-D}{1-D}$, 2 – ∞	$\frac{D}{1+D}$, 0 – 1/2
[43]	6 S 2 L, 5 C	3, 4 4, 2	✓ ✓ ✓	$\frac{4}{1-D}$, 4 – ∞	$\frac{D}{4}$, 0 – 1/4
[44]	3 S, 3 D 3 L, 4 C	4, 2 2, 4	✓ ✓ ✓	$\frac{1+D}{1-D}$, 1 – ∞	$\frac{D(1-D)}{1+2(1-D)^2}$, 0 – 0.183
[45]	4 S 3 L, 5 C	2, 2 2, 2	✓ ✓ ✓	$\frac{2}{1-D}$, 2 – ∞	$\frac{D}{2}$, 0 – 1/2
[46]	4 S 2 L, 4 C	2, 2 2, 2	✓ × ✓	$\frac{2}{1-D}$, 2 – ∞	$\frac{D}{2}$, 0 – 1/2

† S: switch, D: diode, L: inductor, C: capacitor.

‡ CG: Common Ground, Syn.: Synchronous operation, CBC: Continuous Battery Current.

TABLE IV
RMS VALUE OF TOTAL VOLTAGE AND CURRENT STRESS

Ref.	TVS / V_{HV} Step-up, Step-down	TCS / I_{HV} Step-up, Step-down	Duty range Step-up, Step-down
Proposed	$\frac{6-5D+D^2}{1+D-D^2} = 3$ $\frac{2+3D+D^2}{1+D-D^2} = 3$	$\frac{2D^2-5D+5}{(1-D)^3} = 24$ $\frac{2(1+0.25D)^2}{D^3} = 20.25$	0.5 0.5
[28]	$\frac{6-2D}{1+D} = 3$ $\frac{4+2D}{2-D} = 3$	$\frac{5-2D}{(1-D)^2} = 23.75$ $\frac{4+2D}{D^2} = 30$	0.6 0.4
[16]	$\frac{4-2D}{D(2-D)} = 2.86$ $\frac{2+2D}{1-D^2} = 2.09$	$\frac{4-2D}{(1-D)^2} = 28.55$ $\frac{2+2D}{D^2} = 968$	0.698 0.0465
[27]	$4-2D = 2.64$ $2+2D = 2.64$	$\frac{4-2D}{(1-D)^2} = 25.78$ $\frac{2+2D}{D^2} = 25.78$	0.68 0.32
[29]	$\frac{5-D}{1+D} = 2.75$ $\frac{5+D}{2-D} = 3.375$	$\frac{3+D^2}{(1-D)^2} = 21$ $\frac{6-D+D^2}{D^2} = 36$	0.6 0.4
[55]	$4-3D = 1.96$ $2+3D = 2.96$	$\frac{3-D}{(1-D)^2} = 22.65$ $\frac{1+2D}{D^2} = 16.01$	0.68 0.32
[25]	$4-D = 3.32$ $\frac{1+3D}{D} = 6.125$	$\frac{5-2D}{(1-D)^2} = 35.55$ $\frac{3+2D}{D^2} = 35.54$	0.68 0.32

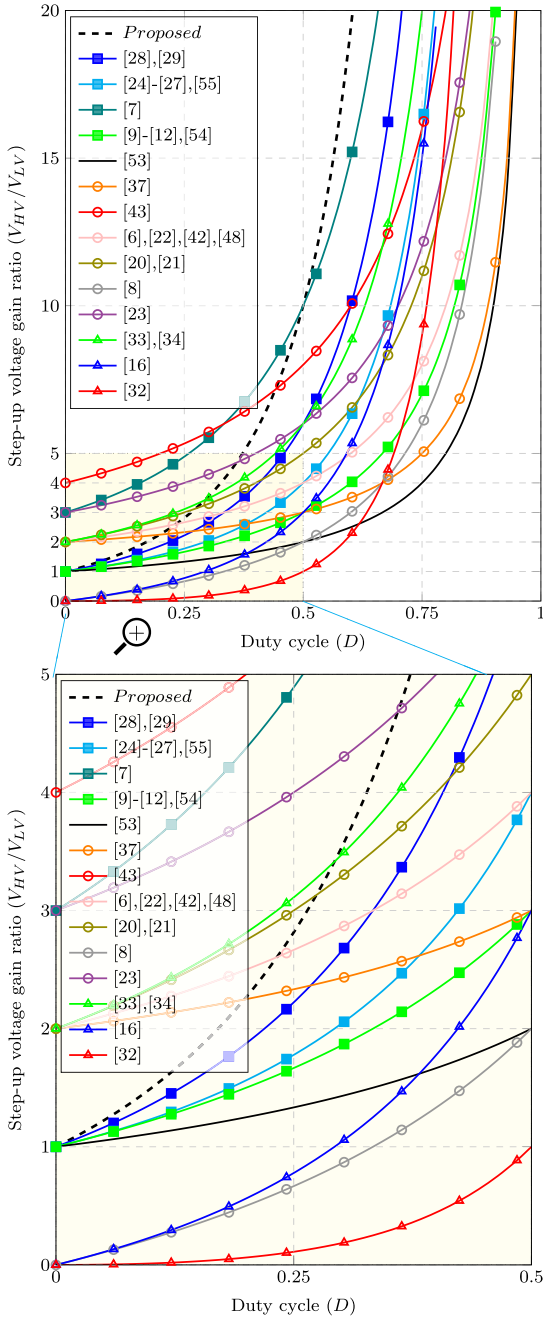


Fig. 9. Voltage gain ratio comparison during step-up direction.

and electrical degradation. The reduced TVS and TCS values in the proposed converter highlight its efficiency and robustness compared to other bidirectional dc–dc converters, making it a more reliable and effective solution for applications requiring efficient energy transfer and dynamic voltage matching.

A comparison between the proposed converter and other bidirectional converters, as detailed in Table III, reveals that our proposed converter boasts a lower count of semiconductor devices compared to the converters outlined in [14], [18], and [23].

In summary, the proposed converter demonstrates several advantages when compared to other converters that share the

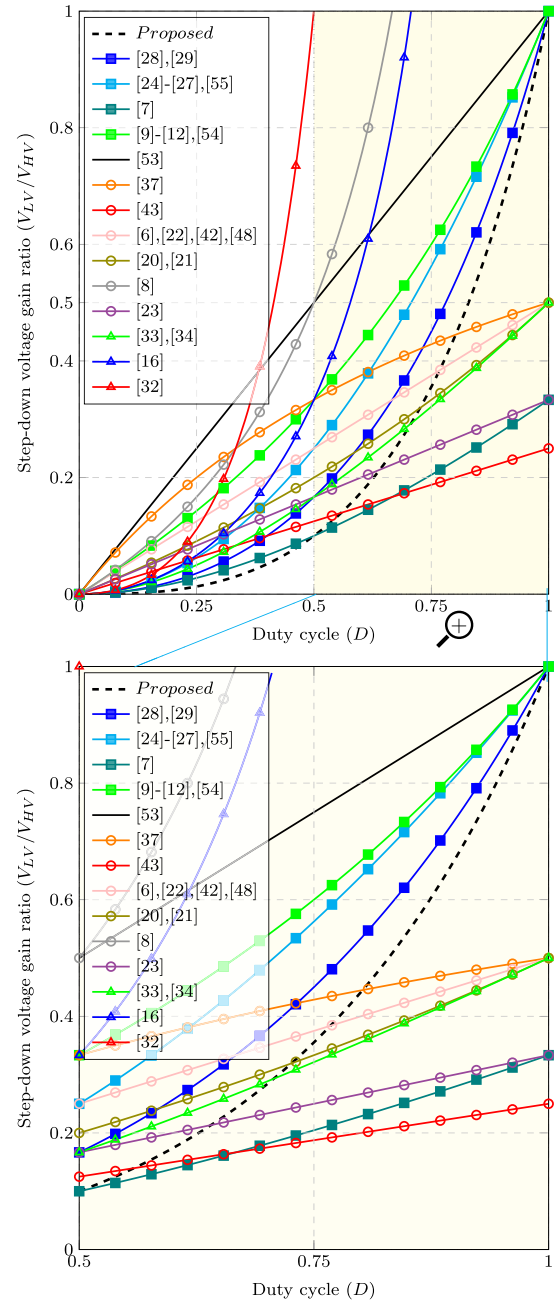


Fig. 10. Voltage gain ratio comparison during step-down direction.

combination of common ground, Syn. operation, and continuous battery current flow. The proposed converter exhibits a broader voltage gain range, achieving the highest wide voltage gain ratio in step-up mode and the lowest unrestricted voltage gain ratio in step-down mode. In addition, it shows a low normalized TVS and normalized TCS values, indicating reduced current stress and improved overall efficiency. These benefits, along with a lower count of semiconductor devices Conducting in each state, underscore the proposed converter’s efficiency, robustness, and reliability, making it a superior choice for applications requiring efficient energy transfer and dynamic voltage matching.

The proposed converter exhibits slightly higher voltage stress across semiconductor devices but significantly reduces current

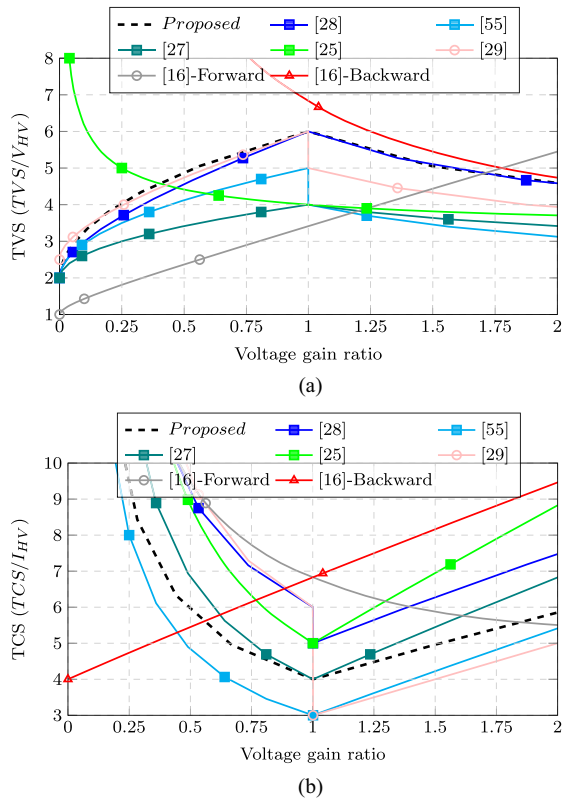


Fig. 11. Total (a) voltage and (b) current stress versus voltage gain ratio.

TABLE V
EXPERIMENTAL TEST CONDITIONS AND PARAMETERS

Parameters	Values
Rated power (P_{out}):	500 W
Switching frequency (f_s):	20 kHz
HV-side voltage (V_{HV}):	400 V
LV-side voltage (V_{LV}):	40 V
Battery source:	7×Ni-Cd batteries (4000mAh)
Inductors L_1 , L_2 , and L_3 :	3 mH, 0.4 mH, and 1.5 mH
Capacitors C_1 , C_2 , C_3 , and C_4 :	10 μ F, 8 μ F, 8 μ F, and 1000 μ F
MOSFETS $Q_{1,2,3}$ and $S_{1,2,3}$:	IPP60R016CM8
Control system:	OPAL-RT OP5600

stress, leading to lower power losses and minimized thermal stress, enhancing its overall performance and efficiency. As shown in Fig. 11, TVS and TCS are normalized by the HV-side voltage, V_{HV} , and HV-side current, I_{HV} , respectively. This normalization standardizes the results, facilitating a clear comparison with other designs.

As an example, Table IV illustrates the duty cycle and normalized TVS and TCS required to achieve a voltage gain ratio of 10 in step-up mode and 0.1 in step-down mode. While the proposed converter exhibits a relatively higher TVS compared to some other converters, it achieves a significantly lower TCS. This reduced TCS implies better efficiency by minimizing current-related losses, such as conduction losses and thermal stress, thereby enhancing the overall performance of the converter.

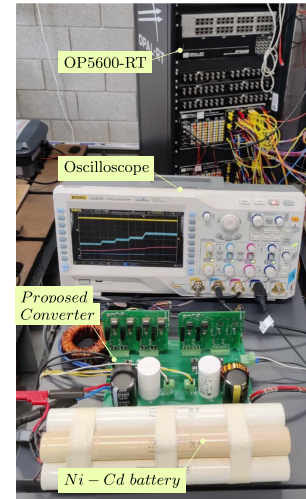


Fig. 12. Laboratory prototype of the proposed bidirectional DC-DC converter.

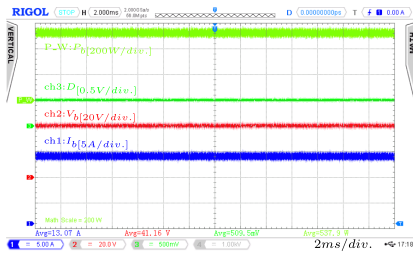
V. EXPERIMENTAL VERIFICATION

To validate the theoretical analysis and obtain experimental results, a prototype of the proposed bidirectional dc-dc converter charging and discharging a 40 V Nickel-cadmium (Ni-Cd) battery are utilized. The prototype is depicted in Fig. 12, and the components used in constructing the prototype are detailed in Table V. Three different tests are conducted to verify the theoretical achievements. First, the steady-state open-loop test was performed to analyze the system's performance under stable conditions without feedback control. Second, we measured the voltage and current of the switches and conducted a ZVS test. This test is crucial for reducing switching losses and ensuring the switches operate efficiently. Finally, we carried out a closed-loop test to evaluate the system's behavior with feedback control, which helps maintain the desired performance by adjusting the control inputs based on the system's output.

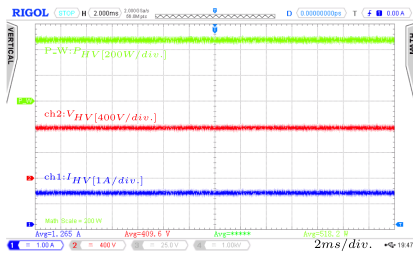
A. Steady-State Open-Loop Test

Fig. 13(a) presents the experimental outcomes concerning the input current, voltage, duty-cycle, and instantaneous power of step-up mode. Similarly, Fig. 13(b) displays the experimental results pertaining to the output current, voltage, and instantaneous power during discharge (boost) mode. From these figures, it is observed that the input and output powers measure 537.9 and 518.2 W, respectively. Consequently, the efficiency of the proposed converter during discharge mode is calculated to be 96.33%. In addition, at a duty cycle of 0.5 and a battery-side voltage of 41.16 V, the HV-side voltage is depicted as 409.6 V during discharge mode.

The experimental outcomes related to V_{C2} , V_{C3} , and V_{C4} are illustrated in Fig. 14(a). It is noted that the voltage across these capacitors agrees with the (4) and (5), given a battery-side voltage of 40 V and a duty cycle of 0.5, during step-up mode. The average voltages measured across capacitors C_2 , C_3 , and C_4 are 81.78, 161.8, and 405.6 V, respectively. Furthermore, the current passing through L_1 , L_2 , and L_3 , which traverses the active switches, is recorded and depicted in Fig. 14(b). The

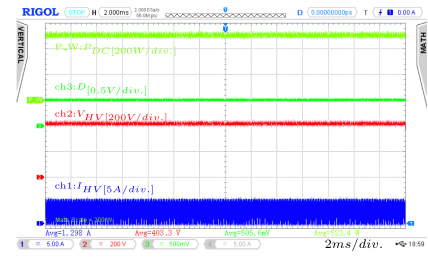


(a)

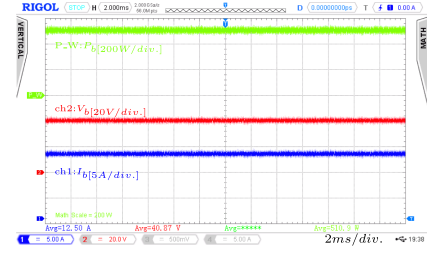


(b)

Fig. 13. Step-up operation mode (a) input voltage, current, power, and duty cycle and (b) output voltage, current, and power.

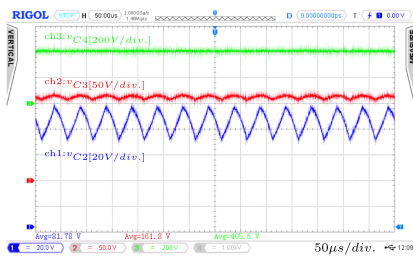


(a)

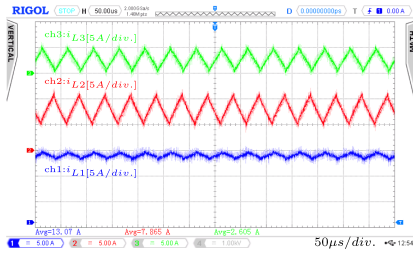


(b)

Fig. 15. Step-down operation mode (a) input voltage, current, power, and duty cycle and (b) output voltage, current, and power.

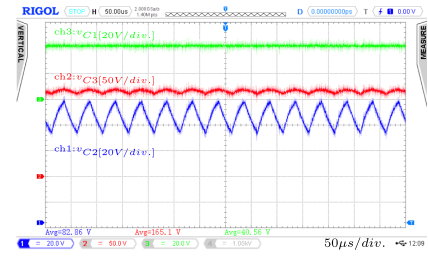


(a)

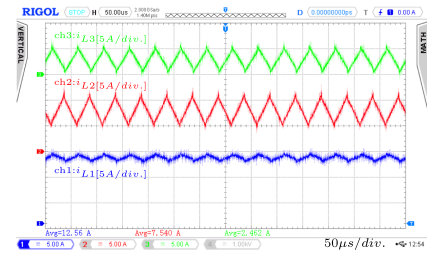


(b)

Fig. 14. Step-up operation mode (a) capacitor voltage and (b) inductor current.



(a)



(b)

Fig. 16. Step-down operation mode (a) capacitor voltage and (b) inductor current.

average currents measured across inductors L_1 , L_2 , and L_3 are 13.07, 7.865, and 2.605 A, respectively.

Fig. 15(a) and (b) presents the experimental results for input current, voltage, duty-cycle, and instantaneous power, as well as output current, voltage, and instantaneous power, respectively, during charge (buck) mode. According to these figures, the input and output powers are measured to be 523.4 and 510.9 W, respectively. Consequently, the efficiency of the driver is estimated to be 97.6 % during charge mode.

The figures show that with a duty cycle of 0.5 and an HV-side voltage of 403.3 V, the battery-side voltage is maintained at 40.87 V during charge mode. The experimental results for V_{C1} , V_{C2} , and V_{C3} are depicted in Fig. 16(a). With an HV-side voltage of 403.3 V and a duty cycle of 0.5, the observed voltages

across the capacitors are 82.86, 165.1 V, and 16.51 V, respectively, confirming the validity of (11).

Furthermore, since the currents passing through L_1 , L_2 , and L_3 traverse the active switches, these currents are monitored and displayed in Fig. 16(b). The average currents measured across inductors L_1 , L_2 , and L_3 are 12.56, 7.54, and 2.462 A, respectively.

B. Voltage and Current of Switches and ZVS Test

One of the critical considerations in power electronics devices is the voltage and current stresses endured by the semiconductor components. To assess this parameter in the proposed bidirectional dc–dc converter, the current and voltage stress experienced

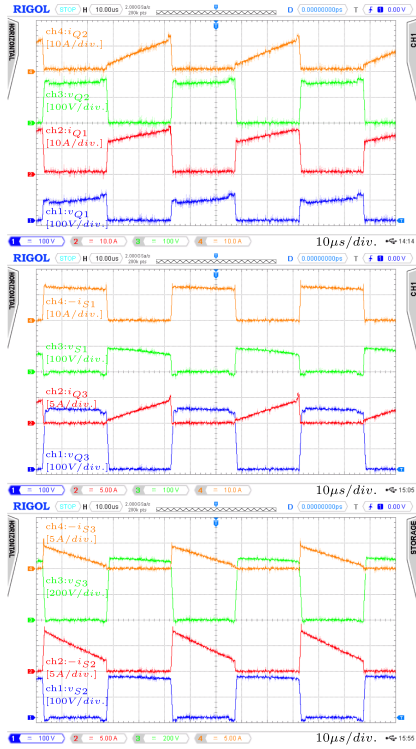


Fig. 17. Step-up operation mode voltage and current of switches.

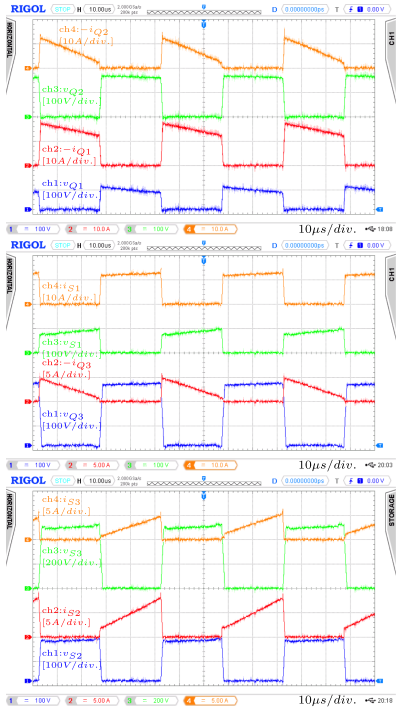


Fig. 18. Step-down operation mode voltage and current of switches.

by all the main semiconductor devices used, are depicted in Figs. 17 and 18 for step-up and step-down mode, respectively.

Fig. 19 illustrates the Syn. operation of the proposed converter in both step-down and step-up modes. In the step-up mode, during the time delay δT_s , the gate signals and the voltage across the switches of S_1 , S_2 , and S_3 are zero. When S_1 , S_2 , and S_3 are

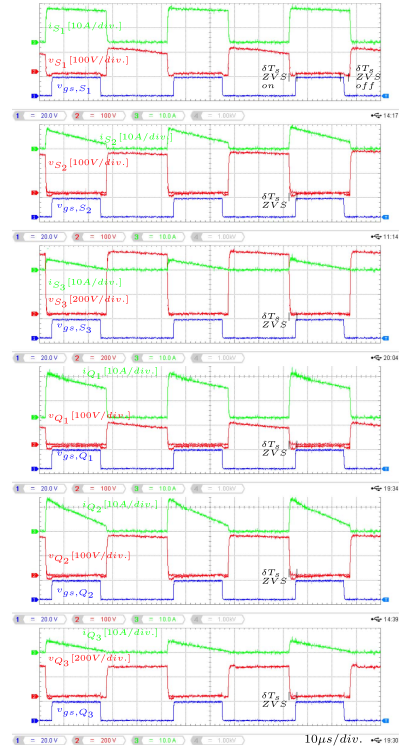


Fig. 19. ZVS operation mode during step-up and step-down modes.

subsequently turned ON, the current flows through the controlled power semiconductor S_1 , S_2 , and S_3 from source to drain due to their lower ON-state resistance and voltage drop, using the gate signals. Similarly, in the step-down mode, during δT_s , the gate signals and voltage across the the switches of Q_1 , Q_2 , and Q_3 , as shown in Fig. 19. Afterward, the current flows through the controlled power semiconductor Q_1 , Q_2 , and Q_3 using the gate signals. As a result, the controlled MOSFETs S_1 , S_2 , and S_3 in the step-up mode, and Q_1 , Q_2 , and Q_3 in the step-down mode, can be turned ON and OFF with ZVS.

C. Closed-Loop Test

Fig. 20(a) illustrates the performance of the step-up mode under steady-state operation and during a step change in the battery-side current reference from 4.5 to 14.5 A. It can be seen that the input LV side current tracks the reference, and the LV side voltage varies from 39.96 to 39.85 V. Therefore, the output voltage across the HV side load changes from 239.9 to 431.9 V with the step change in the reference battery-side current. Subsequently, D varies stepwise from 0.408 to 0.512.

Similarly, Fig. 20(b) shows the performance of the converter in step-down or charging mode under steady-state operation and in response to a step change in the battery-side current command from 14.5 to 4.5 A. In this scenario, D decreases stepwise from 0.5107 to 0.3665. The HV side voltage source remains at 400 V by the dc source, while the battery-side voltage steps from 40.46 to 41.43 V. These results demonstrate the proper performance of the proposed current controller under the change of reference of battery side current which is essential for an appropriate and

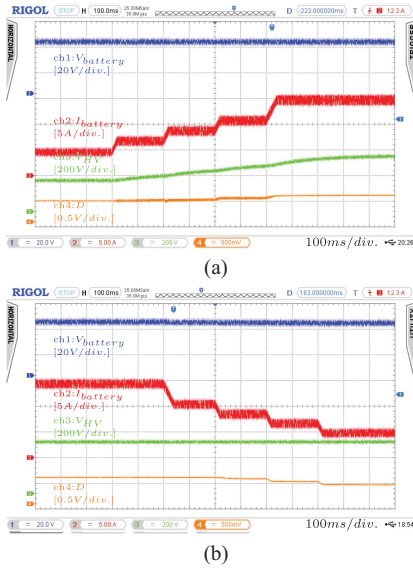


Fig. 20. Transient operation of (a) step-up (discharging) and (b) step-down (charging) modes.

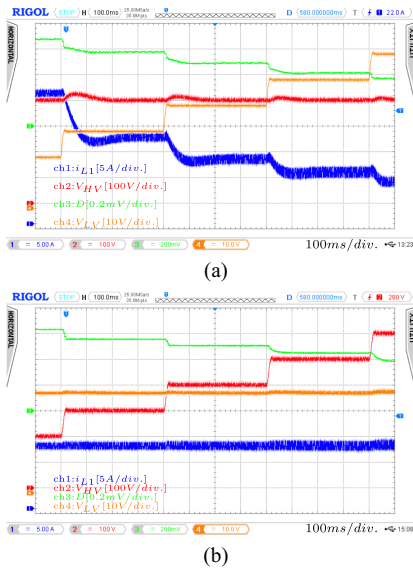


Fig. 21. Transient operation in input voltage of (a) step-up (discharging) and (b) step-down (charging) modes.

smooth behavior of the proposed converter when connected to the dc bus.

Fig. 21(a) demonstrates the step-up mode performance of the proposed converter under steady-state conditions and during a step change in the LV-side voltage reference from 20 to 60 V. The results show that the inductor L_1 current accurately tracks the reference, and the LV-side current adjusts from 25 to 8 A accordingly. Meanwhile, the HV-side output voltage remains constant at 400 V, even with the step change in the LV-side voltage reference. This stability is achieved as the duty cycle (D) shifts stepwise from 0.68 to 0.48.

Similarly, Fig. 21(b) presents the step-down (charging) mode performance under steady-state conditions and in response to a step change in the HV-side voltage from 200 to 600 V. In this

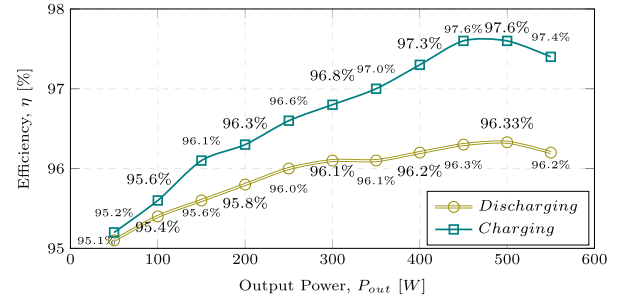


Fig. 22. Proposed bidirectional DC-DC converter efficiency curve versus output power levels.

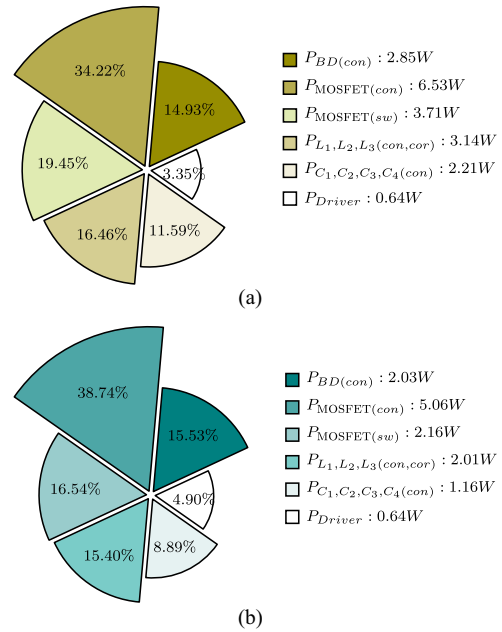


Fig. 23. Power loss break down of the proposed converter at η_{max} for (a) discharging and (b) charging modes.

case, D decreases stepwise from 0.64 to 0.39, while the LV-side voltage remains steady at 40 V, and the inductor L_1 current is maintained at 12 A.

These results highlight the converter's ability to handle a wide voltage gain ratio effectively, ensuring stable and smooth operation under varying LV-side and HV-side voltage conditions. This capability is critical for ensuring proper behavior when the converter is integrated into dc microgrids.

D. Proposed Converter Evaluation

Fig. 22 shows the measured efficiency versus output power curves under different modes of operation. The maximum efficiency of the proposed converter during charging and discharging modes is 97.6% and 96.33%, respectively. The input and output powers for the measurement of efficiency were obtained by using the math functions of the RIGOL DS4024 digital oscilloscope on the measured voltage and current waveforms.

As discussed in Table IV, the RMS values of the currents in the step-down mode are lower than those in the step-up mode. This reduction in RMS current leads to lower conduction

and switching losses in the step-down mode. Consequently, the efficiency of the charging mode, which corresponds to the step-down operation, is higher compared to the discharging mode.

The power loss breakdown of the proposed converter at maximum efficiency is shown in Fig. 23. The primary source of power loss is the conduction loss of MOSFETs ($P_{\text{MOSFET(con)}}$), accounting for 34.22% during discharging mode and 38.74% during charging mode. This is followed by the switching loss of MOSFETs ($P_{\text{MOSFET(sw)}}$) at 19.45% and 16.54%, and the core and conduction losses of inductors ($P_{L_1, L_2, L_3(\text{con, cor})}$) at 16.45% and 15.40%. Other contributors include the conduction loss of body diodes ($P_{\text{BD(con)}}$) at 14.93% and 15.53%, the conduction loss of capacitors ($P_{C_1, C_2, C_3, C_4(\text{con})}$) at 11.59% and 8.89%, and the driver circuit losses (P_{Driver}) at 3.35% and 4.90% during discharging and charging modes, respectively.

VI. CONCLUSION

In this article, a novel bidirectional dc–dc converter with a cubic voltage gain ratio is proposed and analyzed for use in bidirectional battery charging applications. The proposed converter is designed to address the limitations of existing converter topologies, offering a common ground connection, wide and HV gain range, and improved semiconductor utilization. Key findings from the study include the following.

- 1) *Lower current stress*: The proposed converter exhibited a low TCS devices compared to existing converters, enhancing the reliability and efficiency of the system.
- 2) *Syn. operation*: The proposed design facilitated Syn. operation, minimizing losses associated with the body diode of switches and providing ZVS for the complementary switch, further enhancing efficiency.
- 3) *Wide voltage gain range*: The converter's ability to cover the entire range of voltage gain ratios from 0 to 1 in charging and from 1 to a reasonable value in discharging ensures its suitability for a variety of applications and scenarios.
- 4) *Highest voltage gain ratio*: The proposed converter offers the highest voltage gain ratio compared to existing bidirectional dc–dc converters, making it highly efficient and suitable for a wide range of applications.

Theoretical analysis and experimental validation demonstrated the converter's effectiveness in dynamic voltage matching between the battery and the dc-link voltage, ensuring efficient energy transfer in both charging and discharging scenarios. A prototype of the proposed converter was constructed and tested with a 40 V Ni-Cd battery. The experimental results closely matched the theoretical predictions, confirming the converter's practical viability.

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