Carrier-Based Minimum-Loss Discontinuous PWM With Neutral-Point Voltage Balancing for Three-Level NPC Inverters

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***Abstract*—This article analyzes zero-clamping possible regions of three-level inverters and investigates the selection criteria for positive, negative, and zero clamping in discontinuous pulsewidth modulation (DPWM). Based on this analysis, a carrier-based minimum-loss DPWM (MLDPWM) is proposed to minimize the switching loss of the three-level inverters. The proposed method further increases the clamping region furthermore in the vicinity of a peak current by applying the zero clamping. Consequently, the switching loss can be minimized by reducing the number of switching near the peak current, considering all ranges of power factor angles and modulation indices. The performance of the proposed method is compared with that of the conventional DPWM method in the aspect of switching loss function. Moreover, the neutral-point voltage balancing is achieved by adjusting the clamping region while maintaining the principles of proposed MLDPWM. Finally, the effectiveness of the proposed method is verified by simulation and experimental results.**

***Index Terms*—Discontinuous pulsewidth modulation (DPWM), minimum loss, neutral-point (NP) balancing, switching loss, three-level inverter.**

I. Introduction

THREE-level voltage-source inverters (VSIs) are increasingly used in both grid-connected and motor-drive applications because of their superior advantages over conventional two-level VSIs, such as lower harmonic distortion, higher efficiency, and lower voltage stress across switching devices and plant under control [1], [2].

The performance of the inverters depends on the modulation strategy. Modulation schemes can be classified into two aspects: the implementation methods and the shape of the modulating signals. In terms of the implementation methods, pulse-width modulation (PWM) strategies are categorized into carrier-based PWM (CBPWM) and space-vector PWM (SVPWM). SVPWM requires much more computational burden or look-up tables to perform tasks such as sector identification, switching sequence, trigonometric function, etc. [3], [4], [5]. In contrast, CBPWM generates the duty cycles for the switches through a simple comparison between the reference voltage and the carrier. CBPWM for the three-level inverters was equivalent to the SVPWM method by introducing a zero-sequence voltage, i.e., an offset voltage [6]. Therefore, CBPWM with an offset voltage concept is simpler to implement and reduces computational burden compared to SVPWM [7], [8].

PWM strategies can also be classified based on the shape of the modulating signals into continuous PWM (CPWM) and discontinuous PWM (DPWM). In CPWM, the modulating signals are not clamped, while in DPWM, the modulating signals are clamped to one of the dc-buses, i.e., positive, negative, or neutral-point (NP) of the dc-bus. Compared to CPWM, DPWM reduces switching loss because it has fewer switching transitions due to the clamped phase.

In the case of a two-level inverter, there are mainly four DPWM schemes: DPWM0-DPWM3 [9]. By expanding these schemes, a minimum-loss DPWM (MLDPWM) was suggested to reduce the number of switching near the maximum current phase in [10]. To minimize the switching loss, clamping regions should be close to the positive and negative peak of output current. For the two-level inverters, MLDPWM achieves 50% switching loss reduction within 30° lagging to 30° leading power factor (PF) angle because the peak current occurs at maximum or minimum voltage references. However, the switching loss at lower PFs cannot be reduced by 50% due to the inherent limitation of two-level inverters where the peak current occurs at a medium voltage reference.

The conventional DPWM schemes in two-level inverters can be easily implemented in three-level inverters in the case of

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TABLE I
COMPARISON OF THE PROPOSED METHOD WITH EXISTING METHODS

References	Implementation method	PF angle optimization	NP voltage balancing	Zero clamping utilization
[12], [13], [14]	SVPWM	Yes	Passive	Yes
[15], [16], [17]	CBPWM	No	Active	No
[18], [19]	CBPWM	No	Active	No
[20]	CBPWM	Yes	Active	No
Proposed method	CBPWM	Yes	Active	Yes

CBPWM [10]. In contrast to the two-level inverter where only positive or negative dc-bus is possible to clamp, it is possible to clamp the voltage reference to the NP of the dc-bus in the three-level inverters [11]. It can be said to be zero clamping. Owing to the existence of zero clamping, the switching loss of the three-level inverter can be further reduced at lower PFs compared to the two-level inverter. It means that the operation principle of MLDPWM for the two-level inverters cannot be directly applied to the three-level inverters.

For the reduction of switching loss, various DPWM schemes have been proposed for the three-level inverters. In [12], [13], and [14], a method for MLDPWM of the three-level inverters was proposed for the lower PF range where the zero clamping state is applied by the SVPWM. However, a lot of computation are required to implement the MLDPWM, such as sector judgement, clamping state selection, and switching sequence arrangement. Moreover, the NP voltage was self-balanced without any active NP control, which is sensitive to the system configuration. In [15], [16], and [17], the carrier-based DPWM was proposed, where an NP voltage balancing is considered at the same time. The deviation of NP voltage was suppressed by changing the clamping regions. However, the effects on NP current according to the clamping state were not analyzed in detail, which provokes large fluctuations of offset voltage. In [18] and [19], the NP voltage ripple was suppressed by injecting the offset voltage properly. However, these methods are only focused on the high PF range, i.e., DPWM1, where the zero clamping is not effectively adopted by the PF angle. In [20], the carrier-based MLDPWM was implemented to minimize the switching loss for while keeping the NP voltage balancing. However, the zero clamping was not utilized at all, where the maximum current phase cannot be clamped to the NP at low PFs.

The characteristics of the above-mentioned algorithms can be summarized as in Table I. From Table I, it is easy to observe that the proposed method can achieve the minimum switching loss for all PF ranges by applying the zero clamping state. In addition, the active NP balancing algorithm can be compatible with the MLDPWM scheme.

This article proposes a carrier-based MLDPWM optimized for the three-level neutral-point clamped (NPC) inverters, considering all ranges of PF angles and MI regions. First, the zero clamping issue is analyzed to select appropriate clamping states in the voltage space vector. Based on this analysis, an offset voltage reference is generated, accounting for the effects of both PF angle and MI. The performance of the proposed method is evaluated in comparison with that of the conventional strategies in terms of both switching loss and conduction loss. Moreover, the NP current is analyzed according to the clamping states. The NP voltage balancing is achieved by adjusting the ratio between the clamping states while maintaining the clamping regions near the peak current. Simulation and experimental results are provided to show the effectiveness of the proposed method.

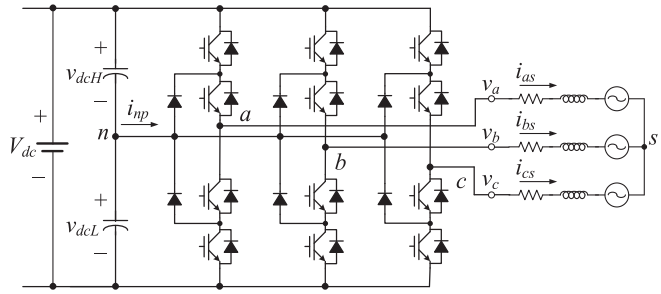

Fig. 1. Circuit schematic of the three-level NPC inverter.

The contents of this research, previously presented in [21], have been significantly enhanced to broaden its scope and improve clarity. The proposed MLDPWM scheme extends its applicability to low MI regions, where the zero clamping is always feasible. Moreover, NP voltage balancing has been newly incorporated into the analysis, which now encompasses all MI and PF regions while considering NP voltage balancing. The proposed NP balancing algorithm can be integrated with DPWM schemes and eliminates the need for separate dc-link sources, enabling both MLDPWM and NP voltage balancing to be achieved using only a single dc-link source in a three-level inverter. Extensive simulation and experimental results are included to demonstrate the effectiveness of the proposed scheme under conditions where the NP between the capacitors is floating.

II. ANALYSIS OF DPWM FOR THREE-LEVEL INVERTER

A. Voltage Space Vector Representation

Fig. 1 represents the circuit schematic of the three-level NPC inverter with resistive-inductive-source (R-L-E) loads. There are 27 combinations of switching state in the three-level inverters. The states "+," "−," and "0" are defined as when the upper switches are ON, the lower switches are ON, and the neutral switches are ON, respectively. All voltage vectors of switching state combinations are shown in Fig. 2. The voltage vectors can be classified into four types according to their magnitude: zero-voltage vectors (0), small-voltage vectors ($V_{\rm dc}/3$), medium-voltage vectors ($V_{\rm dc}/\sqrt{3}$), and large-voltage vectors ($2V_{\rm dc}/3$), where $V_{\rm dc}$ means the dc-link voltage. The duration of three zero-voltage vectors and a pair of redundant small-voltage vectors can be adjusted to implement the PWM schemes and control the NP voltage. Reference of the voltage vector, $\mathbf{V}^*$, can be expressed as

$$\mathbf{V}^* = \mathrm{MI}\frac{V_{\rm dc}}{2}\begin{bmatrix}\cos\theta_v \\ \sin\theta_v\end{bmatrix} \tag{1}$$

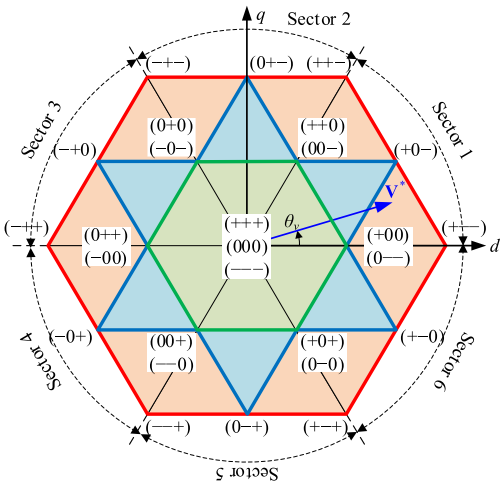

Fig. 2. Space vector hexagon of the three-level inverter with switching states.

where MI and θ_v are the modulation index and the phasor angle in the voltage space vector, respectively. In this article, the range MI $\leq 2/\sqrt{3}$ is addressed in detail, which is the linear modulation region of the three-level inverter.

Three-level voltage space vector hexagon has six sectors. Similar to a two-level space vector hexagon, each sector can clamp the voltage reference to a positive or negative dc-bus. In addition, zero clamping to the neutral point is possible in the inner hexagon and the center triangle of each sector, which are represented in green and blue regions, respectively. All phase voltage references can be clamped to the NP in the inner hexagon (green area), which region is defined as follows:

$$v_{\max}{}^* - v_{\min}{}^* \leq \frac{1}{2}V_{\mathrm{dc}} \tag{2}$$

where $v_{\max}{}^*$, $v_{\min}{}^*$, and $v_{\mathrm{mid}}{}^*$ represent the maximum, minimum, and medium values among the phase voltage references, respectively.

At the center triangle of each sector (blue area), the medium voltage reference is only available to clamp with the NP. This criterion is derived as follows:

$$\begin{aligned} v_{\max}{}^* - v_{\min}{}^* &> \frac{1}{2}V_{\mathrm{dc}} \\ v_{\max}{}^* - v_{\mathrm{mid}}{}^* &\leq \frac{1}{2}V_{\mathrm{dc}} \\ v_{\mathrm{mid}}{}^* - v_{\min}{}^* &\leq \frac{1}{2}V_{\mathrm{dc}}. \end{aligned} \tag{3}$$

Otherwise, the positive and negative dc-bus clamping are only possible in the outer hexagon except for above regions (red area). These regions are defined as follows:

$$\begin{aligned} &v_{\max}{}^* - v_{\min}{}^* \leq V_{\mathrm{dc}}, \\ &\left(v_{\max}{}^* - v_{\mathrm{mid}}{}^* > \frac{1}{2}V_{\mathrm{dc}}\right) \| \left(v_{\mathrm{mid}}{}^* - v_{\min}{}^* > \frac{1}{2}V_{\mathrm{dc}}\right). \end{aligned} \tag{4}$$

Conventional DPWM schemes for the two-level inverter consider only positive and negative clamping. However, the zero clamping is possible depending on the location of $\mathbf{V}^*$ for the three-level inverter. The zero clamping possible region is affected by MI. In addition, there is an issue about how to divide the duration of positive, negative, and zero clamping.

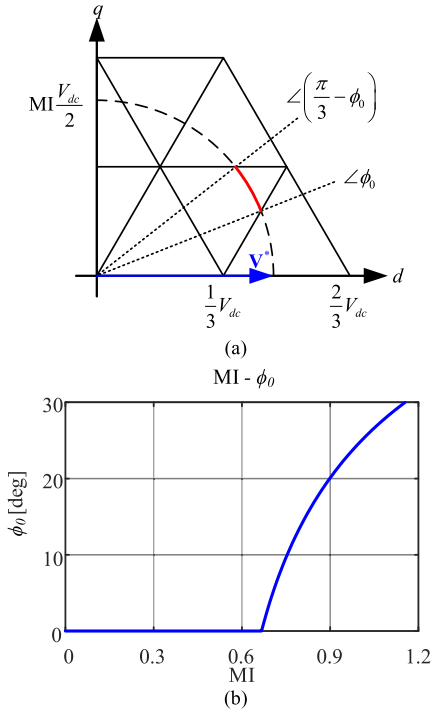

Fig. 3. (a) Representation of ϕ_0, $\pi/3$ - ϕ_0, and the zero clamping possible range (red line) in Sector 1. (b) Relationship between ϕ_0 and MI.

B. Effects of MI on Zero Clamping Possible Region

There are intersections between the zero clamping possible region and the trajectory of $\mathbf{V}^*$ when MI $\geq$ 2/3. As shown in Fig. 3(a), the intersection angles ϕ_0 and $\pi/3$-ϕ_0 are dependent on MI. The range between two angles is defined as a zero clamping possible range for the given MI. As MI becomes lower, the zero clamping possible range, i.e., $\pi/3 - 2\phi_0$, is getting larger. In this case, ϕ_0 can be expressed as

$$\phi_0 = \frac{\pi}{3} - \sin^{-1}\left(\frac{1}{\sqrt{3}\mathrm{MI}}\right). \tag{5}$$

When MI is lower than 2/3, there is no intersection, and zero clamping is possible regardless of θ_v. It can be defined as $\phi_0 = 0$, which means that $\mathbf{V}^*$ is always located in the zero clamping possible region. As a result, the relationship between ϕ_0 and MI can be depicted as shown in Fig. 3(b).

III. Proposed Minimum Loss Discontinuous Modulation Scheme

A. PWM Strategy With Minimum Switching Loss

The inverter loss consists of the conduction and the switching losses. The conduction loss depends on current-voltage characteristics of switching devices under the constant dc-link voltage; the switching loss depends on both the current in switching and

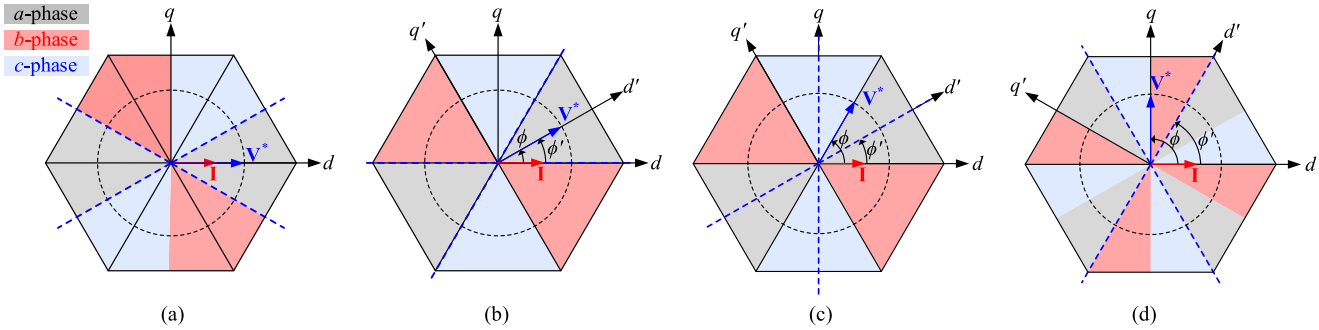

Fig. 4. Switching patterns of MLDPWM according to ϕ in case of the two-level inverter. (a) ϕ=0°. (b) ϕ=30°. (c) ϕ=60°. (d) ϕ=90°.

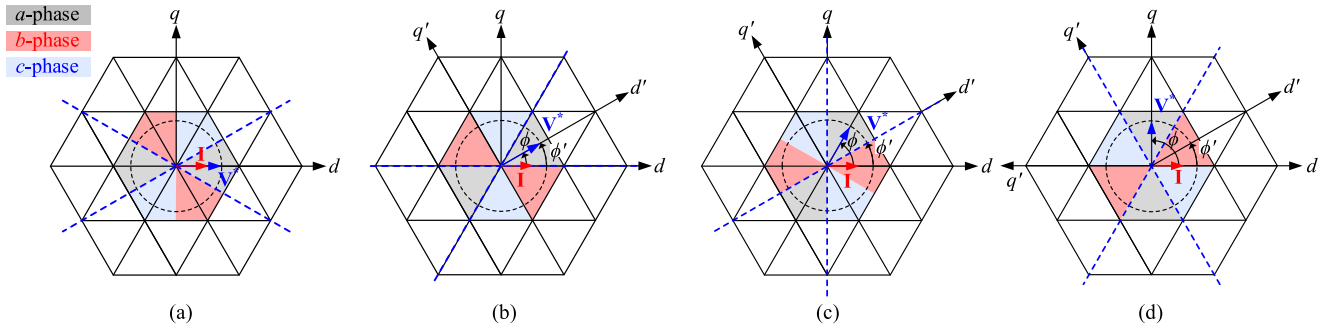

Fig. 5. Switching patterns of MLDPWM according to ϕ in case of the three-level inverter in the inner hexagon. (a) ϕ=0°. (b) ϕ=30°. (c) ϕ=60°. (d) ϕ=90°.

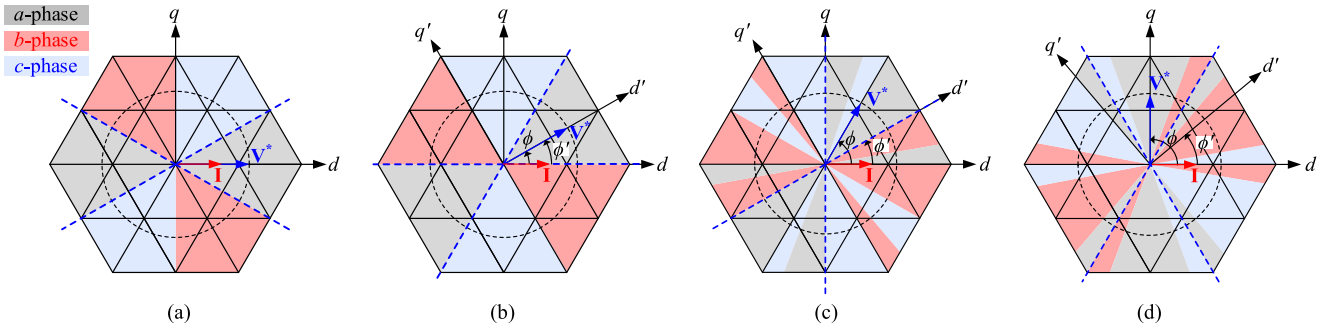

Fig. 6. Switching patterns of MLDPWM according to ϕ in case of the three-level inverter out of the inner hexagon. (a) ϕ=0°. (b) ϕ=30°. (c) ϕ=60°. (d) ϕ=90°.

the switching frequency. The conduction loss is almost constant regardless of PWM schemes and the switching frequency [10]. On the other hand, the switching loss can be reduced by choosing the appropriate PWM scheme because it is related to switching patterns.

For DPWM schemes, each output leg has 120° clamping interval over one electrical period. To minimize the switching loss, it is desirable to distribute 60° clamping intervals near the positive and the negative peak of output current. With consideration of possible clamping, Figs. 4–6 illustrate the clamping regions of three-phase according to ϕ in the cases of the two- and three-level inverters, in which black, red and blue shaded regions denote nonswitching regions of a-phase, b-phase and c-phase, respectively. In the figures, $\mathbf{V}^*$, $\mathbf{I}$, and ϕ denote the voltage vector reference, current vector, and PF angle, respectively. The blue dashed line means that the position of $\mathbf{V}^*$ for 60° around the peak current of a-phase, which corresponds to ideal nonswitching regions of a-phase.

Fig. 4 shows the clamping regions of three-phase according to ϕ in the case of the two-level MLDPWM. When ϕ is zero and PF is unity, the a-phase switch is clamped to a positive dc-bus for 60° around the positive peak current and to a negative dc-bus for 60° around the negative peak current, respectively. In this case, the offset voltage reference, ${v_{sn}}^*$, is generated as follows [10]:

$$ {v_{sn}}^* = \begin{cases} \frac{V_{dc}}{2} - {v_{\max}}^* & ({v_{\max}}^* + {v_{\min}}^* \geq 0) \\ -\frac{V_{dc}}{2} - {v_{\min}}^* & ({v_{\max}}^* + {v_{\min}}^* < 0) \end{cases} . \quad (6) $$

To minimize the switching loss, the clamping regions should be rotated to match with the blue dashed line as possible. It can

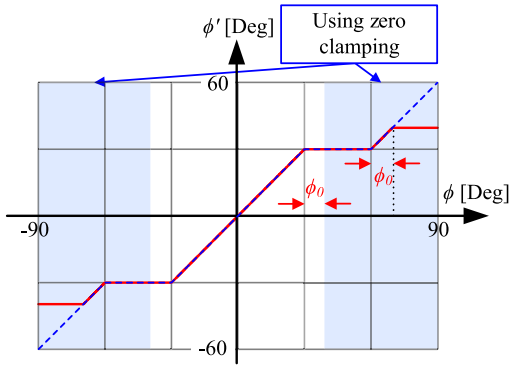

Fig. 7. Relationship between ϕ and ϕ' for MLDPWM of the two-level (dashed line) and three-level (solid line) inverters.

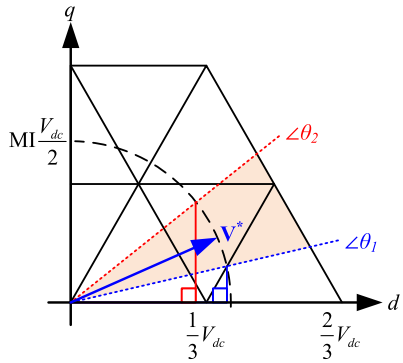

Fig. 8. Selective zero clamping (shaded area) in the zero clamping possible region of Sector 1.

be implemented with the offset voltage calculation by $\mathbf{V}'$ instead of $\mathbf{V}^*$, which is defined as

$$\mathbf{V}' = \mathbf{R}(-\phi')\,\mathbf{V}^* \tag{7}$$

where $\mathbf{R}(\theta)$ is the counterclockwise rotation matrix by θ and ϕ' is the rotating angle for MLDPWM.

$$\mathbf{R}(\theta) = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}. \tag{8}$$

Instead of (6), the offset voltage for changing the clamping region can be set as follows:

$$v_{\mathrm{sn}}{}^* = \begin{cases} \frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{max}}{}^* & \left(v'_{\mathrm{max}}{}^* + v'_{\mathrm{min}}{}^* \geq 0\right) \\ -\frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{min}}{}^* & \left(v'_{\mathrm{max}}{}^* + v'_{\mathrm{min}}{}^* < 0\right) \end{cases}. \tag{9}$$

In (9), $v'_{\mathrm{max}}{}^*$ and $v'_{\mathrm{min}}{}^*$ are the maximum and minimum values among the modified three-phase voltage references which are defined as follows:

$$\begin{bmatrix} v'_{\mathrm{as}} \\ v'_{\mathrm{bs}} \\ v'_{\mathrm{cs}} \end{bmatrix} = \begin{bmatrix} \cos 0 & \cos\frac{2\pi}{3} & \cos\frac{4\pi}{3} \\ \sin 0 & \sin\frac{2\pi}{3} & \sin\frac{4\pi}{3} \end{bmatrix}^{\mathrm{T}} \mathbf{V}'. \tag{10}$$

In the case of the two-level inverter, the relationship between the rotating angle and the PF angle, ϕ' and ϕ, is represented as a dashed line in Fig. 7 [7]. As shown in Fig. 4, when ϕ is less than 30°, the clamping region can coincide with the ideal clamping region. However, when ϕ is larger than 30°, the clamping region cannot match the blue dashed line due to the inherent limitation of possible clamping area of the two-level inverters where the zero-clamping is not possible.

Fig. 5 shows the clamping regions of three-phase according to ϕ in the case of inner hexagon for the three-level inverter. In the inner hexagon, the a-phase switch can be clamped to one of the dc-buses regardless of ϕ by virtue of the zero clamping. When ϕ is less than 30°, the proposed scheme has the same clamping regions as the two-level MLDPWM where the zero clamping is not applied. However, a portion of the zero clamping increases gradually to clamp the maximum current phase as ϕ is greater than 30°. As shown in Fig. 5(c) and (d), the clamping regions of the proposed scheme overlap the blue dashed line thanks to the existence of zero clamping. Therefore, the clamping regions are entirely consistent with the ideal clamping region under all PF regions in the inner hexagon.

Fig. 6 shows the clamping regions of three-phase according to ϕ out of the inner hexagon for the three-level inverter. Likewise, the a-phase switch is clamped to the positive dc-bus or the negative dc-bus when ϕ is less than 30°. The zero clamping is applied by the proposed clamping scheme in the vicinity of a peak current when ϕ is greater than 30°. As shown in Fig. 6(c) and (d), the clamping regions of the proposed scheme overlap the blue dashed line much more than that of the two-level MLDPWM at low PFs. Within the blue dashed line, the zero clamping possible region is fully utilized to clamp the maximum current phase.

The relationship between ϕ' and ϕ in the proposed scheme is represented in Fig. 7. Unlike the case of two-level inverter, the correlation between ϕ' and ϕ could be changed for the case of the three-level inverter. The zero clamping is utilized when $|\phi|$ is greater than $|\phi_0|$+30°, which is marked as shaded regions. ϕ' is affected by not only ϕ but also ϕ_0, which means that the effects of MI and PF are taken into account to rotate the clamping region.

To implement the switching patterns shown in Figs. 5 and 6, an additional condition is required to determine the zero clamping state. Fig. 8 shows the zero clamping region of Sector 1 where the discriminant angles, θ_1 and θ_2, are set to ϕ_0 and $|\phi| - \pi/6$, respectively. The shaded region in Fig. 8 is identical to the following equation:

$$|\mathbf{V}^*|\cos\theta_2 \;\leq\; v^*_{\mathrm{max}} \;\leq\; |\mathbf{V}^*|\cos\theta_1. \tag{11}$$

Extending this concept to all sectors, the offset voltage reference of the proposed scheme is set to $-v_{\mathrm{mid}}{}^*$ when the following condition is satisfied:

$$\begin{aligned} &|\mathbf{V}^*|\cos\theta_2 \leq v^*_{\mathrm{max}} \leq |\mathbf{V}^*|\cos\theta_1 \qquad (\text{Sector } 1,\ 3,\ 5) \\ &|\mathbf{V}^*|\cos\theta_2 \leq |v^*_{\mathrm{min}}| \leq |\mathbf{V}^*|\cos\theta_1 \qquad (\text{Sector } 2,\ 4,\ 6). \end{aligned} \tag{12}$$

If the above-mentioned condition is not satisfied, the offset voltage reference remains as the value which is already generated by (9). Meanwhile, $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ can be clamped to

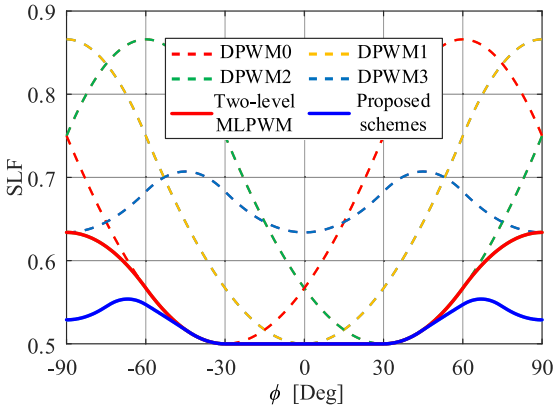

Fig. 9. SLF characteristics of different PWM strategies when MI=0.8.

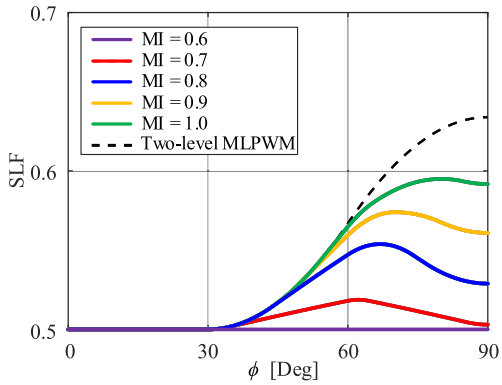

Fig. 10. SLF characteristics of the proposed MLDPWM scheme.

the NP where $\mathbf{V}^*$ is in the inner hexagon. There is a degree of freedom in the choice of the offset voltage if $v_{\max}{}^*$ and $v_{\min}{}^*$ are clamped in the low MI range, i.e., MI $\leq 1/\sqrt{3}$. In this case, one of the pole voltage references could be clamped to the neutral point at any time during an electrical period.

B. Impact on Power Loss of MLDPWM

In [9], DPWM schemes were evaluated in respect of the switching loss under the assumption that the switching loss is proportional to the magnitude of the phase current in switching as

$$\overline{P_{\text{sw}}} = k \int_0^{2\pi} |I_{\text{sw}}(\theta)|\, d\theta. \tag{13}$$

The coefficient k in (13) was determined by the switching frequency, turn-ON/OFF characteristics of a switch, etc. The switching loss function (SLF) was defined as the ratio between the switching losses of DPWM scheme and CPWM scheme as follows:

$$\text{SLF} = \frac{\overline{P_{\text{sw}}}\,(\text{DPWM})}{\overline{P_{\text{sw}}}\,(\text{CPWM})}. \tag{14}$$

SLF characteristics of the conventional DPWMs, the two-level MLDPWM, and the proposed scheme are represented in Fig. 9 when MI = 0.8. The conventional DPWMs can be divided into four schemes: DPWM0, DPWM1, DPWM2, and DPWM3, which are generalized as a phase-shift dependent DPWM [22], [23]. The two-level MLDPWM [10], [20] is implemented to seamlessly change the DPWM schemes depending on the PF angle. The two-level MLDPWM and the proposed three-level MLDPWM schemes have the same SLF when $|\phi| \leq 30°$. However, the proposed scheme has a lower SLF than the two-level MLDPWM when $|\phi| > 30°$. In the case of $\phi = 90°$, SLF has been enhanced by 16.6% compared to the two-level MLDPWM by the proposed three-level MLDPWM.

Fig. 10 shows SLF variations of the proposed scheme according to MI and ϕ. SLF of the proposed scheme is further enhanced as MI becomes lower. Especially, SLF is kept constant at 0.5 regardless of ϕ under the condition of MI < 2/3. The switching loss is remarkably reduced at low MI because the zero clamping could be fully utilized. It reveals that the proposed three-level MLDPWM is more effective at lower MI and lower PF when compared to the two-level MLDPWM.

For the NPC topology, the current should flow through the two switches in all states where the voltage drops across the switching devices are quite similar. However, the current flows through only one switch for the positive and negative clamping for the T-type topology [24], [25]. Thus, MLDPWM can further decrease the conduction loss of the T-type inverter when $\mathbf{V}^*$ is in the inner hexagon by minimizing the zero clamping region.

IV. Proposed NP Voltage Balancing Scheme

A. Analysis of NP Current for MLDPWM

The NP current, i_{np} shown in Fig. 1, would incur the voltage difference between high- and low- side dc-link voltage, i.e., $\delta v_{\text{dc}} \equiv v_{\text{dcH}} - v_{\text{dcL}}$. It is imperative that i_{np} is regulated to be an average of zero, and $v_{\text{sn}}{}^*$ can be changed for this purpose. The transfer function from $v_{\text{sn}}{}^*$ to i_{np} is analytically derived at the steady-state, which can be categorized into four cases as follows [24]:

$$i_{\text{np}} = \begin{cases} -\frac{P_{\text{out}}}{v_{\text{dcH}}} & (v_{\text{sn}}{}^* \geq -v_{\min}{}^*) \\ -\frac{P_{\text{out}}}{v_{\text{dcH}}} + \left(\frac{1}{v_{\text{dcH}}} + \frac{1}{v_{\text{dcL}}}\right)(v_{\min}{}^* + v_{\text{sn}}{}^*) i_{\min} & (-v_{\text{mid}}{}^* \leq v_{\text{sn}}{}^* < -v_{\min}{}^*) \\ \frac{P_{\text{out}}}{v_{\text{dcL}}} - \left(\frac{1}{v_{\text{dcH}}} + \frac{1}{v_{\text{dcL}}}\right)(v_{\max}{}^* + v_{\text{sn}}{}^*)\, i_{\max} & (-v_{\max}{}^* \leq v_{\text{sn}}{}^* < -v_{\text{mid}}{}^*) \\ \frac{P_{\text{out}}}{v_{\text{dcL}}} & (v_{\text{sn}}{}^* < -v_{\max}{}^*) \end{cases} \tag{15}$$

where P_{out} is the output power defined as

$$P_{\text{out}} = v_{\max}{}^* i_{\max} + v_{\text{mid}}{}^* i_{\text{mid}} + v_{\min}{}^* i_{\min}. \tag{16}$$

$i_{\max}$, i_{mid}, and $i_{\min}$ in (16) are the currents of corresponding phases to $v_{\max}{}^*$, $v_{\text{mid}}{}^*$, and $v_{\min}{}^*$, respectively.

The boundary of i_{np} is limited depending on the location of $\mathbf{V}^*$ in the voltage hexagon as shown in Fig. 2. There are options to choose $v_{\text{sn}}{}^*$ for the proposed MLDPWM when $\mathbf{V}^*$ is in the inner hexagon. $v_{\text{sn}}{}^*$ can be altered between the positive clamping and zero clamping during $v_{\max}{}^*$ clamping, i.e., ($v_{\text{sn}}{}^* = v_{\text{dcH}} - v_{\max}{}^*$) $\|$ ($v_{\text{sn}}{}^* = -v_{\max}{}^*$). Likewise, $v_{\text{sn}}{}^*$ can be selected

between the zero clamping and negative clamping during $v_{\mathrm{min}}{}^*$ clamping, i.e., $(v_{\mathrm{sn}}{}^* = -v_{\mathrm{min}}{}^*) \parallel (v_{\mathrm{sn}}{}^* = -v_{\mathrm{dcL}} - v_{\mathrm{min}}{}^*)$. There is no degree of freedom to choose $v_{\mathrm{sn}}{}^*$ during $v_{\mathrm{mid}}{}^*$ clamping, i.e., $(v_{\mathrm{sn}}{}^* = -v_{\mathrm{mid}}{}^*)$. Thus, the effects of $v_{\mathrm{sn}}{}^*$ selection in the inner hexagon are derived as follows:

$$i_{\mathrm{np}} = \begin{cases} -\frac{P_{\mathrm{out}}}{v_{\mathrm{dcH}}} & (v_{\mathrm{sn}}{}^* = v_{\mathrm{dcH}} - v_{\mathrm{max}}{}^* \| v_{\mathrm{sn}}{}^* = -v_{\mathrm{min}}{}^*) \\ -\frac{(v_{\mathrm{max}}{}^* - v_{\mathrm{mid}}{}^*) i_{\mathrm{max}}}{v_{\mathrm{dcH}}} - \frac{(v_{\mathrm{mid}}{}^* - v_{\mathrm{min}}{}^*) i_{\mathrm{min}}}{v_{\mathrm{dcL}}} & (v_{\mathrm{sn}}{}^* = -v_{\mathrm{mid}}{}^*) \\ \frac{P_{\mathrm{out}}}{v_{\mathrm{dcL}}} & (v_{\mathrm{sn}}{}^* = -v_{\mathrm{max}}{}^* \| v_{\mathrm{sn}}{}^* = -v_{\mathrm{dcL}} - v_{\mathrm{min}}{}^*) \end{cases} . \tag{17}$$

For intervals of $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ clamping, $v_{\mathrm{sn}}{}^*$ could be altered to minimize i_{np} fluctuations. However, abrupt changes of $v_{\mathrm{sn}}{}^*$ would cause large voltage harmonics and current oscillations, which should be minimized [26]. Instead, the ratio between $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ clamping is utilized to balance the NP voltage while the concept of the zero clamping is maintained. This means that the duration of redundant zero- and small-voltage vectors can be modified to achieve the dc balancing.

Meanwhile, there are no options to change $v_{\mathrm{sn}}{}^*$ when $\mathbf{V}^*$ is out of the inner hexagon. In this case, $v_{\mathrm{sn}}{}^*$ effects are classified into three cases as follows:

$$i_{\mathrm{np}} = \begin{cases} -\frac{P_{\mathrm{out}}}{v_{\mathrm{dcH}}} - \left(\frac{1}{v_{\mathrm{dcH}}} + \frac{1}{v_{\mathrm{dcL}}}\right)(v_{\mathrm{max}}{}^* - v_{\mathrm{min}}{}^* - v_{\mathrm{dcH}})\, i_{\mathrm{min}} & \\ \qquad (v_{\mathrm{sn}}{}^* = v_{\mathrm{dcH}} - v_{\mathrm{max}}{}^*) & \\ -\frac{(v_{\mathrm{max}}{}^* - v_{\mathrm{mid}}{}^*) i_{\mathrm{max}}}{v_{\mathrm{dcH}}} - \frac{(v_{\mathrm{mid}}{}^* - v_{\mathrm{min}}{}^*) i_{\mathrm{min}}}{v_{\mathrm{dcL}}} \quad (v_{\mathrm{sn}}{}^* = -v_{\mathrm{mid}}{}^*) & , \\ \frac{P_{\mathrm{out}}}{v_{\mathrm{dcL}}} - \left(\frac{1}{v_{\mathrm{dcH}}} + \frac{1}{v_{\mathrm{dcL}}}\right)(v_{\mathrm{max}}{}^* - v_{\mathrm{min}}{}^* - v_{\mathrm{dcL}})\, i_{\mathrm{max}} & \\ \qquad (v_{\mathrm{sn}}{}^* = -v_{\mathrm{dcL}} - v_{\mathrm{min}}{}^*) & \end{cases} \tag{18}$$

where $v_{\mathrm{mid}}{}^*$ clamping is only possible when $\mathbf{V}^*$ is at the center triangle of each sector as aforementioned.

There is no degree of freedom to adjust i_{np} after the durations of each clamping state are fixed. As an alternative, the durations of $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ clamping can be adjusted to change i_{np} over an electrical period. The redundancy in switching states is utilized to achieve the dc balancing by adjusting the averaged NP current [27].

B. NP Balancing Strategy With MLDPWM

The NP balancing schemes based on the offset voltage concept have been widely utilized owing to their simple structure [27], [28], [29]. The dc offset voltage can be injected to not only balance a dc voltage but also minimize an impact on total harmonic distortion (THD) performance, particularly. However, these methods cannot be directly applied with the proposed MLDPWM because the offset voltage must be set among the clamping voltages for the DPWM schemes.

The NP current averaged over one electrical period could be changed by adjusting the clamping voltage intervals. The duration of $v_{\mathrm{mid}}{}^*$ clamping is fixed to minimize the switching loss for the proposed DPWM scheme. Thus, the durations of $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ clamping are controlled to achieve the NP balancing. Fig. 11 shows the principle of the NP balancing algorithm compatible with the DPWM schemes. The balancing angle, θ_{bal}, indicates the ratio between $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ clamping, which can be adjusted to balance the NP voltage. In this case, the NP controller has only a minimum impact on the spectrum distribution at slight unbalance conditions.

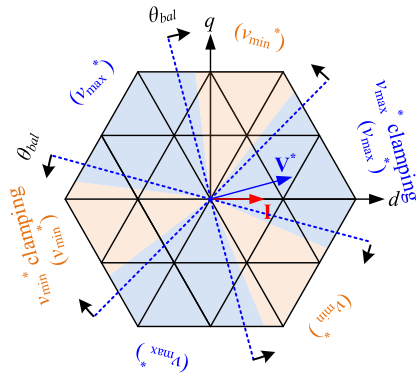

Fig. 11. Principle of the proposed NP balancing algorithm.

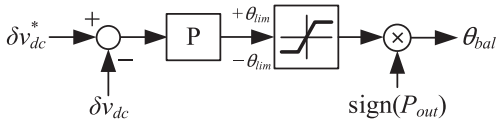

Fig. 12. Block diagram of the proposed NP balancing controller.

Fig. 12 shows the block diagram of the proposed NP balancing controller. A proportional (P) controller with an output limiter is applied to minimize the voltage deviation, δv_{dc}. θ_{lim} should be limited within an acceptable range under $\pi/6$. Moreover, the output of proportional controller is multiplied by the sign of the output power, sign(P_{out}). The controller keeps a negative feedback loop for not only the inverter operation ($P_{\mathrm{out}} > 0$) but also the converter operation ($P_{\mathrm{out}} < 0$), which is optimized to the positive and negative clamping. Finally, θ_{bal} is utilized to minimize the NP voltage deviation based on the NP current analyses. During the normal operations, its impact on the original design is minimized.

Fig. 13 shows a flowchart of the proposed MLDPWM scheme with NP balancing algorithm. First, ϕ is calculated by the difference between $\mathbf{V}^*$ and $\mathbf{I}$. The rotating voltage vector, $\mathbf{V}'$, is derived with the rotation matrix by ϕ'. Then, the offset voltage is determined where not only $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ clamping but also $v_{\mathrm{mid}}{}^*$ clamping is considered. The NP balancing controller is applied to control the ratio between $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ clamping while maintaining $v_{\mathrm{mid}}{}^*$ clamping. It has a low impact on the original MLDPWM scheme by reducing the proportional gain. Then, $v_{\mathrm{sn}}{}^*$ is calculated based on the clamping voltage. $v_{\mathrm{max}}{}^*$ and $v_{\mathrm{min}}{}^*$ can be clamped to the NP in the case of low MI operation. In this article, $v_{\mathrm{sn}}{}^*$ is set to minimize offset voltage fluctuations while maintaining NP voltage balancing. Thus, the positive and negative clamping is usually adopted to minimize the number of $v_{\mathrm{sn}}{}^*$ changes and δv_{dc} deviation.

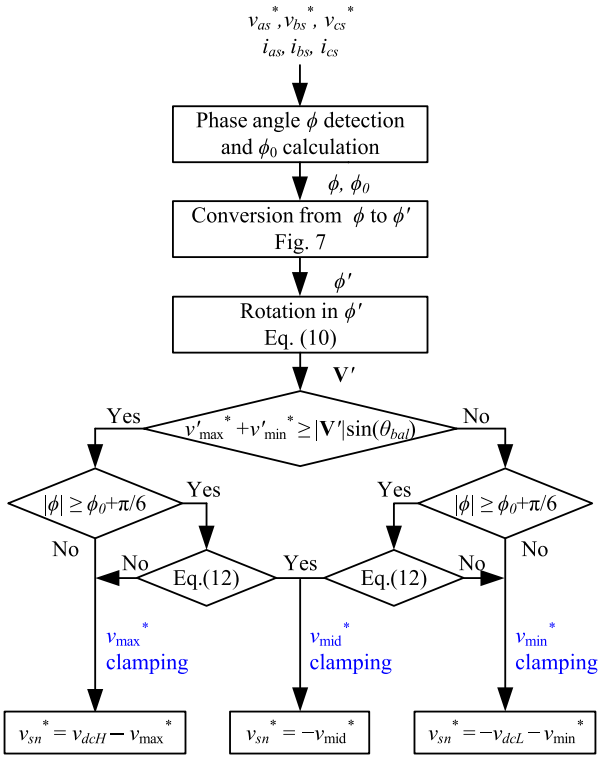

Fig. 13. Flowchart of the proposed MLDPWM scheme with NP balancing strategy.

TABLE II
SYSTEM PARAMETERS

Parameter	Value
Rated power, P_{rated}	5 kVA
Rated current, I_{rated}	20 A_{peak}
Dc-link voltage, V_{dc}	400 V
Dc-link capacitance, C_{dcH}, C_{dcL}	5.5 mF
Switching frequency, f_{sw}	20 kHz
Sampling frequency, f_{samp}	20 kHz
Filter inductance, L	2.5 mH
Filter resistance, R	60 mΩ

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

Simulation was carried out to evaluate the proposed scheme in MATLAB/SIMULINK with PLECS, where the inverter losses are estimated using PLECS model. The three-level NPC inverter with IGBT power modules, Semikron SK50MLI066, is connected to R-L-E loads, where the system parameters are set as in Table II. As shown in Fig. 1, the NP between the capacitors is floating and the NP balancing control is required. The proposed MLDPWM schemes are applied with the NP balancing algorithm as shown in Fig. 13. The conventional two-level MLDPWM scheme is combined with the offset voltage-based NP balancing algorithm, which was implemented for the three-level inverter in [20]. The output currents and dc-link voltages are measured to implement the control algorithms. There are no additional sensors to implement the proposed scheme compared with the conventional schemes. The proportional gain of NP controller is set to 0.01.

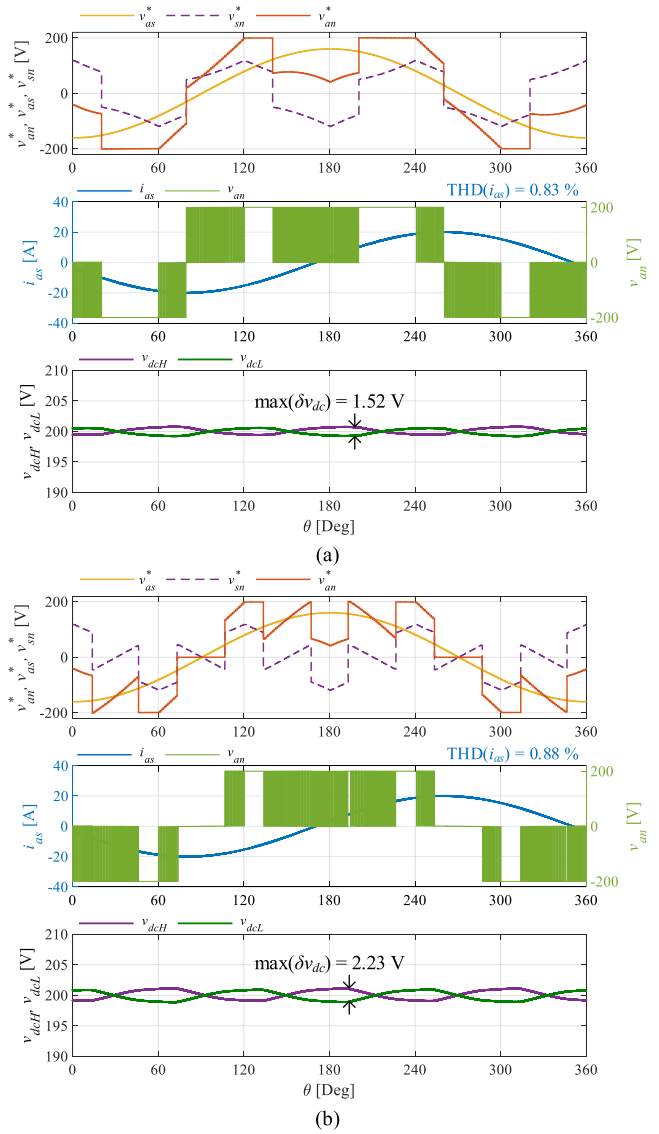

Fig. 14. Simulation results: Waveforms of the voltage reference and switching patterns in MI = 0.8, $\phi = 80°$ with (a) the conventional MLDPWM scheme and (b) the proposed MLDPWM scheme.

Fig. 14 shows the waveforms of voltage references, phase current, switching patterns of a-phase, and dc-link voltages at MI = 0.8 and $\phi = 80°$. Compared to the conventional two-level MLDPWM scheme shown in Fig. 14(a), the proposed three-level MLDPWM scheme shown in Fig. 14(b) reveals clamping region in the vicinity of the current peak. In case of the proposed scheme, there is no switching near $\theta = 90°$ and 270° using zero clamping where the current peak occurs. The switching loss is reduced by 23.2% from 54.8 to 42.1 W by applying the proposed scheme. Otherwise, the conduction losses of each scheme are 80.3 and 80.2 W, respectively, which reveals that the proposed scheme can minimize the inverter loss of the three-level NPC inverter. The proposed MLDPWM method actively uses zero clamping to minimize switching losses; inevitable NP current occurs. Thus, max(δv_{dc}) is slightly larger than the conventional method, but the voltage difference between the

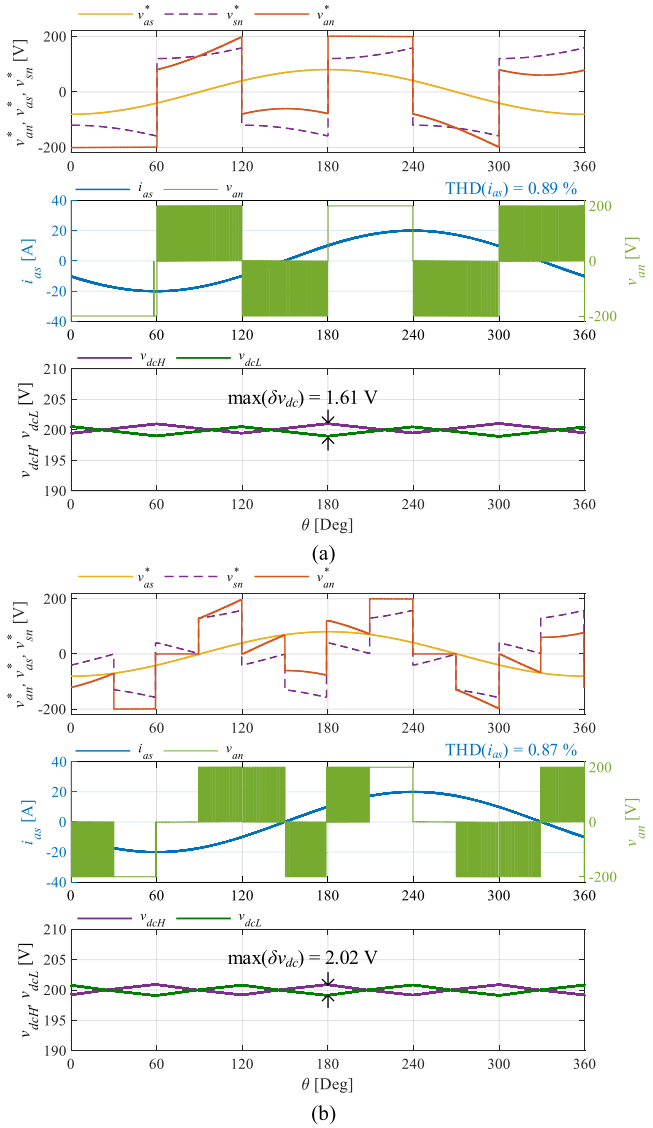

Fig. 15. Simulation results: Waveforms of the voltage reference and switching patterns in MI = 0.4, $\phi = 60°$ with (a) the conventional MLDPWM scheme and (b) the proposed MLDPWM scheme.

dc-link capacitors, i.e., $v_{\mathrm{dcH}} - v_{\mathrm{dcL}}$, is well regulated to less than 5 V by applying the proposed NP balancing controller. The dc-link voltage ripple can be slightly increased compared to the conventional method due to the zero clamping state, which can be suppressed by increasing the proportional gain of NP controller.

Fig. 15 shows the simulation results at MI = 0.4 and $\phi = 60°$. The proposed scheme reduces the number of switching when the phase current is near the peak compared to the conventional scheme. The zero clamping is always possible around the current peak in the case of low MI operation, which can minimize the switching loss. The switching loss is reduced by 20.3% from 55.6 to 44.3 W, while the conduction loss remains almost constant at 79.9 W. The current THD of the proposed scheme, i.e., THD(i_{as}), is similar to the conventional scheme. Thus, the propose scheme improves the inverter efficiency by

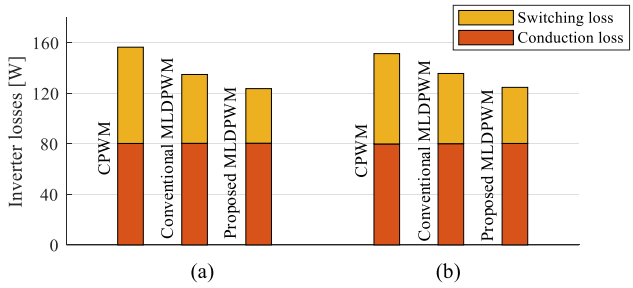

Fig. 16. Simulation results: Loss distributions for different modulation schemes under (a) MI = 0.8, $\phi = 80°$, (b) MI = 0.4, $\phi = 60°$.

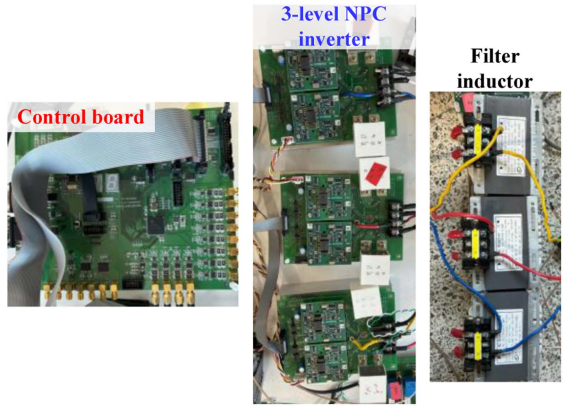

Fig. 17. Experimental setup: 5 kVA three-level NPC inverter with *L* filter.

minimizing the switching loss at lower PF while maintaining the NP balancing.

Fig. 16 shows the loss distributions for different modulation schemes at low PFs. The switching and conduction losses of the proposed MLDPWM are compared with those of the CPWM and the conventional MLDPWM. The conduction losses are almost constant for all the schemes because the conduction loss is proportional to the magnitude of the phase current. The proposed MLDPWM results in lower switching loss compared to the CPWM and the conventional MLDPWM by reducing the number of switching near the peak current. The proposed method is more efficient in high-frequency switching applications, where the proportion of the switching loss increases compared to the conduction loss.

B. Experimental Results

The proposed method was experimentally verified in a 5-kVA three-level NPC inverter system with inductor filters as shown in Fig. 17. The control algorithms were executed in a digital signal processor, TI TMS320F28377D, on the control board. Only the single core is dedicated to implementing the control algorithms and modulation schemes, where the carrier-based MLDPWM is executed within 5 μs. The system parameters of the experimental setup are the same as those used in the simulation. The dead time is set to 2 μs. The inverter losses are calculated using a power analyzer, HIOKI PW3390, where the dc input power and the ac output power are measured simultaneously. It is difficult

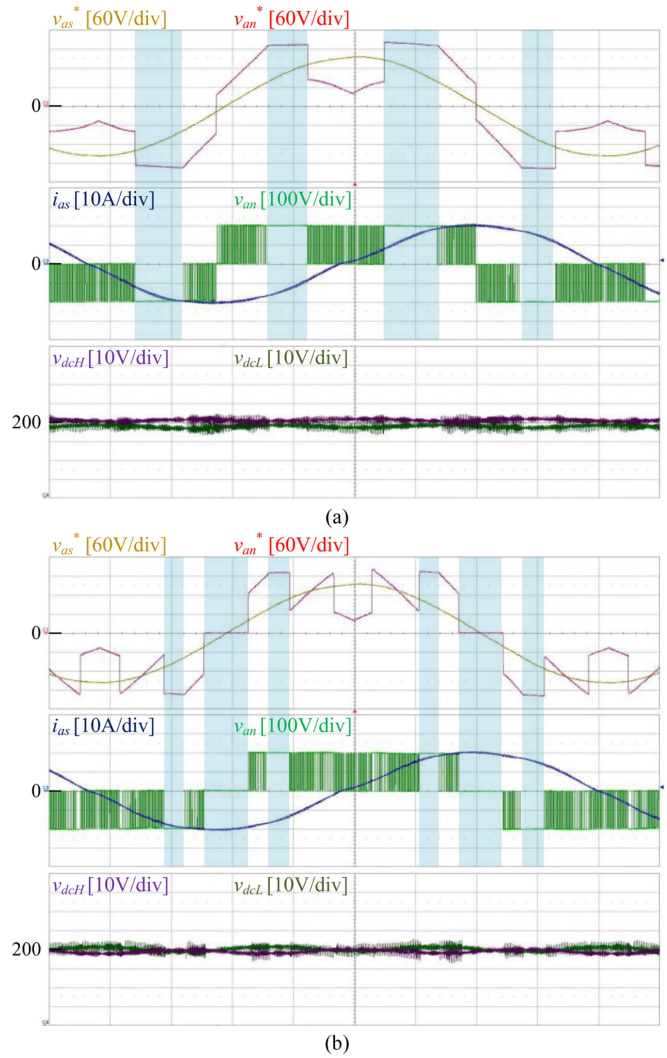

Fig. 18. Experimental results: Waveforms of the voltage reference and switching patterns in MI = 0.8, $\phi = 80°$ with (a) the conventional MLDPWM scheme and (b) the proposed MLDPWM scheme.

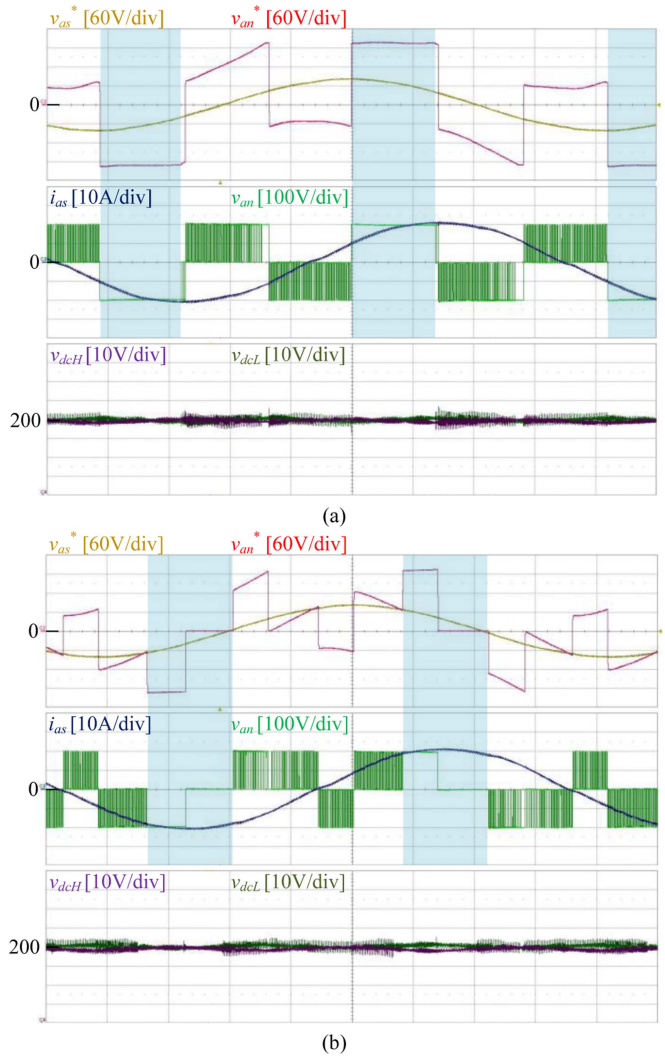

Fig. 19. Experimental results. Waveforms of the voltage reference and switching patterns in MI = 0.4, $\phi = 60°$ with (a) the conventional MLDPWM scheme and (b) the proposed MLDPWM scheme.

to distinguish between the switching and conduction losses. Therefore, the effectiveness of DPWM schemes is compared in terms of the inverter losses.

Fig. 18 shows the waveforms of voltage references, phase current, switching patterns of a-phase, and dc-link voltages when MI = 0.8 and $\phi = 80°$. The conventional two-level MLDPWM only utilizes the positive and negative clamping near the current peak as shown in Fig. 18(a). Otherwise, the proposed three-level MLDPWM utilizes the zero clamping near the current peak as shown in Fig. 18(b), which reduces the switching loss. It can be seen that the proposed MLDPWM scheme has clamping regions closer to the current peak compared to the conventional scheme, where the NP balancing is still achieved. The inverter loss is reduced by 10.9% from 156 to 139 W, which depends on the nonswitching regions near the current peaks of each phase.

Fig. 19 shows experimental results when MI = 0.4 and $\phi = 60°$. Likewise, the inverter loss is decreased by matching the clamping region to the current peak as shown in the shaded area. The voltage reference in the conventional scheme cannot be clamped to the neutral point as shown in Fig. 19(a). In contrast, the voltage reference in the proposed scheme is clamped to the neutral point near the current peak as shown in Fig. 19(b), which can reduce the switching loss to a minimum at low PFs. The inverter loss is reduced by 7.6% from 145 to 134 W. Furthermore, the difference between v_{dcH} and v_{dcL}, i.e., δv_{dc}, is maintained below 5 V when the proposed scheme is combined with the NP balancing controller by adjusting the ratio between positive and negative clamping, i.e., θ_{bal}.

The inverter loss, the current THD of a-phase, THD(i_{as}), and the maximum dc-link voltage difference, max(δv_{dc}), are listed in Table III according to the operating conditions. The proposed scheme minimizes not only the inverter loss but also the current THD. The switching loss and low-order harmonics induced by the dead time can be further reduced by minimizing the number of switching near the peak current. Furthermore, the difference between v_{dcH} and v_{dcL} is kept below 5 V by

TABLE III
EXPERIMENTAL RESULTS

Conditions		Conventional MLDPWM			Proposed MLDPWM		
MI	PF angle	Loss	THD(i_{as})	max(δv_{dc})	Loss	THD(i_{as})	max(δv_{dc})
0.4	60°	145 W	4.09 %	3.2 V	134 W	2.91 %	3.5 V
0.8	80°	156 W	5.39 %	2.7 V	139 W	4.05 %	4.0 V

applying the proposed method as well as by the conventional method. The dc balancing can be achieved by the NP balancing schemes. Thus, the proposed method can minimize the inverter losses by applying the zero clamping under the similar THD(i_{as}) and max(δv_{dc}).

VI. CONCLUSION

This article analyzes the zero clamping possible region in the voltage space vector of a three-level inverter. Based on the analysis, a carrier-based MLDPWM optimized for the three-level NPC inverters has been proposed within all ranges of PF angle (from 90° leading to 90° lagging) and modulation index (from 0 to $2/\sqrt{3}$). The proposed method outputs the offset voltage reference where both PF angle and MI are considered. The performance of the proposed method is compared with that of the conventional methods in the aspect of the SLF. Moreover, an NP balancing algorithm has been proposed to change the ratio between clamping states, which could work together with the proposed MLDPWM scheme. The proposed algorithm does not require any additional hardware and complex computation. Simulation and experimental results are provided to verify the performance of the proposed method. Compared to the conventional schemes, the proposed scheme minimizes the switching loss at lower PF while maintaining the NP balancing for the three-level NPC inverter.

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