Capacitance Distribution in Charge Pumps With Capacitive Load to Reduce Area and Input Energy

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***Abstract*—This work introduces a novel design strategy for reducing and optimizing the silicon area and input energy of Dickson charge pumps with a purely capacitive load. The strategy relies on the sizing of the pumping capacitors using a linear distribution, as counter-imposed to the conventional uniform distribution, which allows up to 75% (90% theoretical) of area savings without altering the transient performance. Theoretical analysis shows that the design strategy leads to the additional advantage of decreasing the input energy, thus relaxing the constraints of the ancillary circuitry. Design guidelines are provided to maximize the achievable improvements. Simulation results using a 65-nm CMOS technology confirm the validity of the proposed approach under various practical scenarios.**

***Index Terms*—Boost converters, dc–dc converters, Dickson charge pump (DCP), energy efficiency, energy harvesting, silicon area saving, switched capacitor converters.**

I. Introduction

A SWITCHED capacitor converter is among the best solutions for fully integrated dc–dc converters, even though it requires energy-hungry and expensive blocks in terms of silicon area occupation [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. Focusing on boost conversion, the widely adopted topology is the Dickson charge pump (DCP) [19], for which the literature reports a large number of works providing novel circuit solutions, optimized designs, and unconventional applications [20], [21], [22], [23], [24], [25].

Optimization of the DCP, which is the target pursued in this article, is constrained by the nature of the load, which can be: 1) purely capacitive, typical of power switches and piezo transducer drivers, capacitive power transfer, and some kinds of memories and 2) resistive and capacitive, characteristic of power converters [20], [21]. Specifically, for DCPs with only capacitive load, the performances that can be optimized are the rise time and the input energy during the start-up phase and/or steady state. To pursue optimization, the parameters that can be tuned are the conversion ratio; the frequency, duty cycle, or amplitude of the signals used to clock the charge pump (CP); or the capacitor for the charge transferring, called pumping capacitors [26], [27].

In the domain of CPs with capacitive loads, a few works have presented design optimization strategies. Two of them address the conventional DCP [28], [29], while one refers to a CP with unconventional sizing of the pumping capacitors among the stages [30]. In particular, Palumbo and Pappalardo [28] presented optimized strategies for designing CPs having only capacitive loads and targeting minimum silicon area, which is equivalent to minimum rise time, and minimum power consumption. This approach allows us to define the number of stages that minimize silicon area (and rise time) or maximize power efficiency for a given input and output voltage. In [29], to optimize a DCP with a capacitive load, a topology exploiting a clock boosting has been used. Starting from an accurate and simple model of the dynamic behavior of the DCP, the proposed design allows achieving a reduction of the rise time, or the area, between 10% and 60%, at the cost of a slight increase of circuit complexity.

All the previously cited papers built their design strategies under the silent common assumption that the DCP pumping capacitors have the same capacitance value. This is equivalent to stating that the total DCP capacitance is equally distributed along the stages, as originally introduced by Dickson [19].

Saeed et al. [30], on the contrary, introduced a novel sizing methodology for DCPs with pure capacitive loads based on the rearrangement of the total CP capacitance along the stages as a function of the capacitive load. The authors do not provide a closed-form solution, but a finite set of distributions that, under particular conditions, could reveal counterintuitive advantages and allow minimizing the rise time by no more than 25% for a defined silicon area.

In the domain of CPs without uniform capacitance distribution, the first solution that exploits a linear capacitance distribution was proposed in [31]. In that work, the idea of linearly distributing the total pumping capacitance along the stages was in-depth investigated, and conditions to achieve performance improvements were introduced. However, assuming this distribution, although a closed-form equation for the CP output resistance cannot be obtained, plots for an optimum design were provided to reduce the rise time for a given output capacitance value.

In this framework, this article introduces a novel design strategy for reducing and optimizing the silicon area and input

Received 17 February 2025; accepted 19 March 2025. Date of publication 24 March 2025; date of current version 30 June 2025. This work was supported in part by the Italian Minister of Research Programma Operativo Nazionale Ricerca e innovazione 2014-2020, Azione n. IV.6, and in part by the European Union (NextGeneration EU) through the Ministry of Education and Research National Recovery and Resilience Plan Project SAMOTHRACE under Grant ECS00000022. Recommended for publication by Associate Editor K. Chen. *(Corresponding author: Andrea Ballo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3554143.

Digital Object Identifier 10.1109/TPEL.2025.3554143

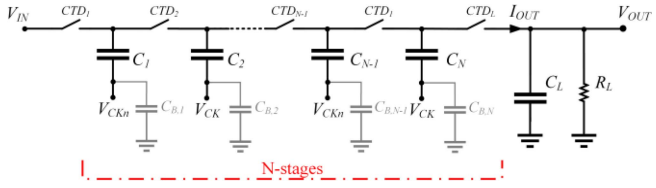

Fig. 1. Schematic diagram of the CP.

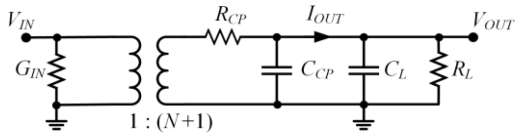

Fig. 2. Equivalent model of the CP in Fig. 1.

energy of DCPs with purely capacitive load. As demonstrated, exploiting the linear distribution of the total capacitance of the CP, up to 75% of area saving can be achieved without altering the transient performance as compared to the traditional sizing of the pumping capacitors.

Moreover, analytical derivation, adapting the equation model for DCP output resistance, shows that the design strategy leads to a further advantage in terms of input energy reduction, which also relaxes the constraints of the auxiliary circuits.

Design guidelines for maximizing the achievable improvements are provided, and simulation results using a 65-nm CMOS technology successfully validate the design strategy in various practical scenarios.

As compared with the prior art, the proposal in this article:

1) outclasses the maximum performance achievable with the approach proposed in [28] by breaking the limit given by the conventional distribution of the total CP capacitance;
2) does not require auxiliary blocks, as compared with [29];
3) does not need or is limited by a finite set of distributions, in contrariwise [30];
4) allows decreasing the occupied area of the CP by percentages higher than all the previously published works.

The rest of this article is organized as follows. Section II reports the analytical model of the DCP with linearly distributed capacitance, rewriting the main performance parameters in terms of the equivalent output resistance and capacitance. Section III introduces the proposed design strategy showing the theoretical possible advantages. Section IV reports extensive simulation results and comparisons between different cases of study in various scenarios. Finally, Section V concludes this article.

II. Analytical Description of the CP With Linearly Distributed Capacitance

The specific application sets the target output voltage, capacitive load, and number of stages. Hence, to reduce the input energy required by the CP during the pumping-up phase, we can reduce the CP total capacitance, C_{TOT}, or opportunely address the charge transfer along the CP stages.

Let us consider the simplified block scheme of an N-stage CP shown in Fig. 1, where each stage is made up of a capacitance, C_k, and a charge transfer device (CTD). In a first approximation, each CTD is modeled with a switch whose forward resistance and voltage drop are negligible. The capacitance, C_k, of the kth with $k = 1, 2, \ldots, N$, is set by the linear progression in [31]

$$C_k = \frac{C_{\text{TOT}}}{N}\left[1 + a\frac{2k-(N+1)}{N-1}\right]. \tag{1}$$

The slope a ranges from -1 to 0 to enable the benefit conditions as resulting in [31]. It is worth noting that the progression is designed to ensure that the sum of all the pumping capacitances coincides with C_{TOT} and that nullifying the slope ($a = 0$) gives the design solution back to the conventional Dickson topology.

Again, looking at Fig. 1, the output current, I_{OUT}, feeds the load, modeled by C_L and R_L, across which the output voltage, V_{OUT}, is generated. Finally, the bottom parasitic capacitances, depicted as $C_{\beta,k}$, are also included. Typically, being the area of the capacitors dominant over the entire circuit, it can be assumed that $C_{\beta,k}$ is exclusively associated with the stage capacitor, C_k. Therefore, as is often done, the bottom parasitic is accepted as proportional to the pumping capacitance by the technology-dependent factor, β [32], [33]. Without losing consistency, the effects of the top stray capacitances are neglected, as they are at least one order of magnitude lower than $C_{\beta,k}$. As in the conventional DCP, the signals used to clock the structure are generated from the input voltage; thus, their amplitude is equal to V_{IN}.

As shown in [33] and [34], the CP in Fig. 1 can be modeled by the equivalent circuit in Fig. 2, where the input conductor, G_{IN}, given by

$$G_{\text{IN}} = f\sum_{k=1}^{N} C_{B,k} = f\beta C_{\text{TOT}} \tag{2}$$

models the total power loss due to continuous commutations of the stray capacitances. Using (1), the output resistance and self-capacitance of the CP are, respectively, expressed by

$$R_{\text{CP}} = \sum_{k=1}^{N}\frac{1}{fC_k} = \frac{N^2}{fC_{\text{TOT}}}\sum_{k=1}^{N}\left\{N\left[1+a\frac{2k-(N+1)}{N-1}\right]\right\}^{-1} \tag{3}$$

$$C_{\text{CP}} = C_{\text{TOT}}A(N)\left[1 + a\frac{\left(7N^2-N+2\right)(N+1)}{\left(4N^2+3N+2\right)(2N-1)}\right] \tag{4}$$

where $A(N)$ is a function of N, and it was defined in [35].[1]

Neglecting the CTD forward resistance allows assuming that the CP works in slow switching limit (SSL), where the charge is entirely transferred between adjacent stages in a half-clock period. This clarifies the value of R_{CP} reported in (3), which only depends on the capacitive impedance offered by the pumping capacitors. Finally, the transformer operates as an ideal power converter. Hence, the I–V output characteristic of the CP is given

[1]From [35], we have $A(N) = \frac{4N^2+3N+2}{12N(N+1)}$, for even N; $A(N) = \frac{4N^2-N-3}{12N(N+1)}$, (for odd N).

by

$$V_{\mathrm{OUT}} = (N+1)\, V_{\mathrm{IN}} - R_{\mathrm{CP}} I_{\mathrm{OUT}}. \tag{5}$$

Neglecting the effect of the current load (i.e., R_L is infinite or very high compared to R_{CP}), the transient behavior of the circuit in Fig. 2 is characterized by the time constant

$$\tau_{\mathrm{CP}} = R_{\mathrm{CP}} \left(C_{\mathrm{CP}} + C_L\right) = R_{\mathrm{CP}} C_{\mathrm{CP}} \left(1 + C_L / C_{\mathrm{CP}}\right). \tag{6}$$

Considering (3) and (4), the intrinsic time constant in (6), $R_{\mathrm{CP}} \cdot C_{\mathrm{CP}}$, is independent from C_{TOT}. Moreover, from (6), we can use C_L/C_{TOT} to opportunely size the CP.

Neglecting second-order effects, such as reverse losses of the CTDs or inverse saturation currents of the parasitic junctions, the total energy demand of the CP can be expressed by

$$E_{\mathrm{IN}} = E_{\mathrm{CP}} + E_{\mathrm{SW}} \tag{7}$$

where E_{CP} represents the energy required by the CP to charge the internal capacitors and the output one and is given by

$$E_{\mathrm{CP}} = 0.5 \left(C_{\mathrm{CP}} + C_L\right) V_{\mathrm{OUT}}^2 \tag{8}$$

The term E_{SW} in (7) is the energy loss caused by continuous switching of the stray capacitances, expressed by

$$E_{\mathrm{SW}} = 0.5 G_{\mathrm{IN}} V_{\mathrm{IN}}^2 T_{\mathrm{ON}} \tag{9}$$

where T_{ON} is the operating time. Obviously, from (7), it is apparent that the switching energy loss is dominant when the operating time is long enough to make (8) negligible.

Finally, the power conversion efficiency in the steady state can be written as

$$\eta = \frac{V_{\mathrm{OUT}} I_{\mathrm{OUT}}}{V_{\mathrm{IN}} I_{\mathrm{IN}}} = \frac{1 - \frac{R_{\mathrm{CP}} I_{\mathrm{OUT}}}{(N+1) V_{\mathrm{IN}}}}{1 + \frac{G_{\mathrm{IN}} V_{\mathrm{IN}}}{(N+1) I_{\mathrm{OUT}}}} \tag{10}$$

where I_{IN} identifies the total input current of the CP.

A. Comparison With the DCP

Before proceeding with the description of the proposed design strategy in order to realize the effective advantages introduced by the linear distribution, it is useful to compare the parameters for a CP with linear distributed capacitance, henceforth indicated as LD-CP, with those of the conventional DCP (i.e., LD-CP with $a = 0$).

It is apparent that the input loss equivalent conductance, given by (2), scales with the CP area, since it depends on C_{TOT} only. Hence, a reduction of the area determines a proportional reduction of G_{IN}.

As concerning the CP output resistance, R_{CP}, since from (3) it is difficult to manage and express it in a compact analytical form, according to the Appendix, we approximate it as

$$R_{\mathrm{LD-CP}} \approx R_{\mathrm{DCP}} B(N, a) \tag{11}$$

where R_{DCP} is the value of R_{CP}, with $a = 0$ (DCP case) and

$$B\left(N, a\right) \approx \frac{2\left(\frac{0.92N-1}{2N-1}\right) a^2 + \left(2\frac{0.92N-1}{2N-1} + 1\right) a + 1}{a^2 + 2a + 1} \simeq \frac{0.92a^2 + 1.92a + 1}{a^2 + 2a + 1}. \tag{12}$$

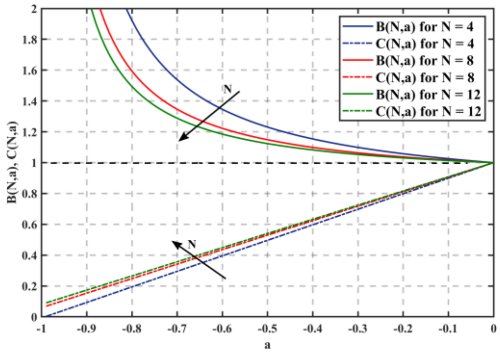

Fig. 3. Linear distributed CP equivalent parameters versus distribution slope for different number of stages.

The self-capacitance of the conventional DCP, C_{DCP}, and the proposed LD-CP, $C_{\mathrm{LD-CP}}$, is obtained from (4) setting $a = 0$ and $a \neq 0$, respectively. Assuming that the total occupied area of the two solutions is proportional to the total capacitance through the same constant technology parameter,[2] (4) can be rewritten as

$$C_{\mathrm{LD-CP}} = C_{\mathrm{DCP}} C\left(N, a\right) \tag{13}$$

where

$$C(N, a) = 1 + a \frac{\left(7N^2 - N + 2\right)(N+1)}{\left(4N^2 + 3N + 2\right)(2N-1)} \simeq 1 + \frac{7}{8} a. \tag{14}$$

Both the approximations in (12) and (14) hold for $N >> 4$ with an error lower than 10%. From (13) and (14), it is immediately visible that the self-capacitance is reduced for distributions with negative slopes, i.e., $a < 0$.

The coefficients $B(N,a)$ and $C(N,a)$ are plotted in Fig. 3 as functions of the slope a and for different number of stages. By inspection Fig. 3, and (11)–(14), it is apparent that the LD-CP output resistance, $R_{\mathrm{LD-CP}}$, increases by reducing the slope coefficient a, showing an asymptote for $a = -1$. On the other hand, the LD-CP self-capacitance, $C_{\mathrm{LD-CP}}$, linearly decreases with coefficient a.

Concerning the energy values in (7)–(9), they scale almost linearly, as G_{IN} and C_{CP}. Finally, it can be noted that the power conversion efficiency in (10) decreases with $R_{\mathrm{LD-CP}}$ proportionally to the current load (recalling that G_{IN} is independent of the coefficient a), but this parameter is not of interest for pure capacitive load applications.

III. Proposed Design Strategy

The proposed strategy aims to modify the design of a DCP with the main target of reducing its input energy and occupying a smaller silicon area. In this case of study where the load is purely capacitive, two important parameters are the settling time, which is proportional to the time constant, τ_{CP}, and the input energy, which affects the CP power consumption. With this in mind, let

[2] In practical cases, the CP area is dominated by the area occupied by the pumping capacitors. Assuming that the used capacitors are linear and their area is proportional to their capacitances, so $\mathrm{Area}_{\mathrm{CP}}$ is proportional to C_{TOT}.

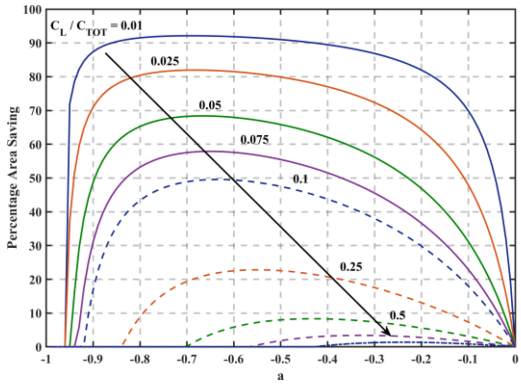

Fig. 4. Percentage area saving versus distribution slope for different C_L/C_{TOT} values.

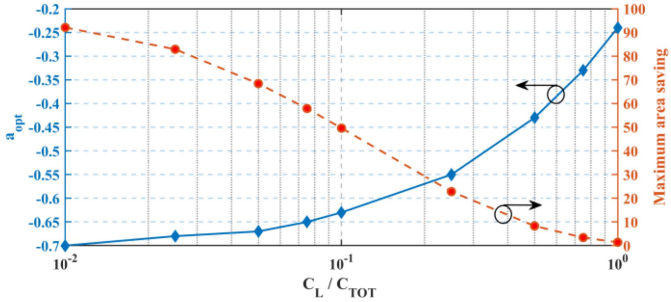

Fig. 5. Optimum slope and percentage of area saving versus C_L/C_{TOT}.

us assume to linearly distribute the total capacitance of the CP and to use a CTD with a negligible voltage drop. In such a case, the SSL condition is met if the CTD ON-resistance satisfies the following relation:

$$R_{\text{CTD}} \ll 1/2fC_{k,\text{AVG}} \tag{15}$$

where $C_{k,\text{AVG}}$ is the average value of the pumping capacitances.

For a typical design strategy, the area of the CP is chosen to fulfill the settling time constraint. In particular, to design the CP, the number of stages, through (5), is set to provide the output voltage requirement, the clock frequency, through (3) and (6), defines the intrinsic time constant, $R_{\text{CP}} \cdot C_{\text{CP}}$, and the ratio C_L/C_{TOT} is used to satisfy the transient behavior constraint.

Starting from the aforementioned considerations to set the value of the distribution slope, a, the conventional DCP and LD-CP are designed for the same constraints (i.e., same output and input voltages and rise time). Under this condition, both CPs have the same time constant, thus, to satisfy the rise time constraint; from (6), we can write

$$\begin{aligned} &R_{\text{DCP}}C_{\text{DCP}}\left(1+C_L/C_{\text{DCP}}\right) \\ &= R_{\text{LD-CP}}C_{\text{LD-CP}}\left(1+C_L/C_{\text{LD-CP}}\right). \end{aligned} \tag{16}$$

From (11) and (13), we get

$$\frac{R_{\text{LD-CP}}C_{\text{LD-CP}}}{R_{\text{DCP}}C_{\text{DCP}}} = B(N,a)\cdot C(N,a). \tag{17}$$

Moreover, naming $C_{\text{TOT,LD-CP}}$ and C_{TOT} the total capacitance of the LD-CP and DCP, respectively, from (4), $C_{\text{LD-CP}} = A(N)\ C(N,a)\ \ C_{\text{TOT,LD-CP}}$, which evaluated for $a = 0$ yields $C_{\text{DCP}} = A(N)C_{\text{TOT}}$. Hence, from (16) and (17), we get

$$C_{\text{TOT,LD-CP}} = C_{\text{TOT}}\frac{B\left(C_L/C_{\text{TOT}}\right)}{A\left(1-BC\right)+C_L/C_{\text{TOT}}}. \tag{18}$$

In (18), the coefficients A, B, and C coincide with the already defined $A(N)$, $B(N,a)$, and $C(N,a)$, respectively. It is worth noting that (18) divided by C_{TOT} holds the ratio $\text{Area}_{\text{LD-CP}}$ /Area_{DCP} and, in turn, the area saving obtainable by the strategy.

Equation (18) is used to figure out the percentage area saving, plotted in Fig. 4 as a function of the distribution slope, a, and for different ratios C_L/C_{TOT}. Curves in Fig. 4 clearly show that a high amount of silicon area can be saved by using the LD-CP. In particular, the smaller the value of C_L/C_{TOT}, the higher the reduction of the total capacitance of the LD-CP as compared to the DCP, while the advantage in terms of area is nullified for $C_L/C_{\text{TOT}} > 0.1$. Moreover, despite that the field of applications is limited to CP with a pure capacitive load, the proposed strategy is particularly useful when the lowest rise time is required. Indeed, from (6) introducing (3) and (4), the minimum time constant is reached when $C_{\text{CP}} > C_L$, meaning that C_{TOT} must be greater than C_L (i.e., the capacitance of the CP must be greater than the load).

By inspection of the plot in Fig. 4, we can derive the slope, a, which should be used to achieve the maximum area reduction. In other words, it is possible to find an optimum a for each C_L/C_{TOT} ratio, as shown in Fig. 5. However, choosing a slope close to -1 can determine:

1) an increase in the CP sensitivity to second-order effects due to a reduction of the last stage capacitance;
2) the need for a specific driver for the first-stage capacitance since its value can be too high;
3) a reduction of the LD-CP equivalent capacitance, which becomes negligible as compared to C_L.

Thus, the performance is dominated by the output resistance only, which is always worse than that of the DCP, resulting in the loss of the advantages introduced by the linear distribution. In conclusion, as a technical suggestion, it is better to exploit each specific curve concavity to obtain the best tradeoff between area saving and slope.

It is worth noting that the total energy of an LD-CP is reduced as well. Indeed, the two energy components in (7), being proportional to the CP total capacitance, are lowered. In particular, while E_{SW} in (9) is reduced proportionally to the area, E_{CP} in (8) approaches its minimum value when it is equal to $0.5C_LV_{\text{OUT}}^2$.

IV. Simulation Results and Comparison

Validation of the proposed design strategy is divided into two main parts. We start comparing semiideal CPs, which allow us to verify the accuracy of the procedure regardless of the technological parameters. Then, we considered real design cases assuming a 65-nm CMOS technology.

For both cases, the design flow is briefly summarized as follows.

1) The number of stages for each CP pair is obtained from (5).

TABLE I
PERFORMANCE SUMMARY

N	C_{TOT} (pF)			E_{IN} (nJ)			R_{OUT} (kΩ)		
	DCP	LD-CP	ε%	DCP	LD-CP	ε%	DCP	LD-CP	ε%
6	22	20	9.1	15.1	13.7	9.3	163.7	185.6	–13.4
8	60	48	20	37.4	29.6	30.8	106.9	150.7	–41
10	260	104	60	150.8	59.9	60.3	38.8	125.3	–222.9

Considered technological parameter: $\beta = 0.25$.

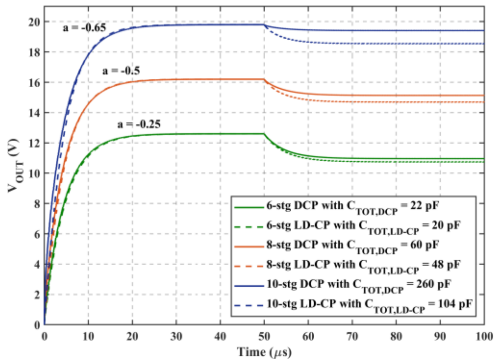

Fig. 6. CP transient response: a 10-μA current load is applied after 50 μs.

2) Starting from the rise time constraint and setting the clock frequency, f, the load capacitance, C_L, and the number of stages (previously calculated), the total CP capacitance, C_{TOT}, is derived for the DCPs.
3) From the plot in Fig. 5, we find the optimum slope, a_{OPT}. Hence, we have for the LD-CP both the CP total capacitance, $C_{TOT,LD-CP}$, from (18) and the values of the pumping capacitances from (1).

It is worth noting that to fully design a CP, and in particular to size the CTD, it is also necessary to consider the CTD ON-resistance, which is constrained by (15).

A. Semi-Ideal CP Design Validation

To validate the theoretical methodology, we considered three DCPs and the corresponding LD-CPs with equal input voltage, but different output voltages for each pair, thus having a different number of stages for each pair.

The design conditions assumed are $V_{IN} = 1.8$ V, $C_L = 20$ pF, $f = 10$ MHz, and the rise time target equal to 10 μs, which is equivalent to an RC time constant of about 4.4 μs. Moreover, the three output voltages, V_{OUT}, are equal to 12, 15, and 18 V, which result in a number of stages for each pair equal to 6, 8, and 10, respectively. These specifications are typical for power and memory applications, which require high on-chip voltage generation [36], [37]. Following the design procedure described previously, the total capacitance of the CP is summarized in Table I, from which the single pumping capacitance can be easily derived.

The transient behaviors of the three CP pairs are shown in Fig. 6. As expected, despite in each pair the LD-CP has a significantly lower total capacitance (see legend in Fig. 6), both CPs of the single pair have almost the same rise time.

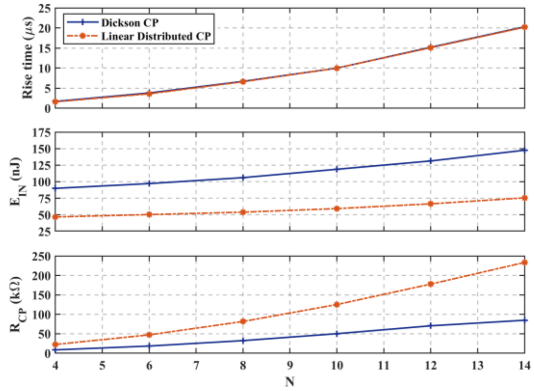

Fig. 7. Rise time, input energy, and output resistance for different number of stages, N; and $C_L/C_{TOT} = 0.1$, and $a = -0.65$ (area of LD-CP halved compared to the DCP one).

In order to evaluate the CPs' output resistance, the CPs were loaded with 10 μA after 50 μs, whose effect appears in the right part of Fig. 6. Of course, as predicted by (11) and (12), the output resistance of LD-CPs is increased, up to 3.2× in the worst case, due to both the linear distribution effect and the reduction of the total pumping capacitance, according to (3).

The main performances of the three CPs are summarized in Table I, where the percentage spread (ε%) for each parameter is also reported. An inspection of these provides further confirmation of the effectiveness of the proposed strategy, as both the input energy and the total pumping capacitance, and so the occupied area, drastically reduced by a factor up to about 60%, in accordance with the analytical model.

Another set of simulations was carried out by varying the number of stages, from 4 to 14, and by setting the ratio $C_L/C_{TOT} = 0.1$. From Fig. 5, the slope $a = -0.65$ and the LD-CP area is half of the DCP one. The corresponding rise time, input energy, and equivalent output resistance are reported in Fig. 7. Upon inspection of this figure, it is apparent that the rise time of both DCP and LD-CP is equal, while the LD-CP input energy is halved, like the total capacitance, and the LD-CP output resistance is more than doubled compared to the DCP. These results prove the validity of the model.

B. Transistor-Level CP Design Validation

Validation at the transistor level was carried out for $N = 8$ and two different load conditions, namely, $C_L = 2$ pF and $C_L = 20$ pF. The four CPs were implemented with a TSMC 65-nm standard low-voltage CMOS process, which provides metal–insulator–metal (MIM) capacitors tolerating up to 5 V ± 10%. The clock frequency is equal to 10 MHz, while the input voltage is 0.6 V.

The chosen topology for the CTD is the dual-branch cross-coupled (or latched) configuration illustrated in Fig. 8(a) [38], [39]. Regular threshold voltage transistors were used for the CMOS pair ($g_{ds,\square} = 16.7$ μA/V @$V_{IN} = 0.6$ V). It should be noted that (15) is valid if the transistors of the CTDs work in the super- or sub-threshold triode region; hence, the ON-resistance

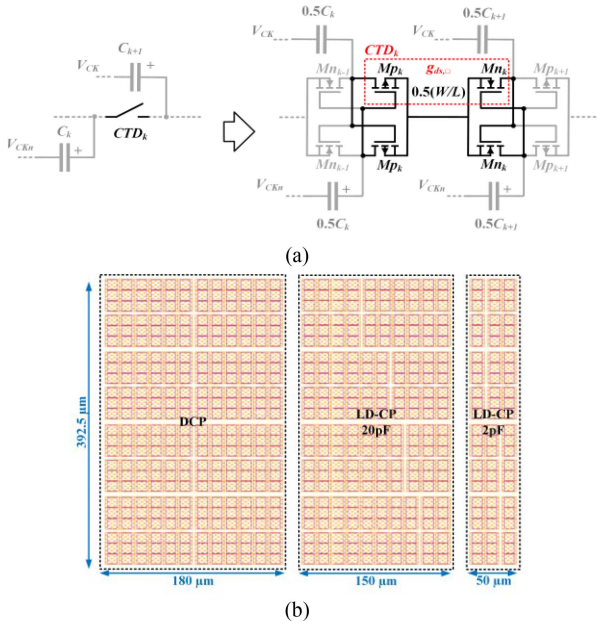

Fig. 8. Dual-branch cross-coupled configuration as (a) CTD and (b) CPs' layout comparison.

TABLE II
DESIGN PARAMETERS FOR THE COMPARED EIGHT-STAGE CPS

		*k*th stage								C_{TOT} (pF)
		1	2	3	4	5	6	7	8	
DCP *All* C_L	C_k (pF)	7.5	7.5	7.5	7.5	7.5	7.5	7.5	7.5	60
	R_k (Ω)	600								
	$(W/L)_k$	10*(600 nm/60 nm)								
LD-CP C_L=20 pF	C_k (pF)	9	8.2	7.3	6.4	5.6	4.7	3.8	3	48
	R_k (Ω)	750								
	$(W/L)_k$	8*(600 nm/60 nm)								
LD-CP C_L=2 pF	C_k (pF)	3.2	2.8	2.4	2	1.7	1.4	1	0.6	15
	R_k (Ω)	2400								
	$(W/L)_k$	3*(600 nm/60 nm)								

can be related to the MOSFET sheet conductance.[3] Therefore, by using this relationship, the MOSFETs' area or their aspect ratio is obtained. The calculated design parameters for the CPs are summarized in Table II.

It must be noted that $C_{k,\mathrm{AVG}}$ in (15) decreases as the total capacitance decreases. This aspect leads to a proportional scaling of the needed minimum CTD resistance and, hence, the decrease in the maximum aspect ratio of the transistors, resulting in a reduction of the total area occupied by the active device. Moreover, the scaling affects the drivers, which, in turn, become smaller than those of the DCP and, therefore, more efficient in terms of efficiency (due to lower equivalent input capacitances and short-circuit currents [33]). Fig. 8(b) shows the layout of the three compared CPs, and to effectively model the loading devices, MIM capacitors, not present in Fig. 8(b), are connected to the CPs' output node in the postlayout schematic.

[3]The MOSFET sheet conductance $g_{\mathrm{ds},\Omega}$ can be expressed as follows [40]:
1) $[K_{\mathrm{EQ}}(V_{\mathrm{IN}} - V_{\mathrm{TH}})]^{-1}$ for the superthreshold triode region
2) $[K_{\mathrm{EQ}} e^{V_{\mathrm{IN}}/nv_T}/v_T]^{-1}$ for the subthreshold triode region
where K_{EQ} is the transconductance parameter, V_{TH} and v_T are the threshold and thermal voltages, respectively, and n is the ideality factor.

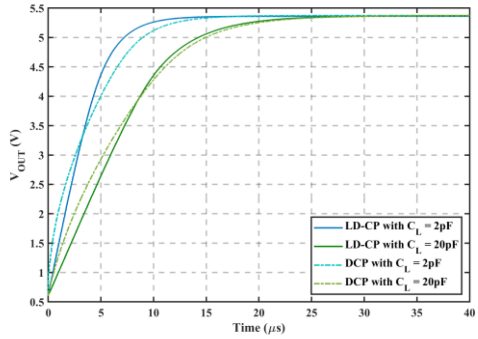

Fig. 9. Transient responses of the compared eight-stage CPs.

TABLE III
MONTE CARLO SIMULATION RESULTS (C_L = 20 PF)

	T_R (µs)			$E_{\mathrm{IN,Start\text{-}Up}}$ (nJ)			$E_{\mathrm{IN,Steady\text{-}State}}$ (pJ)		
	µ	Σ	Δ%	M	σ	Δ%	µ	σ	Δ%
DCP	13.66	0.74	5.4	1.13	0.02	1.8	92.9	0.13	0.1
LD-CP	13.03	0.76	5.8	0.95	0.01	1.1	79.2	0.13	0.1

µ is the mean value, **σ** is the standard deviation, and **Δ%** is the variation coefficient.

TABLE IV
MONTE CARLO SIMULATION RESULTS (C_L = 2 PF)

	T_R (µs)			$E_{\mathrm{IN,Start\text{-}Up}}$ (nJ)			$E_{\mathrm{IN,Steady\text{-}State}}$ (pJ)		
	µ	σ	Δ%	µ	σ	Δ%	µ	σ	Δ%
DCP	8.17	0.42	5.1	0.62	0.02	3.2	92.8	0.08	0.1
LD-CP	6.57	0.33	5	0.24	0.01	4.2	35.9	0.07	0.1

µ is the mean value, **σ** is the standard deviation, and **Δ%** is the variation coefficient.

Fig. 9 reports postlayout transient responses of the compared CPs for C_L = 20 pF and C_L = 2 pF. Again, from Fig. 9, the rise times are equal for both pairs.

The advantages of the proposed strategy are evident in Tables III and IV, which compare the Monte Carlo simulation (1000 iterations over process and mismatch variations) results for DCPs and LD-CPs, at C_L equal to 20 and 2 pF, respectively, in terms of rise time and input energy at a temperature of 27 °C. It is worth noting that the energy is divided into the start-up energy, which is the total energy needed to charge the capacitor batch until the rise time, and steady-state energy, which is the energy required to maintain a stable output voltage for 10 μs.

From the numerical comparison, it is possible to state that the proposed design strategy effectively improves the energy performance, compared with the DCP. In particular, when C_L is 20 pF, the percentage area saving is 20%, while the start-up input energy, $E_{\mathrm{IN,Start\text{-}Up}}$, reduction is 16%. When C_L is 2 pF, the percentage area saving is 75% and the energy saving, during both the start-up and the steady state, $E_{\mathrm{IN,Steady\text{-}State}}$,[4] is 61.3%. Furthermore, it is worth noting that variation coefficients are

[4]It must be specified that the input energy in the steady state, $E_{\mathrm{IN,Steady\text{-}State}}$, as defined in this section, coincides with E_{SW} in (9). From it, the technology-dependent factor, β, can be valued to be about 8.5%.

TABLE V
CORNER AND TEMPERATURE SIMULATION RESULTS ($C_L = 20$ pF)

		T_R (µs)			$E_{IN,\,Start\text{-}Up}$ (nJ)			$E_{IN,\,Steady\text{-}State}$ (pJ)		
		–40°C	27°C	85°C	–40°C	27°C	85°C	–40°C	27°C	85°C
TT	DCP	17.01	13.51	12.05	1.19	1.13	1.1	93	92.9	93
	LD-CP	16.15	12.9	11.56	1.01	0.95	0.92	78.9	78.7	79.1
SS	DCP	23.56	16.01	13.2	1.38	1.24	1.19	92.7	92.8	92.8
	LD-CP	21.8	14.7	12.15	1.15	1.02	0.97	77.3	77.5	77.4
SF	DCP	16.55	13.4	12	1.19	1.13	1.1	92.8	92.8	93
	LD-CP	15.7	12.8	11.55	1	0.95	0.92	78	77.9	77.9
FS	DCP	20.35	14.96	12.85	1.25	1.16	1.12	93	93	93.5
	LD-CP	19.35	14.17	12.25	1.07	0.97	0.94	79.6	79.5	80.1
FF	DCP	14.5	12.65	11.85	1.08	1.05	1.04	93	93.2	95.4
	LD-CP	14.4	12.7	12	0.94	0.91	0.9	80.9	81.2	83.6

µ is the mean value, **σ** is the standard deviation, and **Δ%** is the variation coefficient.

TABLE VI
CORNER AND TEMPERATURE SIMULATION RESULTS ($C_L = 2$ pF)

		T_R (µs)			$E_{IN,\,Start\text{-}Up}$ (nJ)			$E_{IN,\,Steady\text{-}State}$ (pJ)		
		–40°C	27°C	85°C	–40°C	27°C	85°C	–40°C	27°C	85°C
TT	DCP	10.25	8.1	7.15	0.66	0.62	0.6	93	92.9	93
	LD-CP	8.07	6.5	5.85	0.27	0.24	0.23	38.1	35.7	35.7
SS	DCP	14.8	10.11	8.3	0.81	0.72	0.69	92.7	92.8	92.8
	LD-CP	11.2	7.65	6.36	0.34	0.27	0.25	38.9	34.8	33.9
SF	DCP	10.05	8.05	7.15	0.66	0.62	0.61	92.8	92.8	93
	LD-CP	8.05	6.5	5.9	0.27	0.24	0.23	38	37.9	38.1
FS	DCP	12.11	8.97	7.65	0.69	0.64	0.61	93	93	93.5
	LD-CP	9.55	7.1	6.2	0.3	0.25	0.23	40.4	40.3	41.2
FF	DCP	8.15	7.05	6.55	0.56	0.54	0.53	93	93.2	95.4
	LD-CP	6.95	6.15	5.85	0.24	0.22	0.22	39.9	40.4	43.5

µ is the mean value, **σ** is the standard deviation, and **Δ%** is the variation coefficient.

similar for the various CPs, highlighting that no worsening is caused by the linear distribution.

Finally, Tables V and VI present corner and temperature simulation results for C_L equal to 20 and 2 pF, respectively. Inspection of these tables proves that advantages are maintained across corners and temperatures in the range [–40 °C, 85 °C] with a slight reduction in the energy saving, which in the worst case is equal to 16.7% (Slow-Slow corner @ –40 °C).

V. CONCLUSION

This article introduces an approach for optimizing the silicon area occupation and the input energy demand in DCPs with a purely capacitive load. The proposed design strategy exploits the advantages of charge transfer boosting to decrease the required total capacitance and relies on the sizing of the pumping capacitors through a linear distribution, which allows maintaining the rise time unaltered compared to the traditional uniform sizing.

The goal has been achieved by carefully choosing the optimal slope for the linear distribution of the CP total capacitance, which enabled a drastic decrease in the total silicon area and the input energy. Design guidelines are also provided to obtain the optimal values according to the specifications of the output voltage, rise time, and capacitive load.

This approach has been validated by extensive simulation on a semi-ideal model, which confirmed the theoretical predictions. Then, to validate the design approach in a realistic environment, CPs have been designed at the transistor level and compared through postlayout simulation using a 65-nm standard CMOS technology. The obtained results confirmed the proposed design strategy in various scenarios, achieving energy savings of about (but not limited to) 61.3%, with an occupied area 75% smaller than that of the conventional DCP.

The full agreement between the semi-ideal and transistor-level validation results confirms that the proposed design strategy can be applied independently of the technology used, provided that the described operative conditions are satisfied.

APPENDIX

To demonstrate the accuracy of the model introduced in Section II-A, this appendix reports a comparison between the approximated relationship in (12), obtained from (3), and the results of applying a best fit to the simulated curves for different numbers of stages.

The constant in (12), $B(N,a)$, is shown in Fig. 10 as a function of the distribution slope a and for different numbers of stages. From Fig. 10, the maximum accuracy error is about 5%.

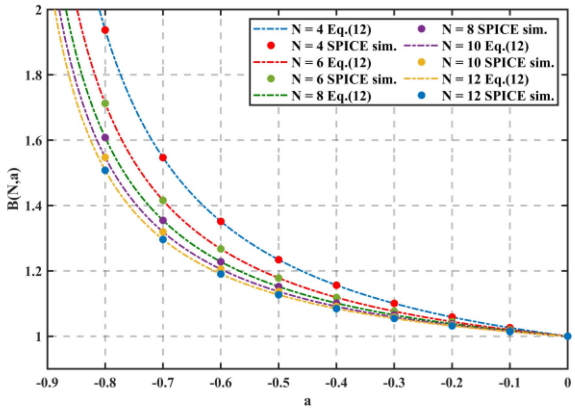

Fig. 10. Stage time constant as a function of the pumping capacitance.

REFERENCES

[1] S. Song, A. Novello, and T. Jang, "Design challenges of fully integrated DC–DC converters for modern power delivery architectures," *IEEE Solid-State Circuits Lett.*, vol. 7, pp. 267–270, 2024, doi: 10.1109/LSSC.2024.3457272.

[2] C.-J. Tsai, C.-H. Hsu, C.-J. Chen, Y.-T. Hung, and C.-Y. Hsieh, "A monolithic all-1.8 V-thin-gate-NMOS KY-boost converter with reused flying-capacitor bootstrap gate driver achieving 94.42% peak efficiency," *IEEE Trans. Power Electron.*, vol. 39, no. 6, pp. 7238–7251, Jun. 2024, doi: 10.1109/TPEL.2024.3374278.

[3] A. Ballo, A. D. Grasso, and G. Palumbo, "A current-efficient pseudo-3D regulated Dickson charge pump," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9878–9890, Aug. 2024, doi: 10.1109/TPEL.2024.3397791.

[4] J. Gao, J. Zhao, K. Nie, and J. Xu, "A low ripple and fast transient response charge pump in CMOS image sensors," *IEEE Sens. J.*, vol. 24, no. 6, pp. 8142–8149, Mar. 2024, doi: 10.1109/JSEN.2024.3359280.

[5] E. Emanović, D. Jurišić, and J. Shor, "A fully integrated, switched-capacitor DC–DC buck converter featuring an inverter-based comparator," *IEEE Access*, vol. 12, pp. 86425–86433, 2024, doi: 10.1109/ACCESS.2024.3412924.

[6] T. Park, H. Kim, M. Jeong, I. Park, and C. Kim, "A fully integrated dual-output continuously scalable-conversion-ratio SC converter for battery-powered IoT applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 8, pp. 3463–3475, Aug. 2024, doi: 10.1109/TCSI.2024.3396702.

[7] Q. Lu, S. Li, B. Zhao, J. Jiang, Z. Chen, and S. Du, "A dynamically reconfigurable recursive switched- capacitor DC–DC converter with adaptive load ability enhancement," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 5032–5040, Apr. 2023, doi: 10.1109/TPEL.2023.3235305.

[8] M. Megahed and T. Anand, "A sub-μW energy harvester architecture with reduced top/bottom plate switching loss achieving 80.66% peak efficiency in 180-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1386–1399, May 2023, doi: 10.1109/JSSC.2023.3241878.

[9] I. Park, J. Jeon, H. Kim, T. Park, J. Jeong, and C. Kim, "A thermoelectric energy-harvesting interface with dual-conversion reconfigurable DC–DC converter and instantaneous linear extrapolation MPPT method," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1706–1718, Jun. 2023, doi: 10.1109/JSSC.2022.3214839.

[10] M. W. Kim and J. J. Kim, "Energy-efficient fast-transient dynamic reconfigurable charge pump for multi-channel electrical stimulation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 6, pp. 2146–2150, Jun. 2023, doi: 10.1109/TCSII.2022.3228871.

[11] I. Park, H. Kim, T. Park, J. Jeong, and C. Kim, "An automotive 12 V-to-1.2 V integrated switched-capacitor DC–DC converter for improved load transient response," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12315–12319, Oct. 2023, doi: 10.1109/TPEL.2023.3292276.

[12] T. S. Ho et al., "Low voltage switched-capacitive-based reconfigurable charge pumps for energy harvesting systems: An overview," *IEEE Access*, vol. 10, pp. 126910–126930, 2022, doi: 10.1109/ACCESS.2022.3226783.

[13] J. Tao, W. Mao, Z. Luo, L. Zeng, and C.-H. Heng, "A fully integrated power converter for thermoelectric energy harvesting with 81% peak efficiency and 6.4-mV minimum input voltage," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 4968–4972, May 2022, doi: 10.1109/TPEL.2021.3134367.

[14] Y. Yamauchi, T. Sai, K. Hata, and M. Takamiya, "0.55 W, 88%, 78 kHz, 48 V-to-5 V Fibonacci hybrid DC–DC converter IC using 66 mm3 of passive components with automatic change of converter topology and duty ratio for cold-crank transient," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9273–9284, Aug. 2021, doi: 10.1109/TPEL.2021.3058207.

[15] S. Dam and P. Mandal, "A hybrid, fully-integrated, dual-output DC–DC converter for portable electronics," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4360–4370, Apr. 2021, doi: 10.1109/TPEL.2020.3019273.

[16] S. Kennedy, D. Morrison, D. Delic, M. R. Yuce, and J.-M. Redouté, "Fully-integrated Dickson converters for single photon avalanche diode arrays," *IEEE Access*, vol. 9, pp. 10523–10532, 2021, doi: 10.1109/ACCESS.2021.3050170.

[17] S. Marconi, G. Spiazzi, A. Bevilacqua, and M. Galvano, "A novel integrated step-up hybrid converter with wide conversion ratio," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2764–2775, Mar. 2020, doi: 10.1109/TPEL.2019.2931875.

[18] P.-H. Chen, H.-C. Cheng, and P.-H. Chen, "A fully integrated step-down switched-capacitor DC–DC converter with dual output regulation mechanisms," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 9, pp. 1649–1653, Sep. 2020, doi: 10.1109/TCSII.2020.3008972.

[19] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976, doi: 10.1109/JSSC.1976.1050739.

[20] T. Tanzawa, "On-chip high-voltage generator design: Design methodology for charge pumps," in *Analog Circuits and Signal Processing*, 2nd ed. Berlin, Germany: Springer, 2016.

[21] A. Ballo, A. D. Grasso, and G. Palumbo, *High-Performance Integrated Charge Pumps: Design and Novel Solutions*. Berlin, Germany: Springer, 2024.

[22] G. Palumbo and D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies," *IEEE Circuits Syst. Mag.*, vol. 10, no. 1, pp. 31–45, First Quarter 2010, doi: 10.1109/MCAS.2009.935695.

[23] C. A. Pinheiro, F. Olivera, and A. Petraglia, "A three-stage charge pump with forward body biasing in 28 nm UTBB FD-SOI CMOS," *IEEE Trans. Circuits Syst. Reg. Papers*, vol. 68, no. 11, pp. 4810–4819, Nov. 2021, doi: 10.1109/TCSI.2021.3112993.

[24] B. Abaravicius, S. Cochran, and S. Mitra, "High-efficiency high voltage hybrid charge pump design with an improved chip area," *IEEE Access*, vol. 9, pp. 94386–94397, 2021, doi: 10.1109/ACCESS.2021.3091808.

[25] Z. Zhou and M. Tan, "A 20-V pulse driver based on All-nMOS charge pump without reversion loss and overstress in 65-nm standard CMOS technology," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 32, no. 10, pp. 1812–1821, Oct. 2024, doi: 10.1109/TVLSI.2024.3435974.

[26] A. Ballo, M. Bottaro, A. D. Grasso, and G. Palumbo, "Regulated charge pumps: A comparative study by means of verilog-AMS," *Electronics*, vol. 9, no. 6, 2020, Art. no. 998.

[27] J. Jiang, X. Liu, W.-H. Ki, P. K. T. Mok, and Y. Lu, "Circuit techniques for high efficiency fully-integrated switched-capacitor converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 2, pp. 556–561, Feb. 2021, doi: 10.1109/TCSII.2020.3046514.

[28] G. Palumbo and D. Pappalardo, "Charge pump circuits with only capacitive loads: Optimized design," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 2, pp. 128–132, Feb. 2006, doi: 10.1109/TCSII.2005.855732.

[29] A. Ballo, A. D. Grasso, G. Giustolisi, and G. Palumbo, "Optimized charge pump with clock booster for reduced rise time or silicon area," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 12, pp. 1977–1981, Dec. 2019.

[30] A. Saeed, S. Ibrahim, and H. F. Ragai, "A sizing methodology for rise-time minimization of Dickson charge pumps with capacitive loads," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 10, pp. 1202–1206, Oct. 2017, doi: 10.1109/TCSII.2017.2687864.

[31] A. Ballo, A. D. Grasso, G. Palumbo, and T. Tanzawa, "Linear distribution of capacitance in Dickson charge pumps to reduce rise time," *Int. J. Circuit Theory Appl.*, vol. 48, no. 4, pp. 555–566, 2020.

[32] T. Tanzawa, "A switch-resistance-aware Dickson charge pump model for optimizing clock frequency," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 6, pp. 336–340, Jun. 2011, doi: 10.1109/TCSII.2011.2158166.

[33] A. Ballo, A. D. Grasso, G. Palumbo, and T. Tanzawa, "A charge loss aware advanced model of Dickson voltage multipliers," *IEEE Access*, vol. 10, pp. 118082–118092, 2022, doi: 10.1109/ACCESS.2022.3218901.

[34] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008, doi: 10.1109/TPEL.2007.915182.

[35] T. Tanzawa and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1231–1240, Aug. 1997, doi: 10.1109/4.604079.

[36] T. Tanzawa, T. Murakoshi, T. Kamijo, T. Tanaka, J. J. McNeil, and K. Duesman, "Design challenge in 3D NAND technology: A 4.8X area- and 1.3X power-efficient 20V charge pump using tier capacitors," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2016, pp. 165–168, doi: 10.1109/ASSCC.2016.7844161.

[37] B. Shen, S. Bose, and M. L. Johnston, "A 1.2V-20V closed-loop charge pump for high dynamic range photodetector array biasing," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 3, pp. 327–331, Mar. 2019, doi: 10.1109/TCSII.2018.2850341.

[38] R. Gariboldi and F. Pulvirenti, "A monolithic quad line driver for industrial applications," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 957–962, Aug. 1994, doi: 10.1109/4.297702.

[39] R. Gariboldi and F. Pulvirenti, "A 70 mΩ intelligent high side switch with full diagnostics," in *Proc. 21st Eur. Solid-State Circuits Conf.*, 1995, pp. 262–265.

[40] F. Pan and T. Samaddar, *Charge Pump Circuit Design*, 1st ed. New York, NY, USA: McGraw Hill, 2006.

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