Analysis and Suppression of Common Mode Noise for Underwater IPT Systems With Parasitic Capacitances

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***Abstract*—The high conductivity of seawater significantly intensifies the parasitic capacitances in the inductive power transfer (IPT) system which exacerbates the common-mode (CM) interference. This special phenomenon critically affects the reliability of underwater IPT systems. To address this issue, this article models the parasitic capacitance of components in IPT systems when immersed in seawater and presents the measurement methods for parasitic capacitance. Subsequently, a refined circuit topological model based on *LCC*-S is built to analyzed the CM crosstalk pathways and the magnitude in different medium. Additionally, a CM noise suppression method based on balanced impedance is derived through mathematical formulation. An experimental platform is constructed with an output power of 1 kW, which is used to validate the feasibility of the proposed design against a conventional *LCC*-S network.**

***Index Terms*—Balanced impedance, common mode (CM) noise, inductive power transfer (IPT), parasitic capacitances, underwater.**

NOMENCLATURE

C_{pn}	Parasitic capacitance between the sea water and sealed case.
C_{cg}	Parasitic capacitance between the two coil spools.
C_{in}	Parasitic capacitance in each turn of the coil.
$C_{\mathrm{ig1}}/C_{\mathrm{ig2}}$	Sum of C_{in} in primary side/ secondary side.
C_{fg}	Parasitic capacitance between the coil and sealing case.
C_{pg}	Parasitic capacitance between the coil and the ground.
C_{Dg}	Parasitic capacitance C_{Dg} between the drain and heat sink of the MOSFET.
C_{sg}	Parasitic capacitance C_{sg} between the diode and the heatsink.
C_{dg}	Parasitic capacitance of the dc input conductors to ground.
I_{Ccg}	CM current flowing through the C_{cg}.
$I_{\mathrm{CM1}}/I_{\mathrm{CM2}}$	CM current in the system.
Z_{Ccg}	Impedance of C_{cg}.
ε_0	Absolute dielectric constant.
ε_1	Relative dielectric constant.
S	Surface area of the two plates facing each other.
h_{ps}	Distance between two coils.
C_{s}	Capacitance to compensate the receiving coil.
$C_{\mathrm{s11}}/C_{\mathrm{s22}}$	Split capacitance of C_{s}.
L_{f}	Compensate inductance in the primary side.
k	Proportion coefficient to describe the split inductance value of L_{f}.
$L_{\mathrm{f11}}/L_{\mathrm{f22}}$	Split inductance of L_{f}.
v_{AN}	Voltage between node A and the reference node *N*.
v_{CE}	Voltage between node C and the reference node *E*.
v_{NG}	Voltage between the node N and the ground.
v_{Lf11}	Voltage of the split inductance L_{f11}.
$v^{\mathrm{dm}}{}_{\mathrm{AB}}$	DM voltage of the A, B point.
$v^{\mathrm{cm}}{}_{\mathrm{AB}}$	CM voltage of the A, B point.
$i^{\mathrm{dm}}{}_{\mathrm{Lf}}$	DM current of the inductor L_{f}.
$i^{\mathrm{cm}}{}_{\mathrm{Lf}}$	CM current of the inductor L_{f}.
v_{equ}	CM voltage of the inductor L_{f}.
$L_{\mathrm{f,eq}}, C_{\mathrm{p,eq}}, C_{\mathrm{s,eq}}$	Equivalent parameter of $L_{\mathrm{f11}}$and L_{f12}, $C_{\mathrm{p11}}$and C_{p12}, $C_{\mathrm{s11}}$and C_{s12} in parallel.
V_{cm}	Equivalent CM voltage source of V_{inv1} and V_{inv2}.

I. INTRODUCTION

AUTONOMOUS underwater vehicle (AUV) is extensively employed in marine research, resource exploration, and so

Received 28 November 2024; revised 16 February 2025; accepted 25 March 2025. Date of publication 2 April 2025; date of current version 30 June 2025. This work was supported in part by the National Natural Science Foundation of China under Grant 52401406, in part by the Taishan Scholars of Shandong Province under Grant tsqnz20240801, and in part by the National Natural Science Foundation of China under Grant 52301398. Recommended for publication by Associate Editor J. Acero. *(Corresponding author: Chunwei Cai.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3557090.

Digital Object Identifier 10.1109/TPEL.2025.3557090

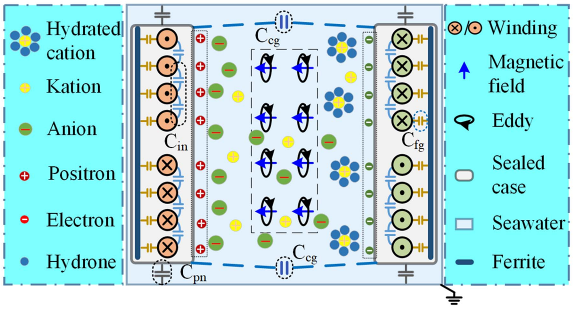


Fig. 1. Interaction between the underwater IPT systems and the seawater environment, including seawater eddy current and parasitic capacitance.

on. However, the limited battery capacity causes the constraint of AUV cruising ability [1]. The inductive power transfer (IPT) technology, which has the advantage of contactless charging capability is an effective solution for energy replenishment in AUV.

The presence of a large number of ions enables seawater to possess good electrical conductivity. Implementing wireless power transmission in the special medium of seawater will inevitably lead to some unique phenomena. As shown in Fig. 1, high-frequency magnetic fields can induce eddy current losses and result in a reduction in the efficiency of the IPT system. Recent studies have investigated the factors influencing eddy current issues in seawater IPT systems. Researchers have quantitatively measured the eddy current loss power and proposed methods for its reduction [2], [3].

After immersion in seawater, the enhanced parasitic capacitance between components (such as coils, devices, and circuits) and the common ground is another unique characteristic of seawater-based capacitive power transfer [4]. As shown in Fig. 1, taking the coil as an example, when the coil is immersed in seawater, the presence of seawater ions around the coupling coils can create a quasi-electric double layer, which intensifies the capacitive effects between the coils and the seawater [5]. Meanwhile, the seawater severs as a common ground, significantly reducing the coupling distance between the coil and the common ground, and the parasitic capacitance C_{pn}, which exists at the junction of sea water and sealed case will sharply increase, the interwinding capacitance C_{cg}, which exists between the two coil spools, will also have a sharp growth and enhance the coupling capability of the parasitic capacitance between the primary and secondary sides [6] and the C_{in} exists in each turn of the coil [7]. The parasitic capacitances above will be enhanced, which exacerbate the conducted electromagnetic interference (EMI) in the IPT system. However, there is little research on the impact of parasitic capacitance on underwater IPT systems, this article will focus on the EMI phenomenon caused by parasitic capacitors to study suppression methods.

The EMI problem is an important research area in the power electronic devices, including the generation, propagation, influence, and suppression. And the common-mode EMI (CM-EMI) is especial common in high-frequency switch power, such as the inverter of IPT system, it is usually caused by the high-frequency dv/dt in MOSFET inverter and parasitic capacitance effect among the switching device and heatsink [8]. The CM noise (current) is typically propagated through parasitic capacitance between the switching device and ground, as well as the parasitic capacitance between the IPT coil windings [9]. In the IPT system, the CM noise will interfere with semiconductor devices and cause the control system to fail that present safety risks. The CM noise suppression methods are usually including the three aspects: the PCB layout design, which reduce the CM noise at the source, the design of transformer coil and application of filter techniques which interrupt the noise in the propagation path [9], [10].

At present, many research teams have made excellent contributions to the application of IPT in underwater AUVs [11], [12], [13]. However, in the authors' previous research [14], the issue of CM noise in IPT system has gradually gained the attention of authors. So, in this article, the issue of CM noise in seawater IPT systems will be subjected to thorough investigation, the principal research content is delineated as follows.

1) The distribution of parasitic capacitance in the seawater IPT system is analysis and the measurement method of the static parasitic capacitance is present.
2) The refined CM noise transmission model based on parasitic capacitance has been established, and distinguishing between models for air and water (freshwater/seawater) media.
3) The CM noise of the IPT system is measured, and its transmission characteristics in different media are analyzed. The suppressibility of CM noise in the seawater is validated by employing a traditional balanced impedance.

II. ANALYSIS AND MEASUREMENT OF PARASITIC CAPACITANCE IN SEAWATER IPT SYSTEMS

Parasitic capacitance is a primary source and propagation path for CM noise in seawater IPT systems. Therefore, it is crucial for the IPT system to consider the parasitic capacitance in the components, analyze the causes of CM noise generation, and implement effective suppression methods. This section will analyze the parasitic capacitance in the components and propose the measurement of the parasitic capacitance in coil and electric devices.

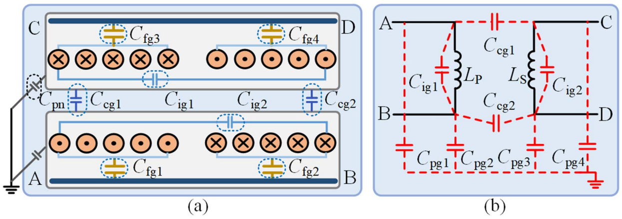
A. Analysis of Parasitic Capacitance in Coupling Coils and Electronic Devices of Seawater IPT Systems

The parasitic capacitance on the inverter side is a major source for the system CM noise. The following analysis will focus on the parasitic capacitance in the coupling devices and power devices.

1) Analysis of Parasitic Capacitance in Coupling Coils: The parasitic capacitance creates a propagation path for CM noise, as shown in Fig. 1. The parasitic capacitance model of coupling coil is simplified in Fig. 2.

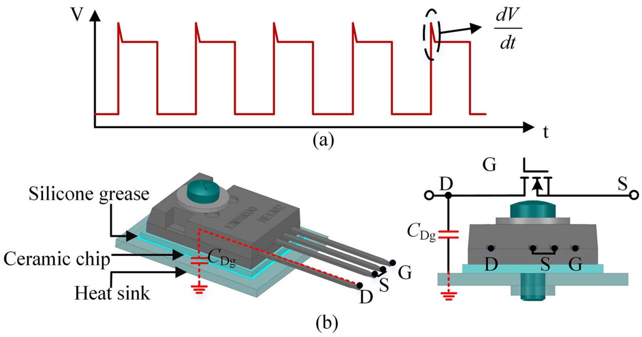
The C_{ig1} can be obtain by (1), and the C_{ig2} can also be obtained in the same. The C_{in} is the interturn capacitance, the q is the turn number of the coil

$$\frac{1}{C_{\mathrm{ig1}}} = \sum_{\mathrm{m}=1}^{2q-2} \frac{1}{C_{\mathrm{inm}}}. \tag{1}$$



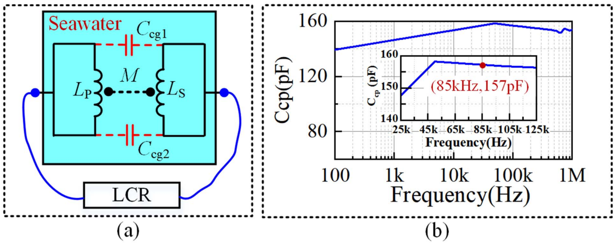
(a) (b)

Fig. 2. Parasitic capacitance in the coupling coils. (a) Equivalent distribution of parasitic capacitance of coil. (b) Coupling coil parasitic capacitance equivalent circuit.



(a)
(b)

Fig. 3. CM noise of MOSFET. (a) Voltage spikes at the inverter output. (b) Parasitic capacitance of the MOSFET during operation.



(a) (b)

Fig. 4. C_{cg} measurement method. (a) Practical measurement scheme of coupling coil interturn capacitance. (b) LCR test result.

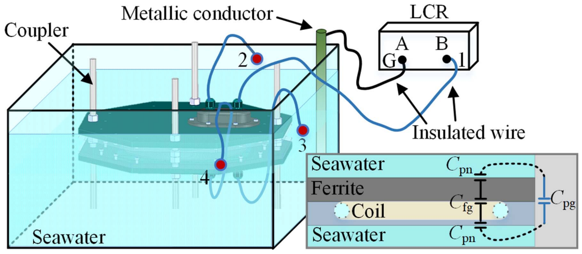


Fig. 5. C_{pg} measurement method.

The C_{pg1} can be obtained by (2), the C_{pg2}, C_{pg3}, and C_{pg4} can also be obtained in the same. The C_{fg} is the parasitic capacitance between the coil and ferrite, the C_{pn} is the parasitic capacitance between the shell and the ground

$$\frac{1}{C_{\mathrm{pg1}}} = \frac{1}{\sum_{\mathrm{m=1}}^{q} C_{\mathrm{fg1m}}} + \frac{1}{C_{\mathrm{pn}}}. \tag{2}$$

The simplified coil structure can be shown in Fig. 2(a), and the simplified equivalent circuit of the coupling coils is shown in Fig. 2(b), it can be seen that the C_{cg} and the C_{ig} have changed the circuit structure, so they are called the structural capacitance, which cannot be ignored when performing EMI analysis.

2) Analysis of Parasitic Capacitance in Electronic Device: The nonlinear characteristics of the MOSFET in the inverter cause the voltage spikes, as shown in Fig. 3(a) when the inverter turn ON and OFF rapidly in response to high-frequency pulse signals. During inverter operation, the drain of the MOSFET acts as a high-frequency fluctuating potential point, leading to a dynamic voltage differential between the drain and the heat sink. The voltage spikes will result in a high dv/dt, which exacerbates the effects of the parasitic capacitance C_{Dg} between the drain and heat sink of the MOSFET shown in Fig. 3(b). The C_{Dg} creates a capacitance-coupled propagation path that connects the inverter to the ground, making the current flow through the IPT system and ground via the parasitic capacitors C_{Dg} and C_{cg} [15].

In the secondary of the IPT system, there is the parasitic capacitance C_{sg} between the diode and the heatsink, it has the similar influence on the CM noise with the C_{Dg}. So, the further detailed explanations is not provided here.

Due to the discrepancy in line impedance at the output port of the inverter, the C_{Dg} at different positions will be charged and discharged to different degrees. This leads to the different voltages across the C_{Dg} of each bridge arm, the voltage difference between the bridge arms results in the CM voltage source. Thus, the inverter is considered the main source of CM noise in the system.

B. Measurement Methods for Parasitic Capacitance in Coupling Coils and Electronic Devices

From the analysis above, the C_{cg} in the coils acts as the structural capacitance and creates a CM noise propagation path between the primary and secondary sides and the parasitic capacitance of the components serves as a noise source for the propagation of CM noise. Therefore, the measurement methods of parasitic capacitance are important in the analysis of CM phenomenon.

1) Structural Capacitance C_{cg} Measurement: The measurement method for the C_{cg} is shown in Fig. 4, it shows the actual experimental measurement of the parasitic capacitance C_{cg} between the two coils. In the Fig. 4(a), the primary and secondary side coils are short-circuited, respectively, during the process of measurement, the capacitance value between the two coils of the device is obtained via the LCR impedance analyzer. In Fig. 4(b), the impedance curve is obtained from actual measurements, and the value is 157 pF in the frequency of 85 kHz.

2) Parasitic Capacitance C_{pg} Measurement: Seawater serves as a conductive medium, the coupling device placed within it is effectively surrounded by a conductive substance [16]. Based on this perspective, the measurement method for C_{pg} is shown in Fig. 5, the value of C_{pg} is obtained by the series connection of C_{pn} and C_{fg} shown in Fig. 2(a). To measure the capacitance C_{pg}, a metal rod is placed in seawater to serve as a medium for connecting to the seawater, and an insulated wire G is drawn from the metal rod to connect to external equipment.

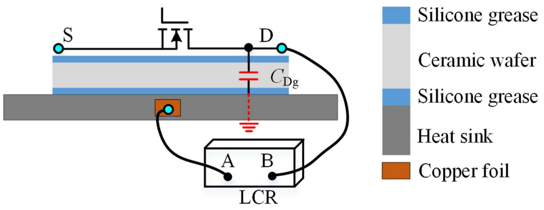


Fig. 6. C_{Dg} measurement method.

The insulating wire port 1 among ports 1 to 4 of the coupling device is connected with G to the LCR meter's test terminals, the measurement of the parasitic capacitance C_{pg1} between wire 1 and the seawater is 298 pF. Similarly, the values of C_{pg2} (293 pF), C_{pg3} (305 pF), and C_{pg4} (304 pF) can be measured. The parasitic capacitance C_{pg} associated with seawater for each port of the coupling device is not entirely identical, this difference is attributed to the inherent parameter inconsistencies that arise during the fabrication of the coupling coils.

3) Parasitic Capacitance C_{Dg} (C_{sg}) Measurement: The full-bridge inverter typically uses thermally conductive silicone grease to bond the MOSFET to the heat sink. As a result, a parasitic capacitance C_{Dg} is formed between the drain of the MOSFET and the heat sink, which resembles a parallel-plate capacitor. This capacitance serves as the primary pathway for the CM current of the MOSFET drain to flow into the ground, as shown in Fig. 6.

In the experiment, a copper foil is used to extract a wire from the heat sink to connect to port A of the LCR, while a test wire is connected from the drain of the MOSFET to port B of the LCR. By measuring the capacitance between ports A and B, the parasitic capacitance C_{Dg} between the inverter and ground can be measurement with 24.3 pF in 85 kHz. The parasitic capacitance C_{sg} has the same measurement method and has a 23.8 pF in 85 kHz.

4) Parasitic Capacitance C_{dg} Measurement: The C_{dg} constitutes the parasitic capacitance of the dc input conductors to ground during operation, it offers a propagation path connected to the ground for CM current noise on the dc side (input/output). The experiment indicates that the C_{dg} to ground is 1 nF, for both the primary and secondary sides in actual operating conditions.

The stability of parasitic capacitance is very important for studying the transmission of CM noise. However, the temperature and conductivity of the seawater environment change at different depths [17]. Liu et al. [4] demonstrated that the fluctuation range of seawater conductivity is from 3.14 to 5.9 S/m, which is much greater than the conductivity of 0.1 S/m through simulation analysis, so the capacitance will not change when the conductivity of the seawater changes. The effect of temperature on capacitance is shown in Fig. 7. It can be seen that when the temperature changes, the capacitance is constant. Therefore, the parasitic capacitance model in seawater IPT system is stable, and this conclusion is the basis for the subsequent analysis of common mode noise.

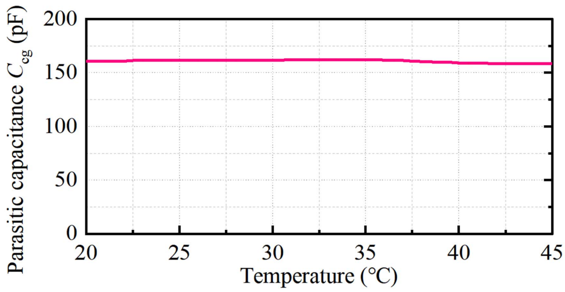


Fig. 7. Capacitance curve with temperature.

TABLE I
PARASITIC CAPACITANCE VALUE OF SYSTEM

Symbol	Measurement results	Symbol	Measurement results
C_{pg1}	298 pF	C_{pg3}	305 pF
C_{pg2}	293 pF	C_{pg4}	304 pF
C_{Dg1} C_{Dg2} C_{Dg3} C_{Dg4}	24.3 pF	C_{dg1} C_{dg2} C_{dg3} C_{dg4}	1nF
C_{cg}	157 pF	C_{sg1} C_{sg2}	23.8 pF

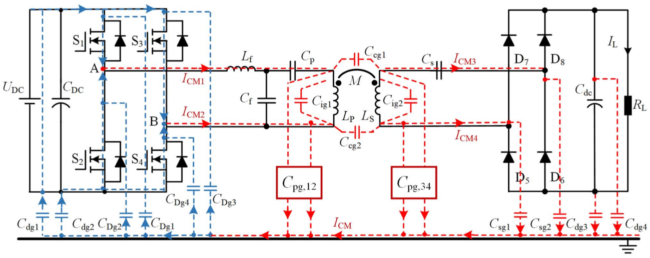


Fig. 8. Parasitic parameter equivalent model of *LCC*-S IPT circuit.

Through the aforementioned analysis and measurement, the values of the parasitic capacitances are shown in Table I. Due to the asymmetry of the inherent parameters of the coupling device caused by the manufacturing process, there are certain deviations present in the actual measurement of the capacitance values.

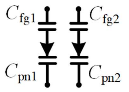
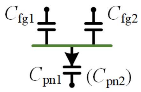
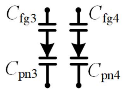
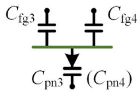
III. REFINED CIRCUIT MODEL ESTABLISHMENT FOR *LCC*-S TOPOLOGY AND CM CURRENT ANALYSIS IN DIFFERENT MEDIA

The establishment of a refined circuit model is essential for guiding the analysis of CM current. The refined model of the IPT system will be developed by incorporating the parasitic capacitance in the coils and electronic devices into the circuit of the IPT system, then the differences in CM current across various media will be evaluated.

A. Establishment of a Refined Compensation Topology Based on Traditional LCC-*S Circuit*

The *LCC*-S topology, which has constant voltage output characteristics and widely used in IPT systems is selected as the CM noise research object. The overall circuit of the *LCC*-S compensated IPT system is shown in Fig. 8 with the parasitic capacitances. In the circuit, an inverter is situated on the primary side, and a rectifier bridge is located on the secondary side. The primary and secondary sides are interconnected through a loosely coupled transformer, which consists of coils arranged

TABLE II
COMPOSITION OF C_{pg} IN DIFFERENT MEDIA

Symbol	Water	Air
$C_{\mathrm{pg,12}}$		
$C_{\mathrm{pg,34}}$		

— Coil seal case

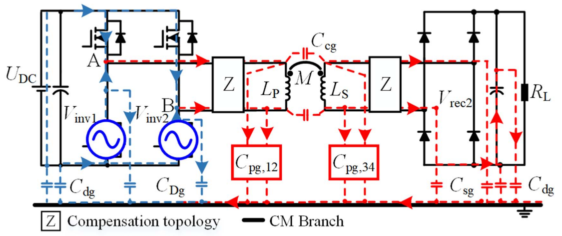


Fig. 9. Propagation path of common current in IPT system.

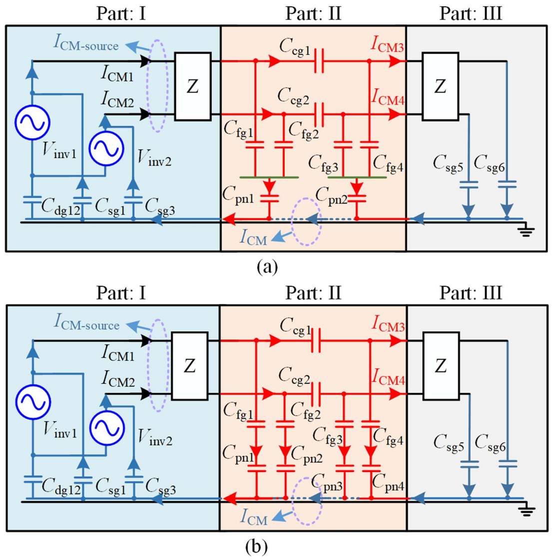


Fig. 10. Simplified propagation path of CM noise. (a) Air. (b) Freshwater/Seawater.

face to face. The capacitors within the dashed line paths represent the parasitic capacitances analyzed above. As previously mentioned, the C_{Dg} serves as a main source of CM noise, which exists in the inverter. The C_{cg} is the structural capacitance that causes the CM current to flow between the primary and secondary sides. The C_{ig} is the interturn capacitance of each winding mainly influencing the differential mode signals and can be disregarded in CM noise analysis. The C_{dg} is the parasitic capacitance to the ground on the dc bus side. C_{pg} is the parasitic capacitance between the winding and the ground through the sealed case, there are some differences between the air and water shown in Table II. The reason for the differences lies in that in freshwater or seawater, the potential switching point of the coil forms capacitance directly with the ground through the water. In contrast, in air, the potential switching point of the coil forms capacitance with the ground through the sealed enclosure of coil.

The parasitic capacitances mentioned above allow the CM currents to flow from the inverter into the ground and return to the CM source, which create the propagation path for the CM noise.

B. CM Current Analysis of the Refined Circuit Model in Different Media

The propagation path of CM current in IPT is shown in Fig. 9 with a dotted line. The arrows show the direction of the current. The Z block is the compensation topology of the IPT system. As mentioned above, the C_{dg} constructed a coupling path between the MOSFET and the ground. The current loop for the CM current through the primary and secondary side is also created.

In Fig. 9, the $V_{\mathrm{inv1}}/V_{\mathrm{inv2}}$ is the equal CM interference source, which is mainly caused by the MOSFETS S_2/S_4 connected with the power line GND in the full-bridge inverter low legs [18]. The drain of S_2/S_4 is directly connected to the GND of power. During the operation of the inverter, there are significant voltage fluctuations at the low-potential side MOSFET, causing the C_{Dg} to undergo intense unbalanced charging and discharging processes, so the S_2/S_4 generates the main CM interference source in the underwater IPT system. In the previous study, the CM noise is only considered in the primary side for the structure capacitance C_{cg}, which is a little small in the air [19]. However, just as Fig. 4(b) shown, the structure capacitance C_{cg} is about 157 pF in seawater, this capacitance value can be used to transfer signal of data or power in the previous paper [20]. Thus, the C_{cg} should be considered when analyzing the CM noise. Above all, the propagation path of CM current can be simplified as in Fig. 10. In Fig. 10, the CM current flows from the primary side to the second side through the C_{cg} and return to the primary side through the CM branch and forms a CM current loop. The depiction of the propagation path of the CM current aids in the analysis of the transmission characteristics of CM noise. According to the propagation path described in Fig. 10, a comparison of the magnitudes of the CM current in different media will be conducted based on the *LCC*-S topology.

The CM current $I_{\mathrm{CM\text{-}source}}$ flowing through the C_{cg} is measured separately in the air, fresh-water, and sea-water. Due to the I_{CM1} and I_{CM2} are two branches of the CM branch, they are measured together as $I_{\mathrm{CM\text{-}source}}$, which can be identified as the joint current flowing through the magnetic coupler, the $I_{\mathrm{CM\text{-}source}}$ can be obtain in (3), which is shown in the Fig. 10

$$I_{\mathrm{CM-source}} = I_{\mathrm{CM1}} + I_{\mathrm{CM2}}. \tag{3}$$

In Fig. 11, the magnitude of CM currents $I_{\mathrm{CM\text{-}source}}$ shows a difference in different electrical conductivity environments. As the conductivity of the medium in which the IPT system operates increases, the $I_{\mathrm{CM\text{-}source}}$ also increases, which is induced by the inverter and flows through the primary and secondary sides of the coupling coils and returning to the inverter side via the common

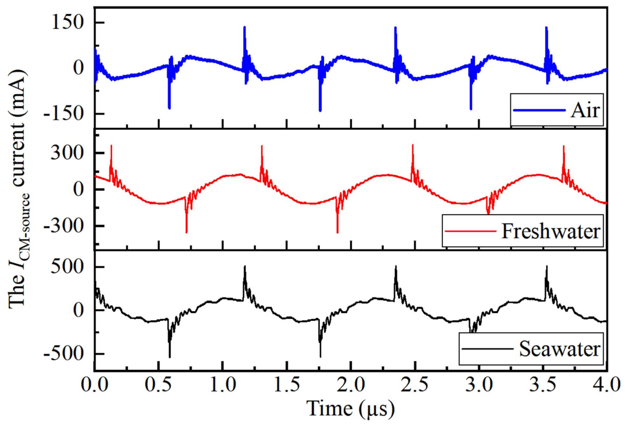


Fig. 11. CM current $I_{\text{CM-source}}$ in different media.

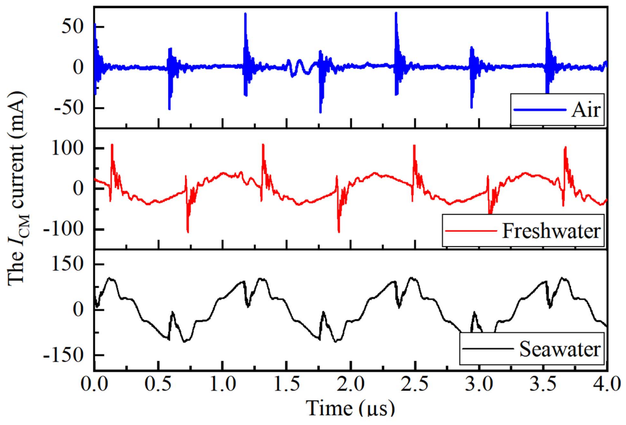


Fig. 12. CM current I_{CM} in different media.

ground. According to the (4), the cause of the increased current is found, the C_{cg} is larger when the conductivity is larger [21]. So, the Z_{Ccg} is smaller and the CM current is larger

$$C_{\text{cg}} = \varepsilon_0 \varepsilon_1 \frac{S}{h_{\text{ps}}}. \tag{4}$$

The ε_0 is the absolute dielectric constant, the ε_1 is the relative dielectric constant, the S is the surface area of the two plates facing each other, and the h_{ps} is the distance between two coils.

The analysis above indicates that when the CM current $I_{\text{CM-source}}$ flowing through the circuit branch, there will be a CM current I_{CM} reflux at the common ground end of the components of the IPT system. In Fig. 12, I_{CM} is measured in air, freshwater and seawater, in which the I_{CM} is small in the air, and large in the sea-water. It has shown that the greater the dielectric constant, the greater the I_{CM}.

In Fig. 12, there is the surge current in the waveform of the I_{CM}, which is caused by the inverter during operation. The surge current is transmitted through capacitance C_{Dg} and conducted into the circuitry by the inverter. In air, the inverters produce minimal noise, the reason is that seawater has low conductivity. On the contrary the inverter generates significantly highest levels noise, the reason is that seawater has the highest conductivity.

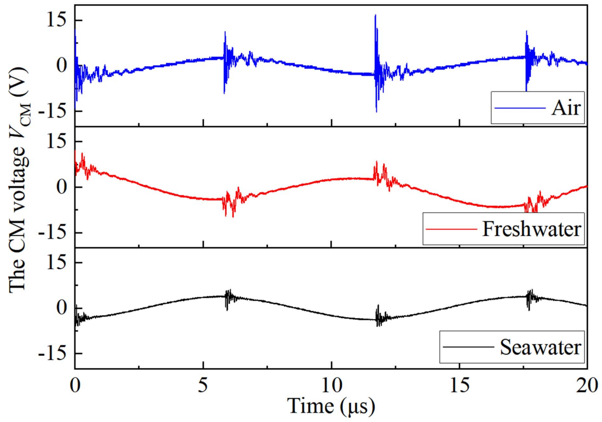
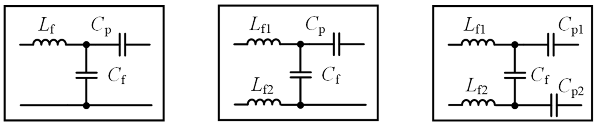


Fig. 13. CM voltage V_{CM} in different media.



Circuit I: LCC-S Circuit II: LLCC-S Circuit III: LLCCC-S

Fig. 14. Compensation circuit Z.

Through the analysis of the waveforms presented in the Fig. 12, it is evident that the differences in conductivity among air, fresh-water, and sea-water lead to significant difference in the CM impedance of the transmission paths. As a result, the attenuation of CM noise in the high electrical conductivity system decreases, leading to the disparity in the intensity of both CM noise and inverter switching noise along the CM path. These differences result in varying amplitudes of CM current across different media. Therefore, the suppression of CM noise in high conductivity seawater IPT system is very important. Through experimental testing, this article also presents the waveform of the voltage across I_{CM}, as shown in Fig. 13. it can be observed that the voltages across the common-mode current in the three different media are similar.

IV. SUPPRESSION METHOD OF COMMON MODE NOISE

The CM current flowing through the circuit topology will cause the CM noise, which can lead to electromagnetic interference problem, impacting the stability of the system. To mitigate CM crosstalk issues within the system, the balanced impedance topologies will be analyzed and examined in suppressing CM noise with seawater IPT system.

This study analyzes the asymmetric compensation circuit *LCC*-S, the semisymmetric compensation circuit *LLCC*-S, and the symmetric compensation circuit *LLCCC*-S, investigating the effect of system symmetry on the CM noise suppression. The topologies of the compensation circuit are shown in Fig. 14.

The parameter for the corresponding compensation network is given by (5), where ω_1 denotes the angular frequency corresponding to the system operating frequency of 85 kHz.

By referencing the CM circuit mentioned in Fig. 10 and combining it with the circuit topology presented in Fig. 14,

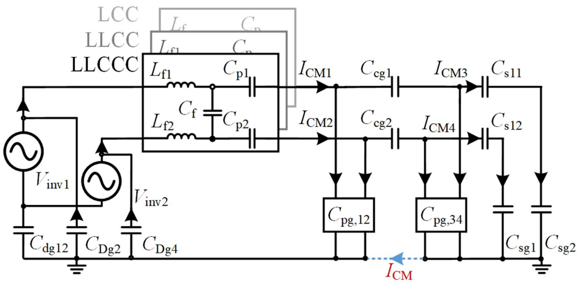


Fig. 15. Common-mode circuits with different topologies.

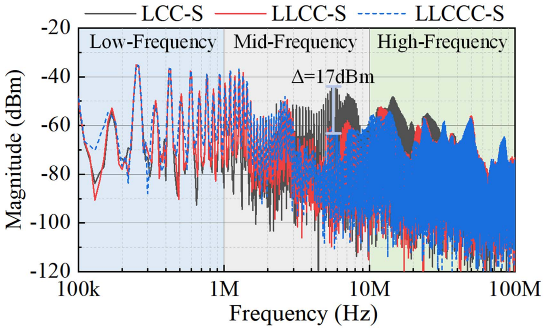


Fig. 16. CM current FFT analysis for three topologies.

the pathways of the CM currents under different compensation topologies can be obtained, as shown in Fig. 15

$$\begin{cases} \omega_1 L_{\mathrm{f}} = \frac{1}{\omega_1 C_{\mathrm{f}}} = \omega_1 L_{\mathrm{P}} - \frac{1}{\omega C_{\mathrm{P}}} \quad \text{(Circuit I)} \\ \omega_1 (L_{\mathrm{f1}} + L_{\mathrm{f2}}) = \frac{1}{\omega_1 C_{\mathrm{f}}} = \omega_1 L_{\mathrm{P}} - \frac{1}{\omega_1 C_{\mathrm{P}}} \quad \text{(Circuit II)} \\ \omega_1 (L_{\mathrm{f1}} + L_{\mathrm{f2}}) = \frac{1}{\omega_1 C_{\mathrm{f}}} = \omega_1 L_{\mathrm{P}} \\ - \left(\frac{1}{\omega_1 C_{\mathrm{P1}}} + \frac{1}{\omega_1 C_{\mathrm{P2}}} \right) \quad \text{(Circuit III)}. \end{cases} \tag{5}$$

In the secondary, capacitor C_{s} is utilized to compensate the receiving coil. To ensure that the impedance conditions of the circuit remain consistent during the potential transition across the receiving coil, this article employs split capacitors C_{s11} and C_{s22} on the secondary side. This configuration allows for a uniform impedance distribution between the receiving coil and the load, satisfying the balanced impedance condition. The calculation method for C_{s11} and C_{s22} is shown in

$$\omega_1 L_S = \frac{1}{\omega_1 C_{\mathrm{S}}} = \frac{2}{\omega_1 C_{\mathrm{S11}}} = \frac{2}{\omega_1 C_{\mathrm{S22}}}. \tag{6}$$

The CM current FFT analysis are shown in Fig. 16, which are the results for the three topologies mentioned in Fig. 15. They present the frequency response of three different configurations—*LCC*-S (solid black line), *LLCC*-S (solid red line), and *LLCCC*-S (dashed blue line). To ensure the reliability of the analysis, the CM currents are measured on a real experimental platform with the same input voltage of 50 V and load of 10 Ω. The frequency spectrum is partitioned into three regions: 1) low-frequency (100 kHz to 1 MHz), 2) mid-frequency (1 MHz to 10 MHz), and 3) high-frequency (10 MHz to 100 MHz). In the low-frequency range, the CM currents for the three compensation network topologies are essentially consistent. In the mid-frequency and high-frequency ranges, the traditional *LCC*-S topology, which exhibits a noise of 17 dB higher compared to the other two topologies and exhibits the weakest suppression of CM noise among the three compensation topologies. In contrast, the *LLCCC*-S network shows the better pronounced effect in suppressing CM noise in the mid to high frequency ranges among the three topologies, However, compared to the *LLCC*-S and *LLCCC*-S topologies, the frequency spectra of the two are quite similar, indicating that the symmetry of the compensation capacitors C_{p} has no impact on common-mode noise. Just as the Fig. 16 shown, the symmetric inductance topology has obvious performance in suppressing CM noise. this article will employ the *LLCCC*-S symmetric topology to mitigate CM noise, which will be analyzed in the subsequence.

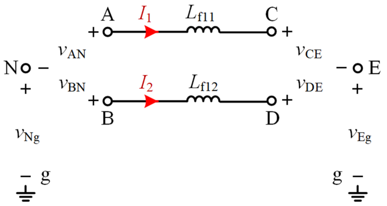


Fig. 17. Equivalent block diagrams of CM and DM for balanced inductors.

The numerical distribution of symmetric impedance has an effect on its CM noise suppression ability, the parameters for *LLCCC*-S are provided in (7), k is the proportion coefficient to describe the split inductance value, the analysis of the value of k and the inhibition ability of CM current is as follows:

$$\begin{cases} L_{\mathrm{f1}} = k L_{\mathrm{f}} \\ L_{\mathrm{f2}} = (1-k) L_{\mathrm{f}}, k \in (0,1) \\ C_{\mathrm{p1}} = C_{\mathrm{p2}} = 2C_{\mathrm{p}}. \end{cases} \tag{7}$$

The analysis is conducted on the relationship between the values of L_{f11} and L_{f12} and the noise sources. The inductor L_{f} is transformed into a split inductor, as shown in Fig. 17. In this configuration, nodes A, B, C, and D represent the four terminals of the split inductor. The node N (E) is a reference node in the circuit with respect to ground. v_{AN} (v_{CE}) represents the voltage difference between node A (C) and the reference node N (E). The v_{NG} is the voltage between the node N and the ground. The v_{Lf11} is the voltage of the split inductance L_{f11}.

Applying KVL to the branches AC and BD of the split inductor, the circuit equations can be obtained, as shown in

$$\begin{cases} v_{\mathrm{AN}} + v_{\mathrm{Ng}} = v_{\mathrm{Lf11}} + v_{\mathrm{CE}} + v_{\mathrm{Eg}} (\mathrm{I}) \\ v_{\mathrm{BN}} + v_{\mathrm{Ng}} = v_{\mathrm{Lf12}} + v_{\mathrm{DE}} + v_{\mathrm{Eg}} (\mathrm{II}) \end{cases}. \tag{8}$$

Applying the voltage definition of CM and DM (9), the system of equations shown in (10) can be derived through mathematical manipulation [22]

$$\begin{cases} v^{\mathrm{cm}}{}_{\mathrm{AB}} = \frac{1}{2} (v_{\mathrm{AN}} + v_{\mathrm{BN}}) (\mathrm{I}) \\ v^{\mathrm{dm}}{}_{\mathrm{AB}} = v_{\mathrm{AN}} - v_{\mathrm{BN}} (\mathrm{II}) \end{cases} \tag{9}$$

$$\begin{cases} v^{\mathrm{dm}}{}_{\mathrm{AB}} + 0 = v^{\mathrm{dm}}{}_{\mathrm{Lf}} + v^{\mathrm{dm}}{}_{\mathrm{CD}} + 0 (\mathrm{I}) \\ v^{\mathrm{cm}}{}_{\mathrm{AB}} + v_{\mathrm{Ng}} = v^{\mathrm{cm}}{}_{\mathrm{Lf}} + v^{\mathrm{cm}}{}_{\mathrm{CD}} + v_{\mathrm{Eg}} (\mathrm{II}). \end{cases} \tag{10}$$

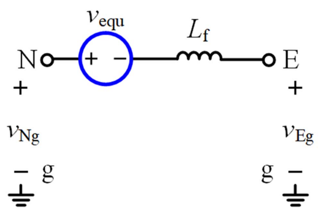


Fig. 18. CM circuit of split L_{f}.

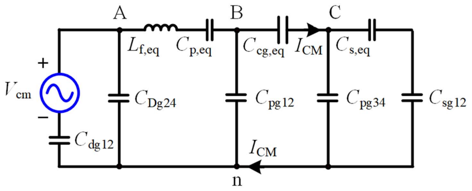


Fig. 19. Simplified circuit of CM current branch.

The structural equation of L_{f11} and L_{f22} split inductors is

$$\begin{pmatrix} v_{\mathrm{Lf11}} \\ v_{\mathrm{Lf12}} \end{pmatrix} = L_{\mathrm{f}} \begin{pmatrix} k & 0 \\ 0 & 1-k \end{pmatrix} \frac{d}{dt} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix}. \tag{11}$$

The definition of CM leads to the formula shown in

$$\begin{cases} i^{\mathrm{cm}}{}_{\mathrm{Lf}} = \frac{1}{2}(i_1 + i_2) \\ i^{\mathrm{dm}}{}_{\mathrm{Lf}} = i_1 - i_2. \end{cases} \tag{12}$$

Thus, (11) can be transformed into the form shown in (13), where the expression for v_{equ} is given in (14)

$$v^{\mathrm{cm}}{}_{\mathrm{Lf}} = v_{\mathrm{equ}} + L_{\mathrm{f}} \frac{di_{\mathrm{cm}}}{dt} \tag{13}$$

$$v_{\mathrm{equ}} = \left| \left(k - \frac{1}{2} \right) L_{\mathrm{f}} \frac{di_{\mathrm{dm}}}{dt} \right|. \tag{14}$$

The CM circuit of the L_{f} can be shown in Fig. 18.

It can be seen that in Fig. 15, the CM circuit depicted on the secondary side contains the same circuit components in CM current branch 1 (consisting of L_{f11}, C_{p11}, C_{cg1}, and C_{s11}) as in CM branch 2 (consisting of L_{f12}, C_{p12}, C_{cg2}, and C_{s12}). Therefore, by equivalently paralleling CM branch 1 and CM branch 2, the simplified CM current branch can be obtained, which is shown in Fig. 19.

The $L_{\mathrm{f,eq}}$, $C_{\mathrm{p,eq}}$, $C_{\mathrm{s,eq}}$ is the equivalent parameter of L_{f11} and L_{f12}, C_{p11} and C_{p12}, C_{s11} and C_{s12} in parallel. The parameters are given in

$$\begin{cases} C_{\mathrm{p,eq}} = C_{\mathrm{p11}} + C_{\mathrm{p12}} \\ C_{\mathrm{s,eq}} = C_{\mathrm{s11}} + C_{\mathrm{s12}} \\ C_{\mathrm{Dg24}} = C_{\mathrm{sg1}} + C_{\mathrm{sg3}} \\ C_{\mathrm{sg12}} = C_{\mathrm{sg1}} + C_{\mathrm{sg2}} \\ C_{\mathrm{pg12}} = C_{\mathrm{pg1}} + C_{\mathrm{pg2}} \\ C_{\mathrm{pg34}} = C_{\mathrm{pg3}} + C_{\mathrm{pg4}} \\ L_{\mathrm{f,eq}} = k\,(1-k)\,L_{\mathrm{f}}, k \in (0,1)\,. \end{cases} \tag{15}$$

The V_{cm} is the equivalent CM voltage source of V_{inv1} and V_{inv2}. I_{CM} is the sum of I_{CM1} and I_{CM2}

$$\begin{cases} V_{\mathrm{cm}} = \frac{1}{2}(V_{\mathrm{inv1}} + V_{\mathrm{inv2}}) \\ I_{\mathrm{CM}} = I_{\mathrm{CM1}} + I_{\mathrm{CM2}}. \end{cases} \tag{16}$$

By applying Kirchhoff's laws to the circuit shown in Fig. 19, the equation presented in (17) can be obtained

$$\begin{bmatrix} G_{11} & G_{12} & 0 \\ G_{21} & G_{22} & G_{23} \\ 0 & G_{32} & G_{33} \end{bmatrix} \begin{bmatrix} U_{\mathrm{AN}} \\ U_{\mathrm{BN}} \\ U_{\mathrm{CN}} \end{bmatrix} = \begin{bmatrix} G_{11} V_{\mathrm{CM}} \\ 0 \\ 0 \end{bmatrix}. \tag{17}$$

The detailed values of the parameters shown in (17) are presented in

$$\begin{cases} G_{11} = j\omega \left(C_{\mathrm{dg12}} + C_{\mathrm{sg13}} + \frac{L_{\mathrm{f,eq}}}{1-\omega^2 L_{\mathrm{f,eq}} C_{\mathrm{p,eq}}} \right) \\ G_{12} = \frac{j\omega L_{\mathrm{f,eq}}}{\omega^2 L_{\mathrm{f,eq}} C_{\mathrm{p,eq}} - 1} \\ G_{21} = \frac{j\omega L_{\mathrm{f,eq}}}{\omega^2 L_{\mathrm{f,eq}} C_{\mathrm{p,eq}} - 1} \\ G_{22} = j\omega \left(\frac{L_{\mathrm{f,eq}}}{1-\omega^2 L_{\mathrm{f,eq}} C_{\mathrm{p,eq}}} + C_{\mathrm{pg12}} + C_{\mathrm{cg,eq}} \right) \\ G_{23} = G_{32} = -j\omega C_{\mathrm{cg,eq}} \\ G_{33} = j\omega \left(\frac{C_{\mathrm{s,eq}} C_{\mathrm{sg56}} + (C_{\mathrm{s,eq}} + C_{\mathrm{sg56}}) C_{\mathrm{pg34}}}{C_{\mathrm{s,eq}} + C_{\mathrm{sg56}}} + C_{\mathrm{cg,eq}} \right). \end{cases} \tag{18}$$

Similarly, since capacitance $C_{\mathrm{s,eq}}$ is an order of magnitude higher than capacitance $C_{\mathrm{sg,56}}$, so the total admittance in the calculation of the series combination can be considered as the admittance of capacitance $C_{\mathrm{sg,56}}$. Consequently, G_{11}, G_{22}, and G_{33} are simplified to

$$\begin{cases} G_{11} = G_{22} = \frac{j\omega L_{\mathrm{f,eq}}}{1-\omega^2 L_{\mathrm{f,eq}} C_{\mathrm{p,eq}}} = \frac{j\omega k(1-k) L_f}{1-\omega^2 k(1-k) L_f C_{\mathrm{p,eq}}} \\ G_{33} = j\omega \left(C_{\mathrm{sg56}} + C_{\mathrm{pg34}} + C_{\mathrm{cg,eq}} \right). \end{cases} \tag{19}$$

Therefore, the expression for the CM current I_{CM} can be obtained as follows:

$$I_{\mathrm{CM}} = \frac{-G_{23}(G_{23} + G_{33}) G_{11} G_{21} V_{CM}}{G^2{}_{12} G_{33} - G_{11} G_{22} G_{33} + G_{11} G^2{}_{23}}. \tag{20}$$

By combining (15), (18), and (19), substituting the relevant parameters into (20), the formula for I_{CM} is obtained, as shown in (21). By factoring out the coefficient in front of the independent variable k, it can be concluded that I_{CM} is composed of the product of A and $f(k)$, which is shown in (22)

$$I_{\mathrm{CM}} = j\omega \frac{(C_{\mathrm{sg56}} + C_{\mathrm{pg34}})}{C_{\mathrm{cg,eq}}} \times \frac{k\,(1-k)\,L_f}{k\,(1-k)\,\omega^2 L_f C_{\mathrm{p,eq}} - 1} \tag{21}$$

$$\begin{cases} A = j\omega \frac{(C_{\mathrm{sg56}} + C_{\mathrm{pg34}})}{C_{\mathrm{cg,eq}}} \\ f(k) = \frac{k(1-k) L_f}{k(1-k)\omega^2 L_f C_{\mathrm{p,eq}} - 1} \end{cases} \tag{22}$$

$$I_{\mathrm{CM}} = A * f(k). \tag{23}$$

In (22), it can be seen when the capacitances are constant, the A is constant, so the magnitude of I_{CM} only depends on the value of parameter k. Therefore, the $f(k)$ is used to denote the polynomial related to k in (22), and the Fig. 20 shows the curve of $f(k)$, the red line segment represents the reasonable range of values for k in this article in (0,1). The curve shows that there is a minimum value of the $f(k)$ when k is set to 0.5. In (23), it can observe that the minimum point of I_{CM} within the range

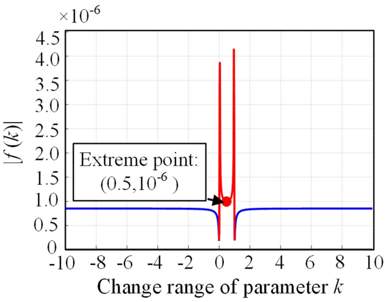


Fig. 20. Curve of $|f(k)|$ as a function of k.

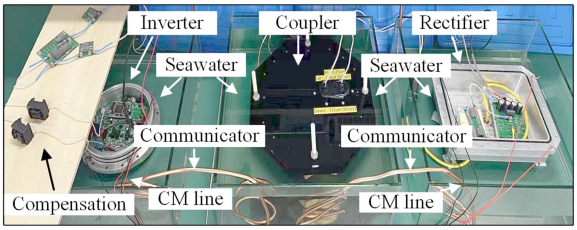
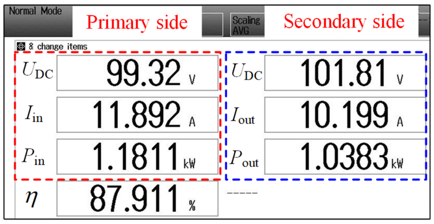


Fig. 21. Experimental platform of the mentioned system.



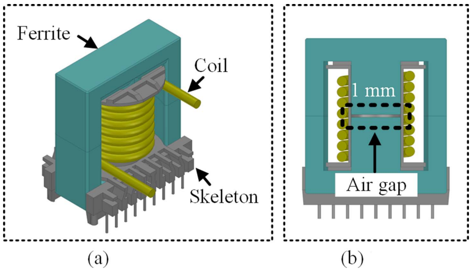
Primary side		Secondary side	
U_{DC}	99.32 V	U_{DC}	101.81 V
I_{in}	11.892 A	I_{out}	10.199 A
P_{in}	1.1811 kW	P_{out}	1.0383 kW
η	87.911 %	-----	

Fig. 22. Performance of the proposed wireless power transfer platform.

of (0,1) corresponds to the minimum point of the function $f(k)$. Therefore, it shows the CM current will be a minimum value when the k is 0.5 within the balanced inductor employed, which is an effective method for suppressing CM noise in the seawater IPT system.

TABLE III
PARAMETER OF SYSTEM

Symbol	Value	Symbol	Value	Symbol	Value
L_{p}	131 μH	L_{s}	118 μH	V_{DC}	100 V
L_{f}	29.2 μH	C_{f}	125.6 nF	f	85 kHz
C_{S1} /C_{S2}	60 nF	R_{L}	10 Ω	C_{P}	34.2 nF
L_{f1} /L_{f2}	14.6 μH	C_{P1} /C_{P2}	68.4 nF	C_{S}	30 nF



(a) (b)

Fig. 23. Inductor fabrication scheme. (a) Overall view. (b) Section view.

TABLE IV
CM CURRENT I_{CM} UNDER DIFFERENT SPLIT COEFFICIENTS

Split Factor k	The Value of $I_{\mathrm{CM\text{-}Amplitude}}$	Attenuation
1	270 mA	—
0.8	186 mA	68.89%
0.7	167 mA	61.85%
0.6	152 mA	56.30%
0.5	125 mA	46.30%

V. EXPERIMENTAL VERIFICATION

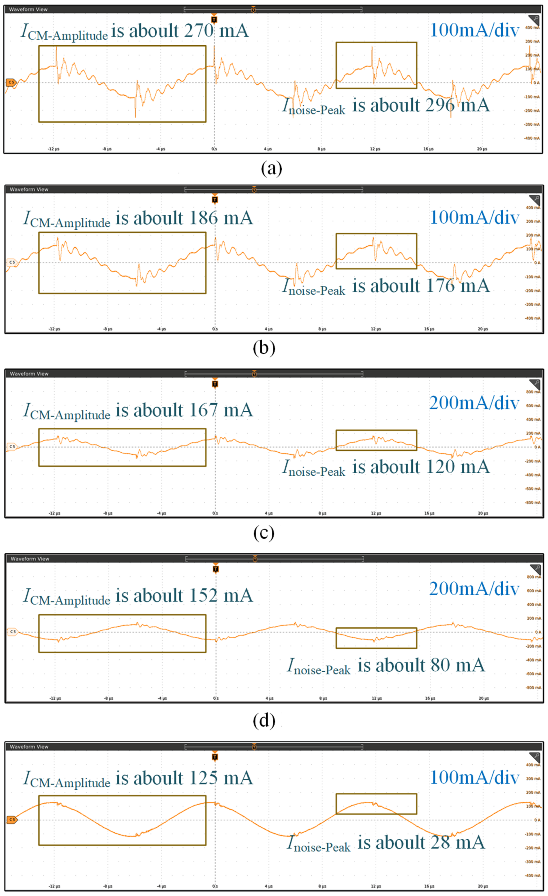
The experimental platform of balanced impedance *LLCCC*-S topology is established to validate the effectiveness on CM noise suppression in seawater IPT systems, which is shown in Fig. 21. There are three tanks filled with seawater to simulate the actual working environment, the water tanks are connected by the metal conductors (used for CM current testing), the metal conductors allow the inverter, coils, and rectifier to interconnect which simulate the real AUV operation environment. The frequency of the WPT system is set to 85 kHz, the input voltage is 100 V, the load is 10 Ω. The proposed system has the ability of achieving wireless power transmission with 1 kW in seawater environment. Furthermore, the transmission efficiency of the system can reach up to 87.9% in Fig. 22. The previously discussed values of parasitic capacitance and the spectral analysis of CM current are obtained through actual measurements conducted on this experimental platform. In addition, this article also establishes an *LLCC*-S experimental platform with inductors of different splitting coefficients to conduct a comparative analysis of the proposed balanced impedance network. The parameter of the *LCC*-S and *LLCCC*-S are shown in Table III.

The inductor with air gap in the core is convenient to adjust the inductance value and demonstrating good disturbance resistance in practical engineering applications, so the inductance is made using the EE-model PC95 core with a 1 mm air gap shown in Fig. 23.

To verify the suppression effects of different splitting coefficients k on CM noise, the experimental measurements are conducted for split coefficients k of 1, 0.8, 0.7, 0.6, and 0.5, to validate the correctness of the theoretical analysis by measuring the magnitude of the CM current I_{CM} in Fig. 24. The result is shown in Table IV, from which it can been seen that when k is 0.5, the CM noise I_{CM} is reduced to 46.3% of its original value, and the degree of attenuation is the maximum among the different values of k.

To investigate the reasons balanced inductors can reduce common-mode noise. The voltage between the drain of the high-frequency potential switching MOSFETS S_2/S_4 and seawater is tested, as shown in Fig. 25 .

The $U_{\mathrm{Dg\text{-}S2}}$ ($U_{\mathrm{Dg\text{-}S4}}$) represents the voltages between the drains of S_2 (S_4) and seawater. The sum of $U_{\mathrm{Dg\text{-}S2}}$ and $U_{\mathrm{Dg\text{-}S4}}$ shows the magnitude of the CM voltage on the output of the inverter. From the Fig. 25, it can be observed that in the conventional asymmetrical *LCC*-S compensation topology, the



(a)

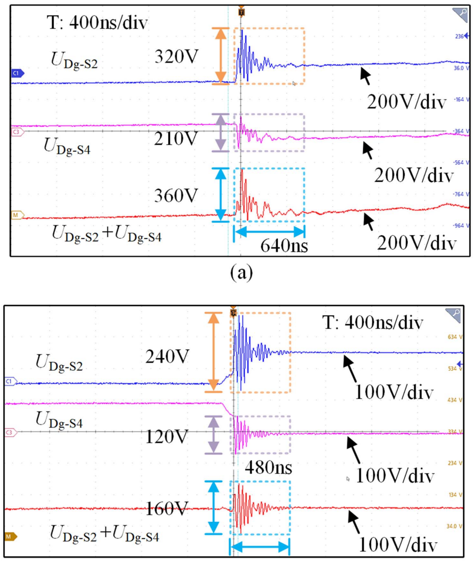
(b)

(c)

(d)

(e)

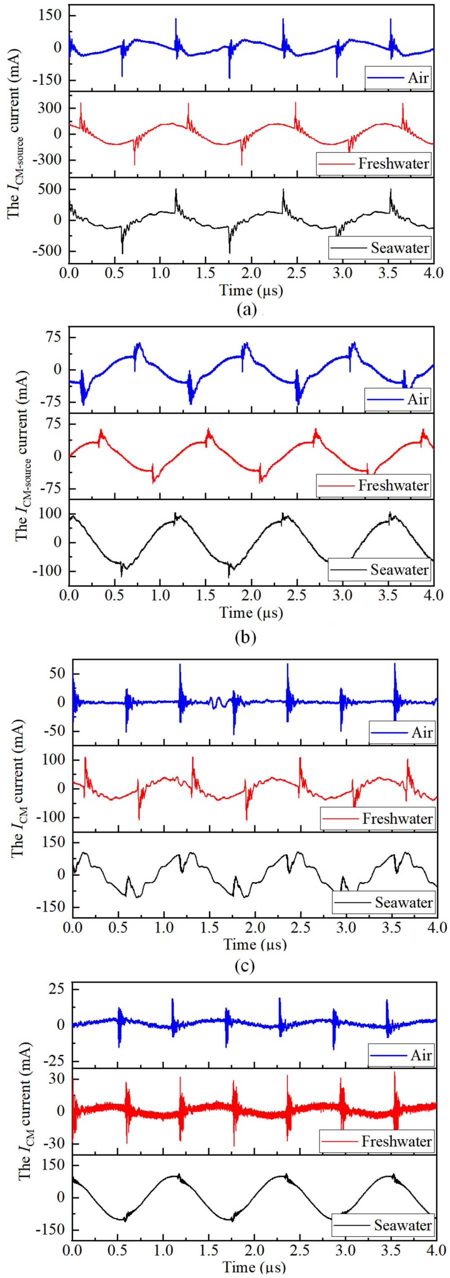
Fig. 24. CM current I_{CM} under different split coefficients *k*. (a) Inductance coefficient $k = 1$. (b) Inductance coefficient $k = 0.8$. (c) Inductance coefficient $k = 0.7$. (d) Inductance coefficient $k = 0.6$. (e) Inductance coefficient $k = 0.5$.



(a)

(b)

Fig. 25. Voltage of $U_{\text{Dg-S2}}$ and $U_{\text{Dg-S4}}$ in different topologies. (a) *LCC*-S topology. (b) *LLCCC*-S topology ($k = 0.5$).



(a)

(b)

(c)

(d)

Fig. 26. I_{CM} of IPT system in three media with asymmetric impedance and symmetric impedance. (a) Asymmetric impedance $I_{\text{CM-source}}$. (b) Symmetric impedance $I_{\text{CM-source}}$. (c) Asymmetric impedance I_{CM}. (d) Symmetric impedance I_{CM}.

voltage potential generated between $U_{\text{Dg-S2}}$ and $U_{\text{Dg-S4}}$ cannot be canceled out and lead to a situation where the sum of the voltages $U_{\text{Dg-S2}}$ and $U_{\text{Dg-S4}}$ is larger than $U_{\text{Dg-S2}}$ or $U_{\text{Dg-S4}}$ that is caused by the asymmetrical impedance connected to the inverter output terminals results in differing line impedances.

Under the same operating conditions, the symmetrical *LLCCC*-S topology mentioned in this study achieves a balanced output line impedance at the inverter output terminals. As a result, the sum of the volage $U_{\text{Dg-S2}}$ and $U_{\text{Dg-S4}}$ is significantly

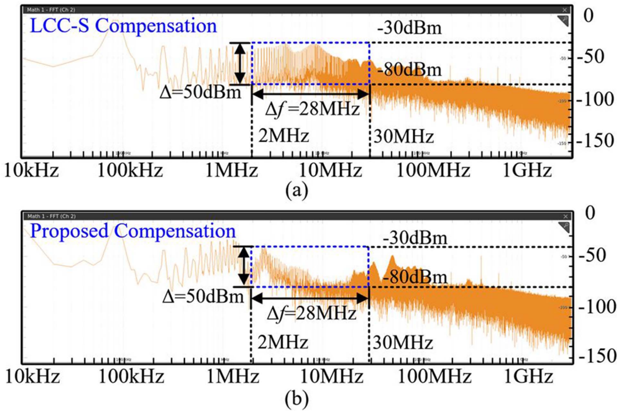


Fig. 27. FFT analysis diagram of inverter side output CM current $I_{\text{CM-source}}$. (a) LCC-S compensation. (b) Proposed compensation.

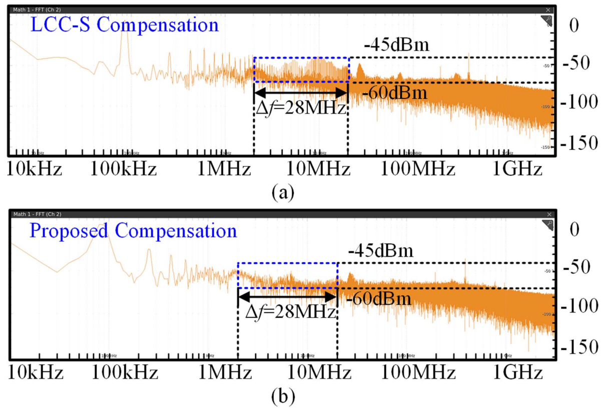


Fig. 28. FFT analysis diagram of CM current in CM line (I_{CM}). (a) LCC-S compensation. (b) Proposed compensation.

reduced and mitigate the CM voltage caused by the matched symmetrical impedance, which causes the voltages of the inverter output ports to cancel each other out at the same time. Consequently, the sum of $U_{\text{Dg-S2}}$ and $U_{\text{Dg-S4}}$ is effectively diminished in Fig. 25(b).

Additionally, compared to the use of line asymmetric impedance on the inverter output side, the proposed *LLCCC*-S topology exhibits a 0.75 times oscillation time in the output waveform than the use of the unbalanced line impedance in *LCC*-S topology, it proves that the symmetrical *LLCCC*-S impedance reduces EMI during power transfer, reduces the switching losses in the MOSFET and enhances the stability of the system.

To verify the consistency of the proposed parasitic capacitance circuit model in air, freshwater, and seawater, this article also conducts the analysis of the CM current $I_{\text{CM-source}}$ on the inverter output side in Fig. 26(a) and (b), as well as the CM current I_{CM} in the CM branch in Fig. 26(c) and (d). From the waveforms in the Fig. 26, it can be observed that the suppression effect of the symmetric topology on common-mode noise is consistent in air, freshwater, and seawater mediums, indicating that the solution is consistent across different media.

In order to analyze the differences in CM noise suppression from a frequency domain perspective, the FFT analysis is conducted using seawater medium as an example. In Fig. 27, the CM current on the inverter output side exhibits significant EMI components in the frequency range of 2 to 30 MHz for the *LCC*-S compensation topology, compared to the proposed compensation topology. This indicates that the proposed topology has effectively suppressed the CM current at the inverter output within the EMI testing frequency range.

By comparing with Fig. 27, it can be observed that as the CM current $I_{\text{CM-source}}$ decreases, the CM branch current I_{CM} also diminishes correspondingly. The combination of Figs. 27 and 28 illustrates that the proposed symmetrical *LLCCC*-S compensation topology exhibits a superior performance in suppressing CM current issues that causing by impedance imbalance in the system compared to *LCC*-S circuit.

VI. CONCLUSION

In this article, the CM noise caused by parasitic capacitance in seawater IPT system is analyzed, and a suppression method is proposed. The analysis of the distribution of parasitic capacitance between components and coils in a seawater high conductivity environment is conducted, and a parasitic parameter fined model for the conventional *LCC*-S topology is established. Subsequently, the measurement methods are taken to test the parasitic capacitance in the seawater IPT system, and through the theoretical analysis, the relationship between the distribution of output circuit impedance from the inverter and the magnitude of CM voltage is quantified based on the parasitic parameter refined model. The CM current suppression topology based on traditional balanced inductance topology *LLCCC*-S is proposed. An IPT system in a seawater environment is constructed to validate the differences between the *LCC*-S compensation and the proposed compensation topology. The designed scheme is ultimately verified to be effective at a system efficiency of 87.91% and an output power of 1 kW. Compared to the conventional *LCC*-S topology, the proposed compensation network has an excellent CM suppression capability within the EMI detection frequency range from 2 to 30 MHz.

Discussion: The authors believe the research content of this article will give a good inspiration to the scholars in the field of seawater IPT, so that the underwater EMI problem has been taken into account during the scheme design. In addition, the author also found the following three problems need to be further studied.

1) Improvement of the measurement method. This article provides a testing scheme for static capacitance. However, it is essential to model the dynamic capacitance when analyzing the impact of changes in system parameters on common-mode noise.
2) Influence of parasitic capacitance change on CM noise. It is essential to consider the impact of variations in parasitic capacitance on CM noise to investigate the mechanisms and suppression strategies of CM noise in seawater IPT system.
3) The impact of metallic material on CM-EMI. The electrical parameters of the coil on the metallic material will change, exploring the influence mechanism of metal on the wire will help to further explore the problem of common mode EMI.

The above issues are crucial for a deeper study of CM noise in IPT systems. The author will further conduct in-depth research to elucidate the transmission mechanisms of parasitic capacitance in IPT systems. Additionally, the author encourages more scholars to focus on common-mode issues in seawater IPT and to discover more innovative research.

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