Analysis and Modeling of a Hybrid MMC Coordinated With a Circuit Breaker Under DC Short-Circuit Fault Conditions

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***Abstract*—In recent years, hybrid modular multilevel converters (H-MMCs), which employ both half-bridge submodules (HB-SMs) and full-bridge submodules (FB-SMs) in each arm, have gained significant attention in high-voltage dc (HVdc) systems. This article thoroughly investigates the behavior of an H-MMC with an arbitrary ratio of FB-SMs per arm, coordinated with a dc circuit breaker (CB), during a pole-to-pole short-circuit (SC) fault. Upon detecting an SC fault, the CB is activated, and the H-MMC is temporarily blocked to reduce the peak fault current. The behavior of the H-MMC during this short interval is highly nonlinear, and this article aims to provide a precise model to analyze the H-MMC's behavior and calculate arm currents, dc fault current, and voltage increase in the FB-SMs. The model accounts for all nonlinear states during the blocking state, including arm current decay and the effect of arm inductors on current commutation, which becomes critical when fast CBs or short dc lines are considered in HVdc systems. A new index is also introduced to compare the power switch requirements for various MMC and CB combinations as a function of the FB-SM ratio and CB interruption times. Finally, the analytical model and mathematical equations are validated through simulations and experimental testing on a scaled-down prototype.**

***Index Terms*—DC circuit breaker (DCCB), dc short-circuit (SC) faults, high-voltage dc systems, hybrid modular multilevel converter (H-MMC), modeling.**

I. Introduction

MODULAR multilevel converters (MMCs) are key elements in voltage source converter-based dc grids. With their modular structure, they offer high efficiency, scalability across various voltage and power ratings, and high-quality ac waveforms [1]. In recent years, several MMC topologies have been developed to enhance performance under different operating conditions. The half-bridge MMC (HB-MMC) is the most widely adopted due to its minimal power device requirements. However, it is highly sensitive to dc-side faults and cannot independently interrupt fault currents [2]. During a dc short-circuit (SC), the current rises sharply and may cause device failure if protective measures are not applied within milliseconds.

Handling dc faults in HVdc systems using dc circuit breakers (DCCBs) is more challenging than in ac systems because dc current does not have natural zero crossings, which results in large arcs in mechanical switches [3]. One solution is using fully solid-state circuit breakers (CBs), which offer fast operation but suffer from high ON-state losses [4]. Hybrid CBs (H-CBs) provide an alternative by combining the low-loss advantages of mechanical switches with the fast response of solid-state switches [4], making them the leading technology in DCCB research [5]. However, H-CBs are constrained by their breaking capacity and cost concerns, primarily due to the need to handle high voltage and current stress, as well as significant energy dissipation requirements [6], [7]. To limit the rise of fault currents and reduce the burden on CBs, large dc reactors or fault current limiters are commonly used. However, these solutions increase equipment size, and large dc reactors can adversely affect system voltage stability [8].

An alternative approach to improve HVdc grid resilience against dc faults is the use of converters with fault current control capabilities [9]. These converters employ bipolar submodules (SMs) in MMCs, such as full-bridge SMs (FB-SMs), which inject countervoltage into the MMC arms during faults to limit current surges. Beyond countervoltage injection, FB-SMs can also synthesize negative voltage states, enabling an adjustable dc-link voltage [10]. This flexibility allows for reducing dc voltage during dc faults or extreme weather, enhancing grid reliability—particularly for overhead lines. However, FB-SMs require twice the number of semiconductors compared to half-bridge SMs (HB-SMs), resulting in higher losses under normal conditions [11].

Hybrid MMCs (H-MMCs), which integrate HB-SMs and FB-SMs, provide a tradeoff between fault-clearing capability, losses, and costs [11], [12]. Depending on the FB-SM percentage per arm, they can reduce the dc-side voltage or inject a countervoltage in the blocking state. The method in [12] blocks all H-MMCs during a fault. While this approach ensures a short fault-clearing time, it disrupts power transmission across the entire dc system. In [13], a dc fault line current control is introduced as the primary protection, allowing only stations near the fault to limit current. Shahriari et al. [14] proposed

Received 18 November 2024; revised 19 March 2025; accepted 16 April 2025. Date of publication 22 April 2025; date of current version 30 June 2025. This work was supported by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) under project numbers 495457353 and 540869154. Recommended for publication by Associate Editor F. Dijkhuizen. *(Corresponding author: Hossein Iman-Eini.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3563582.

Digital Object Identifier 10.1109/TPEL.2025.3563582

an MMC arm and leg energy-balancing technique to enhance MMC stability and support the ac grid during faults. However, both research in [13] and [14] require at least 50% of arm SMs to be FB-SMs, increasing costs and reducing efficiency. In [15], model predictive control extends H-MMC operation with fewer FB-SMs but primarily focuses on dc voltage regulation under normal conditions rather than addressing dc fault conditions. Fang et al. [16] introduced an auxiliary circuit to alter the fault current path, using HB- and FB-SMs for fault clearance with 35% FB-SMs per arm. However, the research in [16] and prior studies lack selective fault isolation or exhibit a slow response due to arm current commutations, both of which can be addressed using cost-effective CBs.

A novel approach has recently emerged for HVdc system protection, utilizing converters with partial dc fault ride-through capability along with cost-effective CBs. This method offers a reliable, selective, and economical solution for HVdc fault management [17], [18], [19]. In [18], a fault management strategy is proposed for dc grids incorporating customized H-MMCs and relatively inexpensive mechanical CBs. Simulation results in [18] indicate that H-MMCs with at least 25% FB-SMs per arm can effectively mitigate both pole-to-pole and pole-to-ground dc faults. Additionally, in [19], the coordination between H-MMCs and mechanical CBs with a 5-ms interruption time is emphasized. Extensive electromagnetic transients (EMT)-based simulations suggest an optimal FB-SM ratio per arm, ranging from 17% to 25%. However, the proposed fault-handling strategy presents several challenges, including considerable circulating currents among MMC arms during fault clearance and increased voltage stress on FB-SMs following CB operation. Both articles [18] and [19] lack sufficient theoretical rigor and precise modeling needed to fully capture the dynamic behavior of H-MMCs during the short fault-clearing period. The equivalent circuits used to analyze H-MMC behavior in the blocking state, as well as those in [8] and [20], fail to account for arm current decay (ACD) between the SM capacitor discharge phase and the ac in-feed transition. This omission results in inaccurate predictions of current waveforms and overvoltage stresses on FB-SMs, particularly when fast CBs and short dc lines are integrated into HVdc systems. Moreover, the existing analytical models fail to consider the distinct behavior of each arm in the MMC, as well as the impact of arm inductors on the gradual commutation of arm currents during an SC fault, leading to further inaccuracies and impeding accurate estimation of current behavior in H-MMCs. Consequently, a comprehensive analytical study of the H-MMC blocking state and its internal variables remains lacking in the literature.

To address the limitations of existing analyses on H-MMC blocking behavior, this article presents a detailed assessment of SC fault current evolution in dc systems based on H-MMCs and CBs. The proposed analytical model is applicable to any FB-SM ratio, ranging from zero (representing an HB-MMC) to one (representing an FB-MMC), and treats CB interruption time as a flexible parameter. It accounts for all nonlinear operating states of H-MMCs, including ACD and the influence of arm inductors during current commutation—both critical when fast CBs, short dc lines, or small dc reactors are employed in HVdc systems. It considers the charge dynamics of FB-SM capacitors, accurately computes arm currents, and estimates overvoltage on FB-SMs. Furthermore, the model enables the evaluation of key parameters such as SM capacitance, arm inductance, and dc inductance in relation to critical variables and electrical stress during the fault interval, which is essential for the proper design of H-MMCs and CBs.

Unlike purely numerical EMT simulation-based methods, which require extensive computational resources and lack direct mathematical formulations, the proposed analytical model offers a computationally efficient and mathematically transparent method for evaluating H-MMC behavior during dc fault events. It enables engineers to perform rapid parametric studies without exhaustive simulation sweeps, facilitating early-stage system design and MMC/CB optimization. Additionally, by explicitly accounting for all operational transitions—including the overlooked ACD phase— the model improves the accuracy of voltage stress estimations and fault current predictions. These advantages make it a valuable tool for grid protection studies and experimental validation in HVdc systems.

In addition to the analytical approach for analyzing the behavior of a blocked H-MMC, the proposed model facilitates the investigation of the coordinated operation of H-MMCs with any CBs under dc SC fault conditions. It examines how the FB-SM ratio and CB interruption time influence key system variables and the maximum stress on components, providing valuable data for accurate and cost-effective design. Additionally, a new index, termed the Switch Requirement Index (SRI), is introduced. Utilizing the proposed analytical model along with this new index helps determine the optimal FB-SM ratio for effective coordinated operation, ensuring improved system performance and cost-effectiveness.

The rest of this article is organized as follows. Section II presents the structure of the H-MMC and derives the marginal FB-SM required for the converter to independently interrupt its fault current. Section III details the modeling of the H-MMC and examines its various operating states during the blocking state. Section IV validates the model's accuracy by comparing it with existing models and simulation results, whereas Section V investigates MMC-coordinated operation with CBs based on the derived analytical model. Section VI presents the experimental results of the H-MMC under fault conditions and compares different configurations. Finally, Section VII concludes this article.

II. Hybrid MMC and Marginal FB-SM Ratio

Fig. 1 shows the schematic of the H-MMC in a symmetrical monopole grid configuration. It consists of six arms, with each arm being a series connection of HB-SMs, FB-SMs, and an arm inductor. The FB-SM ratio per arm (η) is defined as the proportion of FB-SMs to the total number of SMs as

$$\eta = \frac{\text{FB} - \text{SMs}}{\text{Total SMs}} = \frac{N_f}{N_f + N_h} = \frac{N_f}{N} \tag{1}$$

where N_f is the number of FB-SMs per arm and N is the total SMs per arm. Furthermore, the nominal dc-side voltage is defined as V_{dn}, and the voltage of both the HB- and FB-SM capacitors is set equally, i.e., $V_C = V_{dn}/N$, where a sorting algorithm can be employed for voltage balancing. Since FB-SMs can synthesize

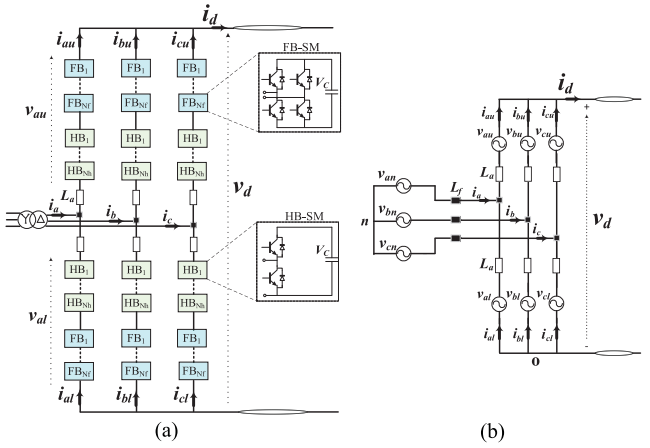

Fig. 1. Hybrid MMC with N_f FB-SMs per arm. (a) Symmetrical monopole grid configuration. (b) Equivalent circuit in steady state.

a negative voltage, $-V_C$, at their terminals, the voltage range that each arm can synthesize is given by

$$-N_f V_C \le V_{xu,l} \le NV_C \text{ or } -\eta V_{dn} \le V_{xu,l} \le V_{dn} \quad (x=a,b,c) \tag{2}$$

where $v_{xu,l}$ represents the arm voltage for phase-x (where x = a,b,c) and the subscripts u and l refer to the upper and lower arms in each leg, respectively. On the other hand, the control system synthesizes the arm voltages as follows:

$$v_{xu} = \frac{V_d}{2} - e_x, \quad v_{xl} = \frac{V_d}{2} + e_x \quad (x=a,b,c) \tag{3}$$

where e_x is the internal electromotive force at phase-x, generated by the MMC's control system to adjust the phase currents, and V_d is the dc-side voltage of the MMC, which is equal to or lower than V_{dn}. From (2) and (3), and considering that the maximum dc-side voltage reaches V_{dn}, the maximum value of e_x is limited to $V_{dn}/2$.

In addition, the arm currents, assuming the second-order circulating current is ideally controlled to zero, are as follows:

$$i_{xu} = \frac{I_d}{3} + \frac{i_x}{2}, \quad i_{xl} = \frac{I_d}{3} - \frac{i_x}{2} \quad (x=a,b,c) \tag{4}$$

where $I_{\rm d}$ is the dc-link current at steady state and i_x is the phase-x current. By applying Kirchhoff's voltage law (KVL) to the lower arm and the ac side source in the equivalent circuit shown in Fig. 1(b) for three phases and doing mathematical calculations, the relation between $e_{\rm x}$ and the external phase voltage at steady state is derived as follows:

$$e_x = v_{xn} - \left(L_f + \frac{L_a}{2}\right)\frac{di_x}{dt} \tag{5}$$

where v_{xn} is the external ac voltage of phase-x, $L_{\rm f}$ is the ac-side filter inductor, and $L_{\rm a}$ is the arm inductor. The voltage drops across arm and filter resistances are small and thus neglected. From (5) and at the unity power factor, it is obtained as

$$v_{xn} \le e_x \text{ and } e_x \le V_{dn}/2 \ \rightarrow v_{xn} \le V_{dn}/2. \tag{6}$$

When a dc fault occurs, the dc-side current rapidly increases and may reach a predefined trip level ($I_{\rm trip}$ of the CB), typically

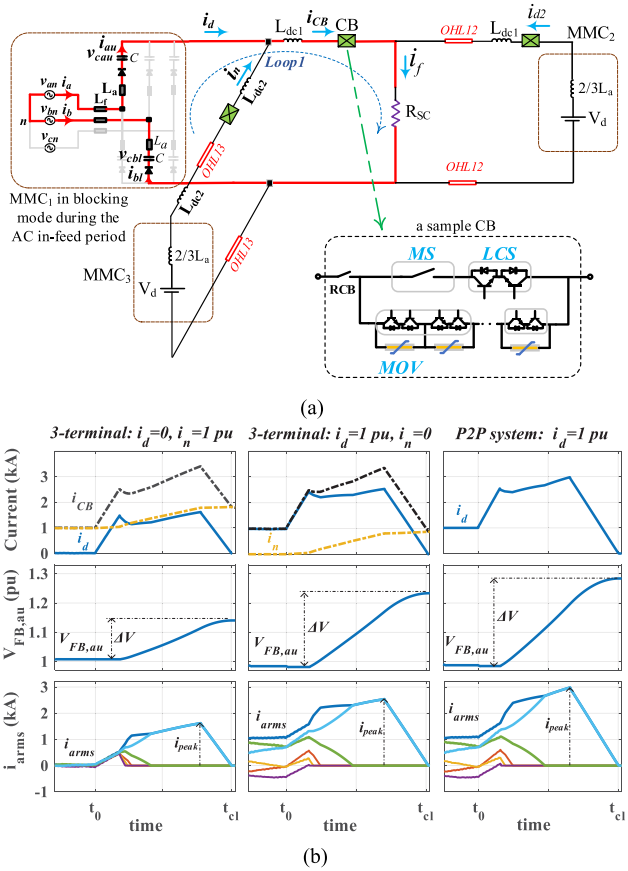

Fig. 2. Modeling of a sample three-terminal dc system under an SC fault near MMC1. (a) Equivalent circuit and schematic of a sample H-CB. (b) Key waveforms of MMC1 and CB current under different configurations and current-sharing scenarios.

two to three times the nominal dc-link current [21]. One method to limit the current rise rate in the MMC near the fault location is temporarily blocking its SMs [8]. In this case, the equivalent circuit shown in Fig. 2(a) is derived for a three-terminal dc network, with an SC fault occurring near MMC1 to model the worst-case scenario.

After blocking MMC1, while other MMCs continue to synthesize their nominal voltage, MMC1 behaves as a nonlinear rectifier, causing current in some arms to decay rapidly to zero. Eventually, current flows through one upper and one lower arm, corresponding to the phases with the highest and lowest voltages, respectively. These arms inject a countervoltage of $2N_fV_C$, diminishing the ac in-feed effect from the ac-side sources. In the H-MMC, the number of FB-SMs per arm can be adjusted to enable self-interruption of the fault current. By keeping the rectified voltage of the blocked MMC below the countervoltage, the following relation is derived as

$$\frac{3\sqrt{3}}{\pi}V_m < 2N_f(V_c+\Delta V_c) \rightarrow \frac{3\sqrt{3}}{2\pi}V_m < N_f\left(\frac{V_{dn}}{N}+\Delta V_c\right) \tag{7}$$

where V_m is the peak phase-neutral voltage and ΔV_C is the voltage increase of the FB-SMs during the blocking state. Neglecting ΔV_C as a safe margin in (7) and considering the maximum value of v_{xn} from (6), the marginal ratio of FB-SMs per arm, $\eta_{\rm mar,}$ is

given by

$$\frac{3\sqrt{3}}{2\pi}V_m < \frac{3\sqrt{3}}{2\pi}\frac{V_{dn}}{2} < N_f\left(\frac{V_{dn}}{N}+\Delta V_c\right) \rightarrow \begin{cases} 0.4N < N_f \text{ or} \\ \eta_{\text{mar}} \approx 0.4 \end{cases}. \tag{8}$$

According to (8), an H-MMC with 40% FB-SMs per arm can theoretically interrupt the SC fault current at its dc terminal. However, when the FB-SM ratio is reduced below 40% to minimize conduction losses, the converter requires an additional CB to interrupt the fault current. Furthermore, as shown in Fig. 2(a), in a multiterminal system, the faulty line current is also supplied by the neighboring line. As a result, CBs are required at both ends of each dc line to interrupt the fault current and isolate the fault in dc grids.

While additional CBs increase the number of protection elements and overall cost, they enhance the robustness and resilience of the HVdc system. Additionally, coordinating H-MMCs and CBs during a dc fault significantly limits peak fault currents in both components, reducing the need for switches with high current ratings, large dc reactors, metal oxide varistors (MOVs) with high energy dissipation requirements, and other overcurrent-rated devices. This coordination ultimately lowers the overall cost and complexity of the HVdc system.

III. Analysis of H-MMC With an Arbitrary FB-SM Ratio Under Short-Circuit Fault Conditions

This section analyzes the H-MMC with an arbitrary FB-SM ratio and derives its analytical model for the fault-blocking state. The analysis considers the worst-case operating condition—a pole-to-pole fault with zero resistance occurring at zero distance from the MMC station— to determine the maximum passing arm current and the overvoltage on the FB-SMs. This assessment is essential for the proper sizing of MMCs and CBs, as well as for ensuring safety and reliable grid operation [22].

As shown in Fig. 2, a key factor influencing the voltage and current stress on MMC1 (the blocked MMC) during a SC fault is the presence of the neighboring line and its current-sharing pattern with MMC1 prior to the fault event. According to Kirchhoff's current law (KCL), the current in the CB in Fig. 2(a) can be expressed as

$$i_{\text{CB}} = i_d + i_n. \tag{9}$$

In (9), the output current from the blocked MMC (i_d) exhibits highly nonlinear behavior, whereas the current from the adjacent line (i_n) can be approximated using linear functions. Examining different scenarios in Fig. 2(b) shows that under similar fault conditions and trip levels, the highest voltage stress on FB-SMs and the highest current stress on MMC arms occur in the point-to-point (P2P) configuration. Therefore, in the following analysis, the case without a neighboring dc line is examined, whereas the system behavior in the presence of a neighboring dc line can be derived using the method given in Section III and some linear approximations.

The following additional assumptions are made for the analytical approach and derivation of the system model.

1) All components are considered lossless and ideal.
2) The ac-side filter L_f is neglected in calculations.
3) The CB is modeled as an ideal mechanical switch with an interruption delay (T_{cb}), in parallel with a semiconductor breaker and the corresponding MOVs.
4) At the fault instant, the ac voltage pattern follows $v_{\text{cn}} < v_{\text{bn}} < v_{\text{an}}$.

In addition, the ac-side voltage and phase currents are determined by the following equations:

$$v_{xn} = V_m \sin(\omega t + \theta_{xn}), \quad x = a, b, c \tag{10}$$

$$i_x = I_m \sin(\omega t + \theta_{xn}), \quad x = a, b, c \tag{11}$$

where I_m is the peak phase current, θ_{xn} represents the phase angle of phase-x at $t = t_0$, and t_0 is the fault instant. Note that in this article, capital letters, e.g., I_d or V_d, represent dc values.

To analyze the H-MMC and the series CB, four operating states for the blocked MMC are considered: SM discharge, ACD, ac in-feed, and fault current decay. Additionally, the ACD and ac in-feed periods are further divided into three regions. Subsequently, to derive the system model, the corresponding equivalent circuits are shown in Fig. 3, and the key waveforms are shown in Fig. 4 for two cases: a fast CB and a slow CB.

SM discharge—Region 0 (t_0 to t_1): After the occurrence of an SC fault at $t = t_0$, the MMC converter continues to operate as it did under prefault conditions. Consequently, due to synthesizing the dc-side voltage V_d, the dc-side current i_d will rapidly increase. The circuit in Fig. 3(a) models this system behavior. By applying KVL to the loop containing the upper and lower arms of one phase and the SC path, the following equation can be obtained:

$$v_{xu} - L_a\frac{di_{xu}}{dt} + v_{xl} - L_a\frac{di_{xl}}{dt} = L_{\text{dc}}\frac{di_d}{dt}. \tag{12}$$

Now, by substituting the upper and lower arm voltages from (3) into (12), the following result is derived:

$$-L_a\frac{di_{xu}}{dt} - L_a\frac{di_{xl}}{dt} = -V_d + L_{\text{dc}}\frac{di_d}{dt}. \tag{13}$$

Summing the equation in (13) for three phases and applying the following KCL at the MMC's upper and lower nodes

$$i_{au} + i_{bu} + i_{cu} = i_d\,, \quad i_{al} + i_{bl} + i_{cl} = i_d \tag{14}$$

the following relation for the dc-side current i_d is obtained as

$$i_d(t) = i_d(t_0) + \frac{V_d}{(L_{\text{dc}} + 2/3L_a)}(t - t_0) \tag{15}$$

where $i_d(t_0)$ represents the dc-side current at the time of the fault event. By substituting the result from (15) into (13) and noting that the difference between the upper and lower arm currents is equal to the phase current, i.e., i_{xu}-$i_{xl} = i_x$, the following relations for the arm currents are derived:

$$\begin{cases} i_{xu}(t) = \frac{I_d}{3} + \frac{1}{2}i_x(t) + \frac{1}{3}(i_d(t) - i_d(t_0)) \\ i_{xl}(t) = \frac{I_d}{3} - \frac{1}{2}i_x(t) + \frac{1}{3}(i_d(t) - i_d(t_0)) \end{cases} \tag{16}$$

where the phase currents i_x are determined from (11). During this time interval, SM capacitors are discharged, causing a sharp rise in the dc-side current. The protection system generates a fault signal at $t = t_1$ when $i_d = I_{trip}$, marking the end of Region 0.

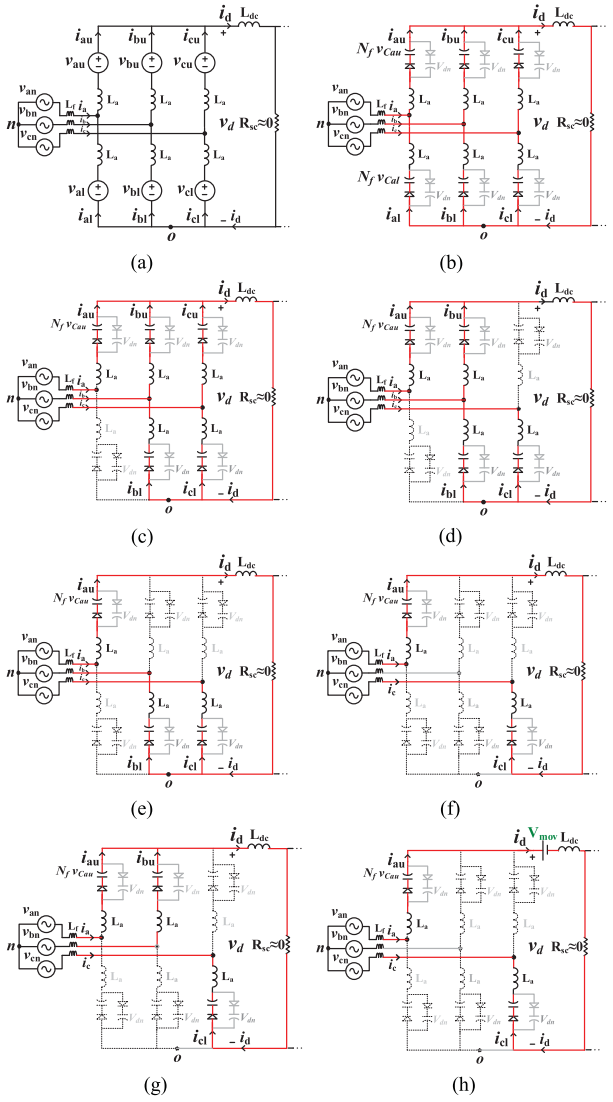

Fig. 3. Analysis of the H-MMC during the dc fault condition with $R_{SC} \approx 0$ and operation in blocking mode (with the constraint: $v_{cn} < v_{bn} < v_{an}$ at the fault instant). (a) SM discharge (Region 0). (b)–(d) ACD period (Regions 1–3). (e)–(g) AC in-feed period (Regions 4–6). (h) Fault current decay (Region7).

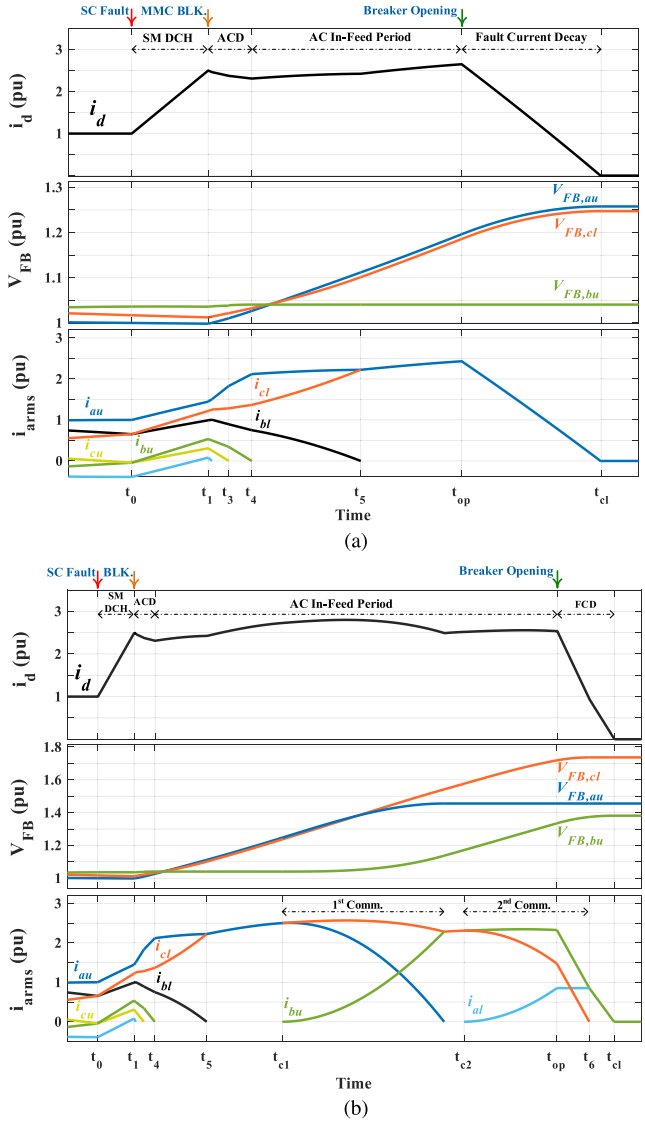

Fig. 4. Key waveforms of the H-MMC with an FB-SM ratio equal to 0.25 under the blocking state and coordination with (a) fast CB and (b) slow CB.

Arm Current Decay—Region 1 *(t_1 to t_2):* After fault detection at $t = t_1$, the H-MMC is blocked, and a trip signal is sent to the CB to open the mechanical switch. The equivalent circuit shown in Fig. 3(b) models the system behavior, assuming the arm current is positive in each arm due to the increase in Region 0. By applying KVL to the loop containing the upper arm of phase-*x*, the SC path, and the voltage source at phase-*x*, it is obtained:

$$L_a \frac{di_{xu}}{dt} + N_f v_{Cxu} + L_{dc} \frac{di_d}{dt} = v_{xn} + v_{no} \tag{17}$$

where v_{Cxu} represents the FB-SM capacitor voltage in the upper arm of phase-*x*, and v_{no} is the neutral point voltage. In addition, another KVL can be written for the loop containing the lower arm and the voltage source at phase-*x* as follows:

$$-L_a \frac{di_{xl}}{dt} - N_f v_{Cxl} = v_{xn} + v_{no} \tag{18}$$

where v_{Cxl} represents the FB-SM capacitor voltage in the lower arm of phase-*x*. By summing (17) and (18) for all three phases, and considering the KCLs in (14) while assuming that the voltages of the FB-SMs are approximately V_{dn}/N, the dc-side and arm currents are obtained as follows:

$$i_d(t) = i_d(t_1) + \frac{-2\eta V_{dn}}{(L_{dc} + 2/3L_a)}(t - t_1) \tag{19}$$

$$\begin{cases} i_{xu}(t) = i_{xu}(t_1) + \frac{1}{3}(i_d(t) - i_d(t_1)) \\ -\frac{V_m}{\omega L_a}(\cos(\omega t + \theta_{xn}) - \cos(\omega t_1 + \theta_{xn})) \\ i_{xl}(t) = i_{xl}(t_1) + \frac{1}{3}(i_d(t) - i_d(t_1)) \\ +\frac{V_m}{\omega L_a}(\cos(\omega t + \theta_{xn}) - \cos(\omega t_1 + \theta_{xn})) \end{cases} \tag{20}$$

where $i_{\mathrm{xu}}(t_1)$ and $i_{\mathrm{xl}}(t_1)$ are determined from (16), and $i_d(t_1)$ is determined from (15). The operation in Region 1 ends when the arm current in the lower leg of phase-a becomes zero. Since this time interval is very short, the sinusoidal term in (20) can be ignored, allowing for the use of first-order equations.

Accordingly, t_2 is obtained as follows:

$$t_2 \approx t_1 - \frac{3\mathrm{I}_m \sin(\omega t_1 + \theta_{an})}{di_d/dt(t_2)} \tag{21}$$

where $di_d/dt(t_2)$ is calculated from (19). Subsequently, the voltage of each FB-SM can be derived by integrating the arm currents:

$$v_{Cxu,l}(t) = v_{Cxu,l}(t_1) + \frac{1}{C_{SM}} \int_{t_1}^{t} i_{xu,l} dt \tag{22}$$

where C_{SM} represents the capacitance of the SM capacitors. In addition, $v_{Cxu}(t_1)$ and $v_{Cxl}(t_1)$ are the initial values of the capacitor voltages at $t = t_1$, which are approximately equal to V_{dn}/N. Since the upper and lower arm current equations are known from (20), the voltage of FB-SMs can be readily determined from (22).

Arm Current Decay—Region 2 (t_2 to t_3): After the current in an arm reaches zero at $t = t_2$, the converter continues its operation with five arms, as depicted in Fig. 3(c). In this region, (17) and (18) can still be used, except that the equation for the lower leg in phase-a is eliminated. By performing some mathematical analysis and considering the KCLs at the upper and lower nodes of the MMC, the following equations for the slopes of i_d and the arm currents are obtained:

$$\frac{di_d}{dt} = \frac{0.5v_{an} - 2\eta V_{dn}}{(L_{dc} + 5/6L_a)} = \frac{0.5V_m \sin(\omega t + \theta_{an}) - 2\eta V_{dn}}{(L_{dc} + 5/6L_a)} \tag{23}$$

$$\begin{cases} \frac{di_{xu}}{dt} = \frac{v_{xn}}{L_a} + \frac{1}{3}\frac{di_d}{dt} \\ \frac{di_{xl}}{dt} = -\frac{(v_{xn}+0.5v_{an})}{L_a} + \frac{1}{2}\frac{di_d}{dt} \end{cases} \tag{24}$$

Since the time interval of Region 2 is very short, the phase voltages v_{xn} is replaced in (23) and (24) with their initial values at $t = t_2$, i.e., $v_{\mathrm{xn}} \approx v_{\mathrm{xn}}(\mathrm{t}_2)$. Then, i_d and the arm currents can be derived by

$$i_d(t) \approx i_d(t_2) + \frac{0.5V_m \sin(\omega t_2 + \theta_{an}) - 2\eta V_{dn}}{(L_{dc} + 5/6L_a)}(t - t_2) \tag{25}$$

$$i_{xu,l}(t) \approx i_{xu,l}(t_2) + \frac{di_{xu,l}}{dt}(t - t_2) \tag{26}$$

where the slopes of the arm currents in (26) are derived from the expressions in (23) and (24) at $t = t_2$. The operation in Region 2 ends when the current in the upper arm of phase-c (or phase-b, depending on the phase-a angle θ_{an} at the fault instant) becomes zero at $t = t_3$, which is estimated by

$$t_3 \approx t_2 - \frac{i_{cu}(t_2) \times L_a}{V_m \sin(\omega t_2 + \theta_{cn}) + 1/3L_a di_d/dt(t_2)} \tag{27}$$

where $i_{\mathrm{cu}}(t_2)$ is calculated from (20).

Arm Current Decay—Region 3 (t_3 to t_4): After the current in the second arm reaches zero, the converter continues its operation with four arms, and the model shown in Fig. 3(d) can be used for analysis. During this period, (17) and (18) remain valid, except that the equations for the lower arm in phase-a and the upper arm in phase-c are eliminated. By performing mathematical analysis and considering the KCLs at the upper and lower nodes of the MMC, the following equations for the slopes of i_d and the arm currents are obtained:

$$\frac{di_d}{dt} = \frac{v_{ac} - 4\eta V_{dn}}{2(L_{dc} + L_a)} = \frac{\sqrt{3}/2V_m \sin(\omega t + \theta_{ac}) - 2\eta V_{dn}}{(L_{dc} + L_a)} \tag{28}$$

$$\begin{cases} \frac{di_{xu}}{dt} = +\frac{(v_{xn}+0.5v_{cn})}{L_a} + \frac{1}{2}\frac{di_d}{dt} \\ \frac{di_{xl}}{dt} = -\frac{(v_{xn}+0.5v_{an})}{L_a} + \frac{1}{2}\frac{di_d}{dt} \end{cases}. \tag{29}$$

where $\theta_{ac} = \theta_{an} - \pi/6$. The duration of Region 3, similar to Regions 1 and 2, is very short, allowing the approximation $v_{xn} \approx v_{xn}(t_3)$ for the sinusoidal terms. Accordingly, i_d and arm currents are derived as follows:

$$i_d(t) \approx i_d(t_3) + \frac{\sqrt{3}/2V_m \sin(\omega t_3 + \theta_{ac}) - 2\eta V_{dn}}{(L_{dc} + L_a)}(t - t_3) \tag{30}$$

$$i_{xu,l}(t) \approx i_{xu,l}(t_3) + \frac{di_{xu,l}}{dt}(t - t_3) \tag{31}$$

where $i_{\mathrm{xu,l}}(t_3)$ in (31) are derived from (26). The operation in Region 3 ends when the current in the upper arm of phase-b becomes zero at $t = t_4$, which is calculated as follows:

$$t_4 \approx t_3 - \frac{i_{bu}(t_3) \times L_a}{\begin{array}{c} V_m(\sin(\omega t_3 + \theta_{bn}) + 0.5\sin(\omega t_3 + \theta_{cn})) \\ +1/2L_a di_d/dt(t_3) \end{array}} \tag{32}$$

where $i_{bu}(t_3)$ can be calculated from (26). Regions 1–3 correspond to the ACD interval, which ends at $t = t_4$. During the interval t_1 to t_4, at least one lower and one upper arm in the same leg conduct, significantly reducing the MMC's dc-side voltage and resulting in dc-side current decay.

AC in-feed period—Region 4 (t_4 to t_5): Once the current in the third arm reaches zero, the circuit model shown in Fig. 3(e) can be used for further analysis. At this stage, the fault point is primarily fed by the ac source, marking the beginning of the ac-in feed period. During this interval, (17) and (18) remain valid, except that the equations for the lower arm in phase-a and the upper arms in phase-b and phase-c are omitted. Through circuit analysis, and by considering $i_{\mathrm{au}} = i_d$, $i_{\mathrm{bl}} + i_{\mathrm{cl}} = i_d$, and $i_{\mathrm{xu,l}} = C_{SM} dv_{Cxu,l}/dt$, the equation for i_d is derived as follows:

$$\left(\frac{2}{3}L_{\mathrm{dc}} + L_a\right)\frac{d^2 i_d}{dt^2} + \frac{1}{C_f} i_d = V_m \omega \cos(\omega t + \theta_{an}) \tag{33}$$

where $C_f = C_{fb}/N_f$ represents the equivalent series capacitance of the FB-SMs in one arm. The differential equation can now be solved by determining the initial conditions i_{d} and $\frac{\mathrm{di_d}}{\mathrm{dt}}$ at $t = t_4$, where $i_d\,(t_4)$ is obtained from (30) and $\frac{\mathrm{di_d}}{\mathrm{dt}}(t_4)$ is found as

$$\begin{aligned} \frac{d_{id}}{dt}(t_4) = & \frac{1}{(L_{\mathrm{DC}} + 1.5L_a)} \\ & \times (1.5v_{an}(t_4) - 0.5N_f \times (2v_{Cau}(t_4) \\ & + v_{Cbl}(t_4) + v_{Ccl}(t_4))) \end{aligned} \tag{34}$$

and the initial values of $v_{\mathrm{Cau}}(t_4)$, $v_{\mathrm{Cbl}}(t_4)$, and $v_{\mathrm{Ccl}}(t_4)$ can be derived from the previous state. With these initial conditions, (34) can be solved, and the arm current i_{au} or i_d can be obtained

as

$$i_{au}(t) = i_d(t) = A_4 \sin(\omega_4 t + \varphi_4) + B_4 \cos(\omega t + \theta_{an}) \tag{35}$$

where

$$B_4 = \frac{V_m \omega}{(2/3L_{DC}+L_a)(\omega_4{}^2-\omega^2)}\ , \omega_4 = \sqrt{\frac{1}{(2/3L_{DC}+L_a)C_f}}. \tag{36}$$

In addition, the constants φ_4 and A_4 can be determined from the initial conditions as follows:

$$\varphi_4 = \tan^{-1}\left(\frac{\omega_4(i_d(t_4) - B_4\cos(\omega t_4 + \theta_{an}))}{di_d/dt(t_4) + \omega B_4 \sin(\omega t_4 + \theta_{an})}\right) - \omega_4 t_4$$

$$A_4 = \frac{i_d(t_4) - B_4\cos(\omega t_4 + \theta_{an})}{\sin(\omega_4 t_4 + \varphi_4)}. \tag{37}$$

After calculating the upper arm current from (35), the lower arm currents can be determined by

$$\begin{aligned} i_{bl}(t) \approx i_{bl}(t_4) + \frac{1}{2}((i_d(t) - i_d(t_4)) \\ - \frac{N_f}{L_a}(v_{Cbl}(t_4) - v_{Ccl}(t_4))(t - t_4) \\ - \frac{\sqrt{3}V_m}{\omega L_a}(\cos(\omega t_4 + \theta_{bc}) - \cos(\omega t + \theta_{bc}))) \end{aligned} \tag{38}$$

$$\begin{aligned} i_{cl}(t) \approx i_{cl}(t_4) + \frac{1}{2}((i_d(t) - i_d(t_4)) \\ - \frac{N_f}{L_a}(v_{Ccl}(t_4) - v_{Cbl}(t_4))(t - t_4) \\ + \frac{\sqrt{3}V_m}{\omega L_a}(\cos(\omega t_4 + \theta_{bc}) - \cos(\omega t + \theta_{bc}))) \end{aligned} \tag{39}$$

where $i_{bl}(t_4)$ and $i_{cl}(t_4)$ can be calculated from (31). According to the initial value of θ_{an} ($\sim$90°), the current i_{bl} reduces to zero at $t = t_5$. Thus, t_5 can be determined from (38) by incrementing t with small time steps and checking the value of i_{bl} at each step. In addition, the voltage of the FB-SMs in the upper arm of phase-a is obtained from relation (22) as follows:

$$\begin{aligned} v_{Cau}(t) = v_{Cau}(t_4) + \frac{A_4}{\omega_4 C}(-\cos(\omega_4 t + \varphi_4) \\ + \cos(\omega_4 t_4 + \varphi_4)) \\ + \frac{B_4}{\omega C}(\sin(\omega t + \theta_{an}) - \sin(\omega t_4 + \theta_{an})). \end{aligned} \tag{40}$$

Similarly, the voltage waveforms for lower arms are derived.

AC in-feed period—Region 5 (t_5 to t_{op}): Once the current in the fourth arm becomes zero, the converter continues operating with two arms, corresponding to the phases with maximum and minimum voltages. The circuit model shown in Fig. 3(f) can be used to analyze the system during this period. Through mathematical analysis and by considering $i_{\mathrm{au}} = i_{\mathrm{cl}} = i_{\mathrm{d}}$, the equation for i_d is derived as

$$\left(\frac{1}{2}L_{dc}+L_a\right)\frac{d^2 i_d}{dt^2} + \frac{1}{C_f}i_d = \frac{\sqrt{3}V_m\omega}{2}\cos(\omega t + \theta_{ac}). \tag{41}$$

Similar to the previous state, the differential equation is solved by determining the initial values of i_{d} and $\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}$ at $t = t_5$, where $i_d(t_5)$ is obtained from (35) and $\frac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t}(t_5)$ is calculated as

$$\frac{d_{id}}{dt}(t_5) = \frac{\sqrt{3}V_m\sin(\omega t_5 + \theta_{ac}) - N_f \times (v_{Cau}(t_5) + v_{Ccl}(t_5))}{(L_{DC} + 2L_a)} \tag{42}$$

and the initial values of $v_{\mathrm{Cau}}(t_5)$ and $v_{\mathrm{Ccl}}(t_5)$ can be obtained from the previous state at $t = t_5$. Subsequently, (41) can be solved, yielding the current waveforms as

$$i_d(t) = A_5 \sin(\omega_5 t + \varphi_5) + B_5 \cos(\omega t + \theta_{ac}) \tag{43}$$

$$B_5 = \frac{\sqrt{3}V_m\omega}{(L_{\mathrm{DC}}+2L_a)(\omega_5{}^2-\omega^2)}\ ,\ \omega_5 = \sqrt{\frac{1}{(0.5L_{\mathrm{DC}}+L_a)C_f}}. \tag{44}$$

In addition, the parameters φ_5 and A_5 are determined from the initial conditions as follows:

$$\varphi_5 = \tan^{-1}\left(\frac{\omega_5(i_d(t_5) - B_5\cos(\omega t_5 + \theta_{ac}))}{d_{id}/dt(t_5) + \omega B_5 \sin(\omega t_5 + \theta_{ac})}\right) - \omega_5 t_5$$

$$A_5 = \frac{i_d(t_5) - B_5\cos(\omega t_5 + \theta_{ac})}{\sin(\omega_5 t_5 + \varphi_5)}. \tag{45}$$

This operating mode continues until the CB opens. However, a commutation process may initiate between the MMC arms before that, as described in the following section.

AC in-feed period—Region 6 (t_{c1} to t_{op}): This state corresponds to the time interval in which current commutation occurs between the MMC arms and ends when the CB opens. Considering the commutation between the upper arms of phase-a and phase-b, the equivalent circuit is derived, as shown in Fig. 3(g).

An approximation of the commutation times can be determined as follows:

$$t_{ck} = \frac{1}{\omega}\left(j\frac{\pi}{3} + \frac{\pi}{6} - \theta_{an}\right) \text{ and } t_{c1} > t_5 \tag{46}$$

where k and j are positive integers. The first commutation instant, t_{c1}, is obtained by selecting the smallest value of j for which the resulting t_{ck} satisfies $t_{\mathrm{c1}} > t_5$. Once t_{c1} is determined, subsequent commutation instants $t_{c2}, t_{c3}, \ldots$ can be calculated by incrementing j accordingly. These times represent the approximate instants at which commutations occur among the MMC arms before the CB opens. A longer CB interruption time may result in multiple commutations.

After determining the beginning of each commutation, the dc-side current i_d and arm currents can be determined using the equations in Region 4, i.e., (34)–(39), except that t_4 is replaced with t_{ck}, and the variables of the active arms are replaced with the corresponding new ones. Additionally, when commutation occurs in the upper arms, such as in Fig. 3(g), the sign of the sinusoidal terms in (34), (38), and (39) should be reversed. This adjustment, for example, applies to the arm currents in Fig. 3(g) as

$$\begin{aligned} i_{au}(t) \approx i_{au}(t_{ck}) + \frac{1}{2}((i_d(t) - i_d(t_{ck})) \\ - \frac{N_f}{L_a}(v_{Cau}(t_{ck}) - v_{Cbu}(t_{ck}))(t - t_{ck}) \end{aligned}$$

$$+\frac{\sqrt{3}V_m}{\omega L_a}(\cos(\omega t_{ck}+\theta_{ab})-\cos(\omega t+\theta_{ab}))) \quad (47)$$

$$i_{bu}(t)\approx i_{bu}(t_{ck})+\frac{1}{2}((i_d(t)-i_d(t_{ck}))-\frac{N_f}{L_a}(v_{Cbu}(t_{ck})-v_{Cau}(t_{ck}))(t-t_{ck})-\frac{\sqrt{3}V_m}{\omega L_a}(\cos(\omega t_{ck}+\theta_{ab})-\cos(\omega t+\theta_{ab}))). \quad (48)$$

The commutation between the two arms ends when the current in one of the commutating arms reaches zero.

In brief, using the equations developed in Regions 4 and 5, and considering the commutation times in (46), the system's behavior in Region 6 is accurately estimated.

Fault current decay—Region 7 (t_{op} to t_{cl}): Fault current decay begins when the CB opens at $t_{op}=t_0+T_{cb}$, where T_{cb} is the interruption delay required for the mechanical switch to fully open. At this stage, MOVs are inserted into the circuit to dissipate the inductive energy stored in the system. The MOVs can be modeled as a dc voltage source with a magnitude equal to V_{mov} and a polarity opposite to the ac side. Since the total MOV voltage is sufficiently large (typically 1.5–2 times the nominal dc voltage), it facilitates a smooth and rapid decay of the fault current. At the instant when the CB opens, the following two cases are recognized for the MMC.

1) *Case 1:* As shown in Fig. 4(a), current is flowing through two arms when the CB opens.
2) *Case 2:* As shown in Fig. 4(b), current is flowing through three arms when the CB opens.

In Case 1, a circuit model such as in Fig. 3(h) can be recognized. By applying KVL to the loop containing the two arms and the SC path, the current equation is obtained as

$$i_d\approx i_d(t_{op})-\frac{V_{\text{mov}}+N_f(V_{Cau}(t_{op})+V_{Ccl}(t_{op}))-\sqrt{3}V_m\sin(\omega t_7+\theta_{ac})}{(L_{\text{dc}}+2L_a)}(t-t_{op}) \quad (49)$$

where all variables at $t=t_{\text{op}}$ are calculated from the equations in Region 5. Finally, the current reaches zero at time t_{cl}, which can be calculated as

$$t_{cl}\approx t_{op}+\frac{(L_{\text{dc}}+2L_a)i_d(t_{op})}{V_{\text{mov}}+N_f(V_{Cau}(t_{op})+V_{Ccl}(t_{op}))-\sqrt{3}V_m\sin(\omega t_{op}+\theta_{\text{ac}})}. \quad (50)$$

In Case 2, similar to Case 1, the same modeling strategy can be applied. Assuming that commutation occurs between the lower arms of phase-a and phase-c when MOVs are inserted, as shown in Fig. 4(b), the following expression for $i_{\text{bu}}=i_d$ can be obtained:

$$i_d\approx i_d(t_{op})-\frac{V_{\text{mov}}+N_f(V_{Cbu}(t_{op})+(V_{Cal}(t_{op})+V_{Ccl}(t_{op}))/2)-1.5v_{bn}(t_{op})}{(L_{dc}+1.5L_a)}(t-t_{op}). \quad (51)$$

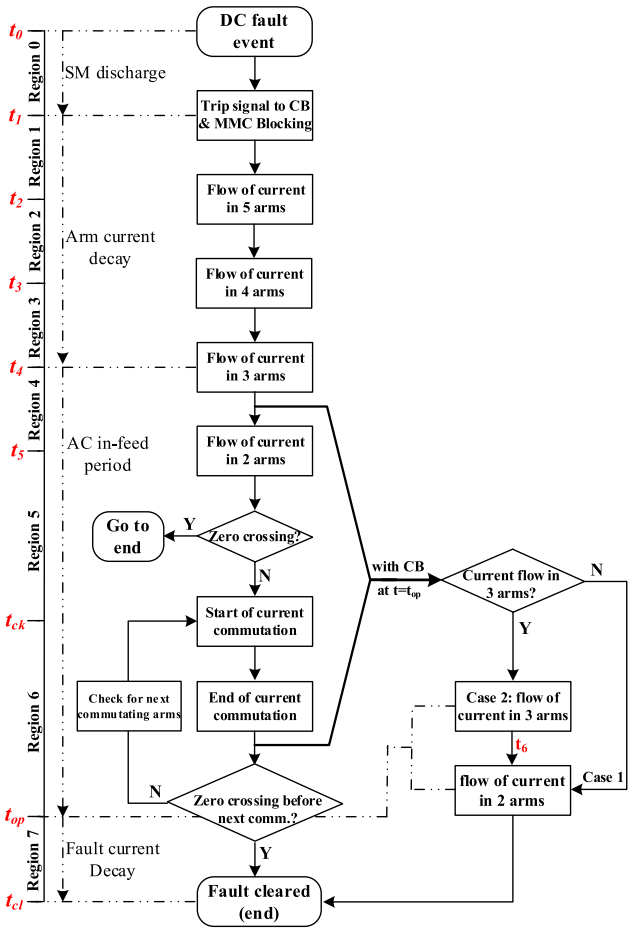

Fig. 5. Flowchart for modeling of an H-MMC with an arbitrary FB-SM ratio under short-circuit fault conditions.

For the two other arms, i.e., i_{al} and i_{cl}, the same equations as in Region 4 apply, except that the variables are redefined based on these two arms. This state ends when the current in one of the arms reaches zero, labeled as t_6. At this point, the current flows through two arms, and the same equations as in Case 1 apply for the remaining period.

To summarize the method of deriving the system model for the H-MMC under SC fault conditions, a flowchart is provided in Fig. 5. The equations extracted for Regions 0–7 are applied to each section to estimate the current and voltage waveforms accordingly. Notably, while the equations for Regions 0–7 follow $v_{\text{cn}}<v_{\text{bn}}<v_{\text{an}}$ at the fault instant, similar equations for other regions can be obtained by substituting one phase variable for another. These additional equations are omitted here to avoid repetition.

According to the flowchart in Fig. 5, the proposed method applies to any FB-SM ratio in H-MMCs, regardless of whether CBs are present in the system. When the CB interruption delay is selected long enough, the MMC's dc-side current will decay to zero before the CB operates, provided the FB-SM ratio exceeds 0.4. Conversely, if a CB is present, it may open during Regions 4–6.

TABLE I
PARAMETERS OF THE SYSTEM UNDER STUDY

Quantity	Symbol	Simulation	Experiment
Nominal active power	P	320 MW	750 W
Nominal dc link voltage	V_{dn}	320 kV	150 V
Nominal dc line current	I_d	1 kA	5 A
Peak of phase voltage	V_m	141 kV	68 V
Peak of phase current	I_m	1.52 kA	7.4 A
CB trip current	I_{trip}	2.5 kA	12.5 A
Number of SMs per arm	N	160	5
SM nominal voltage	V_C	2 kV	30 V
HB-SM capacitance	C_{hb}	6.7 mF	2 mF
FB-SM capacitance	C_{fb}	12 mF	2 mF
Arm inductor	L_{a}	43 mH	4.5 mH
DC reactor	L_{DC}	100 mH	10 mH

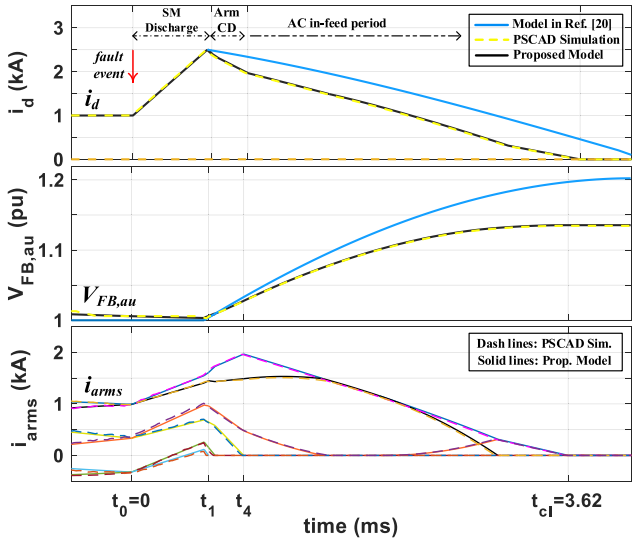

Fig. 6. Verification of the proposed model for $\eta = 0.5$ and $R_{\text{SC}} \approx 0$.

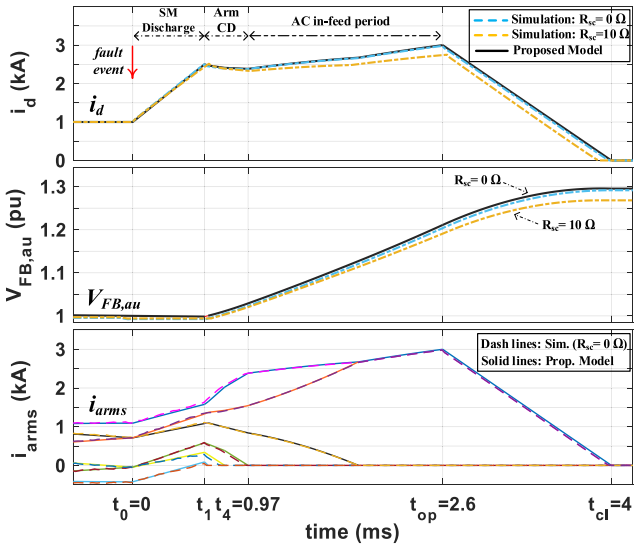

Fig. 7. Verification of the proposed model for $\eta = 0.2$ and $T_{cb} = 2$ ms.

TABLE II
COMPARISON OF APPROACHES FOR ANALYZING BLOCKED MMC BEHAVIOR UNDER DC FAULTS

Method	Analysis approach	FB-SM Range	Closed-form Eqs.		T_{cb} in CB
			ACD	Comm.	
Ref. [17]	EMT Sim.	Discrete η	no	no	1 ms
Ref. [7]	EMT Sim.	η=0	Intro.	no	N/M
Ref. [18]	EMT Sim.	Discrete η	no	no	5-15 ms
Ref. [19]	EMT Sim.	Discrete η	no	no	4.6 ms
Ref. [8]	Analytical	η=0	no	yes	4 ms
Ref. [20]	Analytical	η: 0.5 ~ 1	no	Simp.	--
Proposed	Analytical	η: 0 ~ 1	yes	yes	Flex.

IV. MODEL VERIFICATION AND COMPARISON

To verify the accuracy of the proposed analytical model for the H-MMC and the validity of the analysis, the predicted behavior of the H-MMC under fault conditions is compared with the results from PSCAD/EMTDC simulations as well as the proposed model in [20]. In the selected case study, the nominal dc-side voltage is 320 kV, with a nominal current of 1 kA and a trip level of 2.5 kA for the CB. The fault is a pole-to-pole fault with near-zero resistance, representing worst-case conditions for both the MMC and the CB. The remaining system parameters are listed in Table I, and the parameter selection method is explained in Appendix.

The corresponding verifications of the proposed model are shown in Figs. 6 and 7 for two different FB-SM ratios.

Fig. 6 shows the case study where the FB-SM ratio is 0.5, along with comparisons to the PSCAD/EMTDC results and the dynamic model presented in [20]. It is important to note that the dynamic model in [20] is valid for H-MMCs with an FB-SM ratio of 0.5 or higher. Furthermore, the CB is excluded from this investigation. From Fig. 6, it is observed that there is a notable agreement between the predictions of the proposed model and the PSCAD/EMTDC results, with the curves almost overlapping. However, the proposed model in [20] shows errors of 17% in estimating the fault-clearing time and 49% in calculating the voltage increase in the FB-SMs. These errors primarily arise from neglecting the ACD period in the H-MMC, as shown in Fig. 6, during the time interval from t_1 to t_4.

Furthermore, unlike the model proposed in this article, the model in [20] cannot predict each arm's current waveform. This limitation results in a significant 27% error in estimating the maximum fault current in MMC arms, which occurs at $t = t_4$ rather than at $t = t_1$, as predicted by the model in [20].

Fig. 7 compares the model's behavior with PSCAD/EMTDC results for FB-SM ratios of 0.2, with R_{SC} values close to zero and 10 Ω (or 0.03 p.u.). The model aligns well with simulation results when R_{SC} is near zero. However, as R_{SC} increases, 7% deviations occur, with a decrease in peak current and FB-SM voltage. Nevertheless, the model correctly predicts the worst-case operating conditions in the MMC and CB, which is the objective of this article.

Table II compares existing methods for analyzing blocked MMC behavior under dc faults. It includes both EMT simulation-based and analytical approaches, highlighting key

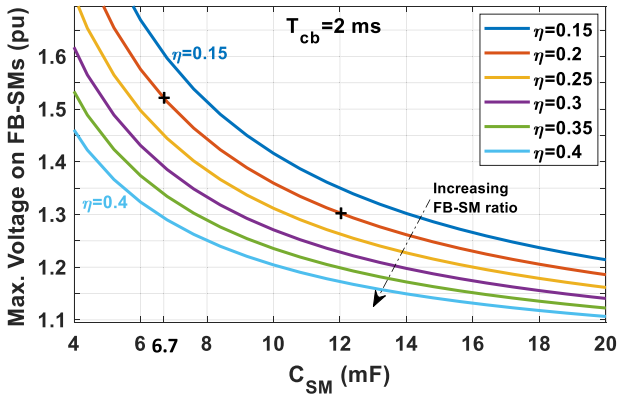

Fig. 8. Impact of SM capacitance on the maximum FB-SM voltage at different FB-SM ratios during coordinated operation.

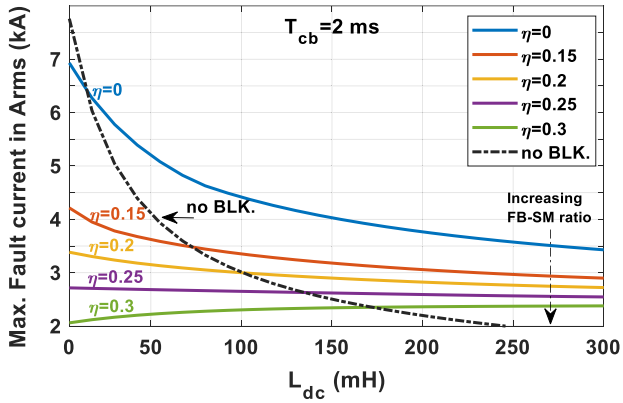

Fig. 9. Maximum fault current in MMC arms versus DC inductor.

aspects such as fault current decay analysis, commutation modeling, FB-SM ratio range, and CB interruption time.

Most prior studies rely on EMT simulations to examine fault current interruption, providing valuable but software-dependent numerical insights. However, analytical methods, including the proposed approach, offer a deeper understanding of MMC behavior during dc faults. Unlike previous works that often overlook certain operating regions of the blocked MMC and gradual arm current commutation, the proposed method captures detailed internal current dynamics and accurately models arm inductor effects, ensuring more precise waveform predictions across the full FB-SM ratio range. Additionally, it treats CB interruption time as a flexible parameter.

V. Investigation of H-MMC Behavior Coordinated With a CB

After developing the analytical model to derive the voltage and current waveforms of an H-MMC in the blocking state, it is further used to analyze the coordinated operation of H-MMCs and CBs under various scenarios and parameter variations. This analysis evaluates the impact on maximum voltage stress in FB-SMs, peak fault current in MMC arms and the CB branch, and maximum energy stress on MOVs across different H-MMC configurations and CB interruption times.

First, the impact of SM capacitance on the maximum voltage stress of FB-SMs is investigated for a given interruption time. Using the analytical model, the maximum voltage stress for different configurations is calculated and presented through multiple plots in Fig. 8. It is observed that as the FB-SM ratio in H-MMCs increases, the voltage stress on FB-SMs decreases. Additionally, for an H-MMC with a given FB-SM ratio, increasing the SM capacitance further reduces the voltage stress on FB-SMs. These plots help determine the appropriate size of FB-SM capacitors in an H-MMC designed for coordinated operation with CBs. Further details on SM capacitance determination are in Appendix.

The second investigation examines the impact of dc reactor size on the operation of the H-MMC and CB during an SC fault. The maximum fault currents in MMC arms and the CB branch are derived using the analytical model and presented for different

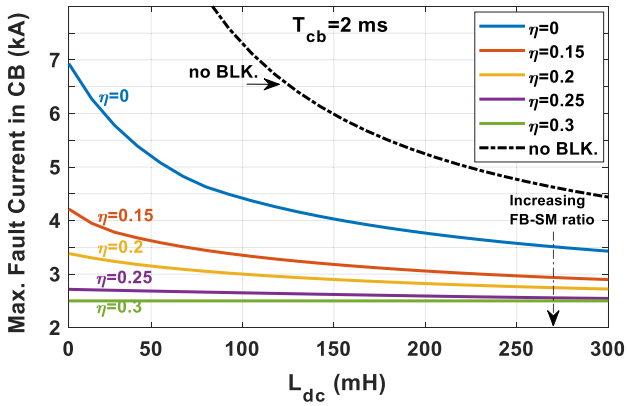

Fig. 10. Maximum fault current through the CB versus DC inductor.

configurations of the H-MMC in Figs. 9 and 10, respectively. Additionally, the plots representing the nonblocking state of the MMC (or dedicated DCCB protection) are shown in dashed lines in these figures. From these plots, the following conclusions can be drawn.

1) For an FB-SM ratio below 0.25 with blocking applied, the maximum fault current in the MMC arms is equal to that in the CB. However, in nonblocking mode, the maximum fault current in the CB is nearly three times the maximum arm current.
2) As the FB-SM ratio increases, the maximum fault current decreases, particularly at low L_{dc} values.
3) At $\eta = 0.25$ (or higher), the maximum fault current in the CB path remains close to the trip level I_{trip} regardless of the L_{dc} value, which is significantly different from the nonblocking mode.
4) Under coordinated MMC protection, the maximum fault current in the CB path is significantly lower than in nonblocking mode, allowing dc systems to be designed with lower L_{dc}, reducing cost and footprint.

Based on the above observations, one can conclude that when coordinated operation between the H-MMC and CB is applied, and the FB-SM ratio is 0.2 or higher, sizing L_{dc} to limit the

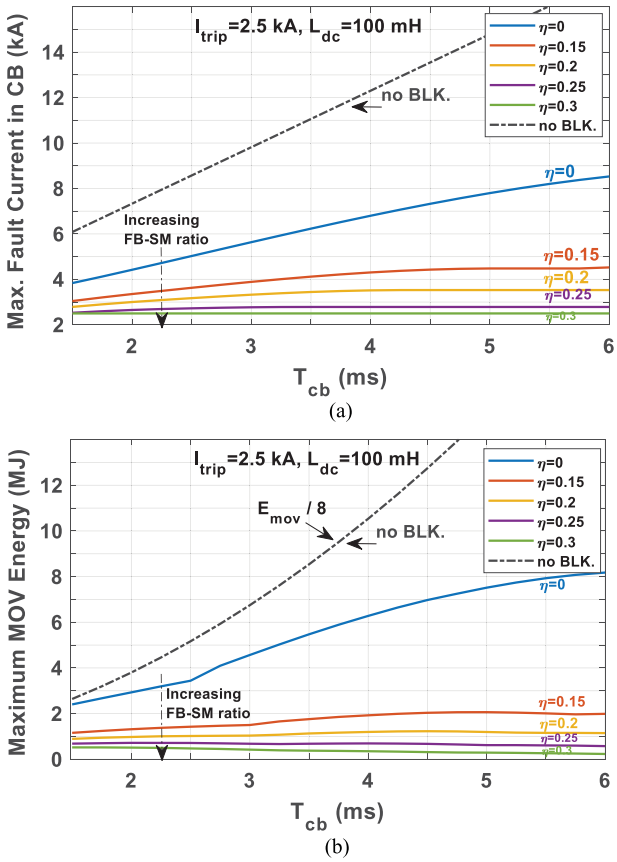

Fig. 11. Effect of CB interruption time on (a) maximum fault current and (b) maximum MOV energy at different FB-SM ratios during coordinated and dedicated DCCB protection (dashed line).

peak fault current—whether in the CB or MMC arms—becomes significantly easier (or more relaxed) compared to approaches that rely on dedicated DCCB protection without MMC blocking. In the latter, large dc reactors are required to reduce the fault current slope and keep CBs within their safe operating area until the MOVs are inserted into the dc lines.

Fig. 11 shows the relationship between CB interruption time, maximum fault current through the CB, and maximum energy stress on the MOVs under different H-MMC configurations. Additionally, the plots for the nonblocking state (or dedicated DCCB protection) are shown in dashed lines.

According to the plots in Fig. 11, an H-MMC with a CB demonstrates reliable performance across a wide range of CB interruption times, particularly when $0.2 \leq \eta$ and MMC blocking is applied. In this scenario, both the maximum fault current and the energy dissipated by the MOVs remain nearly constant and unaffected by CB interruption time— unlike in the conventional DCCB-based fault current interruption approach, as shown by dashed lines in Fig. 11(a) and (b).

For example, in an H-MMC with an FB-SM ratio of 0.2, the maximum fault current remains below 3.6 kA, and the energy stress on the MOVs stays under 1.2 MJ, regardless of the CB interruption time. In contrast, in DCCB-based protection, even with a fast CB with an interruption time of 2 ms, these values rise to 7.4 kA and 30 MJ—2.1 and 25 times higher than in the former case, respectively. This confirms the efficacy of the coordinated operation of H-MMCs with CBs.

In the next investigation, a new index is introduced to compare the required semiconductor—or indirectly, the cost of semiconductors—based on the maximum current and voltage stress in both the H-MMC and the main breaker branch of the CB. This index, termed SRI, is defined as follows:

$$\begin{aligned}\mathrm{SRI} = (12(1-\eta) + 24\eta \cdot \max\left(\frac{V_{\mathrm{FB,max}}}{V_{\mathrm{FB,per}}}, 1\right) \\ \times \max\left(\frac{I_{\mathrm{arm,max}}}{I_{\mathrm{CP,MMC}}}, 1\right) + \left(2 \cdot \frac{V_{\mathrm{mov}}}{V_{dn}}\right) \\ \times \max\left(\frac{I_{\mathrm{CB,max}}}{I_{\mathrm{CP,CB}}}, 1\right)\end{aligned} \tag{52}$$

where $V_{\mathrm{FB,max}}$ represents the maximum voltage stress on FB-SMs, $I_{\mathrm{arm,max}}$ denotes the maximum fault current in MMC arms, and $I_{\mathrm{CB,max}}$ is the maximum fault current in the CB, all derived using the proposed analytical model. Additionally, $V_{\mathrm{FB,per}}$ indicates the permitted maximum voltage on a power switch, whereas $I_{\mathrm{CP,MMC}}$ and $I_{\mathrm{CP,CB}}$ represent the maximum pulsed collector current in the IGBTs of the MMC and CB, respectively.

The first term in (52) accounts for the switch requirement for HB-SMs, the second for FB-SMs, and the third for the main breaker in the H-CB, all normalized to N. This index depends on the selected trip current level $I_{\mathrm{trip},}$ and the power switch ratings in the MMC and CB.

A comparison can now be made between different configurations of H-MMCs and CBs from the perspective of switch requirements, as shown in Fig. 12(a), assuming, for example, $I_{\mathrm{CP,MMC}}$ and $I_{\mathrm{CP,CB}}$ are 2.4 kA, $V_{\mathrm{FB,per}}$ is 2.6 kV, and V_{MOV} is 496 kV for the simulation case study.

Additionally, for a fair comparison, the H-MMC losses during normal operation are derived as a function of the FB-SM ratio in Fig. 12(b). The conduction loss has been normalized to that of an HB-MMC for ease of interpretation.

Based on the plots in Fig. 12(a) and (b), the following observations are made.

1) For H-MMCs with an FB-SM ratio equal to or greater than 0.4, SRI remains independent of CB interruption time.
2) For FB-SM ratios equal to or lower than 0.2, SRI increases significantly as CB interruption time increases.
3) SRI reaches a minimum value for the coordinated operation of H-MMCs and CBs at an FB-SM ratio between 0.2 and 0.3. (The observed minimum in Fig. 12(a) shifts slightly left when higher values for $I_{\mathrm{CP,MMC}}$ and $I_{\mathrm{CP,CB}}$ in (52) are chosen.)
4) Conduction losses during normal operation increase almost linearly with the FB-SM ratio.

Therefore, to limit conduction losses during MMC operation while still benefiting from lower switch requirements, reduced peak current, and lower MOV energy demands, an FB-SM ratio between 0.2 and 0.25 is a reasonable choice. For such an H-MMC, conduction loss can be up to 20% lower than that of typical H-MMCs.

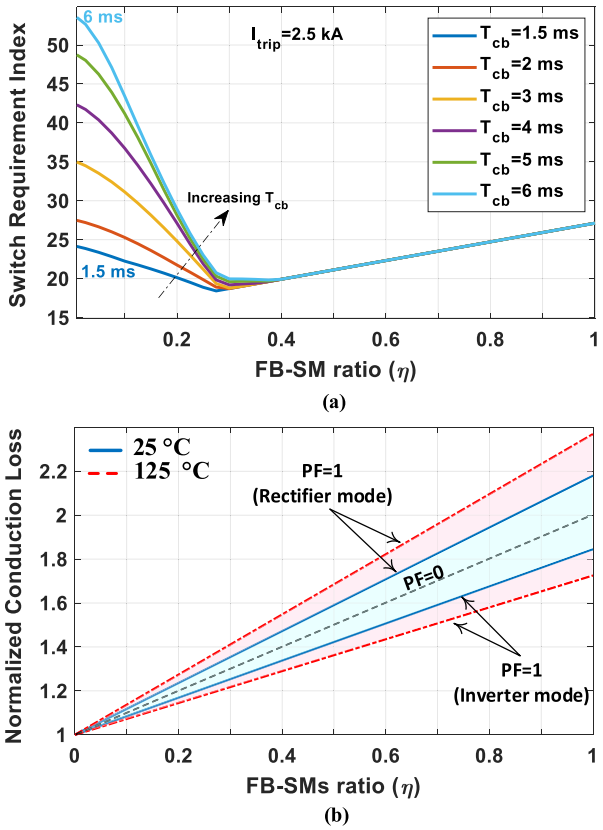

Fig. 12. Effect of the FB-SM ratio on (a) Switch Requirement Index of an H-MMC coordinated with a CB and (b) conduction loss of the H-MMC during normal operation, based on the VI characteristics of the power switch 5SNA1200G330100.

The observations in Section V demonstrate that the MMC-coordinated protection approach reduces peak fault currents, enabling the use of lower-rated IGBTs, smaller dc reactors, and reduced MOV requirements, thereby lowering overall system costs. However, this approach introduces slightly higher conduction losses due to FB-SMs and requires temporary MMC blocking during faults.

Conversely, conventional DCCB-based protection allows continuous MMC operation but leads to higher peak fault currents, necessitating larger dc reactors, higher-rated switches, and increased MOV energy dissipation. While it eliminates the additional conduction losses associated with FB-SMs, it comes at the cost of greater component stress, higher equipment ratings, and increased system costs.

Overall, the choice between these two strategies depends on system design priorities, but MMC-coordinated protection offers a promising balance between cost, reliability, and performance in HVdc applications.

VI. Experimental Verification

To verify the coordinated operation between the H-MMC and the CB in practice, scaled-down versions of both the MMC and CB were implemented in the laboratory. Fig. 13 shows a photo of the setup, and the parameters of the test system are listed in Table I.

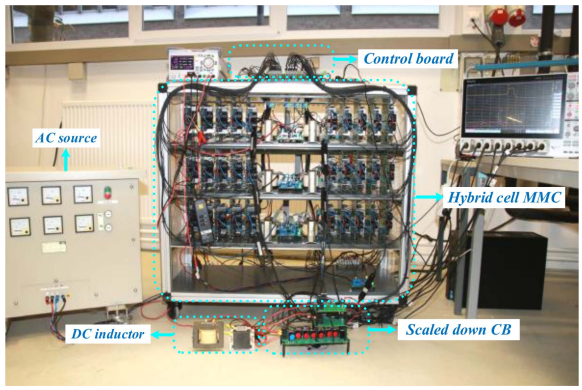

Fig. 13. Photo of the experimental setup and test environment.

The MMC prototype consists of five SMs per arm, each configurable as either an HB-SM or an FB-SM. The FB-SM ratio is manually adjusted before each experiment by selecting the appropriate number of FB-SMs and HB-SMs per arm. For example, to achieve a 20% FB-SM ratio, one FB-SM and four HB-SMs are preconfigured in each arm.

The MMC prototype operates in rectifier mode, connected to an autotransformer on the ac side and controlled in a closed-loop manner to regulate the ac-side current while maintaining a constant dc-side voltage. On the dc side, a 10 mH inductor models the dc reactor, accompanied by a scaled-down CB and a resistive load representing the remaining dc system.

The H-MMC control system utilizes a Zynq-7020 module, integrating an FPGA core and a dual-core ARM processor. The FPGA handles fixed control functions such as PWM generation and ADC, whereas the ARM processor manages MMC and CB control as well as dc fault initiation. To create dc faults, an SC path parallel to the load is activated via an electronic switch, with the Zynq board triggering its turn-on command at a predetermined phase angle. This setup ensures consistent fault initiation and enables a comparative analysis of different H-MMC configurations under similar fault scenarios.

The first experiment verifies the coordinated operation between the H-MMC with a 20% FB-SM ratio and a CB with $T_{cb} = 2$ ms. Following a dc SC fault, the current rises sharply, and upon reaching the trip level ($I_{\text{trip}} = 2.5$ p.u., i.e., 12.5 A), the coordinated fault current interruption process begins.

The corresponding key waveforms—including dc-side current, the voltage of the FB-SM with the highest increase ($V_{\text{FB,au}}$), and all six arm currents—are captured and presented in Fig. 14.

As observed, the maximum fault current at the dc side (or CB branch) reaches 2.6 times its nominal value, the FB-SM voltage increases by 55%, and the maximum arm current rises to 2.4 times its peak value in normal operation. It is also worth mentioning that a larger capacitor size was not selected for the FB-SM capacitors in the low-voltage setup, as the power switches and capacitors have a higher voltage margin compared to a real high-voltage system.

To validate the accuracy of the analytical model in the low-voltage design, analytical results are extracted for the experimental system using the parameters in Table I and compared

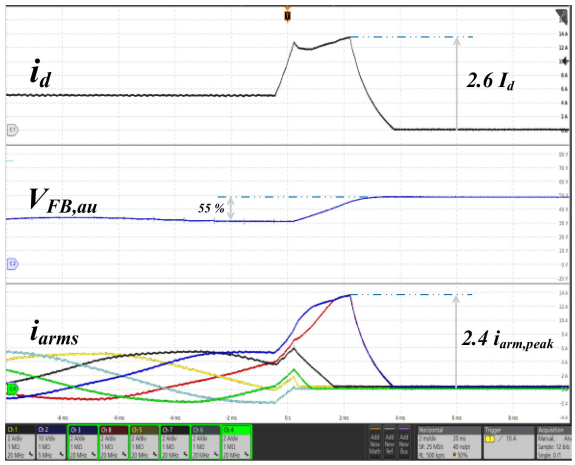

Fig. 14. Key experimental waveforms during fault current interruption in an H-MMC with $\eta = 0.2$ and a CB with $T_{cb} = 2$ ms.

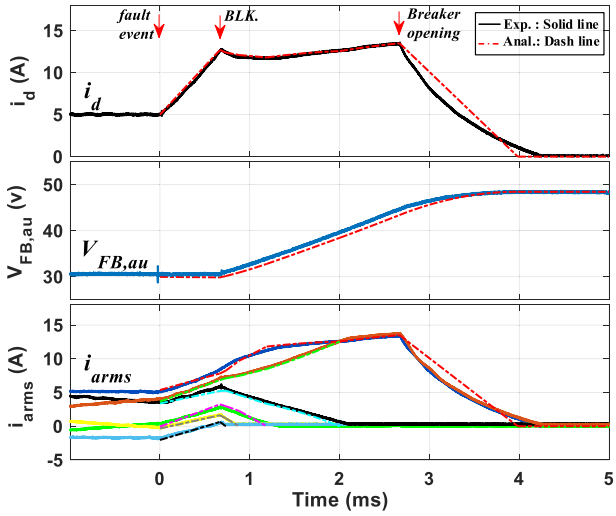

Fig. 15. Comparison of experimental results with the proposed analytical model during an SC fault condition at $T_{cb} = 2$ ms and $\theta_{an}(t_0) = 93°$(data from the analytical model is shown with dashed lines).

with experimental test data in Fig. 15. Solid lines represent the experimental results (same data as Fig. 14, but zoomed in), while dashed lines correspond to the analytical model waveforms. The fault instant is defined as $t = 0$, with analytical model data generated immediately afterward.

The comparison between the experimental results and the analytical model data in Fig. 15 demonstrates a good agreement, validating the proposed model even for low-voltage systems. The most significant deviation occurs during MOV insertion, as the analytical model assumes a constant dc voltage source for MOVs, whereas, in reality, their equivalent voltage exhibits slight variations depending on the flowing current. However, since this variation has no impact on the estimated maximum current and voltage stress in the CB and MMC elements, it can be neglected.

In the next experiment, the dc fault scenario was repeated for six different configurations of H-MMC, i.e., $\eta = 0$, 0.2, 0.4, 0.6, and 1, under the same fault conditions as in the first experiment.

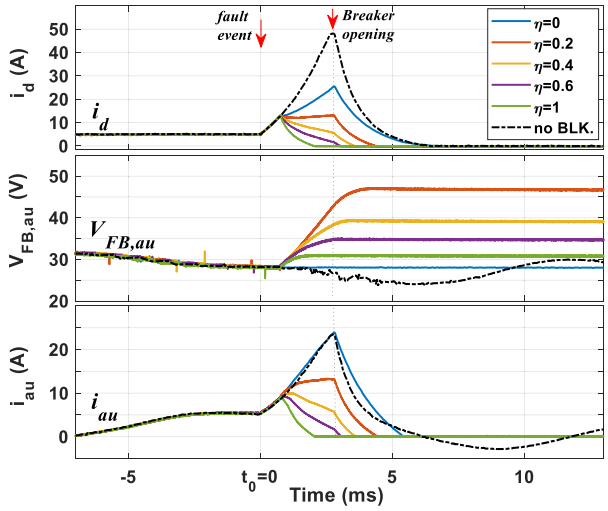

Fig. 16. Fault current interruption with various approaches at $T_{cb} = 2$ ms and $\theta_{an}(t_0) = 93°$: HB-MMC ($\eta = 0$), hybrid MMCs ($\eta = 0.2$, 0.4, 0.6), FB-MMC ($\eta = 1$), and MMC with no blocking (dashed line).

The data from all these fault scenarios were separately collected and then presented together in Fig. 16 to facilitate a comparative analysis of their behavior under similar SC fault conditions. Additionally, the phase-a angle at the fault instant was set to $\theta_{an}(t_0) = 93°$.

The results show that in H-MMCs with $\eta \geq 0.2$, the maximum fault current is at least 50% lower than in the HB-MMC, regardless of whether the HB-MMC is blocked or remains operational at the fault instant. Additionally, the peak current on the dc side is reduced by 50% and 75%, respectively, significantly lowering energy loss in the MOVs. However, the overvoltage on the FB-SMs increases as the FB-SM ratio decreases in the H-MMC configuration. This issue can be mitigated by increasing FB-SM capacitance, bypassing FB-SMs when a critical limit is reached, or implementing the energy absorption branch proposed in [23].

VII. Conclusion

In this article, an analytical model was first presented to analyze the behavior of an H-MMC with an arbitrary FB-SM ratio per arm, coordinated with a DCCB, during a pole-to-pole SC fault. The model applies to any FB-SM ratio from zero to one and considers CB interruption time as a flexible parameter. It accounts for all states of the H-MMC during blocking, including ACD and gradual commutation in MMC arms, which have been neglected in previous studies. Therefore, unlike previous analytical methods, which exhibited significant errors in estimating voltage and current stresses under an SC fault, the proposed model showed good agreement with EMT simulations.

In addition, the coordinated operation of H-MMCs with CBs was investigated, highlighting the impact of the FB-SM ratio and CB interruption time on the fault-clearing process and element stresses. For example, in an MMC-coordinated protection scheme with $\eta = 0.2$ and a slow CB, the maximum fault current and energy stress were 51% and 96% lower, respectively, than those in a fast dedicated DCCB protection with $T_{cb} = 2$ ms.

In brief, this study suggests that coordinated protection using H-MMCs with an optimal FB-SM ratio and CBs provides a balanced tradeoff between fault current limitation, cost efficiency, and overall system performance, making it a promising approach for enhancing HVdc grid protection strategies.

APPENDIX
PARAMETER SELECTION METHODOLOGY FOR H-MMC

The methodology for selecting the main parameters of the H-MMC and dc inductance in a P2P configuration is explained below. The case study is conducted for the simulation scenario presented in Table I.

1) Arm Capacitance Selection

First, the MMC arm capacitance C_{arm} is determined using the following equation [24]:

$$C_{\text{arm}} = \frac{C_{\text{SM}}}{N} = \frac{\text{EP} \cdot S_n}{3{V_{dn}}^2} \tag{53}$$

where S_n is the nominal apparent power of the MMC, and the energy-to-power ratio (EP) is typically selected within a range of 20–50 kJ/MVA [25]. Setting an initial value of 40 kJ/MVA leads to an initial arm capacitance of 42 μF and an SM capacitance of 6.7 mF.

2) Arm Inductance Selection

The arm inductance (L_a) is selected to prevent resonance with arm capacitance, caused by harmonics in the sum of upper and lower arm voltages [26]. According to the research in [24] and [26], the resonant inductance L_{a_res} at the hth harmonic, given modulation index m and frequency ω, is determined by

$$L_{a\_\text{res}} = \frac{1}{C_{\text{arm}}\omega^2} \frac{2(h^2-1)+m^2h^2}{8h^2(h^2-1)}. \tag{54}$$

To avoid resonance at even integer harmonics, L_a is selected within the range $1.4L_{a\_\text{res}}$ to $2.4L_{a\_\text{res}}$, where the lower limit ensures that the arm inductance remains above the second harmonic resonance curve [24], and the upper limit satisfies the condition suggested in [27]. In the simulation case study, the critical arm inductance is derived as $L_{a\_\text{res}} = 25$ mH, resulting in an initial selection range of 35–60 mH for L_a.

3) FB-SM Capacitance Adjustment

In H-MMCs, larger SM capacitors help in limiting FB-SM overvoltage during fault clearing. The required capacitance depends on the FB-SM ratio (η) and CB interruption delay (T_{cb}). A lower η or longer T_{cb} necessitates a higher capacitance. Based on the allowable FB-SM overvoltage for a given η and T_{cb}, the FB-SM capacitor size is determined accordingly.

For example, in an H-MMC with an initial SM capacitance of 6.7 mF, $\eta = 0.2$, $T_{cb} = 2$ ms, and $L_a = 35$ mH, the overvoltage reaches 52%, as shown in Fig. 8. To reduce it below 30%, the FB-SM capacitance needs to be increased to 12 mF. Rather than increasing all SM capacitances in the H-MMC, a selective increase in FB-SM capacitance (C_{fb}) is applied. The feasibility of using different capacitance values for HB-SMs and FB-SMs has been examined in [28]. The equivalent arm capacitance is then modified accordingly, as

$$C_{\text{arm}} = \frac{\frac{C_{hb}}{(N-N_f)} \times \frac{C_{fb}}{N_f}}{\frac{C_{hb}}{(N-N_f)} + \frac{C_{fb}}{n_f}} = \beta \frac{C_{\text{SM}}}{N}, \quad \beta = \frac{\frac{C_{fb}}{C_{hb}}}{(\eta + (1-\eta)\frac{C_{fb}}{C_{hb}})}. \tag{55}$$

In this approach, $C_{hb} = C_{\text{SM}}$ is determined from (53), whereas C_{fb} is selected based on Fig. 8. The scaling factor (β) represents the increase in arm capacitance after updating the FB-SM capacitance. For instance, when the FB-SM capacitance is set to 12 mF, the equivalent arm capacitance increases by 10%. Consequently, with this updated arm capacitance, the L_a range is recalculated using (54), resulting in a new range of 32–54 mH.

4) Optimization of L_a and L_{dc}

An optimization procedure can be applied to determine the optimal L_a and L_{dc} for the H-MMC coordinated with a CB in a P2P system. For example, in the simulation case study, the objective is to minimize L_a for each L_{dc} while satisfying the following constraints:

1) maximum fault current remains below 3 kA
2) FB-SM voltage stays within 1.3 p.u.

Additionally, the cost and mass of air-core inductors can be considered in the selection process, as referenced in [29]. Based on these criteria, the final optimized values are determined as $L_a = 43$ mH and $L_{\text{dc}} = 100$ mH, ensuring reliable system operation under dc faults while satisfying the given constraints and minimizing the mass of the inductors.

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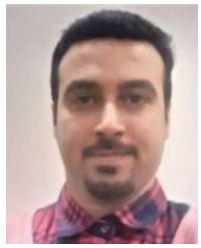

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