An Ultra-High-Speed LED Array Driver Circuit for Structured Illumination

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***Abstract*—Structured light devices are commonly used in many measurements by emitting certain illuminating patterns on objects or scenes, enabling the acquisition of object information. To achieve high-speed and high-accuracy measurements, researchers are focusing on improving the performance of structured light devices. LEDs, with their fast response times, have great potential in high-speed structured light devices. However, the current LED array driver circuits face challenges to balance high power and high speed. In this article, we propose a driver circuit and a pattern display scheme that support high-power LED arrays to refresh structured light patterns at ultra-high rates. We have fabricated a prototype of the driver and used it to drive a 128 × 128 LED chip array. Experimental results demonstrate that the proposed driver outputs over 40 W and supports the LED chip array refresh patterns at rates of up to 25 MHz, which is approximately 1000 times faster than the fastest commercially available structured light device (i.e., the digital micromirror device). The ultra-high-speed LED array device based on the proposed driver can be applied in computational ghost imaging, structured illumination microscopy, Fourier ptychographic imaging and other imaging fields.**

***Index Terms*—Driver, imaging, LED array, structured light device, ultra-high-speed.**

I. Introduction

STRUCTURED light devices are widely used in computational ghost imaging [1], [2], structured illumination microscopy [3], [4], Fourier ptychographic imaging [5], [6], and other imaging fields [7], [8]. As the core components of these imaging systems, structured light devices directly influence the performance of imaging systems. Developing an ultra-high-speed structured light device to enable faster acquisition of object information has been a key research focus in the field of imaging. Currently, commercially available structured light devices such as LCDs [9], LCoSs [10], and digital micromirror devices (DMDs) [11], [12] have clear advantages in terms of resolution and pixel pitch, but their refresh rates remain relatively low. Although DMDs are the fastest commercially available structured light device at present, their maximum refresh rate is only 22 kHz.

LEDs have advantages such as high brightness, high luminous efficiency, long lifetime, and fast response speeds, ranging from tens of MHz to several GHz [13], [14], [15]. As a result, LED arrays have great potential to become the next generation of ultra-high-speed structured light devices [16], traditional LED display is a typical kind of passive matrix LED array device, its driver circuit is mainly composed of a shift register and constant current sources. LED displays typically have a maximum refresh rate of only 60 or 120 Hz, which is close to the resolution limit of the human eye. To achieve a fast refresh rate of structured light patterns, many researchers have dedicated efforts to developing ultra-high-speed LED array devices. Eva et al. [17] developed a 32 × 32 LED array device with a 10-kHz refresh rate for structured light projection. Zhao et al. [18] developed an 8 × 8 LED array device operating at a 100-MHz refresh rate. Neither of these two works have disclosed the design details of the driver. Recently, Johnstone et al. [19] demonstrated a 128 × 128 Micro-LED array capable of displaying patterns at 500 kHz. This Micro-LED array device based on CMOS technology is actively addressed, and each micro-led anode has an individual pixel driver [20]. However, the existing ultra-high-speed LED array devices still face challenges to balance high resolution and high speed.

The primary reason for the low refresh rate of traditional LED displays is that they typically employ a row-scanning display scheme, where rows or columns of the LED array are activated sequentially to display one image. As a result, the refresh rate of LED displays is much lower than the response speed of the LED chips. Clearly, the line-scanning display scheme is not suitable for the development of ultra-fast structured light devices. Theoretically, structured light patterns can be refreshed within the time of displaying one pattern by activating all rows and columns of the LED array [21]. This display scheme can achieve a refresh rate close to the response speed of the LED chips.

To simultaneously activate and drive all rows and columns of the LED array, a new driver circuit that is different from the existing LED array drivers is needed. Our previous work has achieved a preliminary design of the driver [22], but it is only capable of

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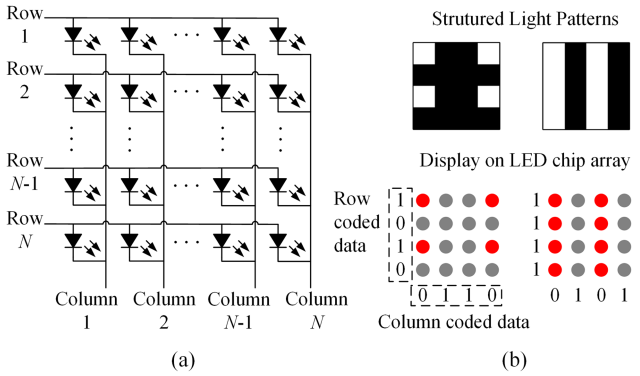

Fig. 1. (a) Schematic diagram of the $N \times N$ LED chip array. (b) Two examples of 4×4 structured light patterns and their display on the LED chip array.

supporting the refresh of patterns for a 32×32 resolution LED array. When the resolution of LED array increases, the critical challenge for the driver is insufficient power during high-speed operation. On the one hand, it is difficult for the driving units to achieve both high-power output and high-speed switching. On the other hand, during high-speed operation of the driver, the issue of insufficient output power caused by the dynamic load response of the power source needs to be addressed. In this article, we proposed a driving scheme based on MOSFET gate driver chips and push-pull MOSFETs, along with a pattern display scheme that suppresses power source dynamic responses. A prototype of the proposed LED array driver was fabricated and tested to validate the feasibility of the proposed solution. The results demonstrate that the LED driver can deliver over 40 W of output power and support the display of a series of structured light patterns on the LED chip array at a refresh rate ranging from 10 to 25 MHz.

II. Operation Principle of Proposed LED Array Driver

A. Basic Display Scheme

As shown in Fig. 1(a), the arrangement and connection of the LED chip array is the same as that of the passive matrix LED array [23]. The positive electrode of each row of LED chips is connected by the same signal line and driven by a row driving signal, and the negative electrode of each column of LED chips is connected by the same signal line and driven by a column driving signal. When the row signal is in a high logic state and the column signal is in a low logic state, the LED chip at the intersection of the row and column lights up.

Fig. 1(b) shows two examples of 4×4 ($N = 4$) structured light patterns and their display on the LED chip array. Each white block of the structured light patterns indicates that this LED pixel needs to be lit, and its value is set to 1. Each black block indicates that this LED pixel needs to be extinguished, and its value needs to be set to 0. The coded data for the rows and columns correspond to the logic levels on the row and column signal lines during pattern display. By activating all the rows and columns using the coded data, the structured light patterns can be displayed directly. Furthermore, each structured light pattern

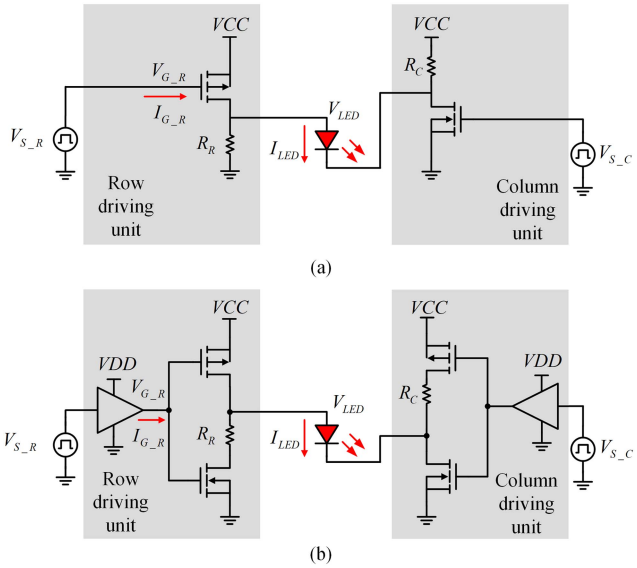

Fig. 2. (a) Schematic diagram of the driving units in the previous work and (b) the proposed driving units.

$P_m(m = 1, 2, 3, \ldots)$ with $N \times N$ resolution can be displayed in a single refresh period without changing the logical state of signals, which is N times faster than using line-scanning display scheme. Notably, due to the structure of the LED chip array, the structured light patterns that can be displayed by the LED chip array typically have a certain symmetry. The o th row with lit LEDs and the p th row with lit LEDs in one pattern have the same values, which can be expressed as

$$P_m(o, 1:N) = P_m(p, 1:N). \tag{1}$$

B. Proposed Driving Unit Circuit Scheme

To implement the display scheme on hardware, each row and column of the array requires an independent driving signal source. The driving signals need to be high-parallelism, high-speed and high-power. FPGA excels at providing a large number of highly parallel electrical signals, with speeds reaching hundreds of MHz. However, the current it provides is only in the range of tens of milliamperes. Therefore, a driver consisting of driving units is designed to enhance the driving capability of these signals from the FPGA.

The designed driver consists of a large number of repetitive driving units. To simplify the description, we only use the 1×1 LED chip array with its driving units as an example. The schematic diagram of driving units in our previous work [22] is shown in Fig. 2(a). Each row driving unit consists of a PMOSFET and a pull-down resistor R_R, and each column driving unit consists of an NMOSFET and a pull-up resistor R_C. However, this scheme can only drive low-resolution LED arrays. As the resolution of the LED array increases, MOSFETs capable of handling higher currents must be used, but these MOSFETs have large parasitic capacitance. The low instantaneous current I_{G_R} provided by the control signal source results in slow charging of large parasitic capacitance of MOSFET, which significantly reduces the switching speed of the MOSFET and

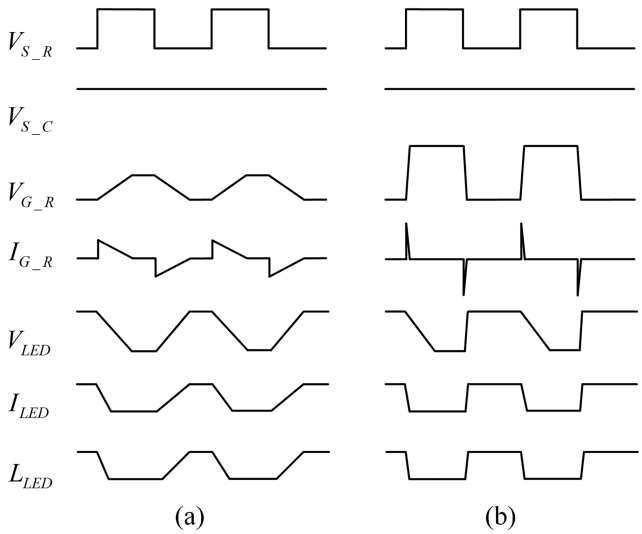

Fig. 3. Waveform diagram of (a) the driving units in the previous work and (b) the proposed driving units.

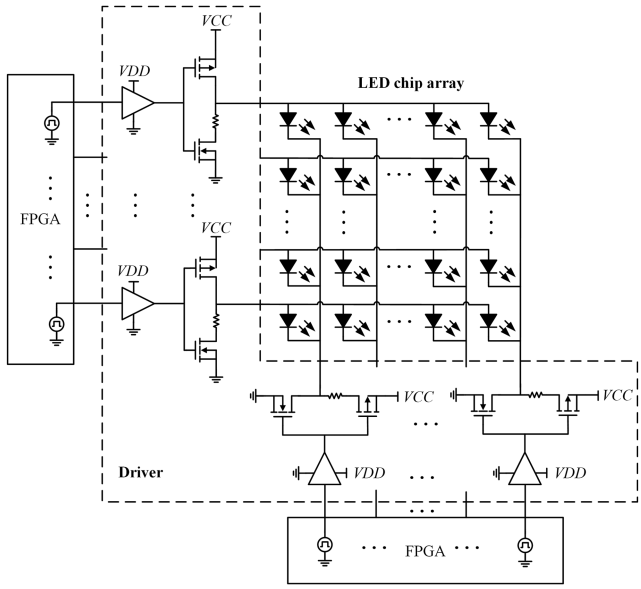

Fig. 4. Full schematic diagram of the proposed driver scheme.

ultimately leads to insufficient output power from the driver. To address this problem, we propose a driving unit scheme as shown in Fig. 2(b). In the row and column driving units, the MOSFET gate driver [24] is powered by an external power source *VDD* and used to deliver high current pulses to the common gate of the high-power push-pull MOSFET, enabling them to achieve fast switching speeds. The push-pull MOSFETs are structured with an upper PMOSFET and a lower NMOSFET, allowing the driver circuit to achieve low power consumption. In addition, the resistors R_R and R_C are reserved compared to Fig. 3(a) to avoid the damage of MOSFETs when both MOSFETs are on simultaneously in row or column driving unit. It is worth noting that when the state of the LED chip is OFF to ON, there is no resistance on the current path, which ensures that the LED chip can be lit fast, and the power consumption provided by the power source is almost entirely on the LED.

Fig. 3(a) and (b) shows the waveform diagrams of the driving unit scheme of Fig. 2(a) and (b). After using the proposed driving unit scheme, the peak instantaneous gate current I_{G_R} is significantly enhanced. Therefore, the gate voltage V_{G_R} stabilizes quickly, enabling faster switching of the MOSFETs. Due to the high-speed switching of MOSFETs, the rising edge of the LED voltage V_{LED} and current I_{LED} is sharp, causing the LED light intensity L_{LED} to stabilize quickly. The resistance affects the falling edge of voltage, but the light intensity of the LED L_{LED} can still drop to 0 in a short time, as the LED will only light up when the voltage exceeds the threshold. It should be noted that the waveforms shown in Fig. 3(a) and (b) are captured when VCC is used as an ideal power source. Actual power supplies, however, have dynamic load response time and require further analysis.

C. Proposed Driver Circuit Scheme

As shown in Fig. 4, two FPGAs are used to output N row control signals and N column control signals, which are all highly parallel. The rated current of each control signal from FPGA is only tens of milliamps (mA). Each row control signal is connected to the input of a row driving unit, and the output of the row driving unit is connected to a row signal line in the LED chip array. Each column control signal is connected to the input of a column driving unit, and the output of the column driving unit is connected to a column signal line in the LED chip array. In the entire driver design, all MOSFET gate driver chips share the same external power source VDD, and all push-pull MOSFETs share the same external power source VCC.

The operating current of a small-pitch LED chip (chip size in microns) is generally 0–25 mA. For example, if the operating current of a single LED is set to 5 mA, each row or column driving unit needs to be capable of carrying at least $N \times 5$ mA of current. For the entire driver, the demand for driving current is substantial, reaching up to $N \times N \times 5$ mA. When $N = 128$, the current provided by the driver can reach tens of amps.

D. Dynamic Load Response Suppression

A practical linear dc voltage source is not an ideal power supply, and it possesses dynamic load response characteristics and limited regulated capabilities. When subjected to heavy load variations, the power supply requires considerable adjustment time, which can be up to several tens of microseconds. Therefore, suppression power supply's dynamic load response is crucial for achieving high-speed and high-quality light intensity.

To better describe this problem, $2 \times N$ LED chip array with its driving circuits is present as an example is shown in Fig. 5. Two row driving units drive two rows of LED chips, respectively. The negative electrodes of all LED chips are grounded. A practical voltage source VCC with dynamic load response can be equivalent to an ideal voltage source $\mathrm{VCC}_{\mathrm{ideal}}$ with a variable resistor R_{CC}. When the load of VCC changes, the value of R_{CC} changes. The greater the load changes, the longer the power

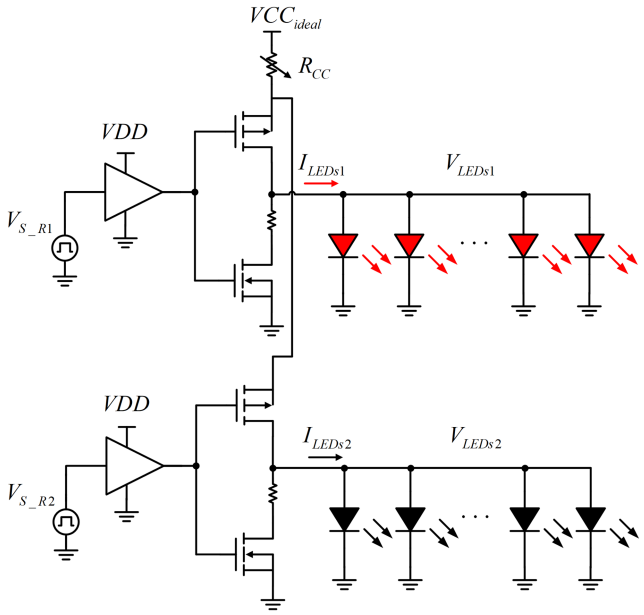

Fig. 5. Schematic diagram of $2 \times N$ LED chip array with the row driving units and the practical voltage source.

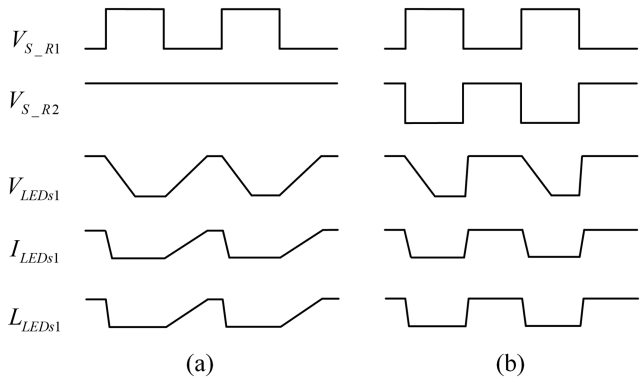

Fig. 6. Waveform diagram of the driving circuit with (a) changed load and (b) constant load.

supply adjustment time. Fig. 6(a) and (b) shows the waveform diagram of the driving circuit in Fig. 5 with changed load and constant load. When the control signal voltage V_{S_R1} for the first row driving unit is flipped at frequency f and the control signal voltage V_{S_R2} for the second row driving unit remains high, the LEDs in the first row are lit and extinguished at the same frequency with V_{S_R1}, which causes the load to change between 0 and N lit LEDs. Due to the dynamic response of VCC, the rising time of the voltage V_{LEDs1} and current I_{LEDs1} in the first row are both long as shown in Fig. 6(a). L_{LEDs1} is the total light intensity waveform of all the LEDs in the first row, which is proportional to I_{LEDs1}.

To suppress the influence brought by dynamic response of the voltage source on the driving signal, we propose a pattern display scheme for the simplified driving circuit. As shown in Fig. 6(b), when the control signal V_{S_R1} and V_{S_R2} alternately flip, the two rows of LED chips are alternately lit. Except for the short switching time when MOSFETs are switched at high speed,

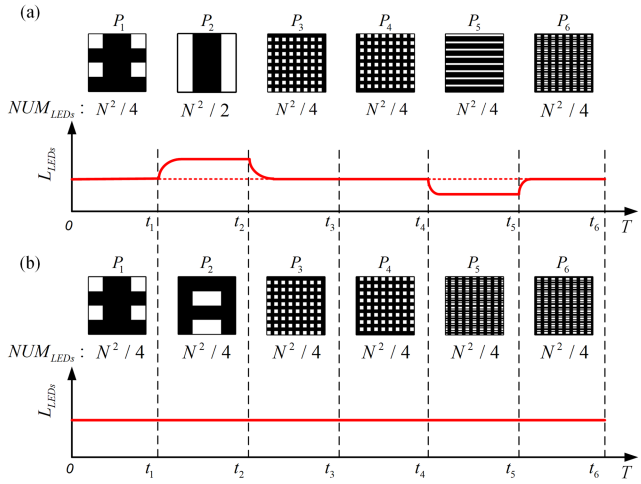

Fig. 7. (a) Patterns displaying with load change. (b) Patterns displaying without load change.

the load of VCC remains unchanged. Therefore, V_{LEDs1}, I_{LEDs1}, and L_{LEDs1} will not be affected by the dynamic load response of the power source and quickly reaches a stable value.

Similarly, when the pattern display scheme is applied to the array, load change should be avoided when the structured light patterns are displayed. Considering that the total driving current is proportional to the total light intensity of the LED chip array. Here, we present a method for measuring the total light intensity. When the $N \times N$ LED chip array displays a series of patterns $P_m(m = 1, 2, 3, \ldots)$ with $N \times N$ resolution, the total light intensity of the LED chip array is L_{LEDs}. L_m is the stable value of the total light intensity for P_m, which can be expressed as

$$L_m = \sum_{i=1}^{N} \left(\sum_{j=1}^{N} P_m(i, j) \right). \tag{2}$$

where i and j represent the pixel coordinates in the pattern P_m. NUM_{LEDs} is the total number of LEDs required to be lit for one pattern. Fig. 7(a) shows the light intensity change caused by load change, which includes two typical cases. First, $\text{NUM}_{\text{LEDs}} = N^2/2$ when the pattern P_2 is displayed, which is $N^2/4$ more than P_1 or P_3. Due to the limited regulated capability of the practical voltage source VCC, the increase in load leads to a decrease in the output voltage of the driver. As a nonlinear component sensitive to voltage values, small change in voltage will cause big change in the light intensity of the entire LED array. In addition, when the displayed pattern is switching from P_1 to P_2 or P_2 to P_3, there is a prolonged period of light intensity changes before reaching a stable value, caused by the dynamic load response of the voltage source VCC. Second, though the pattern P_5 has same total of $N^2/4$ lit LEDs as P_4 or P_6, the number of lit LEDs in one lit row is N for P_5, which is $N/2$ more thanP_4 or P_6. Due to the internal resistance of MOSFETs, this leads to a decrease in the overall load. Therefore, a decrease in overall light intensity of the LED array and a long-time light intensity fluctuation happens.

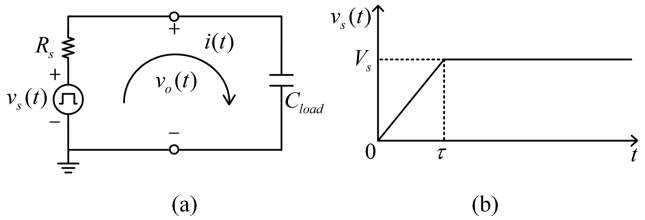

Fig. 8. (a) Simplified circuit model of capacitance charging. (b) Waveform diagram of the simplified circuit model.

To suppress the dynamic load response of the power source, a constant load must be achieved by restricting the patterns. We propose two rules for patterns as follows. Rule 1: Each pattern must light the same total number of LEDs. Rule 2: Each pattern must have the same number of LEDs lit in each lit row or lit column. As shown in Fig. 7(b), these patterns all meet our proposed pattern display rules, and their total light intensity remains constant. In computational ghost imaging, this solution is perfectly compatible due to the certain symmetric characteristic of Hadamard patterns [21]. However, it is noteworthy that there may be some minor tradeoffs in other different application fields. For example, in fringe projection-based 3-D measurement, it requires sequentially displaying binary fringe patterns to modulate the object. There may be cases where the number of lit LEDs slightly varies across different fringe patterns. To achieve a constant load, methods such as lighting additional LEDs and physical masking can be adopted.

III. Analysis and Simulation on Driving Unit Circuit

A. Analysis on Driving Unit Circuit

The switching process of the MOSFET is essentially the charging and discharging of internal parasitic capacitances by the signal source. A simplified circuit model of capacitance charging is shown in Fig. 8(a). The voltage of the signal source is $v_s(t)$. R_s is the internal resistance of the signal source, which determines the driving capacity of the signal source.

The rise edge of the ideal square wave signal is a step function, but the rise edge of the actual square wave signal source often has a certain slope, as shown in Fig. 8(b). The function of actual square wave signal can be expressed as

$$v_s(t) = \frac{V_s}{\tau}\left(t - (t-\tau)u(t-\tau)\right) \tag{3}$$

where τ is the rise time before signal stabilization, and V_s is the constant value after signal stabilization. And its Laplace transform is expressed as

$$\mathcal{L}(v_s(t)) = V_s(s) = \frac{V_s}{\tau}\left(\frac{1}{s^2} - \frac{1}{s^2}e^{-s\tau}\right). \tag{4}$$

The system transfer function in Fig. 8(a) is expressed as

$$H(s) = \frac{V_o(s)}{V_s(s)} = \frac{1}{C_{\text{load}}R_s s + 1}. \tag{5}$$

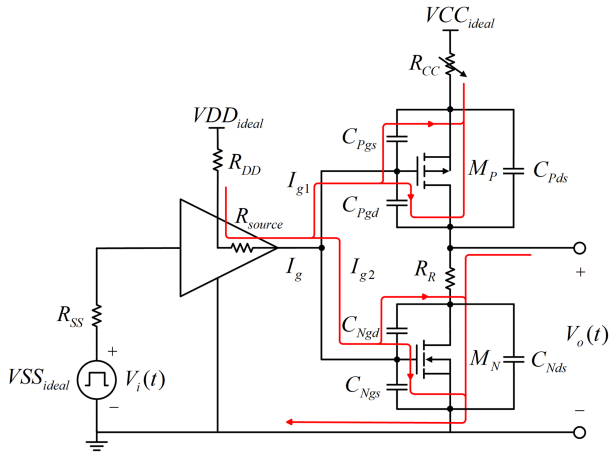

Fig. 9. Schematic diagram of the proposed driving unit with main parasitic capacitance and current flow when the upper PMOSFET is OFF and the lower NMOSFET is ON.

Therefore, the voltage $v_o(t)$ on the load capacitance can be calculated as

$$\begin{aligned} v_o(t) &= \mathcal{L}(V_o(s)) \\ &= \frac{V_s}{\tau}\left(t - C_{\text{load}}R_s u(t) + C_{\text{load}}R_s e^{-\frac{t}{C_{\text{load}}R_s}}\right)\ldots \\ &\quad - \frac{V_s}{\tau}\left(((t-\tau) - C_{\text{load}}R_s u(t-\tau)\right. \\ &\quad \left. + C_{\text{load}}R_s e^{-\frac{t-\tau}{C_{\text{load}}R_s}}\right)u(t-\tau)\Big). \end{aligned} \tag{6}$$

And the loop current $i(t)$ can be calculated as

$$\begin{aligned} i(t) &= C_{\text{load}}\frac{V_s}{\tau}\left(1 - e^{-\frac{t}{C_{\text{load}}R_s}}\right) \\ &\quad - C_{\text{load}}\frac{V_s}{\tau}\left(1 - e^{-\frac{t-\tau}{C_{\text{load}}R_s}}\right)u(t-\tau). \end{aligned} \tag{7}$$

According to (6) or (7), the charging time can be approximately calculated as

$$t_{\text{on}} \approx 4C_{\text{load}}R_s. \tag{8}$$

The discharging time can also be obtained by a similar calculation. It can be clearly seen from (8) that the internal resistance R_s of the driver determines charging time under a certain capacitive load. And when $t = \tau$, the instantaneous current reaches its maximum as

$$i_{\max} = i(\tau) = C_{\text{load}}\frac{V_s}{\tau}\left(1 - e^{-\frac{\tau}{C_{\text{load}}R_s}}\right). \tag{9}$$

The designed row driving unit circuit with main parasitic capacitances [25], [26] is shown in Fig. 9. The current flow when the upper PMOSFET M_P is OFF and the lower NMOSFET M_N is on is also illustrated as an example. When the simplified circuit model illustrated in Fig. 8 is applied to the design of the driving unit circuit illustrated in Fig. 9, the equivalent capacitive load C_{load} for this driving unit can be calculated as

$$C_{\text{load}} = C_{Pgs}//C_{Pgd}//C_{Ngs}//C_{Ngd}. \tag{10}$$

TABLE I
PARAMETERS OF THE DRIVING UNIT CIRCUIT

C_{Pgs}	90 pF
C_{Pgd}	10 pF
I_{P_D}	-0.8 A
C_{Ngs}	49 pF
C_{Ngd}	6 pF
I_{N_D}	0.8 A

where C_{Pgs} is the gate-source capacitance of M_P, $C_{Pgd}$is the gate-drain capacitance of M_P, C_{Ngs} is the gate-source capacitance of M_N, C_{Ngd} is the gate-drain capacitance of M_N. Moreover, the equivalent resistance $R_s = R_{\text{source}} \ll R_{SS}$, where R_{source} is the output internal resistance of the MOSFET gate driver, R_{SS} is the internal resistance of FPGA. According to (8), the MOSFET gate driver can greatly increase the switching speed of the two MOSFETs due to its low internal resistance and the ability to provide high instantaneous current.

Of course, the actual switching process is more complex than the simplified circuit model illustrated in Fig. 8. For instance, the Miller effect during the switching process increases the equivalent capacitance of the gate, and the parasitic capacitances of the MOSFET are voltage dependent [27]. However, the switching time of the MOSFET is still proportional to R_s and C_{load}.

B. Simulation on Driving Unit Circuit

To illustrate the effectiveness of the proposed driving unit circuit scheme, two PSPICE simulations are conducted to compare the two schemes mentioned in Section II-B. In the simulations, a row of 128 LEDs is driven by a row driving unit, with the negative electrodes grounded. The same PMOSFET is used in both simulations. In addition, the simulations do not consider the dynamic load response of the power supply. The parameters of the MOSFETs used in the simulations are listed in Table I, with their definitions provided in Section III-A.

Fig. 10 shows the simulation waveforms of the driving unit in the previous work. The voltage signal V_i from FPGA switches at a frequency is 2.5 MHz. Its amplitude is 3.3 V and its edge time is 2 ns. Due to the influence of the FPGA signal source's internal resistance RSS, both the rise time and fall time of the MOSFET gate voltage V_g are 118 ns. The peak current of the MOSFET gate I_g is only 0.024 A, which results in a long time required for charging and discharging the MOSFET's input capacitance. Due to the influence of the MOSFET gate voltage and current, the rise time of the output voltage V_o and output current I_o of the row driving unit is 105 ns. The fall time of the output voltage V_o is 76 ns, which is mainly decided by the R_R, and the fall time of I_o is 36 ns. The stable value of I_o is 450 mA, which is below the maximum drain current I_{P_D}. The first simulation results demonstrate that the driving unit based on the scheme in the previous work cannot achieve high-speed output. Fig. 11 shows the simulation waveforms of the proposed driving unit. The MOSFET gate driver provides a peak current I_o of up to 0.65 A to the common gate of the push-pull MOSFETs, reducing

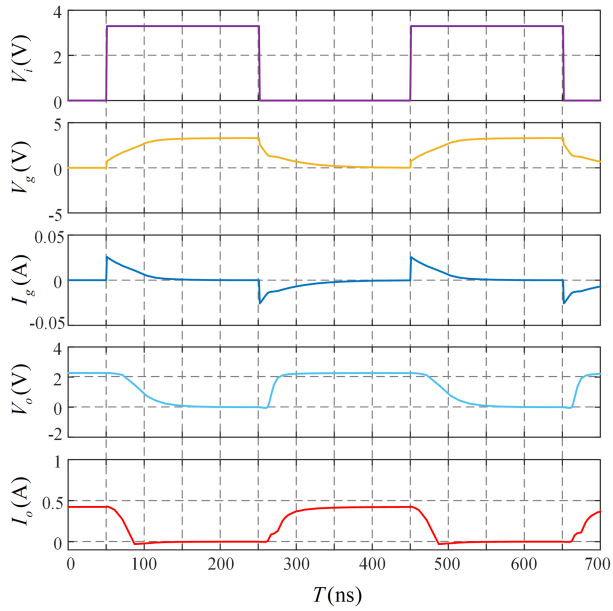

Fig. 10. Simulation waveforms of the driving unit in the previous work.

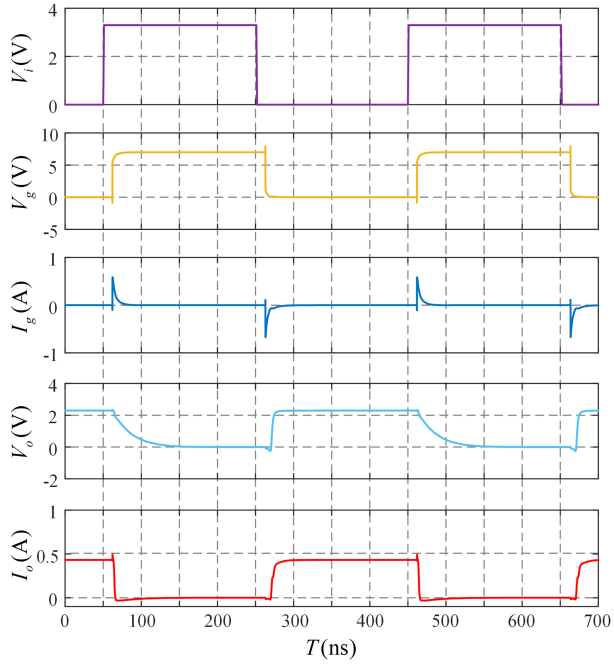

Fig. 11. Simulation waveforms of the proposed driving unit.

the edge time of V_g to 8 ns. The rise time of I_o is 10 ns, and the fall time is 3 ns. The second simulation results demonstrate that the proposed driving unit scheme can significantly reduce the edge time of V_o and I_o.

IV. PERFORMANCE EVALUATION OF PROPOSED LED ARRAY DRIVER

A. Design and Prototype of the LED Array Device

The full structure diagram of the $N \times N$ ultra-high-speed LED array device based on the proposed driver is as shown in

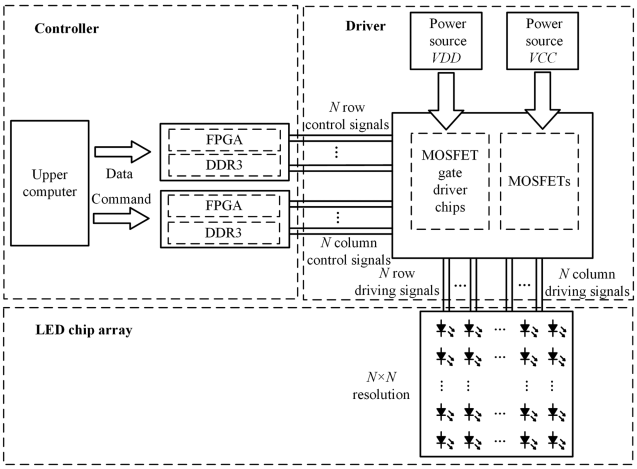

Fig. 12. Full structure diagram of the $N \times N$ LED array device based on the proposed driver.

Fig. 12, which also includes the controller and the LED chip array. The following is a brief description of the process from data storage to pattern refreshing. First, the upper computer sends a data transmission command and encoded pattern data to the proposed controller, which is composed of two FPGAs. The two FPGAs prestore the row and column encoding data into external DDR3 respectively. After receiving the display command from the upper computer, the two FPGAs begin to read their prestored data from external DDR3 and generate N row control signals and N column control signals respectively. Then, the driving capability of each control signal is enhanced by the proposed driving unit, which is composed of MOSFET gate driver chips with VDD supplying power and MOSFETs with VCC supplying power. Finally, the LED chip array displays patterns under control and driving of the signals from the driver.

The fabricated prototype of 128 $\times$ 128 LED array device based on our proposed driver is shown in Fig. 13. The response time of the used LEDs (ET-0201QRC, 620–630 nm, 0.65 mm $\times$ 0.35 mm, 25 mA) is 40 ns. In experimental tests, a single pixel detector (Thorlabs, PDA8A/M, Ø0.8 mm, 50 MHz) is used to detect light intensity, and a digital oscilloscope (PicoScope, 6404D, 2.5 GS/s, 500 MHz) with probes (PicoScope, TA133, 500 MHz) are used to sample electrical signals.

B. Experimental Results

To validate the simulation, we conducted comparative experiments mentioned in Section III-B. The measurement waveforms of the driving unit in the previous work are shown in Fig. 14, and the measurement waveforms of the proposed driving unit are shown in Fig. 15. V_i is the voltage waveform of the control signal generated by the FPGA and its frequency is 2.5 MHz. V_g is the voltage waveform of the MOSFET gate V_o is the output voltage and V_L is the voltage measured by the single pixel detector after converting the captured light signal of a LED into an electrical signal. Compared to previous solutions, the proposed driving scheme significantly reduces the switching time of V_g, decreasing it from 89 to 10 ns. This reduction leads

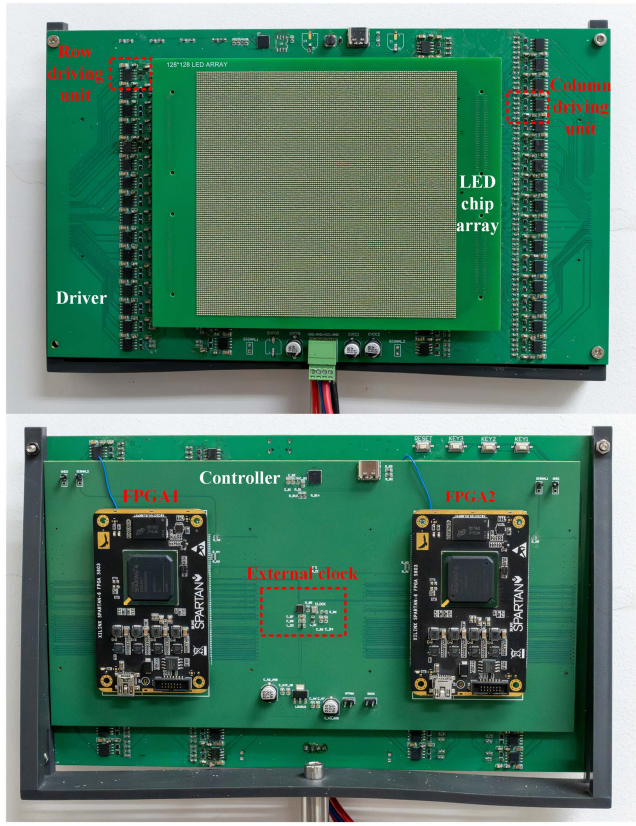

Fig. 13. Fabricated prototype of the LED device based on proposed driver.

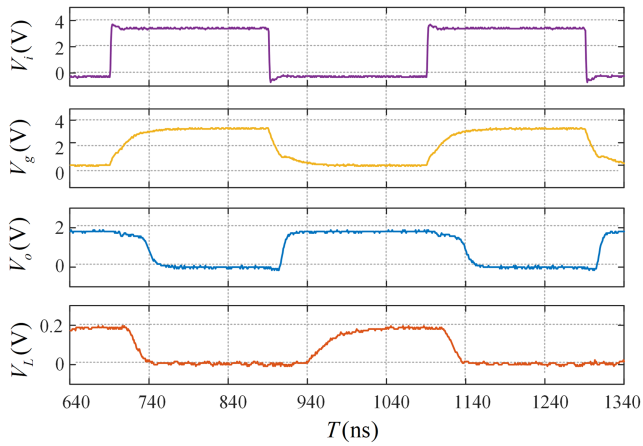

Fig. 14. Measurement waveforms of the driving unit in the previous work.

to a decrease in the rise time of V_L from 122 to 41 ns and the fall time of V_L from 45 to 25 ns. The experimental results indicate that the proposed solution enables the LED to switch ON and OFF more rapidly, allowing its light intensity to reach a steady state more quickly. Better gate driver chips would not enhance the transient performance of V_L. The experimental results agree with the simulation results, which substantiates the effectiveness of our proposed solution.

Furthermore, to demonstrate the performance of the driving circuit when a series of patterns are displayed on the 128 $\times$ 128 LED chip array, we measured the voltages of the

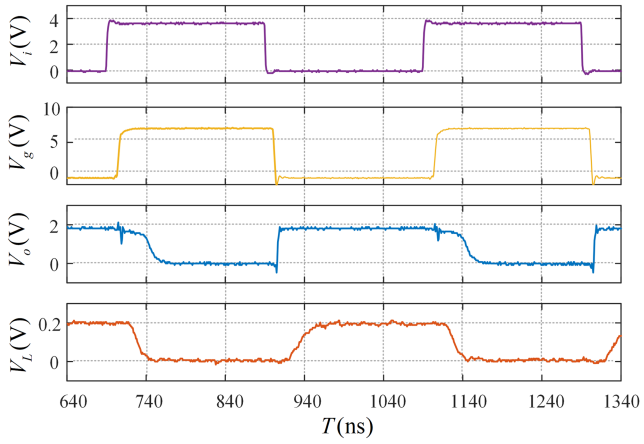

Fig. 15. Measurement waveforms of the proposed driving unit.

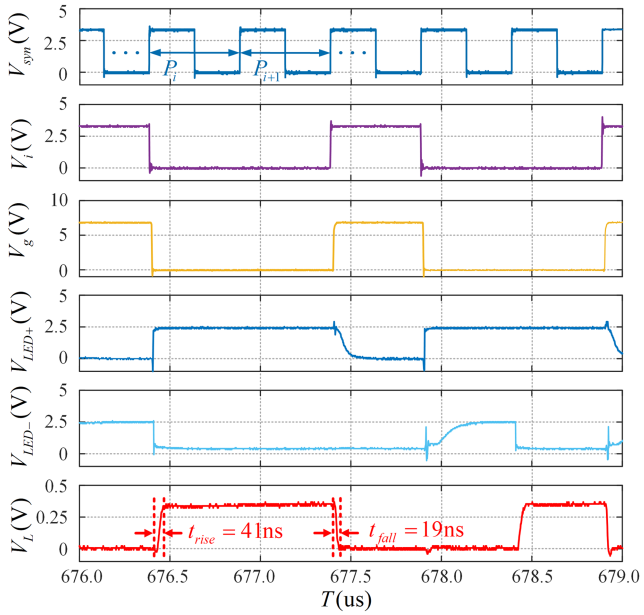

Fig. 16. Measurement results of a driving unit and a single LED when a series of patterns are displayed.

driving circuit and the light intensity of individual LEDs. The measurement results are shown in Fig. 16. All the patterns in the experiment used our proposed pattern display scheme. V_{sync} is the voltage waveform of the synchronization signal from FPGA. The pattern switching is triggered by the rising edge of V_{sync}. The frequency of V_{sync} is 2 MHz. When the rising edge of V_{sync} occurs, the current pattern displayed by the LED array switches to the next pattern. A common active crystal oscillator with a clock frequency of 100 MHz is used for two FPGAs. V_i is the voltage waveform of control signal generated by the FPGA. The amplitude of V_i is 3.3 V and its edge time is 2 ns. V_g is the voltage waveform of the MOSFET gate, and its amplitude is 7 V. The rise time of V_g is 10 ns and fall time is 4 ns. $V_{\text{LED}+}$ and $V_{\text{LED}-}$ are the anode voltage and cathode voltage of the LED. For one single LED, there are four states of voltage at both ends due to voltage changes at the anode and cathode. However, the LED is only lit when the anode voltage is high and the cathode voltage is low,

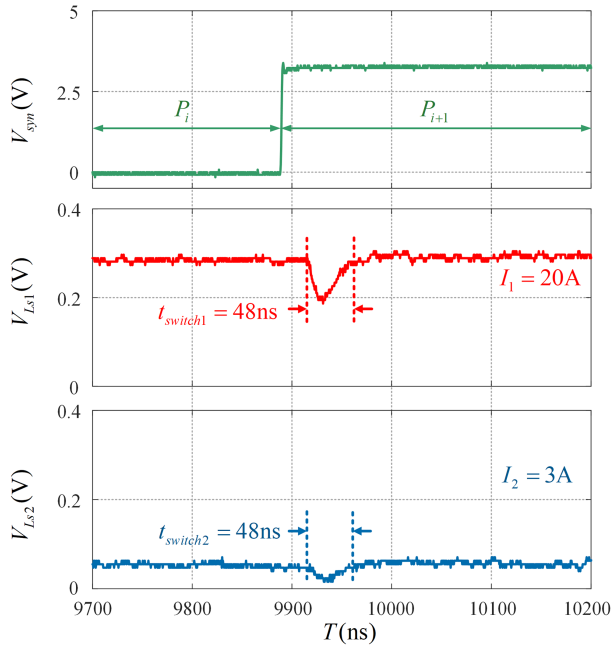

Fig. 17. Measurement results of the LED array when the proposed driver outputs different power.

and the voltage at both ends of the LED is about 2 V in Fig. 16. The rise time of $V_{\text{LED}+}$ is 7 ns, and the fall time is 140 ns. The fall time of $V_{\text{LED}-}$ is 7 ns, and the rise time is 200 ns. V_L is the voltage measured by the single pixel detector after converting the captured light signal of one single LED into an electrical signal. t_{rise} and t_{fall} are the rise time and the fall time of V_L.The difference in patterns will cause a slight change for t_{rise} when patterns switching, in the range of 40 to 100 ns, which is close to the limited response time of the LED. Parasitic effects are the primary cause of slight variations in the switching times of different patterns. t_{fall} is usually lower than the LED rise time, in the range of 20–40 ns.

We also measured the total light intensity of the LED array when the proposed driver outputs different currents. Measurement results of are shown in Fig. 17. V_{sync} is the voltage waveform of the synchronization signal. The pattern switching is triggered by the rising edge of V_{sync}. Both V_{Ls1} and V_{Ls2} are the voltage measured by the single pixel detector after converting the captured light signal of the total lit LEDs into an electrical signal, but they are measured at different outputs. Whether the output current provided by the driver is $I_1 = 20$ A or $I_2 = 3$ A, the switching time of light intensity is 48 ns when the pattern is displayed, which is close to the response speed of a single LED. Compared to the previous driver design that can only provide 3 A current, the experimental results show that the proposed driver and pattern display scheme can meet the requirements of high speed and high power. Also, measurement results show that both the electrical signals and the optical intensity signals exhibit good quality. This indicates that the impact of parasitic inductance on signals is minor at the operating frequency, which ranges from 0 to 25 MHz.

Structured light devices are typically used in conjunction with high-performance detectors to measure objects. In practice, the resolution required for structured light devices is not very high

in most imaging fields, with 128 × 128 being the commonly used resolution. For example, a 128 × 128 LED array can project fringe patterns with high accuracy, and when paired with a high-speed, high-resolution CMOS array detector, it enables the rapid acquisition of high-precision 3-D information about objects. The driver scheme we proposed offers high scalability. When applying this driving scheme to higher-resolution LED arrays, it is only necessary to increase the same number of row/column driving units according to the number of added row/column signal lines.

The limitation on the refresh rate of our designed driver board lies in the response speed of the currently used LED, which is only 25 MHz. Micro-LEDs, with their characteristic dimensions measuring merely tens of micrometers, can achieve response speeds operating in the gigahertz (GHz) range. When the signal frequency reaches GHz levels, parasitic inductance [28] will become the primary factor affecting the quality of high-speed signals. Detailed analysis of parasitic inductance, along with strategies to reduce it and mitigate its impact, will undoubtedly be one of the critical challenges. Furthermore, alternative approaches utilizing GaN or SiC FETs [29], [30], [31] may also be considered to enhance the driver's performance during high-frequency operation.

V. Conclusion

In this article, an ultra-high-speed driver circuit for structured lighting is proposed, which can support high-power LED arrays to refresh structured light patterns at ultra-high rates. To suppress the influence of dynamic load response of the power supply, a pattern display scheme is adopted to improve the accuracy of both electrical and optical signal intensities during high-speed operation. The prototype of the proposed driver is fabricated and tested. The experimental results show that the driver can output over 40 W and drive a 128 × 128 LED array to refresh the patterns at a rate of 10–25 MHz, which is approximately 1000 times faster than DMD.

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