An Optimum Transient Response Synchronous Buck Converter Employing a Novel Analog Multiplier Controller

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***Abstract*—An ultrafast step response synchronous buck converter has been developed for battery-powered and hand-held electronic applications. The proposed converter has an impressive settling time of only two clock periods and a 1.8 A output current capability. This fast step response makes the proposed converter an ideal choice for dynamic voltage scaling technique in the mentioned applications. The proposed design utilizes an analog multiplier controller (AMC), which provides an optimum disturbance-damping mechanism to remove any output voltage error in just two clock periods. In addition, the synchronization feature of the AMC buck converter eliminates the electromagnetic interference concern in fast buck converters. In order to realize the proposed controller a multiplier block and a novel residual time generator block are employed. The proposed AMC buck converter achieves a fast 2–2.3 μs settling time for 1.3 A load step and a 3–3.5 μs settling time for 1 V reference step with 1 MHz of switching frequency. Furthermore, The AMC buck converter has a high output current density of 1.38 A/mm^2 with 96% peak efficiency. The proposed design has been implemented in a 180 nm bipolar-CMOS-DMOS (BCD) technology with a die size of 910 μm $\times$ 1500 μm.**

***Index Terms*—Analog multiplier, dynamic voltage scaling (DVS), electromagnetic interference (EMI), fast step response, synchronous buck converter.**

I. Introduction

TRANSIENT response of dc–dc converters is one of the most studied issues in recent years. Frequently varying and high slew rate load current of multiple digital/analog systems integrated into battery-powered portable devices increases the demand for high-speed response of the power supply regulators. Large and fast varying load currents supplied by a low-speed regulator, requires a high volume of output capacitors to limit the fluctuations of the supply voltage, which is a challenging issue in compact battery-powered systems [1]. Dynamic voltage scaling (DVS) is also a prevalent technique in battery-powered systems to reduce power consumption, which requires a fast output voltage transient response in switching converters to minimize undershoot/overshoot and settling time [2]. In a conventional switching converter using the averaged model [3], the system bandwidth is designed much lower than the switching frequency to ensure the model accuracy, which results in a high transient response time [4]. Therefore, increasing the system bandwidth of conventional converters necessitates higher switching frequency, which results in efficiency degradation. Many techniques have been reported to reduce the response time of the system without increasing the switching frequency. Although the hysteretic mode [5] and constant on time (COT) [6], [7], [8], [9] control techniques achieve fast settling time, they do not have a predictable switching frequency, which makes electromagnetic interference (EMI) a concern. In addition, the authors in [10] and [11] introduced a frequency locking circuit to decrease hysteretic control mode switching frequency variations, which increases the silicon area and complexity. Moreover, the authors in [6], [7], [8], [9], [10], and [11] have 5–10 clock periods for their settling time, that is still a high settling time relative to the clock period. A monolithic capacitor current method that utilizes nonlinear optimized feedback to achieve optimum transient time is introduced in [2], which can decrease the settling time relative to the clock period. Also, optimal transient time methods [12], [13] utilize state-plane analysis to extract the optimum settling condition for the converter where both ON and OFF state of the switch is controlled by controller and as a result, the switching frequency is determined by the controller parameter and can vary during transients. However, both monolithic capacitor current and optimal transient time methods face issues related to the switching frequency uncertainty and EMI. The auxiliary linear regulator [14], [15] is a power- and area-inefficient technique to improve the transient response since it uses an auxiliary switch to provide the output current directly from the input voltage supply in an output transient. This leads to an increasing power loss, especially in a frequently varying load or reference voltage condition. Also, the auxiliary switch should be implemented with large size to handle transient load currents and consequently increases the silicon area and cost. Dual edge pulsewidth modulator [16] outperforms conventional modulation schemes in terms of both small- and large-signal dynamic performances. However, it requires off-chip compensation network components, which increases printed circuit board area and still has a long 70

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clock cycle settling time. Linear hybrid feedback/feedforward technique (HFFT) [17] omits off-chip compensation network and improves settling time. However, it requires on-chip capacitors for integrator block, which decreases current density. In addition, it cannot break the switching frequency and bandwidth tradeoff to achieve fast transient response. Active ramp tracking control [18] provides full duty pulsewidth modulation (PWM) signal by making the ramp waveform V_{DD} or GND in the load current transient condition using transient detector circuitry to decreases settling time. However, it requires large output inductor to decreases inductor current ripple and has potentially large overshoot/undershoot during large load or reference step. In this work, an optimum settling time of a typical synchronous PWM dc–dc converter with an LC output filter is investigated. It is shown that the optimum settling time for the PWM dc–dc converter is equal to two switching clock periods of the converter. Therefore, an optimum PWM controller can eliminate any disturbance in inductor current and output voltage in at least two periods of clock. Using the complementary metal-oxide-semiconductor (CMOS) four-quadrant analog multiplier in [19] a novel analog multiplier PWM controller (AMC) for a synchronous dc–dc buck converter is proposed to achieve the optimum two-clock period settling time for both inductor current and output voltage. The two-clock settling time of the proposed AMC converter shows an impressive improvement in comparison with typical synchronous linear controlled PWM converters with settling time more than ten clock cycles [17], [20]. Also, the synchronous operation of the proposed AMC converter with fixed turn-ON times is an advantage of the design, which makes the proposed converter suitable for EMI sensitive applications.

The rest of this article is organized as follows. In Section II, the optimum switch turn-OFF time point of a PWM controller during a clock period in a typical synchronous dc–dc converter is extracted and the optimum settling time is achieved. The proposed novel controller system design is explained in Section III. In Section IV, the circuit implementation of the proposed controller blocks is discussed. Experimental results are provided in Section V. Finally, Section VI concludes this article.

II. Optimum Switch Turn-off Time Point (OSTOP)

In a typical synchronous PWM voltage-mode ($K_C = 0$) or current-mode ($K_C = 1$) dc–dc buck converter of Fig. 1, usually turn-ON time point of the high side switch (M_P) is at the rising edge of the clock and the M_P switch turn-OFF time point (STOP) is set by the controller in a period of clock. During an output voltage (V_{OUT}) or inductor current (I_L) disturbance that can occur by the load or reference voltage (V_{REF}) transient, there is always an OSTOP in each period of the clock that minimizes the settling time. For a synchronous dc–dc converter with an LC output filter to settle, both I_L and V_{OUT} must reach to their steady state. The minimum assumable settling time for a typical PWM synchronous dc–dc converter is the duration of one clock period but it can be shown that it is impossible for a dc–dc converter with an LC output filter to damp both I_L and V_{OUT} disturbances in one period of clock as will be explained.

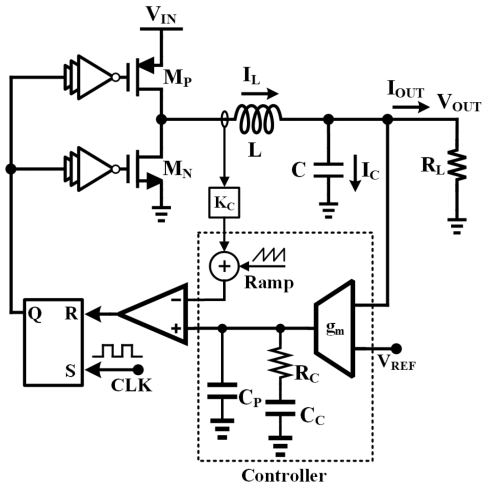

Fig. 1. Typical structure of buck converter.

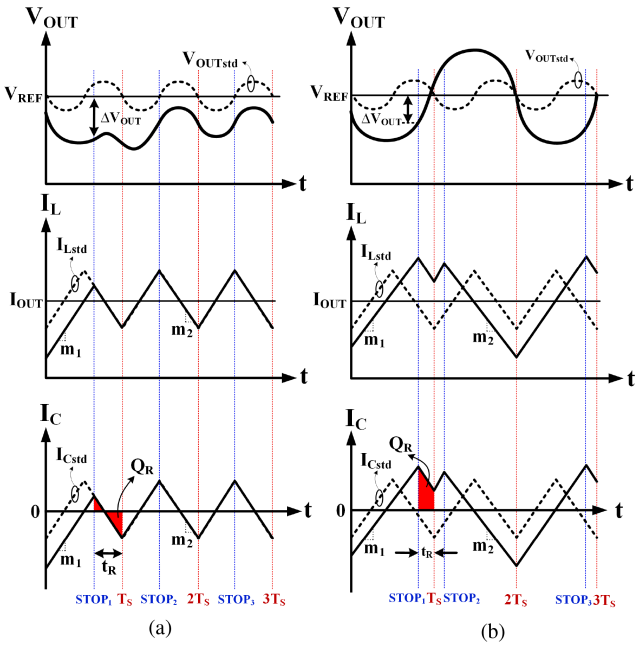

Fig. 2. Disturbed Output voltage and inductor current at $t = 0$. Choosing the STOP in such a way that (a) inductor current and (b) output voltage be at steady state at T_S.

In Fig. 2(a) disturbed V_{OUT}, I_L and output capacitor current (I_C) waveforms of a dc–dc buck converter are illustrated. I_{Lstd}, I_{Cstd}, and V_{OUTstd} diagrams are I_L, I_C, and V_{OUT} steady-state waveforms, respectively. For I_L to settle at the end of the first clock period ($t = T_S$), the STOP must be at the intersection moment of I_L waveform with the falling edge of I_{Lstd} waveform or its extension assuming that the disturbance amplitude of V_{OUT} is much lower than its dc value so that the I_L rising slope (m_1) and falling slope (m_2) during disturbance are constant and equal to the rising and falling slopes of I_{Lstd}, respectively [3], [12], [13]. This assumption is valid for constant switching frequency and small deviations in the output voltage. In other words, for I_L to settle at T_S, the STOP must be at the moment that causes I_L

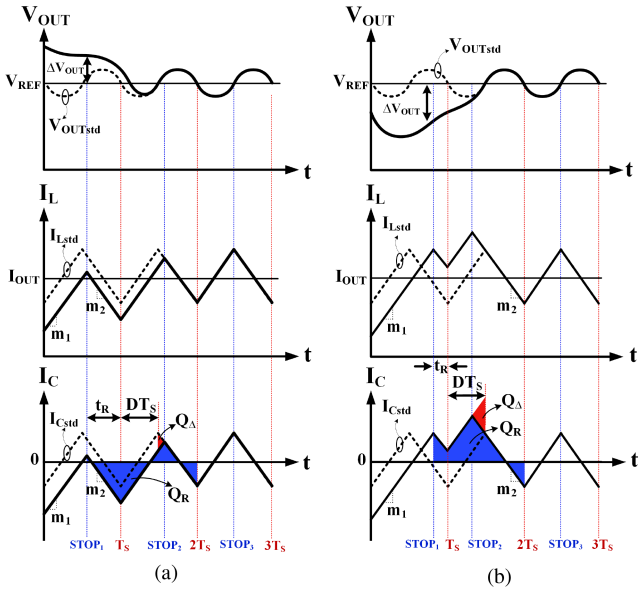

Fig. 3. Disturbed output voltage and inductor current at $t = 0$. Settling in two periods of clock (a) overshoot and (b) undershoot of the output voltage.

and I_{Lstd} to be equal at T_S, as shown in Fig. 2(a). Consequently, there is only one STOP that can result in I_L settling at T_S. This STOP leads to a certain amount of charge that will be charged into the output capacitor (Q_R) during $t_R = T_S$-STOP$_1$, which is equal to the area under the output capacitor current waveform (I_C). Based on Fig. 1 I_C is

$$I_C = I_L - I_{\text{OUT}} \tag{1}$$

where I_{OUT} is the output current of the buck converter. Also Q_R is dependent on t_R and the falling slope of I_L and can be calculated by choosing the STOP. In addition, in order to settle V_{OUT} at T_S, Q_R must satisfy

$$-\Delta V_{\text{OUT}}(t = \text{STOP}_1) = \frac{Q_R}{C} \tag{2}$$

where $\Delta V_{\text{OUT}} = V_{\text{OUT}} - V_{\text{REF}}$ and C is the output capacitor. ΔV_{OUT} is dependent on the disturbance amplitude of V_{OUT} at $t = 0$. Moreover, as mentioned above Q_R is determined by STOP and independent of ΔV_{OUT} so it will not be necessary to satisfy (2). In other words, choosing the STOP in such a way that I_L settles at T_S will not necessarily lead to V_{OUT} reaching its steady state at T_S [see Fig. 2(a)]. Conversely, choosing the STOP in such a way that results in V_{OUT} to reach its steady state at T_S will not necessarily result in I_L to reach its steady state at T_S, as shown in Fig. 2(b). Therefore, settling both V_{OUT} and I_L in one clock period is not always possible in a dc–dc converter with an LC output filter.

On the other hand, considering two periods of clock for settling I_L and V_{OUT} of the converter, it is always possible to satisfy both I_L and V_{OUT} settling conditions because there are two STOPs in two periods of clock that can be chosen to satisfy both I_L and V_{OUT} settling conditions at $t = 2T_S$ as shown in Fig. 3. The second STOP (STOP$_2$) is chosen in such a way that the condition of I_L settling is realized at $2T_S$ and based on that, the first STOP (STOP$_1$) is set at a moment to satisfy V_{OUT} settling condition of (2) with Q_R from the STOP$_1$ to $2T_S$

$$Q_R = \int_{\text{STOP}_1}^{2T_S} I_C(t)dt. \tag{3}$$

The settling condition of I_L at $2T_S$ as mentioned above is

$$I_L(2T_S) = I_{\text{Lstd}}(2T_S). \tag{4}$$

Knowing m_1 and m_2 in a buck dc–dc converter with the output inductor value of (L) are

$$m_1 = \frac{V_{\text{IN}} - V_{\text{OUT}}}{L} \quad m_2 = \frac{V_{\text{OUT}}}{L} \tag{5}$$

respectively, where V_{IN} is the input voltage of the converter. It should be noted that (5) is valid for constant switching frequency and small deviations in the output voltage as mentioned previously. Also, $I_{\text{Lstd}}(2T_S)$ can be calculated as

$$I_{\text{Lstd}}(2T_S) = I_{\text{OUT}} - \frac{DT_S(V_{\text{IN}} - V_{\text{OUT}})}{2L} \tag{6}$$

where D is the duty cycle of converter in steady state and T_S is the period of clock. Also $I_L(t)$ can be written as

$$I_L(t) = \begin{cases} I_L(\text{STOP}_1) - m_2(t - \text{STOP}_1), & \text{STOP}_1 \le t \le T_S \\ I_L(T_S) + m_1(t - T_S), & T_S \le t \le \text{STOP}_2 \\ I_L(\text{STOP}_2) - m_2(t - \text{STOP}_2), & \text{STOP}_2 \le t \le 2T_S. \end{cases} \tag{7}$$

Using (6) and (7) in (4), STOP$_2$ in terms of STOP$_1$ and I_L(STOP$_1$) can be calculated and based on that by combining (1), (3), and (7), Q_R can be calculated as

$$Q_R = \left[I_C(\text{STOP}_1) - \frac{V_{\text{OUT}}}{2L}(t_R + DT_S)\right] \times (t_R + DT_S) + \frac{(DT_S)^2}{2}\left(\frac{V_{\text{IN}}}{L}\right) - Q_\Delta. \tag{8}$$

In (8), t_R is the residual time from STOP$_1$ to T_S and Q_Δ is

$$Q_\Delta = \frac{L}{2V_{\text{IN}}}(\Delta I_L)^2 \tag{9}$$

where $\Delta I_L = I_{\text{Lstd}}(T_S) - I_L(T_S)$. Substituting (8) in (2) leads to

$$-\Delta V_{\text{OUT}}\Big|_{t=\text{STOP}_1} = \left[\frac{I_C(\text{STOP}_1)}{C} - \frac{V_{\text{OUT}}}{2LC}(t_R + DT_S)\right] \times (t_R + DT_S) + \frac{(DT_S)^2}{2}\left(\frac{V_{\text{IN}}}{LC}\right) - \frac{Q_\Delta}{C}. \tag{10}$$

Since I_L and V_{OUT} settling conditions at $2T_S$ are independent, there is only one state for STOP$_2$ and STOP$_1$ that can satisfy both

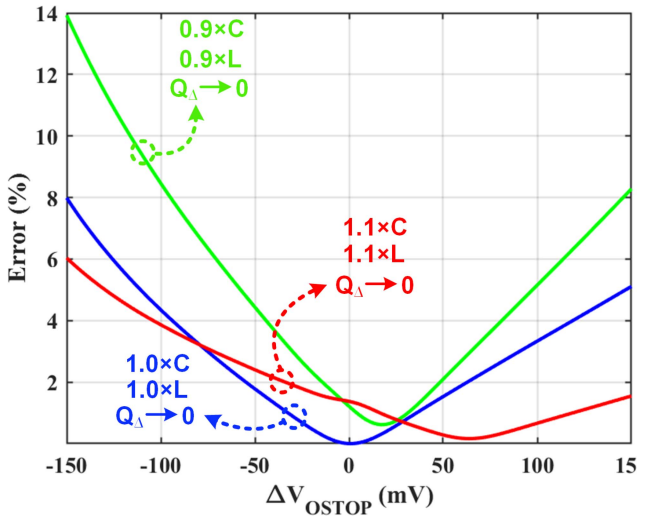

Fig. 4. Percentage of the remaining error at $2T_S$ according to the amplitude of the output voltage disturbance at STOP_1 due to removing Q_Δ and variation in the value of the output capacitor and inductor.

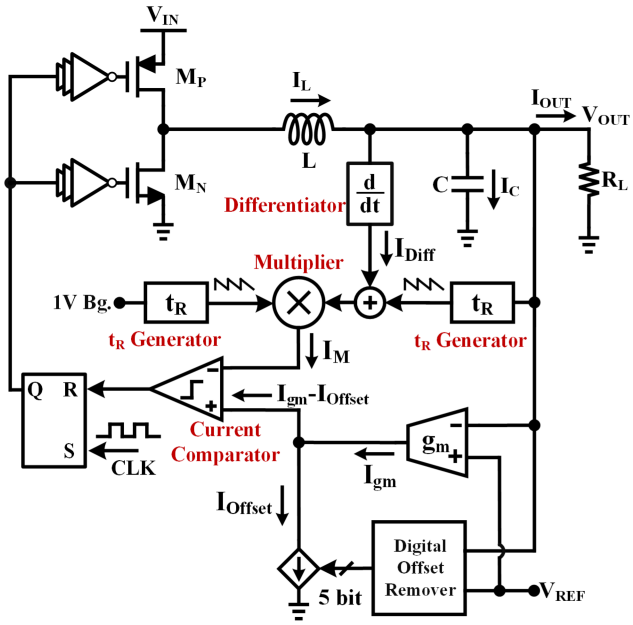

Fig. 5. Proposed structure of dc–dc buck converter controller.

conditions. As a result, STOP_1 and STOP_2 are OSTOP of the first (OSTOP_1) and second (OSTOP_2) clock periods, respectively. Choosing OSTOP_1 in the first clock period ensures I_L and V_{OUT} to settle at $2T_S$, by choosing OSTOP_2 in the second clock period. Consequently, OSTOP_2 and $\text{STOP}_3 = 2T_S + DT_S$ ensures I_L and V_{OUT} to be at steady state at $3T_S$ too (see Fig. 3), so (10) is also satisfied at OSTOP_2. In the same way, it can be concluded that (10) is satisfied at OSTOP of each clock period.

III. Proposed Controller Design

As explained in Section II, (10) is satisfied at OSTOP of each clock period. The proposed idea for the controller is to extract left and right side of (10) and turn M_P OFF as soon as left and right sides of (10) are equal to achieve optimum settling time. The term $\frac{DT_S}{2}(\frac{V_{\text{IN}}}{LC_O})$ on the right side of (10) is constant and can be ignored for the sake of simplicity of the controller implementation. This will cause an offset error in the output voltage that can be removed by an offset remover block as described in Section IV. Furthermore, Q_Δ on the right side of (10) can be ignored to reduce the complexity of implementation. Q_Δ is zero in the steady state and is proportional to the square of Δi_L and, therefore, is negligible in small-signal perturbation. However, in large signal perturbation removing Q_Δ can lead to certain settling latency. In Fig. 4 for $C = 3.3\ u\text{F}$ and $L = 1\ u\text{H}$, the percentage of residual output voltage error at $2T_S$ caused by ignoring Q_Δ according to the output voltage disturbance amplitude at STOP_1 is depicted

$$\text{Error}(\%) = 100 \times \frac{\Delta V\text{out}(t = 2T_S)}{\Delta V\text{out}(t = \text{STOP}_1)}. \tag{11}$$

Based on Fig. 4, for disturbances with an amplitude of less than 150 mV, the remaining error at $2T_S$ is less than 8% and more than 92% of the disturbance amplitude will be reduced at $2T_S$. Consequently, still a near optimum settling time can be achieved by ignoring Q_Δ in (10). In practical implementation, the output inductor and capacitor values are not constant and have variations that can add errors to (10). In Fig. 4, the effect of $\pm 10\%$ variation in the output capacitor and inductor values is also illustrated. The simplified form of (10) by removing Q_Δ and the dc term is

$$-\Delta V_{\text{OUT}}\Big|_{t=\text{STOP}} = \left[\frac{I_C(\text{STOP}_1)}{C} - \frac{V_{\text{OUT}}}{2LC}(t_R + DT_S)\right] \times (t_R + DT_S). \tag{12}$$

The right side of (12) is simplified into multiplication of two signals and the left side is proportional to ΔV_{OUT}. In Fig. 5, the proposed buck converter structure is illustrated. ΔV_{OUT} is extracted by a g_m block with V_{OUT} and V_{REF} as inputs. The right side of (12) is implemented using an analog multiplier presented in [19]. t_R and i_C are extracted by t_R generator block and differentiator block, respectively. The structure of these blocks are presented in Section IV. The left and right side of (12) are compared using a current comparator. In each period of clock the SR-Latch is set by the rising edge of the clock, which turns M_P on and is reset by current comparator as soon as its inputs are equal, which turns M_P OFF.

IV. Building Blocks

A. Multiplier

In order to realize the proposed AMC buck converter, a multiplier block has been used, which its schematic is presented in Fig. 6 [19]. For two independent differential inputs of (V_{in1}) and (V_{in2}), the differential output current ($I_{O1} - I_{O2}$) is

$$I_{O2} - I_{O1} = 2K(V_{\text{in2}} \times V_{\text{in1}}) \tag{13}$$

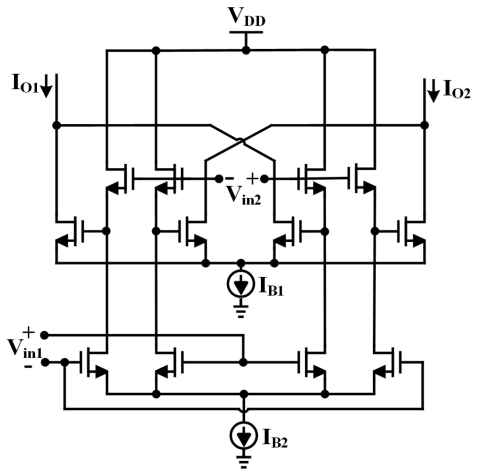

Fig. 6. Analog multiplier block schematic [19].

where

$$K = \mu_n C_{OX} \frac{W}{L} \tag{14}$$

and $\mu_n C_{OX}$ is the transconductance coefficient of n-MOS transistor in saturation region and $\frac{W}{L}$ is width to length ratio of transistor channel. In this design, bias currents (I_{B1} and I_{B2}) are chosen to be 32 μA and $\frac{W}{L}$ is 2 for all transistors. As a result, $K = 0.5$ mA/V^2 and is constant in the saturation region of transistors. For small signal voltage amplitude of V_{in1} and V_{in2}, transistors are in saturation region. Maximum voltage amplitude for V_{in1} and V_{in2} to maintain transistors in the saturation region and for the multiplier to work linearly is 0.3 V, which is extracted using simulation. The system is designed to maintain V_{in1} and V_{in2} voltage amplitudes less than 0.15 V in the steady state to ensure linear operation of the multiplier.

B. Differentiator

In the proposed AMC buck converter, the differentiator is used to extract I_C. Ideally, the output current of the differentiator (I_{Diff}) is proportional to I_C, but because of the electrical series resistance (ESR) and electrical series inductance (ESL) effect in real ceramic capacitors, I_{Diff} is not exactly proportional to I_C. For a real capacitor and an ideal differentiator I_{Diff} can be written as

$$I_{\text{Diff}} = K_{\text{Diff}} \frac{I_C}{C} + K_{\text{Diff}} \text{ESR} \frac{d(I_C)}{dt} + K_{\text{Diff}} \text{ESL} \frac{d^2(I_C)}{dt} \tag{15}$$

where K_{Diff} is the differentiator coefficient. Since I_C waveform is triangular in the buck converter, ESR and ESL cause steps and spikes, respectively, in I_{Diff} as illustrated in Fig. 7. High-frequency spikes caused by ESL are filtered out through system blocks.

A common structure of the differentiator is used in [21] and [22]. However, it has a limited output voltage swing and does not compensate the ESR effect of the output capacitor. In order

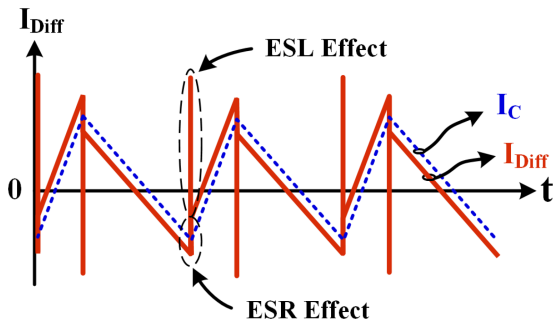

Fig. 7. Differentiator output current in the proposed AMC buck converter, considering the output capacitor ESR and ESL effects.

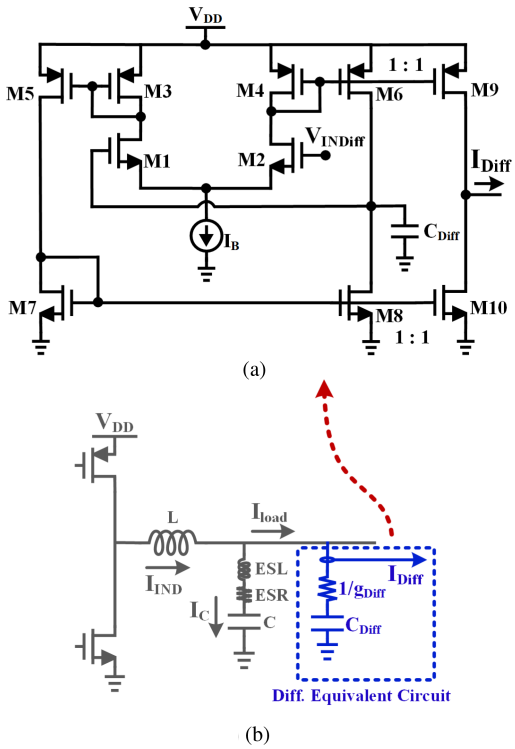

Fig. 8. (a) Schematic and (b) simplified equivalent circuit of the proposed differentiator.

to improve the output swing of the differentiator as well as ESR effect compensation, the differentiator structure of Fig. 8(a) is proposed. The equivalent circuit of the proposed differentiator is shown in Fig. 8(b). g_{Diff} in the equivalent circuit is the transconductance of M1 and M2 transistors. The drain/source conductance of transistors is ignored over $1/g_{\text{Diff}}$. By choosing a proper g_{Diff} such that $1/g_{\text{Diff}}$ corresponds to the output capacitor ESR, the ESR effect in the differentiator output current can be suppressed. In the proposed differentiator of Fig. 8(a), $K_{\text{Diff}} = C_{\text{Diff}}$ and the proper value for g_{Diff} to suppress ESR effect is

$$g_{\text{Diff}} = \left(\text{ESR} \frac{C_O}{C_{\text{Diff}}} \right)^{-1}. \tag{16}$$

In the proposed AMC converter design, the output capacitor is a 3.3 μF ceramic capacitor with 5 $m\Omega$ of ESR and C_{Diff} is 3.3 pF.

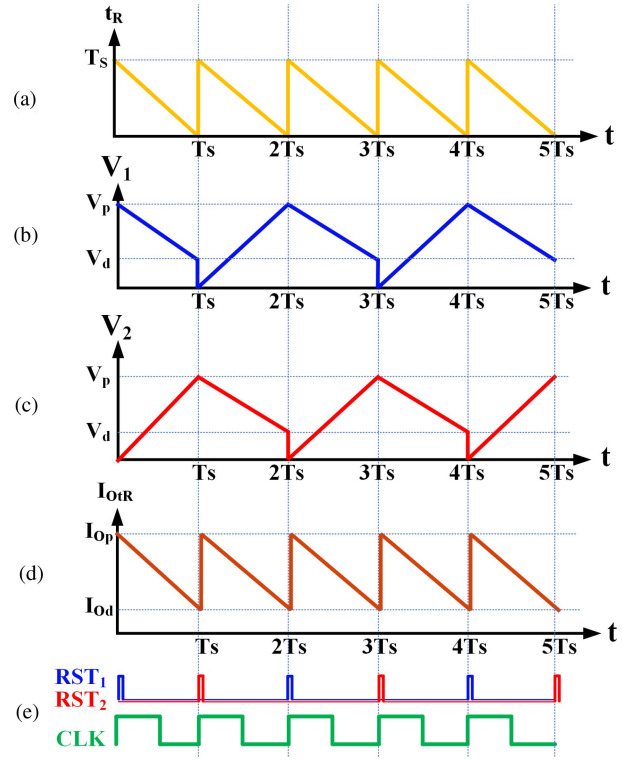

Fig. 9. (a) Residual time to the end of clock period, t_R generator block waveforms. (b) V_1. (c) V_2. (d) I_{OtR}. (e) RST_1, RST_2, and CLK.

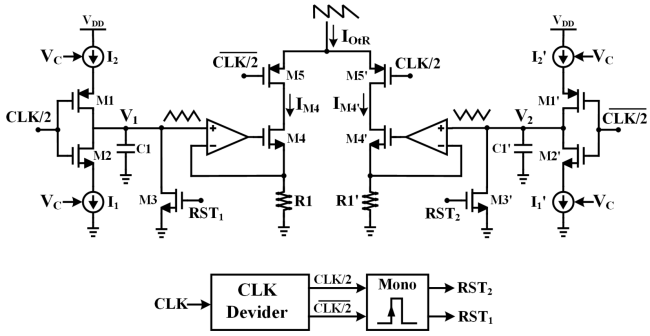

Fig. 10. t_R generator.

Therefore, the proper value for g_{Diff} is 0.2 $m\mho$ and (15) without ESR and ESL effects is

$$I_{\mathrm{Diff}} = (10^{-6}) i_C. \tag{17}$$

C. t_R Generator

The t_R generator block concept is introduced for the first time in the proposed AMC converter, which extracts the residual time to the next clock rising edge. The expected t_R signal is a reverse saw-tooth signal, which is T_S at the beginning of each period of the clock and is zero at the end of the period as shown in Fig. 9(a). The structure of t_R generator is shown in Fig. 10. It consists of two similar parts. Each part includes a current-starved inverter connected to a V-to-I converter. In the proposed t_R generator, these two parts are used together with CLK/2 and $\overline{\mathrm{CLK}/2}$ inputs connected to a single pole dual throw ($M5$ and $M5$' switches). At each cycle of CLK/2 and $\overline{\mathrm{CLK}/2}$ two inverted quasi-triangular voltage waveforms are generated at V_1 and V_2 nodes by the current-starved inverters as shown in Fig. 9(b) and (c), respectively. V_1 and V_2 voltages are converted to I_{M4} and I_{M4}' currents, respectively, using two differential amplifiers, $R1$, $R1$' resistors, $M4$ and $M4$' transistors. The falling slope of I_{M4} and I_{M4}' are switched to the t_R generator output current (I_{OtR}) by $M5$ and $M5$', respectively, to create an inverted saw-tooth waveform in I_{OtR} [see Fig. 9(d)]. $M3$ and $M3$' transistors reset V_1 and V_2 to zero by RST_1 and RST_2 pulses, respectively, at the end of their period. The maximum value of I_{OtR} is defined as (I_{Op}) and can be written as

$$I_{\mathrm{Op}} = \frac{V_p}{R_1} = \frac{I_2 T_S}{R_1 C_1} \tag{18}$$

where V_p is the peak value of V_1 and V_2 signals as shown in Fig. 9(c) and (d), respectively. Also, the minimum value of I_{OtR} is defined as (I_{Od}) and can be written as

$$I_{\mathrm{Od}} = \frac{V_d}{R_1} = \frac{(I_2 - I_1) T_S}{R_1 C_1} \tag{19}$$

where V_d is the value of V_1 and V_2 signals at end of the period as shown in Fig. 9(c) and (d), respectively. I_2 and I_1 are shown in Fig. 10, which are voltage control current sources with V_C control voltage and g_b transconductance. Choosing $I_1 = \frac{I_2}{1+D} = g_b V_C$ in (18) and (19) I_{OtR} will be

$$I_O = I_{\mathrm{Od}} + (I_{\mathrm{Op}} - I_{\mathrm{Od}}) \left(\frac{t_R}{T_S} \right) = \frac{g_b V_C}{R_1 C_1} (t_R + D T_S). \tag{20}$$

In the structure of Fig. 10, all corresponding parameters in left and right side are equal. RST_1 and RST_2 signals are generated by a 15 ns mono stable circuit at rising edge of CLK/2 and $\overline{\mathrm{CLK}/2}$ to reset $C1$ and $C1$' capacitors, respectively. In the right side of (12), the term $t_R + DT_S$ is used twice. One is proportional to V_{OUT} and the other one is with constant coefficient of one. Therefore, two t_R generator blocks are in the proposed AMC buck converter of Fig. 5. One with control voltage connected to V_{OUT} and the other one connected to a 1 V band-gap reference voltage.

D. Digital Offset Remover (DOR)

The DOR block in the proposed AMC buck converter is used to remove the steady-state error of V_{OUT}. The speed of the DOR block is much lower than the system controller, and therefore, it does not interfere with the system performance. A conventional analog offset remover (AOR) block diagram is illustrated in Fig. 11(a), which utilizes an area consuming capacitor [2]. In order to, eliminate the bulky capacitor of the conventional offset remover the novel DOR is introduced, as shown in Fig. 11(b). The proposed DOR consists of a comparator that compares V_{OUT} with V_{REF} and sets up/down direction through a DQ flip–flop. The counter output is connected to a 5 bit digitally controlled current source (DCCS) and counts by CLK/2 of the system. Since the proposed AMC is designed to settle in two system clock cycles, a maximum of one LSB bit variation will occur at the control input of the DCCS during any perturbation in V_{OUT}

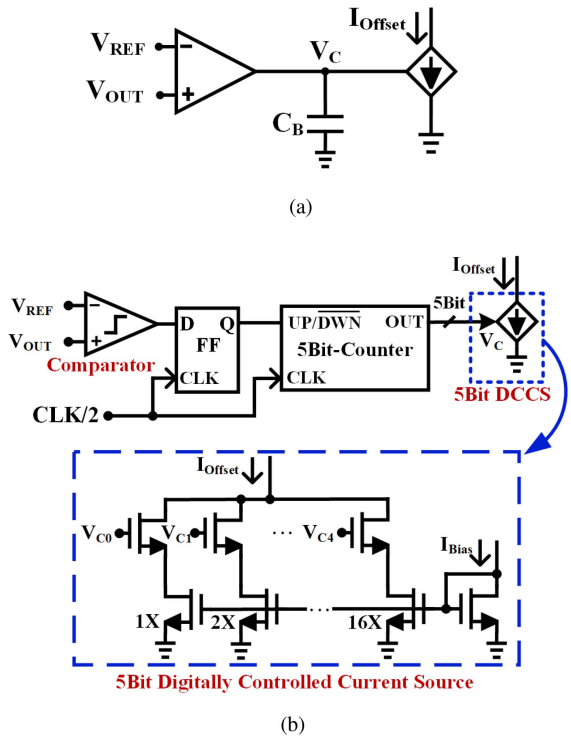

Fig. 11. (a) Conventional AOR. (b) Proposed DOR.

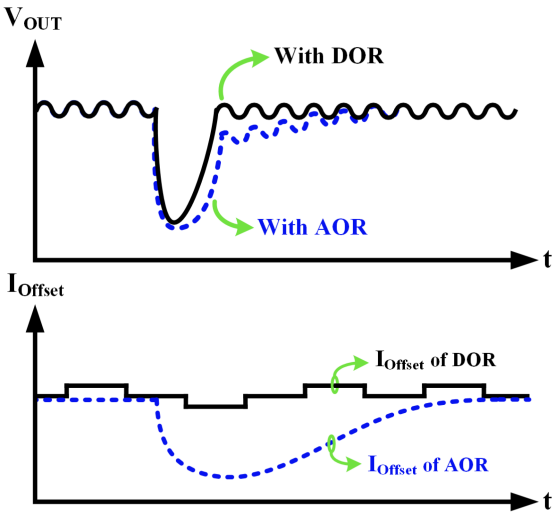

Fig. 12. Conceptual wave form of analog and DOR output current during a disturbance and their effect on the output voltage of the converter.

or I_L. In the conventional AOR shown in Fig. 11(a), during an output voltage perturbation depending on its amplitude, V_C can vary significantly and it takes a long time for V_C to return to steady state. Therefore, during a large output voltage perturbation, a significant offset will be generated in the output voltage that takes a long time to be removed, as shown in Fig. 12. In the proposed DOR, due to the discrete states in the DCCS a one or two-bit ripple in the output of the counter is inevitable. However, it causes a much smaller variation in the output voltage than the output voltage ripple, which can be ignored.

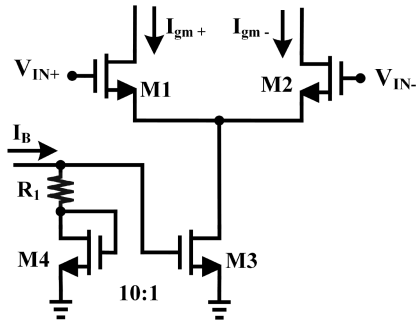

Fig. 13. Proposed temperature/process compensated g_m block.

E. g_m Block

The g_m block is used to extract left side of (12). The structure of g_m block is a typical differential input pair with current source tail as shown in Fig. 13. Also, R_1 is added in series with $M4$ in the proposed structure to compensate the process/temperature variation of both g_m and multiplier blocks as is explained in the following. The $M4$ transistor size is chosen much larger ($10X$) than $M3$ so $M4$ gate-source voltage is almost equal to MOSFET threshold voltage (V_{th}). Therefore, the gate-source bias voltage of M3 equals $V_{th} + R_1 I_B$. I_B is a process/temperature compensated bias current and R_1 is a precise low-variation resistor ($< \pm 3\%$ variation). As a result, the transconductance of the block is calculated as follows:

$$g_m = \frac{I_{gm+} - I_{gm-}}{V_{\text{IN}+} - V_{\text{IN}-}} = \mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} \times (I_B R_1). \quad (21)$$

The term $\mu_n C_{ox}$ is present in both g_m and $I_{O1} - I_{O2}$ in (13), which appears on both the left and right sides of (12) so it can be removed from both sides of (12). Therefore, the system is independent of the term $\mu_n C_{ox}$, and temperature/process dependency of the both multiplier and g_m blocks is eliminated in the system.

V. Simulation and Measurement Results

The proposed AMC buck converter is fabricated in a 180 nm bipolar-CMOS-DMOS (BCD) technology. The input voltage ranges 3.8–5 V and the output voltage can be set from 1.8 to 3.3 V with a maximum of 1.8 A output current. A 1 μH inductor with a 3.3 μF capacitor are used as the output filter and the switching frequency is 1 MHz. Theoretically, since the proposed converter can remove any disturbance within two period of clocks, using ideal blocks in Fig. 5, and increasing the switching frequency can further improve the settling time. However, limited switch driver speed to decrease undesired EMI/EMC effect and limited bandwidth of system block including multiplier and differentiator contribute as two major limiting factors that prevent increasing the switching frequency. The die photograph is depicted in Fig. 14 with a total area of 910 μm $\times$ 1500 μm and a controller area of 400 μm $\times$ 230 μm.

In order to show the improvement of the proposed AMC controller compared with typical controllers (see Fig. 1), a well-tuned dual-loop PI controller with same values of L, C, switching frequency, input, and output voltage as in the proposed

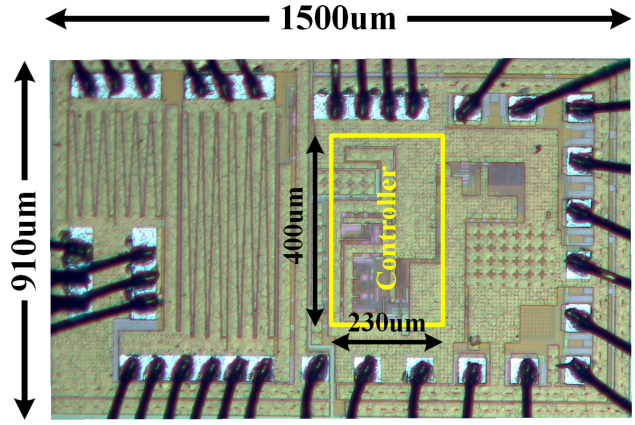

Fig. 14. Die photograph.

TABLE I
CONTROL PARAMETERS OF THE TYPICAL DC–DC BUCK CONVERTER

C_P	C_C	R_C	g_m	K_C
1 pF	55 pF	40 KΩ	100 $\mu\mho$	1

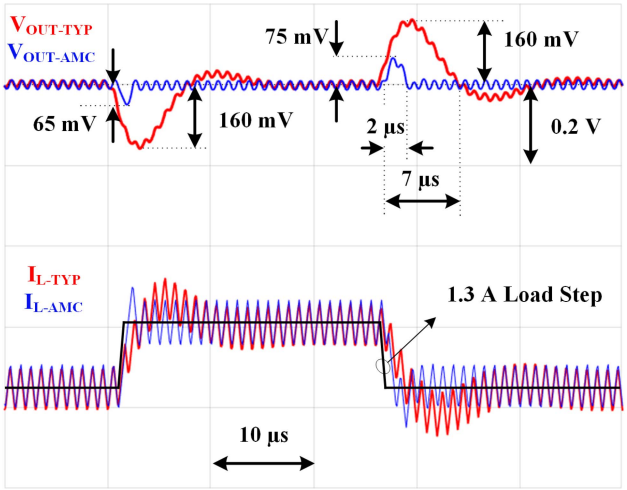

Fig. 15. Simulation results of load step response of the proposed AMC and typical buck converter.

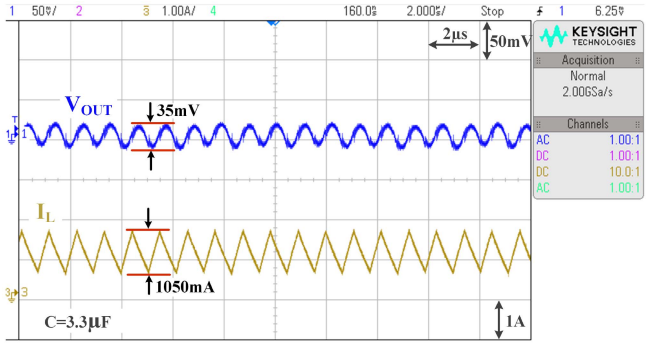

Fig. 16. Measured steady-state waveforms of the output voltage and inductor current.

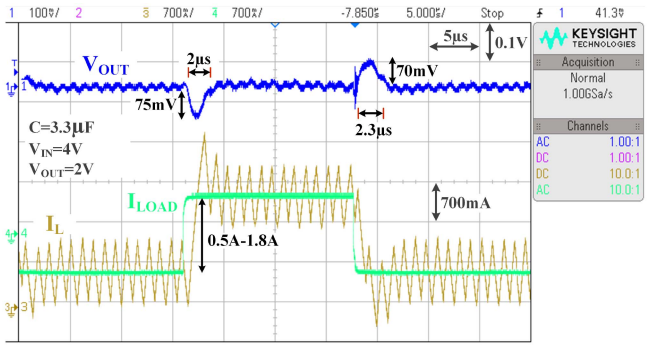

Fig. 17. Measured load 0.5 to 1.8 A transient step response.

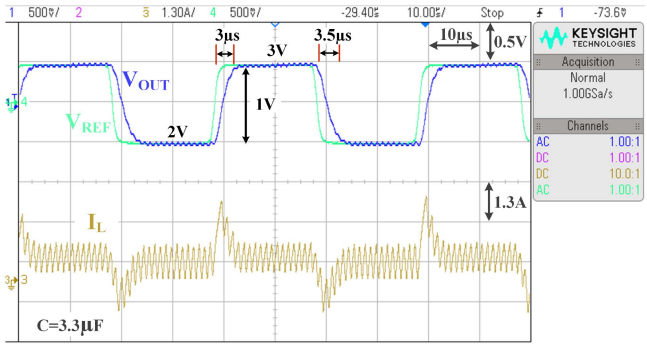

Fig. 18. Measured reference step response.

AMC controller is implemented. The control parameters of the converter are shown in Table I. The simulation results of the load step response of the proposed AMC converter are compared with the typical converter in Fig. 15. The input voltage in both converters is 4 V and the output voltage is 2 V. The typical converter has 160 mV overshoot/undershoot with 7 μs settling time. However, the proposed AMC converter achieves only 2 μs and 70 mV settling time and overshoot/undershoot, respectively, which is a significant improvement in comparison with a typical converter.

The measured steady-state waveforms of output voltage and inductor current are depicted in Fig. 16 with 35 mV of peak to peak output voltage ripple and 1050 mA inductor current ripple. The measured load 0.5–1.8 A transient step response is shown in Fig. 17. The proposed converter shows a 2 μs settling time for low to high and 2.3 μs for high to low load step response. Within about 2 switching clock periods, settling time is achieved in load step measurement, as shown in Fig. 17. The reference step response of the converter for DVS applications is also depicted in Fig. 18. A 3 μs and 3.5 μs settling time is measured for 2–3 V and 3–2 V reference step, respectively, with no overshoot or undershoot. A 25 KHz sinusoidal is also applied to the input reference, where the measured output voltage and inductor current waveforms are shown in Fig. 19. The output voltage follows the input reference sinusoidal waveform with a 1.3 μs delay. Measured efficiency in terms of the output current is shown in Fig. 20. A 96% peak efficiency is achieved for 0.85 A output current, 3.3 V output voltage, and 3.8 V input voltage.

The proposed AMC converter is compared with state of the art buck converters in Table II. It shows the best load step response among all the prior arts except [14], which uses an additional auxiliary switch to bypass the output LC filter in the output transients at the cost of extra loss, especially in

TABLE II
PERFORMANCE SPECIFICATIONS OF THE PROPOSED BUCK CONVERTER AND COMPARISON WITH THE STATE-OF-THE-ART

Reference	JSSC '18 [10]	TPEL '21 [7]	TPEL '19 [16]	TPEL '23 [14]	JSSC '19 [23]	JESTPE '21 [17]	LTM4691 '20 [24]	**This work**
Technology	350 nm CMOS	130 nm CMOS	130 nm CMOS	350 nm CMOS	65 nm CMOS	180 nm CMOS	NA	**180 nm BCD**
Controller type	Hysteretic Quasi-V2	COT	Dual-edge PWM	Linear regulation	Time domain current mode	HFFT	PWM	**AMC**
Capacitor (μF)	4.7	10	14	4.7	4.7	10	22	**3.3**
Inductor (μH)	2.2	2.2	0.29	4.7	0.22	2.2	0.47	**1**
V_{IN} (V)	3.3	7–15	2.5	2.8–3.6	1.8	2.7–4.2	2.5–3.6	**3.8–5.0**
V_{OUT} (V)	1.5–1.8	5–7	1.29	1.8–2.5	0.15–1.69	1–2.5	0.5–2.5	**1.8–3.3**
Switching frequency (MHz)	2.5 Unsynch.	2 Unsynch.	1.26 Unsynch.	1 Unsynch.	10 Synch.	2.5 Synch.	1 Synch.	**1 Synch.**
Max I_{OUT} (A)	0.7	2	1.5	0.5	0.6	1	2	**1.8**
Peak efficiency (%)	92	95.5	N.A.	95	94.9	94	94	**96**
Load step settling time (μs)	2.5	2.7 (H to L) 3 (L to H)	60	1.6 (H to L) 2 (L to H)	3.5	5.5	10	**2.3 (H to L)** **2 (L to H)**
Load step (A)	0.51	1	0.95	0.45	0.48	0.7	1.4	**1.3**
STPR	6.25	5.4 (H to L) 6 (L to H)	75.6	1.6 (H to L) 2 (L to H)	35	13.75	10	**2.3 (H to L)** **2 (L to H)**
Reference step settling time (μs)	N.A.	N.A.	N.A.	N.A.	3.5 (H to L) @ 0.5 V 3 (L to H) @ 0.5 V	N.A.	N.A.	**3.5 (H to L) @ 1 V** **3 (L to H) @ 1 V**
Area (mm^2)	0.9 × 1.014	2 × 1.5	N.A.	1.8 x 1.49	2.38 x 0.89	1.4 x 1.05	NA	**1.5 x 0.91**
Current density ($\frac{A}{mm^2}$)	0.77	0.67	N.A.	0.19	0.28	0.68	NA	**1.32**
FOM [23]	7.61	1.41	N.A.	7.49	12.8	8.36	3.8	**1.02**

CMOS: Complementary Metal-Oxide-Semiconductor, BCD: Bipolar-CMOS-DMOS
The bold values represent the measured parameters of the proposed work.

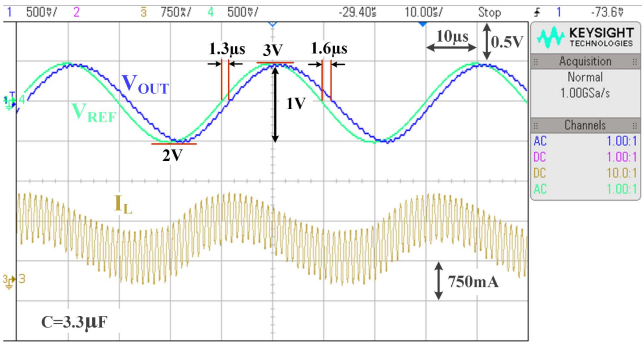

Fig. 19. Measured output voltage and inductor current waveforms for a 25 KHz reference sinusoidal input.

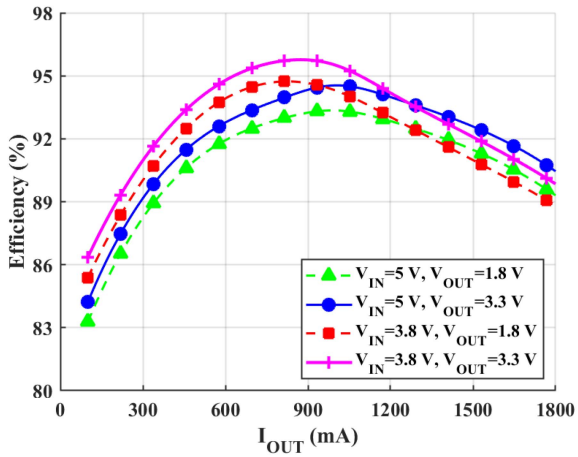

Fig. 20. Measured efficiency for different input/output voltages.

frequently varying load current condition. This auxiliary switch also occupies a large silicon area to implement, resulting in a low output current density of 0.19 A/mm^2. The proposed AMC controller eliminates any bulky compensation capacitor and is implemented in only 0.092 mm^2 area. The output current density of the proposed AMC converter is 1.32 A/mm^2, which is the highest among prior art buck converters in Table II. The proposed AMC converter achieves the fast transient response while having low switching frequency, which can maintain high efficiency of the converter. It should be noted that unsynchronous converters sacrifice the EMI due to uncertain switching frequency to achieve a fast step response. However, the proposed synchronous converter provides a fast transient response with a fixed switching frequency thanks to the novel AMC controller.

In addition, the fast reference step response of the proposed converter makes it a good choice for DVS applications. A figure of merit (FOM) [23] is presented in Table II as

$$\text{FOM} = \frac{\text{Settling Time } (\mu s)}{\text{Peak Eff. } (\%) \times \text{Load Step } (A) \times \text{Max } I_{OUT} \ (A)}. \quad (22)$$

The proposed AMC converter shows a fast 2.3 μs settling time during a large 1.3 A load step and has the highest peak efficiency in Table II. As a result, it achieves a 1.02 FOM, which is the best among state of the arts in Table II. A settling time to clock

period ratio (STPR) parameter can be defined as a controller optimization FOM, which is more than 10 for synchronous converters in Table II. The STPR for unsynchronous designs in Table II is mostly less than 10, which shows that unsynchronous arts have shorter settling time than synchronous ones. However, they suffer undesired EMI issues. The STPR for the proposed AMC buck converter is 2–2.3, which shows an impressive improvement among synchronous arts and is also better than most unsynchronous designs.

VI. Conclusion

In this article, an optimum settling time over inductor current or output voltage perturbed condition is considered for a synchronous buck converter. Using transient time analysis, it has been theoretically proven that at least two clock periods are needed for a synchronous buck converter with an LC output filter to settle. Based on the presented analysis the optimum STOP condition to minimize the settling time of the synchronous buck converter is extracted and an AMC structure is proposed to realize the optimum STOP condition achieving the optimum of two clock cycle settling time over any perturbed output voltage or inductor current conditions. The proposed AMC structure utilizes an analog multiplier and a novel t_r generator. Moreover, a novel DOR block is introduced to remove the steady-state error of V_{OUT}. The digital implementation of the DOR eliminates the area consuming capacitor used in typical offset removers. The proposed design has been implemented in a 180 nm BCD technology with a 910 μm $\times$ 1500 μm die size. The proposed AMC buck converter achieves a fast 2 μs– 2.3 μs settling time for 1.3 A load step and a 3 μs–3.5 μs settling time for 1 V reference step, which is impressive for DVS application. Furthermore, The AMC buck converter has a high output current density of 1.32 A/mm^2 with 96$\%$ peak efficiency.

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