An Easy-to-Implement Flexible Commutation Design With Reduced Switching Losses, di/dt and dv/dt for High-Speed and High-Power IGBTs

Yikang Xiao, *Student Member, IEEE*, Shiqi Ji, *Senior Member, IEEE*, Mingyu Yang, *Student Member, IEEE*, and Zhengming Zhao, *Fellow, IEEE*

***Abstract*—The high-frequency and high-power operation of power converters has imposed stringent requirements on the switching loss and electromagnetic interference performance of power devices, particularly for the increasingly popular high-speed insulated-gate bipolar transistors (IGBTs). Conventional soft-switching techniques with snubbers encounter significant challenges in high-frequency and high-power scenarios due to their inherent complexity and the substantial influence of parasitic parameters. This article presents an easy-to-implement flexible commutation design aimed at reducing switching losses, di/dt and dv/dt simultaneously in high-speed power IGBTs for high-frequency and high-power applications. The proposed design includes a snubber capacitor and two printed-circuit-board-based coupled inductors as the busbar, facilitating soft-switching conditions for the IGBTs, along with a lossless energy recovery circuit to achieve lossless operations. Importantly, the design incorporates only passive components and specially utilizes distributed parasitic parameters, ensuring both ease of implementation and high performance. The proposed design is experimentally validated through double-pulse tests using a high-power and high-speed IGBT rated at 1.2 kV/140 A, with the switching performance analyzed comprehensively in comparison to a conventional hard-switching design.**

***Index Terms*—di/dt and dv/dt, flexible commutation design, high-frequency and high-power converter, high-speed insulated-gate bipolar transistors (IGBTs), switching loss.**

I. Introduction

HIGH-FREQUENCY converters have become increasingly attractive for modern high-power conversion applications such as renewable energy systems [1], [2], data center power supplies [3], [4], electric vehicle charging [5], [6], and motor drives [7]. The primary advantage of high-frequency operation is the reduction in size and weight of passive components, such as filter inductors and capacitors, which leads to increased power density and reduced costs. In addition, higher switching frequencies enable faster response times and reduced harmonics. In high-frequency and high-power applications, insulated gate bipolar transistors (IGBTs) are preferred over metal-oxide-semiconductor field-effect transistors (MOSFETs) and gallium-nitride high-electron-mobility transistors due to their superior voltage and current handling capabilities. Recently, high-speed IGBTs have been commercially developed, which can operate at frequencies ranging from tens to hundreds of kilohertz [8], [9], [10]. However, high-frequency operation significantly increases switching losses, which account for a large portion of total energy dissipation. Furthermore, high-frequency operation demands power semiconductor devices with high switching speeds, introducing challenges such as increased voltage and current stresses and substantial electromagnetic interference (EMI) due to high di/dt and dv/dt. To mitigate these issues, soft-switching techniques are employed.

Soft switching can be achieved through converter-level topology design. Resonant converters, one of the earliest soft-switching methods [1], [11], [12], [13], [14], [15], [16] have gained considerable attention in recent years, particularly LLC-based converters (e.g., *LLC*, *CLLC*, *CLLLC*). These converters employ a resonant tank, composed of inductors and capacitors, in combination with appropriate control strategies to achieve zero-voltage switching (ZVS) or zero-current switching (ZCS) conditions for the power switches. While resonant converters reduce switching losses and facilitate high-frequency operation, they also present several challenges, including topology limitations, as well as increased conduction losses and high voltage and current stresses resulting from the circulating energy, and the need for wide-frequency-range operation due to pulse-frequency-modulation control.

In contrast, power-switch-level soft-switching designs, such as snubber circuits, offer the advantage of preserving traditional pulsewidth modulation (PWM) control while achieving soft switching. These designs incorporate auxiliary switches and LC components into the commutation loop to create soft-switching conditions without altering the overall converter topology. The additional switches and LC components function only during the commutation processes, allowing the converter to revert to traditional PWM operation once the power switches are in their steady ON/OFF states. This approach decouples power-switch-level commutation from converter-level control, making it applicable across a wide range of topologies and control strategies.

Over the past several decades, various active and passive snubber circuits have been proposed. Active snubber circuits

Received 29 October 2024; revised 4 March 2025; accepted 9 April 2025. Date of publication 14 April 2025; date of current version 30 June 2025. This work was supported by the Program of National Natural Science Foundation of China under Grant 52277189. Recommended for publication by Associate Editor D. Dong. *(Corresponding author: Shiqi Ji.)*

The authors are with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: chic2020@tsinghua.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3560679.

Digital Object Identifier 10.1109/TPEL.2025.3560679

employ auxiliary active switches and LC components to manage switching transitions [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]. Notable active snubber circuits include zero-voltage transition (ZVT) [17], [18], [19], [20], [21], [22], [23], [24], [25] and zero-current transition (ZCT) [20], [23], [25], [26], [27], [28], [29] circuits, which utilize LC components and appropriate control of auxiliary switches to achieve soft-switching for the main power switches during switching transitions. A key challenge in designing ZVT and ZCT circuits is ensuring soft switching for both main and auxiliary switches to enhance overall efficiency. Furthermore, the resonant nature of these circuits subjects auxiliary switches to higher stresses than the main switches, increasing costs. The need for high-bandwidth sensors, control, and gate drive circuits for auxiliary switches adds complexity and reduces reliability as well.

Passive snubber circuits offer a simpler, more cost-effective, and reliable alternative to active methods, as they require only passive diodes and LC components. Traditional passive snubbers, such as the resistor-capacitor-diode snubber, are easy to implement and effective in reducing turn-OFF losses and suppressing voltage stresses [30], [31], [32], [33], [34], [35]. However, the resistive elements in these circuits result in inefficiencies, especially at high switching frequencies, limiting their application to low-power and low-frequency scenarios. Recently, nondissipative snubbers have been proposed [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48]. Some provide either soft turn-ON or soft turn-OFF conditions. For example, in [36], a snubber capacitor is applied in parallel with the power switch to provide ZVS turn-OFF condition. This snubber is effective for the dual-active-bridge (DAB) converter as the converter normally operates in ZVS turn-ON condition. However, the snubber will induce large turn-ON current stresses and losses when the DAB converter loses its ZVS condition. And this snubber is not suitable for traditional hard-switching power converters either. Meanwhile, Kwon et al. [37] proposed a snubber that achieves zero-voltage turn-ON for the active power switch. But the power switch operates under hard turn-OFF conditions. Conversely, other nondissipative snubbers achieve both soft turn-ON and soft turn-OFF simultaneously [38], [39], [40], [41], [42]. However, these designs often face topology limitations, making them applicable to boost/buck structures and less suitable for half-bridge or full-bridge configurations. In addition, they often induce higher voltage and current stresses on the main power switches. Previous works, such as [46], [47], [48], have explored the properties required for effective snubber circuits that simultaneously can achieve soft turn-ON and soft turn-OFF conditions and synthesized a series of snubber topologies for both buck/boost and half/full-bridge structures.

However, several common challenges associated with existing solutions persist in high-power, high-frequency applications.

1) *Complexity*: Existing designs often incorporate a great number of high-voltage and high-current components, which complicates the overall system. This can also introduce additional constraints in terms of heat management, efficiency, and reliability, particularly when scaling for higher power levels.
2) *Challenges of lumped elements*: The use of lumped elements in snubbers presents several technical challenges. For instance, the lumped inductors are required to handle high currents without saturating when the power switches are in the steady ON/OFF states, resulting in increased losses, volume, weight, and costs.
3) *Difficulties in layout design*: As switching speeds and frequencies rise, the inductance and capacitance values required for snubbers are often in the nanohenry (nH) and nanofarad (nF) ranges, which are comparable to the parasitic parameters in the commutation loop. Consequently, parasitic parameters can significantly impact and even participate in the snubbing process in high-frequency and high-speed scenarios, leading to difficult layout design of the commutation loop.

To address these challenges, this article proposes an easy-to-implement flexible commutation design aimed at reducing switching losses, di/dt and dv/dt of the high-speed IGBTs used in high-frequency, high-power converters. The proposed design targets systems operating at voltages ranging from hundreds to thousands of volts and currents in the several hundred ampere range, with switching frequencies spanning from tens to hundreds of kilohertz. The main features of the design include the following.

1) *Soft-switching performance and lossless operation*: The proposed design enables both soft turn-ON and soft turn-OFF for the main power switches and auxiliary diodes, effectively reducing switching losses. Furthermore, it avoids the use of resistive elements, ensuring a lossless operation of the snubber circuit.
2) *Low voltage and current stresses*: By carefully managing the parasitic parameters and utilizing the inherent inductances of printed circuit board (PCB) traces, the design ensures smooth operation of the main power IGBTs, without causing additional voltage and current stresses theoretically.
3) *Minimal auxiliary component requirements*: The proposed design employs only passive components, eliminating the need for complex control systems or sensors. It requires only three high-voltage components (one capacitor and two diodes), while the remaining components are rated for low voltage and current levels. The high-voltage capacitor is rated at half the voltage of the dc input, while the diodes have voltage ratings equivalent to the dc input. Notably, all these high-voltage components only need low current ratings.
4) *Easy implementation with full utilization of parasitic parameters*: The design constructs an optimal power current commutation path in a spatially concise and clear manner, and develops a corresponding PCB layout which incorporates the parasitic inductance generated by PCB traces into the overall design of the snubber circuit, facilitating a smaller overall design size compared to alternatives utilizing lumped inductors or lumped coupled inductors. In addition, it eliminates the need for a magnetic core in the coupled inductors, reducing both volume and weight while avoiding additional losses.

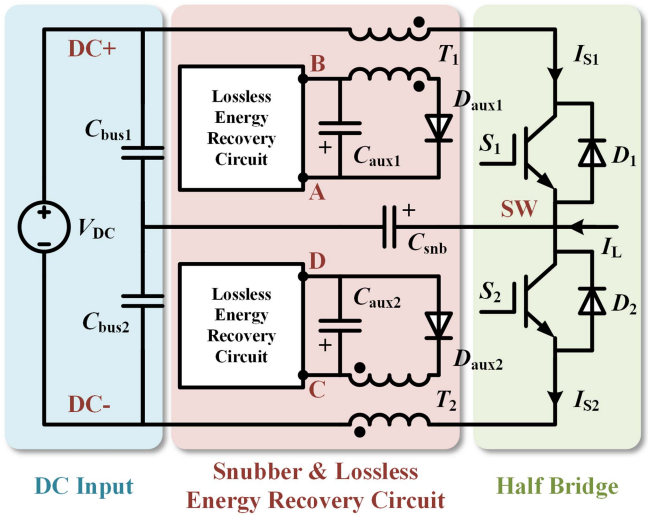


Fig. 1. Schematic circuit of the proposed design.

5) *Topology generalizability*: The proposed design supports the basic half-bridge structure and can be easily extended to other configurations, such as full-bridge and three-phase bridge structures.

The rest of this article is organized as follows. Section II provides the schematic circuit of the proposed design. The implementation method of the proposed design is discussed in Section III, highlighting the design of the PCB-based distributed coupled inductors and summarizing the requirements for each component, demonstrating the easy-to-implement characteristic of the proposed design. The operating principles, including theoretical waveforms and the current paths for all circuit modes, are elaborated in Section IV. Double-pulse tests (DPTs) are conducted on both the proposed design and the conventional hard-switching design in Section V, where the key switching performances and the influences of circuit parameters in the proposed design are analyzed. Finally, Section VI concludes this article.

II. Schematic Circuit of the Proposed Design

Fig. 1 illustrates the schematic circuit of the proposed commutation design for the half-bridge structure utilizing IGBT devices (S_1 and S_2). This configuration includes a snubber circuit and a lossless energy recovery circuit (ERC). The snubber circuit consists of a snubber capacitor (C_{snb}), two coupled inductors (T_1 and T_2), two auxiliary capacitors (C_{aux1} and C_{aux2}), and two auxiliary diodes (D_{aux1} and D_{aux2}). The lossless ERC is depicted in Fig. 2, which consists of two diodes (D_{erc1} and D_{erc2}), an inductor (L_{erc}) and a capacitor (C_{erc}).

In this design, the ZCS turn-ON condition for S_1 and S_2 is facilitated by the primary-side self-inductances of T_1 and T_2, while the ZVS turn-OFF condition is ensured by C_{snb}. When either S_1 or S_2 turns ON (depending on the direction of the load current), the load current commutates directly from one IGBT to the other, inducing significant voltage drops across T_1 and T_2. These voltage drops allow the voltage across S_1 (V_{S1}) or S_2 (V_{S2}) to decrease rapidly before its current increases.

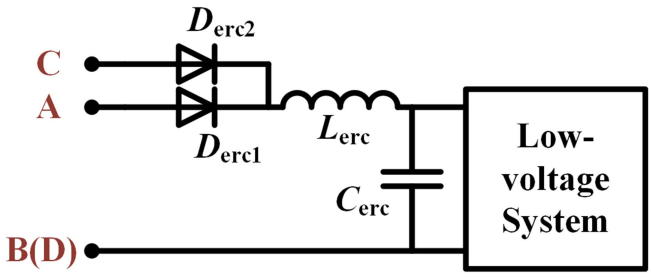


Fig. 2. Schematic circuit of the lossless ERC.

After the IGBT is fully turned on under ZCS conditions (i.e., the voltage across the IGBT drops to its on-state voltage), the current begins to rise. During this phase, T_1 and T_2 serve to limit the current slew rate (di/dt). Similarly, when S_1 or S_2 turns OFF, the load current commutates first from one IGBT to C_{snb}, and subsequently from C_{snb} to the other IGBT. The existence of C_{snb} facilitates a rapid decrease in the current flowing through S_1 (I_{S1}) or S_2 (I_{S2}) before the voltage begins to rise. Once the IGBT is fully turned-OFF under ZVS conditions (i.e., the current flowing through the IGBT drops to zero), its voltage begins to rise, meanwhile C_{snb} limits the voltage slew rate (dv/dt).

The negative impact on the turn-OFF voltage overshoots induced by T_1 and T_2 is mitigated through their secondary-side circuits. Specifically, during the turn-OFF transient of either S_1 or S_2, both D_{aux1} and D_{aux2} conduct, clamping the voltages across T_1 and T_2 through capacitors C_{aux1} and C_{aux2}, thus preventing additional voltage spikes across S_1 and S_2. Moreover, the negative impact on the turn-ON current overshoots caused by C_{snb} is also eliminated by the cooperation of T_1, T_2, D_{aux1}, D_{aux2}, C_{aux1}, and C_{aux2}. Specifically, when S_1 or S_2 turns ON, C_{snb} is discharged by the resonance between C_{snb}, T_1 and T_2. The existence of T_1 and T_2 prevents the direct short-circuiting of C_{snb} upon IGBT turn-ON, thereby avoiding surge currents in the IGBT. During the resonance process, when the currents flowing through the primary windings of T_1 and T_2 begin to decrease, D_{aux1} and D_{aux2} turn-ON, and the resonant energy is absorbed by C_{aux1} and C_{aux2}. Consequently, the energy in T_1, T_2, and C_{snb} is softly transferred to C_{aux1} and C_{aux2}, resetting the components without inducing additional turn-OFF voltage overshoot or turn-ON current overshoot on S_1 and S_2.

The energy stored in C_{aux1} and C_{aux2} is further recycled by the lossless ERC. In this circuit, C_{aux1}/C_{aux2}, D_{erc1}/D_{erc2}, L_{erc}, and C_{erc} form a resonant pathway, through which the energy stored in C_{aux1} and C_{aux2} is transferred unidirectionally to C_{erc}. The energy accumulated in C_{erc} is then used to power the low-voltage subsystems, including components such as the sensing system, control circuitry, gate drivers, cooling fans, and other elements operating within the voltage range from 5 to 24 V.

In the proposed design, the turn-ON and turn-OFF losses of the IGBTs can be flexibly controlled by adjusting the C_{snb} and the self-inductances of T_1 and T_2. Larger self-inductances of T_1 and T_2 improve the turn-ON switching losses of the IGBTs, but may also lead to higher turn-OFF voltage overshoots even though with high coupling coefficients. On the other hand, a larger C_{snb} helps to decrease the turn-OFF switching losses, but may also result in

higher turn-ON current overshoots during the resonance process. The value of C_{snb} can be easily controlled through appropriate device selection. And the self-inductances of T_1 and T_2 can be precisely controlled by designing the geometrical dimensions of the winding loops.

Therefore, the key of this design lies in the implementation of T_1 and T_2, which establish the pathways for power current commutation. It is essential that T_1 and T_2 are designed with high coupling coefficients, superior efficiency, robust current-handling capabilities, compact sizes and weights, and a sufficient level of simplicity. Consequently, the following section offers a detailed discussion on the implementation and the dimensional design equations of T_1 and T_2.

III. Implementation of the PCB-Based Distributed Coupled Inductors Through DC Busbar Design

A. Integration of Coupled Inductors Within DC Busbar Design

In conventional dc busbar designs, laminated configurations are typically employed to minimize stray inductance in the commutation loop, as excessive stray inductance can lead to detrimental effects such as voltage spikes and additional switching losses, particularly in high-speed switching applications. However, this article introduces a novel approach where the stray inductance of the dc busbar is not merely tolerated but purposefully designed to function as the distributed coupled inductors T_1 and T_2. By strategically engineering the distributed parameters of the dc busbar, the coupled inductor structure can be realized directly within the busbar itself, eliminating the need for additional discrete magnetic components. In this implementation, the stray inductance of the dc busbar are deliberately increased, enabling ZCS conditions for the IGBTs during their switching transients.

Given the high switching speeds at which IGBTs operate, the role of the coupled inductors in this system is primarily to regulate the di/dt during the switching transient, while having minimal impact on steady-state operation. Thus, the self-inductances of these coupled inductors must remain low, typically in the range of 50–100 nH. Since switching transients occur on extremely short-time scales, where the voltage and current waveforms exhibit high-frequency components in the tens of megahertz, the designed coupled inductors must ensure excellent high-frequency performance while also maintaining high coupling coefficients to facilitate efficient energy transfer from the primary side—where voltage and current spikes occur—to the secondary side, where this energy can be absorbed. Furthermore, during the steady-state operation, the coupled inductors will be subjected to relatively large currents, necessitating careful attention to magnetic saturation and core losses in the design.

Considering these requirements—high-frequency operation, high current handling, and low inductance values—traditional lumped inductor designs that rely on bulky ferrite cores and cylindrical conductors are not ideal for this application. Instead, this article presents a distributed coupled inductor design that is well-suited for integration into PCBs, leveraging the intrinsic distributed inductance of the dc busbar itself. The PCB-based distributed coupled inductor design offers several notable advantages: First, the design capitalizes on the stray inductance inherent in the current commutation path through the PCB layout. This inherent inductance can be engineered to meet the required values without the need for large, bulky magnetic components. Second, the flat planar copper conductor structure of the PCB enhances high-frequency performance compared to conventional cylindrical copper wires. This is particularly important as the flat conductors help mitigate issues such as the skin effect, thereby enhancing the current handling capacity and reducing high-frequency losses. Another significant advantage of the PCB-based design lies in the ease with which the primary and secondary windings of the coupled inductors can be accurately laminated within the PCB layers. This layer-coupling configuration allows for a much higher coupling coefficient ensuring efficient energy transfer and absorption of transient spikes.

By embedding the coupled inductors within the dc busbar design, this approach optimally utilizes the available PCB real estate while simultaneously enhancing circuit performance. The proposed integration method enables the dc busbar to play an additional role to support commutation and facilitate ZCS conditions, leading to improved switching performances.

B. Implementation of the Coupled Inductors

The distributed coupled inductors proposed in this article are composed of the following four distinct loops.

1) *Loop #1P:* the primary-side loop of T_1.
2) *Loop #1S:* the secondary-side loop of T_1.
3) *Loop #2P:* the primary-side loop of T_2.
4) *Loop #2S:* the secondary-side loop of T_2.

It is important to clarify the coupling relationships between these loops by analyzing the spatial current commutation paths. To illustrate the coupling dynamics, consider the turn-OFF transient of S_2 as an example. In the initial stage of the turn-OFF process, the load current commutates from S_2 to C_{snb}, leading to a significant variation of the magnetic field linked with *Loop #2P*, which induces a substantial voltage. In response, *Loop #2S* is designed to absorb the induced voltage, and the magnetic field generated by the current in *Loop #2S* must spatially compensate for the magnetic field variation caused by *Loop #2P*. Therefore, it is essential that *Loop #2P* and *Loop #2S* overlap completely to ensure effective coupling. In the latter part of the turn-OFF process of S_2, the load current commutates from C_{snb} to S_1, leading to a similar change in the magnetic field associated with *Loop #1P*, which also induces a large voltage. To absorb this voltage, *Loop #1S* must be well-laminated with *Loop #1P*.

As a result, the PCB layout for the proposed distributed coupled inductors can be designed as depicted in Fig. 3. The dc+ and dc− polygon planes are laminated to minimize stray inductance between the dc input and the bus capacitors (C_{bus1} and C_{bus2}). The PCB traces connecting the bus capacitors and the IGBTs are intentionally designed as two large loops, forming the primary-side windings of the distributed coupled inductors. Specifically, the branches containing C_{bus1}, C_{snb}, and S_1 on the top layer form *Loop #1P*, while the loop comprising C_{bus2}, C_{snb},

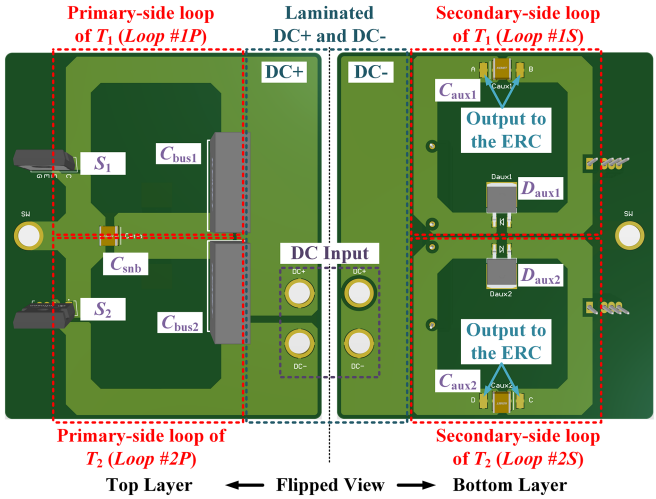


Fig. 3. Top and bottom view of the layout design of the PCB-based distributed coupled inductors.

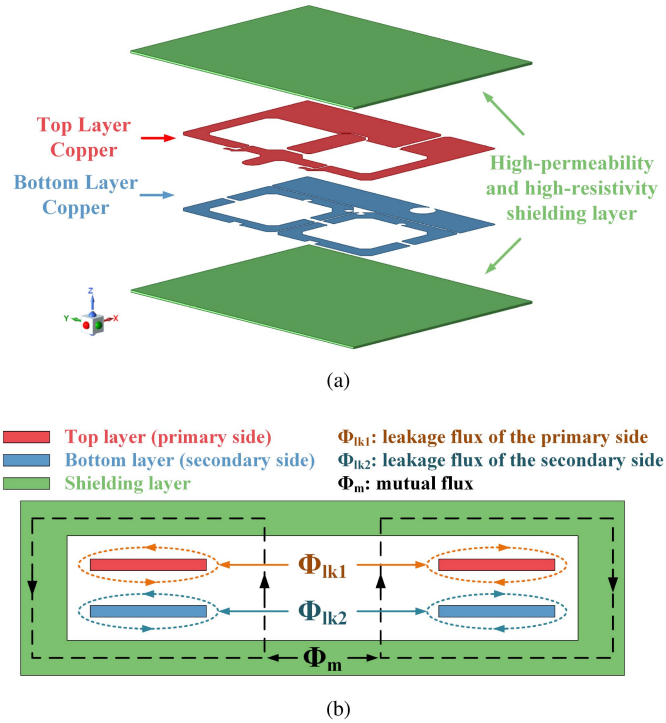


Fig. 4. Shielding design with high-permeability layers to achieve a higher coupling coefficient and reduced EMI. (a) Layer structure. (b) Side cross-sectional view.

and S_2 on the top layer forms *Loop #2P*. On the bottom layer, the loop consisting of C_{aux1} and D_{aux1} forms *Loop #1S*, and the loop consisting of C_{aux2} and D_{aux2} forms *Loop #2S*. To ensure high coupling coefficients for both T_1 and T_2, *Loop #1P* is fully overlapped with *Loop #1S*, and *Loop #2P* is entirely overlapped with *Loop #2S*.

To further enhance the coupling coefficients, two shielding layers composed of high-permeability and high-resistivity materials can be applied to the upper and lower surfaces of the PCB, as depicted in Fig. 4(a). A side cross-sectional view of

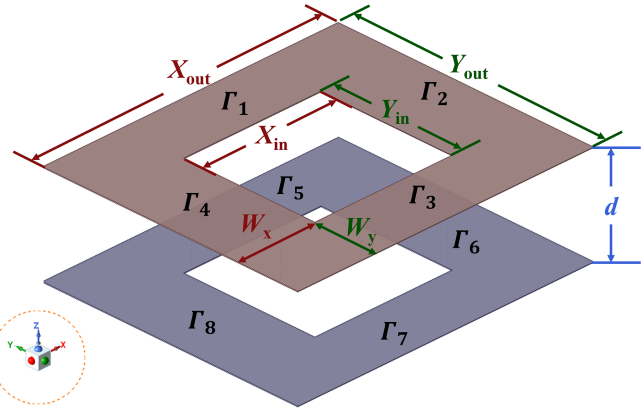


Fig. 5. Simplified layout for analyzing the PCB-based distributed coupled inductors.

the design, along with the magnetic flux distribution, is presented in Fig. 4(b). These shielding layers serve to confine the magnetic flux within the designed structure, thereby reducing EMI to the surrounding environment. Moreover, the shielding layer enhances the permeability of the mutual magnetic flux (Φ_m) path while minimally impacting the permeability of the leakage flux (Φ_{lk1} and Φ_{lk2}) paths, significantly improving the coupling coefficients of the coupled inductors. The shielding layer's design is particularly advantageous because it lacks a central magnetic limb, which prevents the overall magnetic flux from becoming excessively large and potentially leading to saturation of the magnetic material. In addition, the high resistivity of the shielding layer reduces eddy current losses, further improving the system's efficiency.

C. Equivalent Circuit of the Coupled Inductors

For simplicity, both the primary and secondary windings of the distributed coupled inductors are modeled as single-turn rectangular spiral coils, as illustrated in Fig. 5. The four conductor edges that make up the primary winding are designated as Γ_1 to Γ_4, while the four conductor edges of the secondary winding are designated as Γ_5 to Γ_8. The lengths of the outer sides of the coils are represented as X_{out} and Y_{out}, while the lengths of the inner sides are represented as X_{in} and Y_{in}. The trace widths of the coils can be calculated as $W_x = (X\text{out} - X_{\text{in}})/2$ and $W_y = (Y_{\text{out}} - Y_{\text{in}})/2$. The distance between the primary and secondary coils is denoted as d, which is approximately equal to the thickness of the PCB.

The equivalent circuit of the PCB-based distributed coupled inductors, considering the parasitic parameters, is shown in Fig. 6(a). In this equivalent circuit, $L_{\text{lk},p}$ and $L_{\text{lk},s}$ represent the leakage inductances of the primary and secondary sides, respectively, while L_m denotes the magnetizing inductance. C_p denotes the equivalent lumped capacitance of the primary winding, which accounts for the effects of interturn and interlayer capacitances within the primary winding. Similarly, C_s denotes the equivalent lumped capacitance of the secondary winding. C_w represents the interwinding capacitance between the primary and secondary windings. Since both the primary and secondary windings of the coupled inductor consist of a single turn and

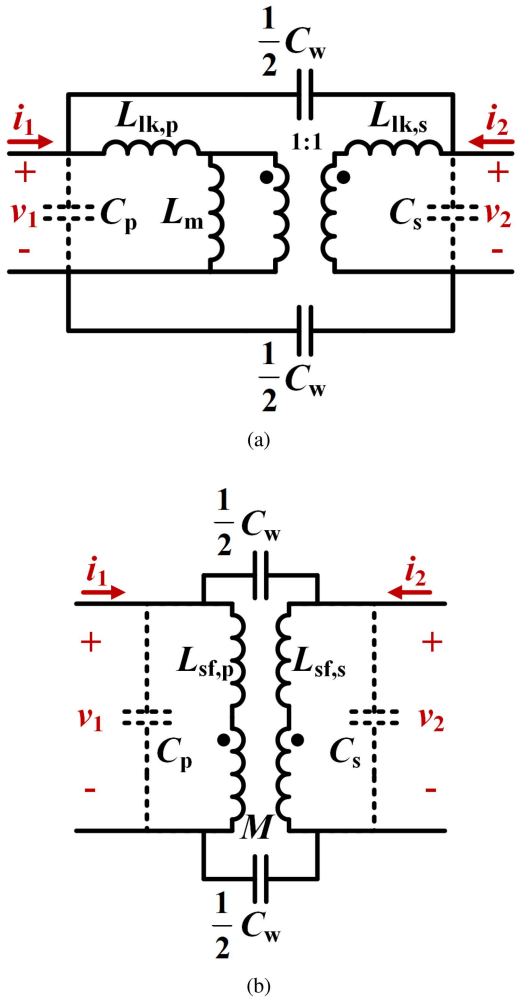


Fig. 6. Equivalent circuit of the PCB-based distributed coupled inductors considering the parasitic parameters. (a) Transformer form. (b) Coupled inductor form.

a single layer, the capacitances C_p and C_s are negligible. C_w can be calculated using the parallel-plate capacitor model, as expressed in (1), where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the free-space permittivity, and ε_r represents the relative permittivity of the PCB material. For the commonly used FR-4 material, $\varepsilon_r \approx 4.4$

$$C_w = \frac{\varepsilon_0 \varepsilon_r \left(X_{\text{out}} Y_{\text{out}} - X_{\text{in}} Y_{\text{in}}\right)}{d}. \tag{1}$$

The circuit shown in Fig. 6(a) can be transformed into its equivalent form, as illustrated in Fig. 6(b), where $L_{\text{sf},p}$ and $L_{\text{sf},s}$ represent the self-inductances of the primary side and secondary side, and M denotes the mutual inductance between the primary and secondary windings. The relationship between the two circuit forms can be expressed as follows:

$$L_{\text{sf},p} = L_{\text{lk},p} + L_m \tag{2a}$$

$$L_{\text{sf},s} = L_{\text{lk},s} + L_m \tag{2b}$$

$$M = L_m. \tag{2c}$$

The coupling coefficient κ of the coupled inductor is defined as (3). In the rest of this article, the mutual inductances (or

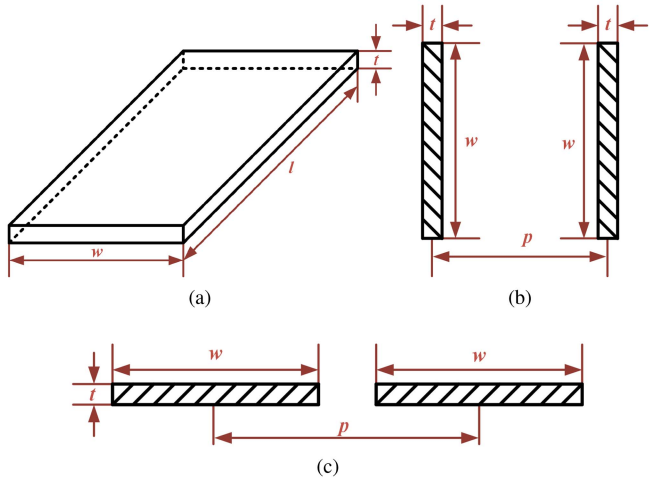


Fig. 7. Finite straight rectangular conductor. (a) Single conductor. (b) Cross-section of two conductors with width-to-width configuration. (c) Cross-section of two conductors with thickness-to-thickness configuration.

magnetizing inductances, which are equal in this case) of T_1 and T_2 are denoted by L_{m1} and L_{m2}, respectively. The primary-side self-inductances of T_1 and T_2 are represented by $L_{\text{sf},1p}$ and $L_{\text{sf},2p}$, while the secondary-side self-inductances are denoted by $L_{\text{sf},1s}$ and $L_{\text{sf},2s}$

$$\kappa = \frac{L_m}{\sqrt{L_{\text{sf},p} L_{\text{sf},s}}}. \tag{3}$$

D. Dimensional Design Equations of the Coupled Inductors

According to the Greenhouse's formula [49], the *partial self-inductance* of a finite straight rectangular conductor [as shown in Fig. 7(a)] with width w, thickness t, and length l, can be calculated as (4), where μ_0 and μ_r are the free-space permeability and the relative permeability of the conductor. For copper material, $\mu_r \approx 1$. The correction factor T is frequency-dependent: it is equal to 1 under dc conditions and approaches 0 as the frequency tends to infinity. GMD and AMD represent the *geometrical mean distance* and the *arithmetical mean distance*, respectively. For thin-film conductors, such as PCB traces, GMD $\approx 0.22313(w+t)$ and AMD $\approx (w+t)/3$

$$L_{\text{sf, partial}} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{\text{GMD}}\right) - 1.25 + \frac{\text{AMD}}{l} + \frac{\mu_r T}{4}\right]. \tag{4}$$

The *partial mutual inductance* between two finite straight conductors is given by (5).

$$L_{m,\text{partial}} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{\text{GMD}} + \sqrt{1 + \frac{l^2}{\text{GMD}^2}}\right) - \sqrt{1 + \frac{\text{GMD}^2}{l^2}} + \frac{\text{GMD}}{l}\right]. \tag{5}$$

The expressions for GMD depend on the configuration of the two conductors. There are two primary configurations for two rectangular conductors: width-to-width [as shown in Fig. 7(b)]

or thickness-to-thickness [as shown in Fig. 7(c)]. Assuming the two conductors are separated by a distance p and $\gamma = w/p$, the GMD for these configurations can be calculated by (6a) and (6b), respectively [49], [50], [51]

$$\ln \frac{\text{GMD}}{p} = \frac{\gamma^2 - 1}{\gamma^2} \ln(1+\gamma) + \frac{2}{\gamma} \arctan \gamma - \frac{3}{2} \tag{6a}$$

$$\ln \frac{\text{GMD}}{p} = -\frac{\gamma^2}{12} - \frac{\gamma^4}{60} - \frac{\gamma^6}{168} - \frac{\gamma^8}{360} - \frac{\gamma^{10}}{660} - \cdots. \tag{6b}$$

Next, the *loop self-inductance* of the primary-side (or secondary-side) winding can be calculated as the sum of the partial self-inductances of all its edges, minus the sum of the partial mutual inductances of its parallel edges, as expressed by (7). Here, L_{sf,Γ_i} represents the partial self-inductance of Γ_i, and $L_{m,\Gamma_i\Gamma_j}$ represents the partial mutual inductance between Γ_i and Γ_j. Note that the partial mutual inductance between two orthogonal conductors is zero, so only the mutual inductances of parallel conductors contribute to the total loop self-inductance

$$L_{\text{sf},p} = L_{\text{sf},s} = \sum_{i=1}^{4} L_{\text{sf},\Gamma_i} - 2\left(L_{m,\Gamma_1\Gamma_3} + L_{m,\Gamma_2\Gamma_4}\right). \tag{7}$$

The *loop mutual inductance* between the primary-side and secondary-side windings can be calculated as the sum of the partial mutual inductances of all parallel primary and secondary conductors, as expressed in (8). Note that the partial mutual inductance between two parallel conductors carrying currents in the same direction is positive, while it is negative for conductors with currents in opposite directions

$$L_m = 2\left(L_{m,\Gamma_1\Gamma_5} + L_{m,\Gamma_2\Gamma_6} - L_{m,\Gamma_1\Gamma_7} - L_{m,\Gamma_2\Gamma_8}\right). \tag{8}$$

Equations (4)–(8) provide a dimensional design guideline for the coupled inductors. In practical design, the target values of the self-inductance and mutual inductance should be determined first. Then, the geometrical dimensions of the primary and secondary loops are derived using the above equations. Finite element analysis can be employed to validate the design and extract precise inductance values. To achieve the desired inductance values, the dimensions of the PCB traces should be optimized through iterative design. For example, increasing the size of the loop (i.e., increasing X_{in}, X_{out}, Y_{in}, and Y_{out}) can help increase both the self-inductance and mutual inductance of the coupled inductor. In addition, decreasing the distance d will improve the mutual inductance and coupling coefficient. However, decreasing d too much may reduce the mechanical strength of the PCB, leading to potential structural issues.

E. Case Study and the Impacts of Parasitic Parameters

In this article, the target values of $L_{\text{sf},p}$ and $L_{\text{sf},s}$ are set to approximately 50–60 nH based on practical experience. The dimensions of the coupled inductors are then designed according to (4)–(8), as shown in Table I. It should be noted that the length l in (4) and (5) should be replaced with the *effective length* of the conductor. For example, the effective length of Γ_1 can be calculated as (9), where $\lambda \in (0, 2)$ is a calibration factor. In this case, $\lambda \approx 0.7$

$$l_{\text{eff}} = X_{\text{in}} + \lambda W_x. \tag{9}$$

TABLE I
GEOMETRICAL DIMENSIONS OF THE COUPLED INDUCTORS

Dimension	Value (mm)	Dimension	Value (mm)
X_{in}	28.6	Y_{in}	27.3
X_{out}	61.6	Y_{out}	53.2
d	0.6	t	0.14

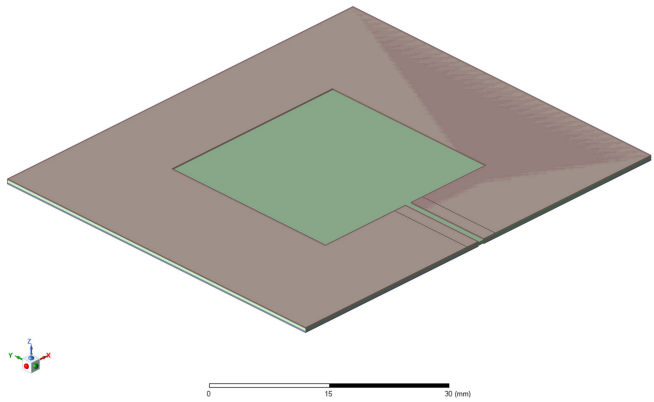


Fig. 8. Ansys Q3D model of the coupled inductors.

TABLE II
CALCULATION AND SIMULATION RESULTS

Parameter	Frequency	Value (formula)	Value (simulation)	Relative error
$L_{sf,p(s)}$ (nH)	@f = 0 Hz	56.61	56.07	0.96%
	@f = ∞	48.96	48.9	0.12%
L_m (nH)	@f = 0 Hz	52.09	53	–1.72%
C_w (pF)	/	211.41	241.13	–12.33%

An Ansys Q3D model, as shown in Fig. 8, is built to precisely extract the parasitic inductances. Table II shows the calculation results using (1), (4)–(8), and the simulation results from Ansys Q3D. The calculation results show high accuracy compared with the simulation, which validates the analysis and design procedure described above.

The leakage inductances can negatively impact the IGBTs during commutation, producing excessive voltage overshoots as the IGBT currents decrease. In an ideal case with no leakage inductance and a coupling coefficient of 1, the voltage across $L_{\text{sf},1p}$ and $L_{\text{sf},2p}$ is clamped by C_{aux1} and C_{aux2} when D_{aux1} and D_{aux2} conduct, which absorbs the voltage overshoots on the IGBTs. However, when leakage inductances are considered, the equivalent circuit from the primary sides of T_1 and T_2 during the turn-OFF transient process becomes as shown in Fig. 9. The equivalent busbar inductance and the voltage overshoot produced by the busbar inductance are then calculated as (10) and (11). Although both the formula calculations and simulation results show a low leakage inductance of about 3–4 nH and a high coupling coefficient of about 0.95, the actual leakage inductance can be higher than these results due to the equivalent series

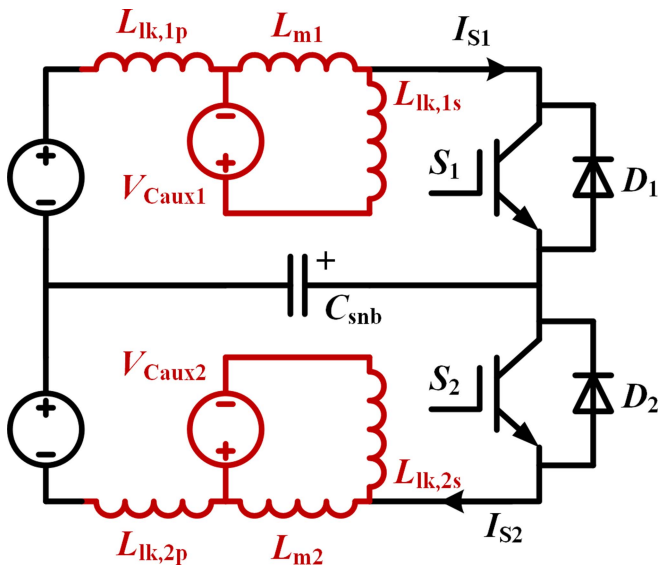


Fig. 9. Equivalent circuit during the turn-OFF transient considering the leakage inductances.

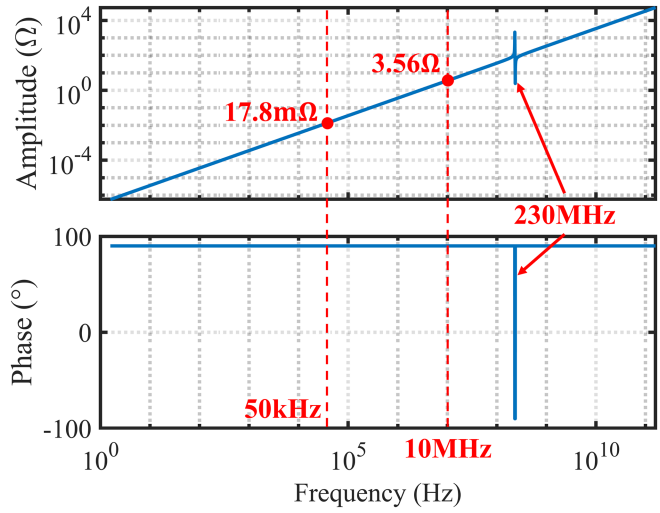


Fig. 10. Impedance characteristics of the coupled inductor considering C_w.

inductance (ESL) of the components, including the IGBTs, C_{snb}, C_{aux1}, C_{aux2}, D_{aux1}, and D_{aux2} in the primary and secondary loops

$$L_{\text{eq}} = L_{\text{lk},p} + \frac{L_m L_{\text{lk},s}}{L_m + L_{\text{lk},s}} = \left(1 - \kappa^2\right) L_{\text{sf},p} \tag{10}$$

$$v_{\text{os}} = L_{\text{eq}} \left(\frac{dI_{S1}}{dt} + \frac{dI_{S2}}{dt} \right). \tag{11}$$

The parasitic capacitance C_w mainly affects the resonant frequency of the coupled inductor and may cause unwanted oscillations, producing extra losses at high frequencies. However, in this article's case, it has very little impact on the switching transients. From Fig. 6, the impedance view from the primary side (with the secondary side open) is expressed as (12), where $\omega = 2\pi f$ represents the angular frequency

$$Z_{11} = \frac{v_1}{i_1} = j\omega \frac{\omega^2 C_w \left(L_{\text{sf},p} L_{\text{sf},s} - L_m^2\right) - 4L_{\text{sf},p}}{\omega^2 C_w \left(L_{\text{sf},p} + L_{\text{sf},s} - 2L_m\right) - 4}. \tag{12}$$

Then, the resonant frequency can be calculated by (13). In this case, the resonant frequency is 230 MHz, which is much higher than the frequency components of the switching transients (typical below 20 MHz). Fig. 10 shows the impedance characteristics calculated from (12), which exhibit ideal inductance behavior across most frequency bands, except near the resonant frequency. Therefore, the parasitic capacitance has very little impact on the switching transients

$$f_{\text{res}} = \frac{1}{\pi \sqrt{\left(L_{\text{sf},p} + L_{\text{sf},s} - 2L_m\right) C_w}}. \tag{13}$$

Another important observation from Fig. 10 is that the coupled inductors are primarily active during the switching transients, which occur on the order of 100 ns. These transients correspond to a frequency range typically around 10 MHz. However, during the steady-state operation of the IGBTs, where the switching frequency is generally below 50 kHz, the impedance of the coupled inductors becomes negligible, effectively behaving as a short circuit.

This observation is confirmed by the impedance calculations presented in (12), where the impedances at 50 kHz and 10 MHz are 17.8 mΩ and 3.56 Ω, respectively. This low impedance at the switching frequency indicates that the coupled inductors do not have a significant effect on the steady-state performance of the IGBTs. Consequently, the influence of the IGBT's switching frequency on the inductor design is minimal, as the inductor's role is primarily limited to the switching transient period. The inductor does not actively engage in the circuit's behavior during the steady-state operation, which is crucial for ensuring that the design of the coupled inductors does not compromise the IGBT's static performances.

F. Implementation of Other Components

C_{snb}: C_{snb} is rated at only $V_{\text{DC}}/2$, which reduces both the cost and size of the snubber. The capacitance of C_{snb} typically ranges from several to tens of nF, which is comparable to the output capacitance of the IGBTs. Since that C_{snb} is also part of *Loop #1P* and *Loop #2P*, it is important to ensure that it possesses a low ESL to maintain high coupling coefficients. Multilayer ceramic capacitors (MLCCs), known for their compact size and low ESL, are, therefore, a suitable choice for C_{snb}. Furthermore, C_{snb} must exhibit stable capacitance and a low dissipation factor. To meet these requirements, Class I ceramic capacitors, such as C0G capacitors, are recommended.

D_{aux1} and D_{aux2}: To ensure effective absorption of voltage overshoots, fast turn-ON and turn-OFF characteristics are required for D_{aux1} and D_{aux2}. Silicon-carbide (SiC) Schottky barrier diodes (SBDs) are recommended. Theoretically, D_{aux1} and D_{aux2} must be rated to withstand a maximum transient voltage of V_{DC} during the turn-ON transients of the IGBTs. Consequently, the voltage ratings of D_{aux1} and D_{aux2} should correspond to the dc-bus voltage, which is considerably lower than the voltage rating of the main power IGBTs because of the voltage margin required in practical applications. However,

TABLE III
COMPONENT REQUIREMENTS OF THE PROPOSED DESIGN

Components	Values	Voltage ratings	Current ratings	Other requirements	Suggested devices
C_{snb}	several to tens of nanofarads	$V_{DC}/2$	About 10% of the IGBTs	Low ESL, low dissipation factor, stable capacitance	C0G MLCC
D_{aux1} and D_{aux2}	/	V_{DC}		Fast turn-ON and turn-OFF	SiC SBD
C_{aux1} and C_{aux2}	several to tens of microfarads	Low	Low	Low ESL	MLCC
D_{erc1} and D_{erc2}	/	Low	Low	/	SMD or IC
L_{erc}	several to tens of microhenries				
C_{erc}	several to tens of microfarads				

the current ratings of D_{aux1} and D_{aux2} can be significantly lower than those of the IGBTs, as D_{aux1} and D_{aux2} only conduct current during switching transients. No current flows through D_{aux1} or D_{aux2} in steady states.

C_{aux1}* and *C_{aux2}: These capacitors absorb the transient energy stored in T_1 and T_2 during the switching transients of the IGBTs. Since that the transient energy is relatively small, capacitors rated at low voltages (e.g., several tens of volts) can be used. Their capacitances typically range from several to tens of microfarads (uF). Moreover, because these capacitors are part of *Loop #1S* and *Loop #2S*, a low ESL is required to ensure high coupling coefficients. Therefore, MLCCs are suitable for C_{aux1} and C_{aux2}.

Components in the lossless ERC: The lossless ERC is designed to handle the relatively small energy stored in C_{aux1} and C_{aux2}. Therefore, all components within the lossless ERC are rated for low voltages and currents, resulting in low costs and minimal impact on the overall commutation design layout. Suitable surface-mount devices (SMDs) or integrated circuits (ICs) can be selected as the components for the lossless ERC. Moreover, since the lossless ERC operates at relatively low frequencies, component design requirements are less stringent. Ordinary rectifier diodes can be utilized as D_{erc1} and D_{erc2}. And parasitic parameters in the recycle loop have minimal impact, negating the need for special layout optimization.

In summary, the proposed design requires only three high-voltage-low-current components (C_{snb}, D_{aux1} and D_{aux2}), while all other components are rated for low voltages and low currents. The component requirements of the proposed design are summarized in Table III.

IV. OPERATING PRINCIPLES

This section presents a theoretical analysis of the commutation process of the proposed design. The scenario considers a load current injecting into the mid-node of the half-bridge. In this case, S_1 remains inactive while the antiparallel diode D_1 functions as the freewheeling diode (FWD) for S_2. The load current can be treated as a constant current source during the commutation process. The theoretical operation waveforms of the proposed design are illustrated in Fig. 11, while Fig. 12 shows the current paths for each mode. The theoretical analysis of the commutation process is described as follows.

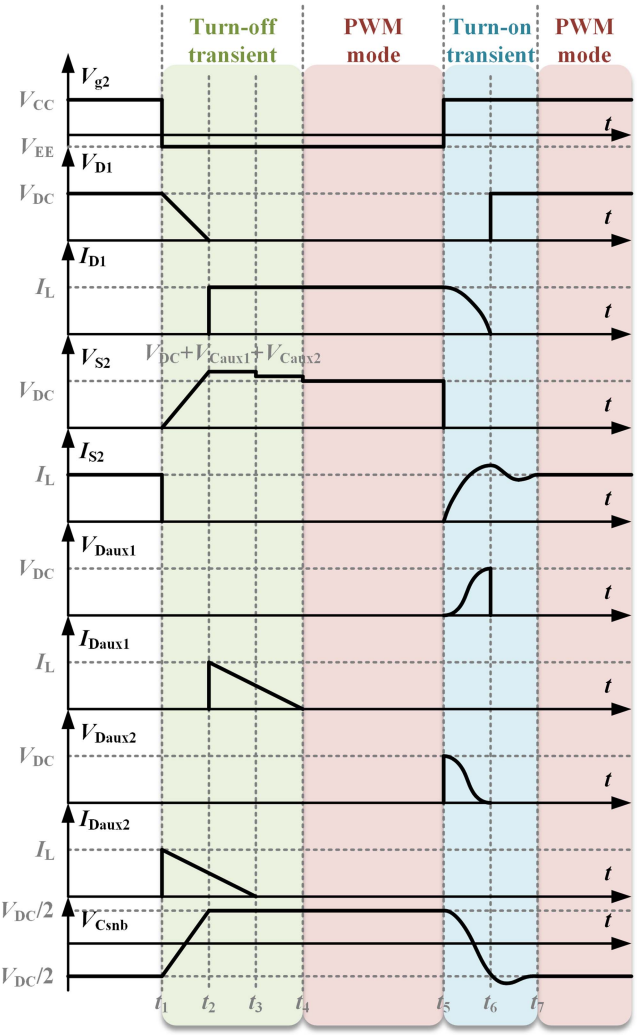


Fig. 11. Theoretical operation waveforms of the proposed design.

A. Turn-Off Commutation

Mode 1 ($t_1 - t_2$): At t_1, the gate drive voltage of S_2 (V_{g2}) transitions from the high value of V_{CC} to the low value of V_{EE}, resulting in the turn-OFF of S_2. The presence of C_{snb} enables S_2 to turn-OFF under ZVS conditions. Consequently, the load current is transferred to C_{snb} from S_2, leading to a linear rise in the voltage across C_{snb} (V_{Csnb}) from $-V_{DC}/2$, as expressed by

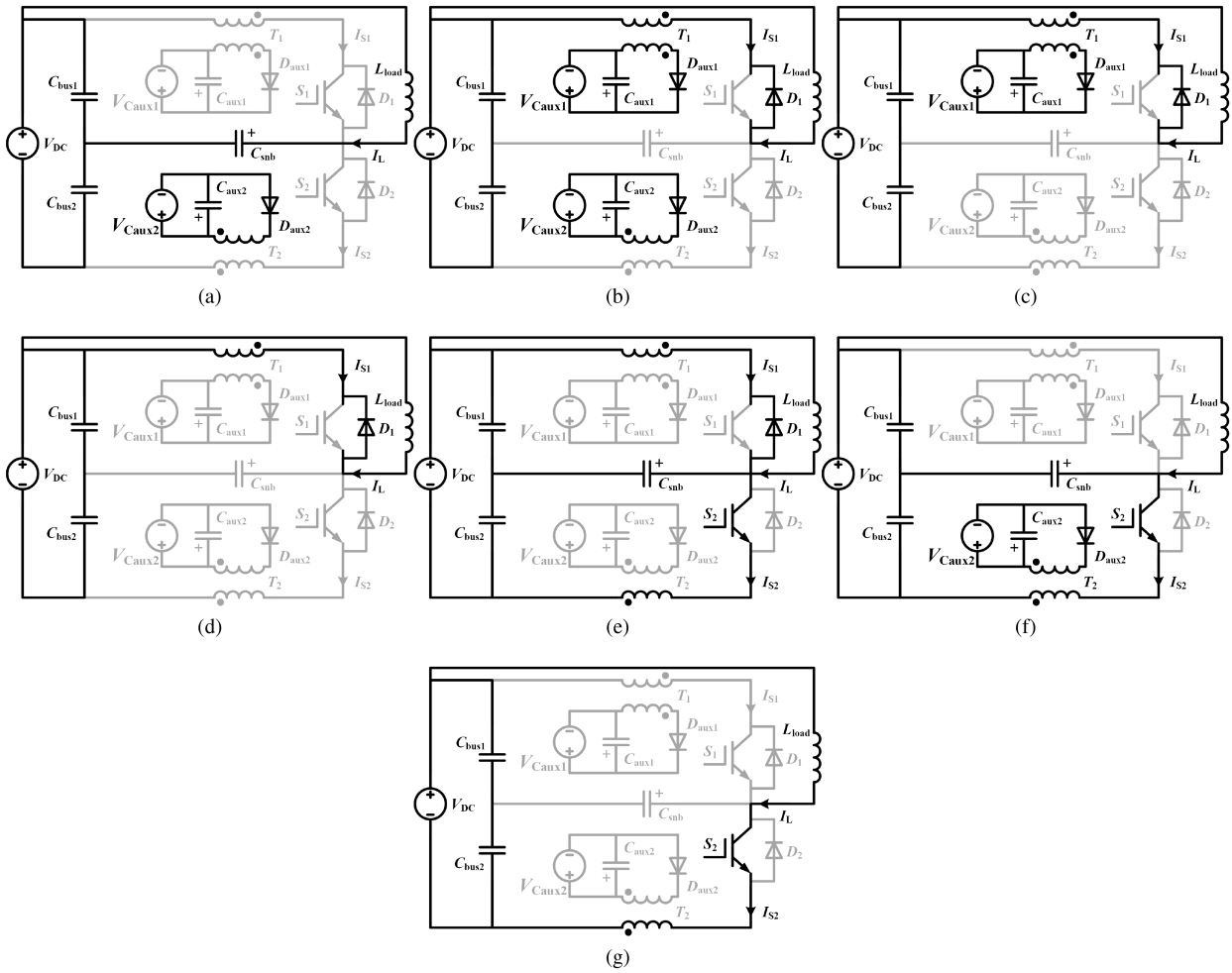


Fig. 12. Current paths of the proposed design at each mode. (a) Mode 1($t_1 - t_2$). (b) Mode 2($t_2 - t_3$). (c) Mode 3($t_3 - t_4$). (d) Mode 4($t_4 - t_5$). (e) Mode 5($t_5 - t_6$). (f) Mode 6($t_6 - t_7$). (g) Mode 7 (after t_7).

(14). Meanwhile, D_{aux2} conducts, clamping the voltage across T_2 through C_{aux2}, thereby suppressing the voltage overshoot on S_2. The energy in T_2 is subsequently transferred to C_{aux2} and recycled by the lossless ERC, causing the current through D_{aux2} ($I_{D\text{aux2}}$) to gradually decrease

$$C_{\text{snb}} \frac{dv_{C\text{snb}}}{dt} = I_L. \tag{14}$$

Mode 2 ($t_2 - t_3$): At t_2, $V_{C\text{snb}}$ reaches $V_{\text{DC}}/2$, activating D_1 under ZVS conditions. The load current shifts from C_{snb} to D_1, generating an induced voltage across T_1. Subsequently, D_{aux1} conducts, and the voltage across T_1 is clamped by C_{aux1}, further suppressing voltage overshoots on S_2. Energy stored in T_1 is transferred to C_{aux1} and recycled by the lossless ERC, causing the current flowing through D_{aux1} ($I_{D\text{aux1}}$) to diminish during this mode. In the ideal scenario, where the coupling coefficients for both T_1 and T_2 are equal to one, the theoretical voltage spike of V_{S2} is given by $V_{\text{DC}} + V_{C\text{aux1}} + V_{C\text{aux2}}$.

Mode 3 ($t_3 - t_4$): At t_3, $I_{D\text{aux2}}$ reaches zero, resulting in D_{aux2} turning OFF under ZCS conditions. At this stage, the energy stored in T_2 is fully recycled.

Mode 4 ($t_4 - t_5$): At t_4, when $I_{D\text{aux1}}$ falls to zero, D_{aux1} turns OFF under ZCS conditions. The energy stored in both T_1 and T_2 is fully recycled, marking the end of the turn-OFF commutation. S_2 then enters into the steady-OFF state.

B. Turn-On Commutation

Mode 5 ($t_5 - t_6$): The turn-ON commutation begins at t_5 when V_{g2} increases from V_{EE} to V_{CC}. $L_{\text{sf},1p}$ and $L_{\text{sf},2p}$ enable a ZCS turn-ON condition for S_2. V_{S2} is perceived as a sudden drop from V_{DC} to 0 at t_5. $L_{\text{sf},1p}$ and $L_{\text{sf},2p}$ then resonate with C_{snb} under the influence of V_{DC} and I_L. I_{S2} increases, while the current flowing through D_1 (I_{D1}) decreases. A discharging current flows through C_{snb}, causing $V_{C\text{snb}}$ to drop from $V_{\text{DC}}/2$. The secondary sides of T_1 and T_2 are blocked by D_{aux1} and D_{aux2}. The state equations of the DPT circuit during this mode can be expressed as

$$\begin{aligned} I_{S1} &= I_{S2} + C_{\text{snb}} \frac{dV_{C\text{snb}}}{dt} \\ L_{\text{sf},1p} \frac{dI_{S1}}{dt} &+ V_{C\text{snb}} - \frac{1}{2} V_{\text{DC}} = 0 \\ L_{\text{sf},2p} \frac{dI_{S2}}{dt} &- V_{C\text{snb}} - \frac{1}{2} V_{\text{DC}} = 0. \end{aligned} \tag{15}$$

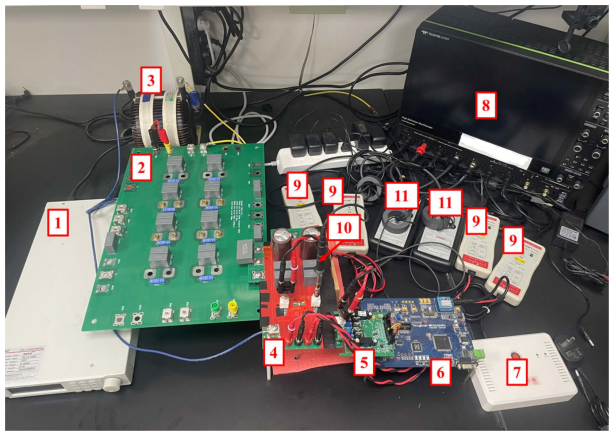


Fig. 13. Picture of the DPT platform. (1: DC power supply; 2: Laminated DC busbar; 3: Load inductance; 4: PCB of the proposed design; 5: Gate drive board; 6: Control board; 7: Power supply for the control board; 8: Oscilloscope; 9: High-voltage differential probes; 10: High-voltage passive probe; 11: High-frequency Rogowski coils.).

Mode 6 ($t_6 - t_7$): When I_{D1} falls to zero, D_1 turns OFF under ZCS conditions. $L_{sf,2p}$ continues to resonate with C_{snb}. As I_{S2} begins to decline, D_{aux2} activates, allowing the secondary side of T_2 to absorb the resonant energy, effectively dampening the resonance.

Mode 7 (after t_7): At t_7, when all resonant energy is fully dissipated, S_2 transitions into the steady-on state.

V. Experimental Verification

The proposed design is implemented and verified in a DPT platform, as depicted in Fig. 13. The high-power, high-speed TRENCHSTOP IGBT7 IKY140N120CH7 from Infineon, rated at 1200 V/140 A and housed in a TO-247-4 package, serves as the device under test. The SiC SBD C6D10065 G from Wolfspeed, rated at 650 V/10 A and housed in a TO-263-2 package, is selected as D_{aux1} and D_{aux2}. A double-pulse signal is applied to the gate terminal of S_2, while S_1 remains in the OFF state via a constant negative gate drive voltage.

V_{S2} is measured using a high-voltage passive probe with a bandwidth of 300 MHz, while V_{S1} is measured using a high-voltage differential probe with a bandwidth of 100 MHz. Both I_{S1} and I_{S2} are measured by high-frequency Rogowski coils with a bandwidth of 50 MHz. Table IV details the equipment used in the DPT platform, and Table V provides the circuit parameters of the DPT platform. As a comparison, a DPT PCB utilizing a conventional hard-switching design is also implemented and tested within the same platform. Figs. 14 and 15 showcase the PCBs of the proposed design and the conventional hard-switching design, respectively.

A. Inductance Extraction

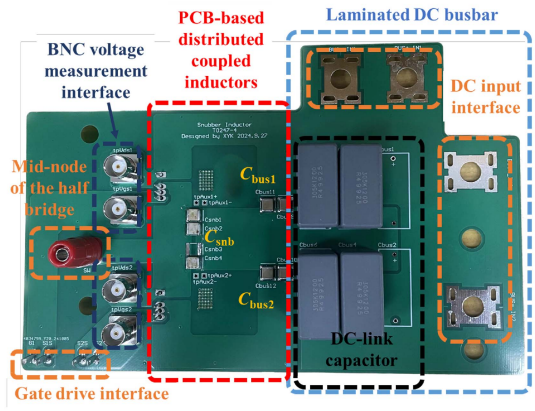
The electronic network analyzer E5061B from Keysight is employed to measure the impedance characteristics of the designed PCB by analyzing its scattering parameters (S-parameters). In this study, the Port 1-2 Shunt Through method is utilized for S-parameter measurement. Fig. 16 illustrates the test

TABLE IV
Equipment Information

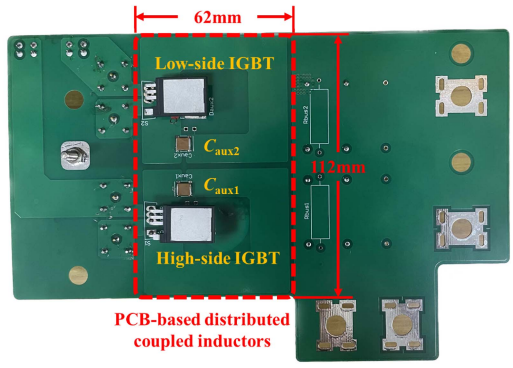
Equipment	Manufacturer	Product model	Ratings	Signal under test
DC power supply	VARIED	RU-18-10001	0-1 kV, 0-1 A	/
Oscilloscope	Teledyne LeCroy	HDO6054B	500 MHz, 10 GS/s	/
High-voltage differential probe	PINTECH	N1015A	1.5 kV, 100 MHz	V_{S1}
High-voltage passive probe	TT-HV150	TESTEC	1.5 kV, 300 MHz	V_{S2}
High-frequency Rogowski coil	PEM	CWT Mini 50HF 1/B	300 A, 50 MHz	I_{S1} and I_{S2}

TABLE V
Circuit Parameters

Parameter	Value	Parameter	Value
V_{DC}	600 V	V_{CC} / V_{EE}	+15 V/0 V
I_L	0–140 A	$R_{g,ext}$	0–3 Ω
L_{load}	300 uH	C_{snb}	6.6–13.2 nF
C_{aux1} and C_{aux2}	1 uF		



(a)



(b)

Fig. 14. PCB of the proposed design. (a) Top view. (b) Bottom view.

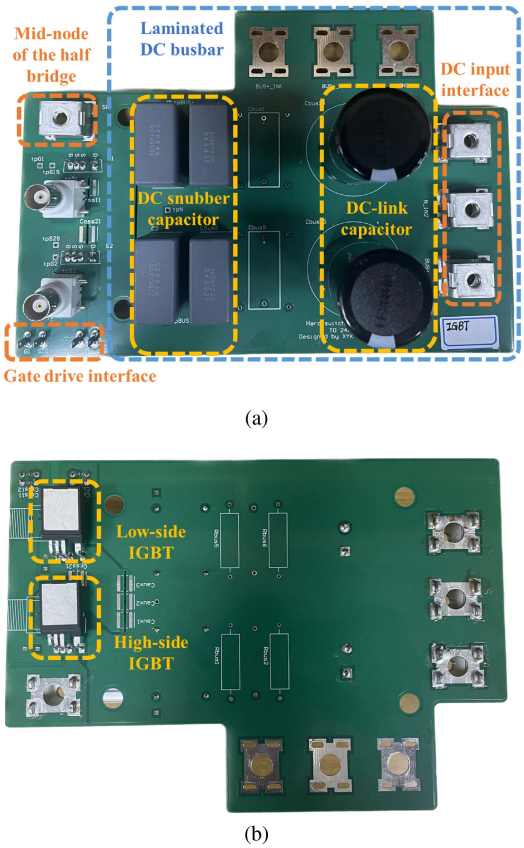


Fig. 15. PCB of the conventional hard-switching design. (a) Top view. (b) Bottom view.

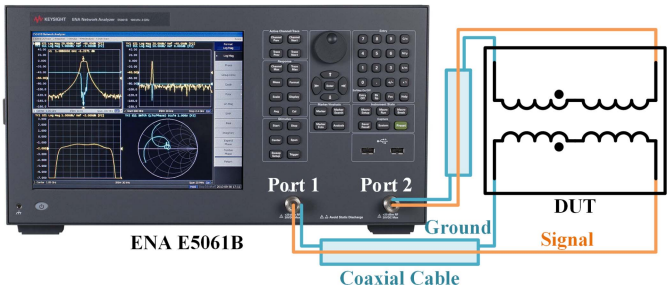


Fig. 16. Test setup for measuring the S-parameters.

setup. S-parameters, shown in Fig. 17(a), describe the reflection and transmission characteristics of a two-port network in the frequency domain and are defined in (16), where a_1 and a_2 represent the incident waves at port 1 and port 2, while b_1 and b_2 correspond to the reflected or transmitted waves at the respective ports

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = \mathbf{S} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}. \tag{16}$$

The impedance parameters (Z-parameters), shown in Fig. 17(b) and defined in (17), can be derived from S-parameters using (18), where Z_0 is the characteristic impedance of the

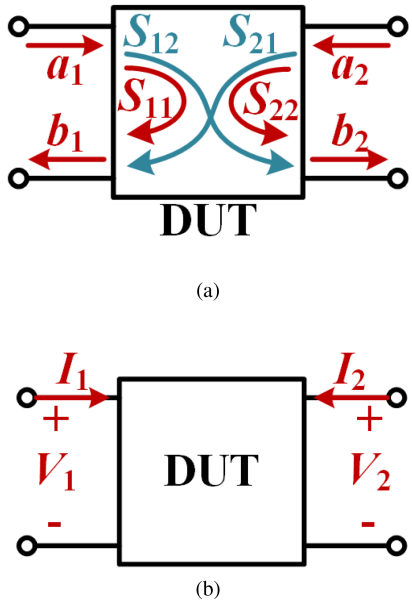


Fig. 17. Diagram of a two-port network. (a) S-parameters. (b) Z-parameters.

system (typically 50 Ω), and $\mathbf{I}$ is the identity matrix

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \mathbf{Z} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{17}$$

$$\mathbf{Z} = Z_0(\mathbf{I} + \mathbf{S})(\mathbf{I} - \mathbf{S})^{-1}. \tag{18}$$

In this case, the parameters Z_{11} and Z_{22} directly indicate the self-inductance of the primary and secondary sides of the PCB-based distributed coupled inductors, while $Z_{12} = Z_{21}$ represents the mutual inductance between the primary and secondary sides, as expressed in (19). Consequently, the inductance parameters can be efficiently extracted by processing the measured impedance data using curve fitting techniques

$$\begin{aligned} Z_{11} &= j\omega L_{\mathrm{sf},p} \\ Z_{22} &= j\omega L_{\mathrm{sf},s} \\ Z_{12} &= Z_{21} = j\omega L_m. \end{aligned} \tag{19}$$

Fig. 18 presents the curve fitting results of the Z-parameters, where the extracted inductance parameters are $L_{\mathrm{sf},p} = 53.89\,\mathrm{nH}$, $L_{\mathrm{sf},s} = 52.97\,\mathrm{nH}$, and $L_m = 46.89\,\mathrm{nH}$.

The designed PCB is also imported into Ansys Q3D to extract its inductance parameters, as shown in Fig. 19. The simulation results yield $L_{\mathrm{sf},p} = 56.98\,\mathrm{nH}$, $L_{\mathrm{sf},s} = 54.35\,\mathrm{nH}$, and $L_m = 45.65\,\mathrm{nH}$, demonstrating good agreement with the measured results. The self-inductances of the primary and secondary sides closely match their target values (approximately 56 nH) calculated in Section III-E. However, the actual mutual inductance is lower than the target value (around 52 nH), primarily due to the large dc bus plane on the primary side, which results in imperfect alignment between the primary and secondary current loops. The measured results yield a coupling coefficient of 0.88, which remains acceptable for this application.

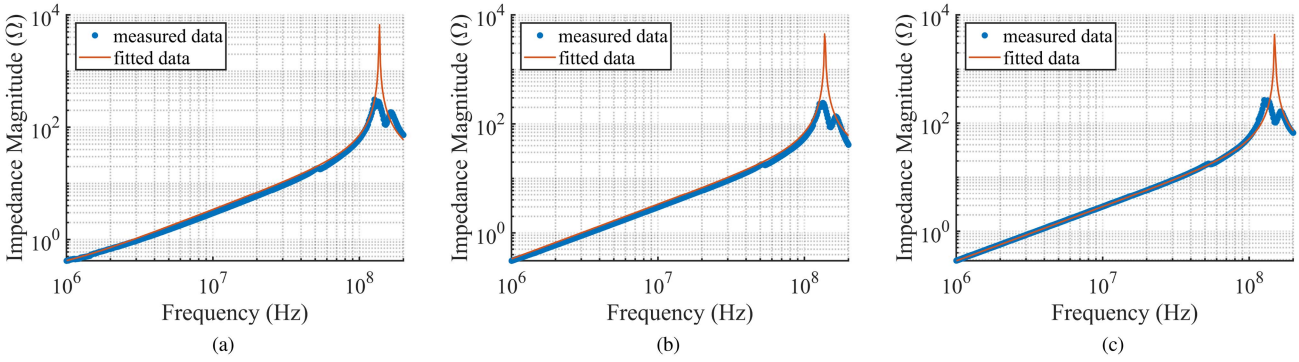


Fig. 18. Curve fitting results of the Z-parameters. (a) Z_{11}. (b) Z_{22}. (c) Z_{12}, Z_{21}.

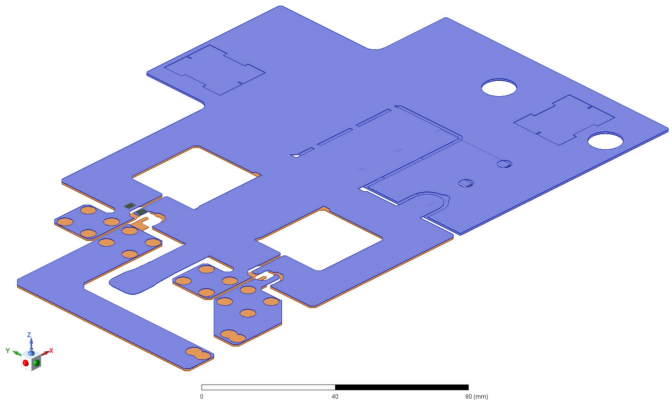


Fig. 19. Ansys Q3D model of the designed PCB.

B. Switching Transient Waveforms Compared to the Conventional Hard-Switching Design

Fig. 20 presents the experimental switching transient waveforms and the switching loss power calculated by $V_{S2} \times I_{S2}$ for both the conventional hard-switching design and the proposed design under test conditions of $V_{\text{DC}} = 600\,\text{V}$, $I_L = 70\,\text{A}$, and $R_{g,\text{ext}} = 0.4\,\Omega$. In Fig. 20(a), the V_{S2} waveform of the proposed design demonstrates a sharp drop from 600 V to approximately 200 V at the onset of the rise in I_{S2}, indicating that S_2 turns ON under ZCS conditions. Similarly, as shown in Fig. 20(b), the I_{S2} waveform exhibits a rapid decrease from 70 A to around 30 A as V_{S2} begins to rise, demonstrating that S_2 turns OFF under ZVS conditions. Consequently, the overlap between the voltage and current waveforms in the proposed design is significantly reduced compared to the conventional hard-switching design, directly contributing to lower switching losses. The turn-ON and turn-OFF losses for the conventional hard-switching design are measured at 1.17 mJ and 1.79 mJ, respectively. In contrast, the proposed design exhibits turn-ON and turn-OFF losses of 1.04 mJ and 1.05 mJ, corresponding to reductions of 11.2% and 41.3%, respectively. As will be discussed in Section V-C, these reductions on switching losses are even more pronounced at higher load currents.

In addition to significantly reducing switching losses, the proposed design effectively maintains acceptable levels of voltage and current spikes. Specifically, the conventional hard-switching design exhibits a current spike of 207.9 A during the turn-ON transient and a voltage spike of 736.5 V during the turn-OFF transient. In comparison, the proposed design shows a comparable current spike of 219.6 A and voltage spike of 814.2 V. Although the current and voltage overshoots in the proposed design are 5.6% and 10.6% higher than that observed in the conventional design, this increase remains within acceptable limits. As will be illustrated in Section V-C, when the load current is higher, the current overshoot in the proposed design can be smaller than that of the conventional hard-switching design. Therefore, the proposed design is capable of reducing switching losses without significantly increasing voltage and current spikes.

Furthermore, both the dv/dt during the turn-OFF transient and the di/dt during the turn-ON transient are substantially lower in the proposed design compared to the conventional hard-switching design. In addition, the reduced di/dt also contribute to lower reverse recovery losses in the FWDs, further enhancing the overall efficiency of the system.

C. Switching Performances Under Various Load Currents

The switching performances, including switching losses, voltage, and current overshoots, di/dt and dv/dt, are evaluated under various load currents (18 A, 36 A, 54 A, 73 A, 92 A, 112 A, and 132 A) while maintaining a constant $V_{\text{DC}} = 600\,\text{V}$ and an external gate resistor $R_{g,\text{ext}} = 0.4\,\Omega$.

Fig. 21 presents a comparison of the switching loss components between the proposed design and the conventional hard-switching design, where E_{on}, E_{off}, E_{rec}, E_{sw}, and E_{tot} denote the turn-ON loss of the IGBT, turn-OFF loss of the IGBT, reverse recovery loss of the FWD, the switching loss of the IGBT ($E_{\text{sw}} = E_{\text{on}} + E_{\text{off}}$) and the total loss of the commutation unit ($E_{\text{sw}} = E_{\text{on}} + E_{\text{off}} + E_{\text{rec}}$), respectively.

At load currents below 54 A, the E_{on} of the proposed design is slightly higher than that of the conventional hard-switching design, attributable to the higher current overshoot in the proposed design under light load conditions. However, as the load current exceeds 54 A, the E_{on} of the proposed design becomes much smaller compared to that of the conventional hard-switching design, benefiting from the ZCS feature as previously described. The E_{off} of the proposed design is consistently lower than that of

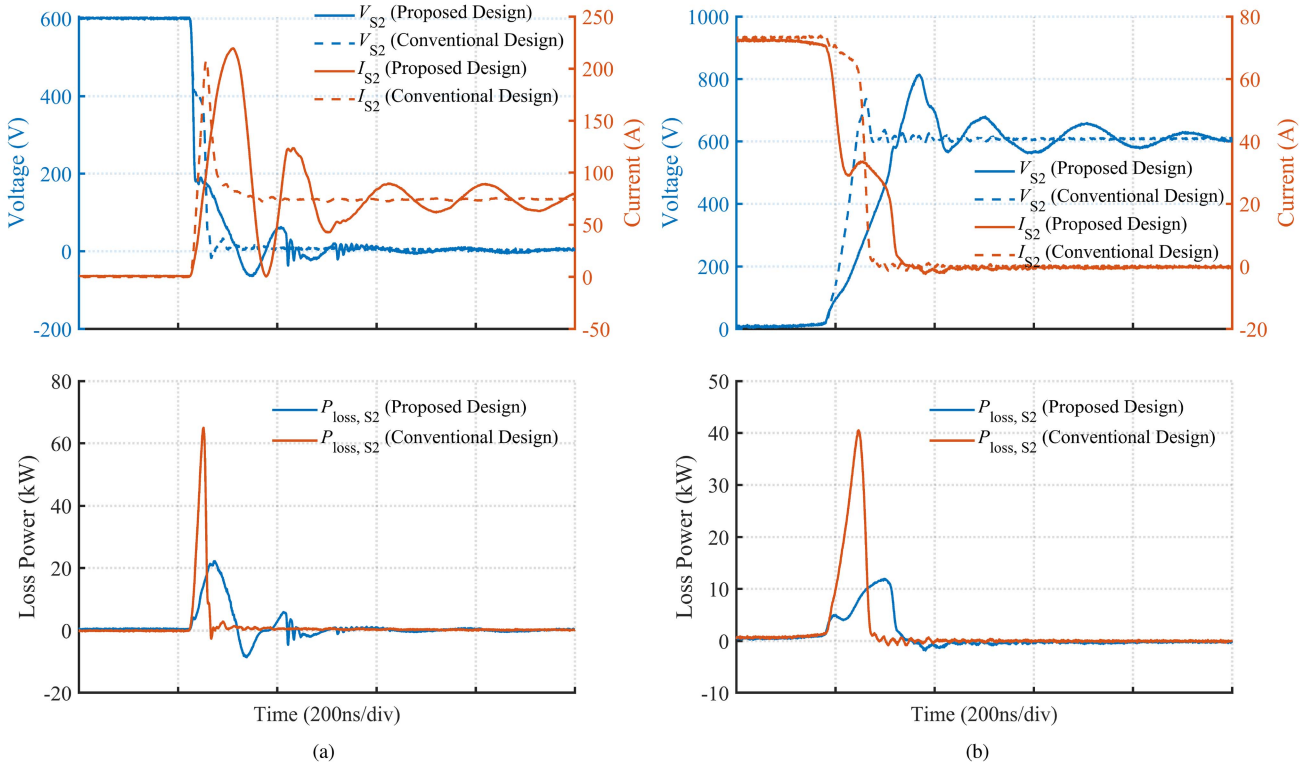


Fig. 20. Comparison of the switching transient waveforms and switching losses between the conventional hard-switching design and the proposed design. (a) Turn-ON transient. (b) Turn-OFF transient.

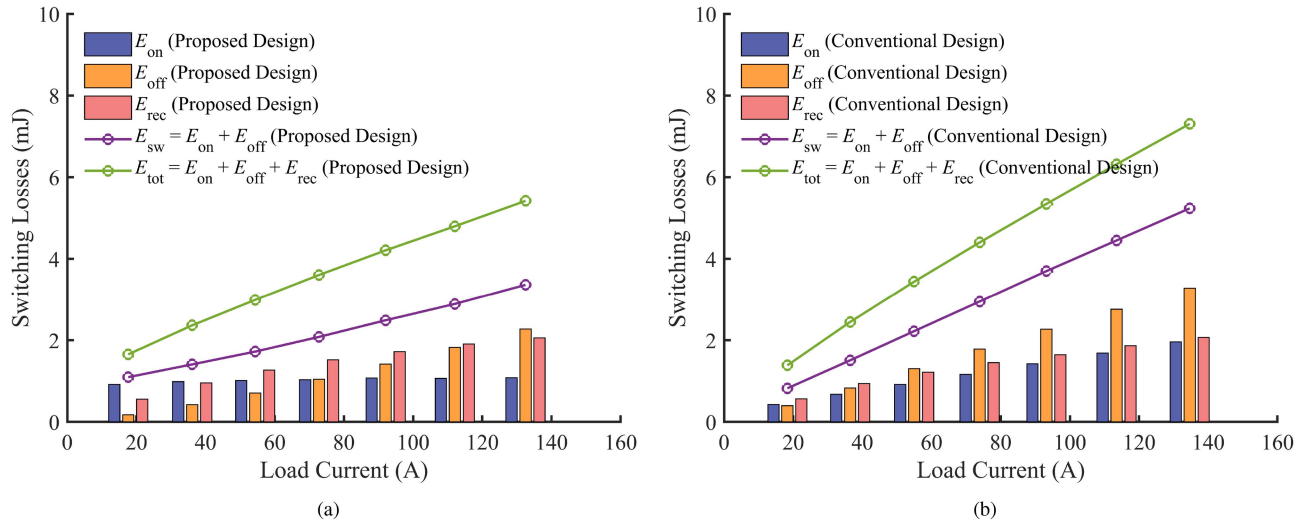


Fig. 21. Comparison of switching losses between the proposed design and the conventional hard-switching design. (a) Proposed design. (b) Conventional hard-switching design.

the conventional hard-switching design across all load currents, owing to the ZVS feature.

Moreover, the E_{rec} of the proposed design is reduced across the entire range of load currents due to the slower di/dt during the IGBT's turn-ON. As a result, the proposed design demonstrates significant reductions in both E_{sw} and E_{tot} compared to the conventional hard-switching design across various load current conditions. At load currents of 18 A, 36 A, 54 A, 73 A, 92 A, 112 A, and 132 A, the E_{sw} of the conventional hard-switching design are 0.82 mJ, 1.51 mJ, 2.22 mJ, 2.95 mJ, 3.70 mJ, 4.45 mJ, and 5.24 mJ, respectively, while the proposed design incurs losses of 1.10 mJ, 1.41 mJ, 1.72 mJ, 2.08 mJ, 2.49 mJ, 2.89 mJ, and 3.36 mJ. This represents an improvement in switching loss reduction by approximately −33.07%, 6.62%, 22.54%, 29.44%, 32.66%, 35.05%, and 35.81% across the respective load conditions. Similarly, the E_{tot} of the conventional hard-switching design are 1.39 mJ, 2.45 mJ, 3.44 mJ, 4.40 mJ, 5.35 mJ, 6.32 mJ, and 7.31 mJ, respectively, while the

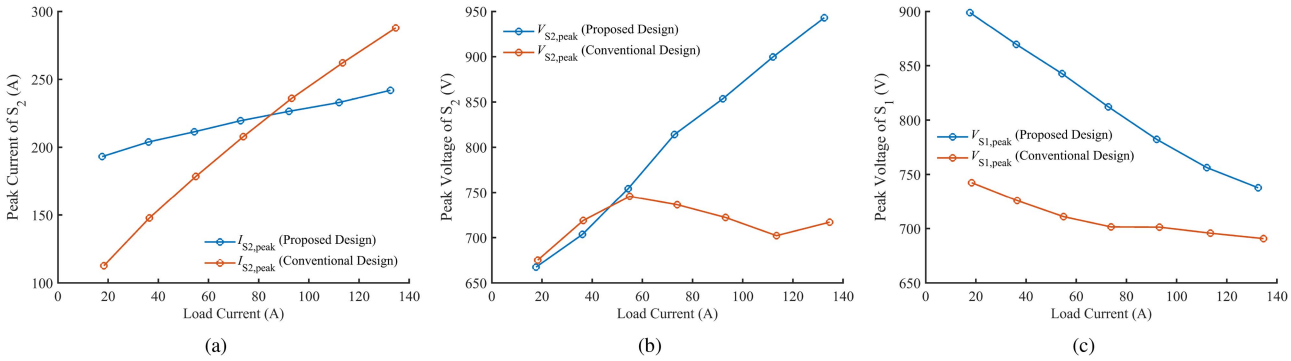


Fig. 22. Comparison of voltage and current overshoots between the proposed design and the conventional hard-switching design. (a) Current overshoot of S_2 during the turn-ON transient. (b) Voltage overshoot of S_2 during the turn-OFF transient. (c) Voltage overshoot of D_1 during the turn-ON transient of S_2.

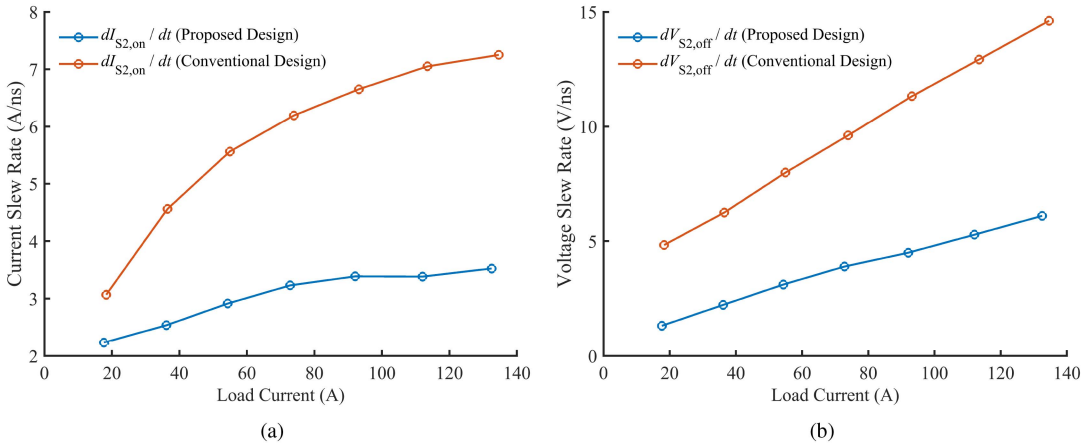


Fig. 23. Comparison of the di/dt and dv/dt. (a) di/dt during the turn-ON transient. (b) dv/dt during the turn-OFF transient.

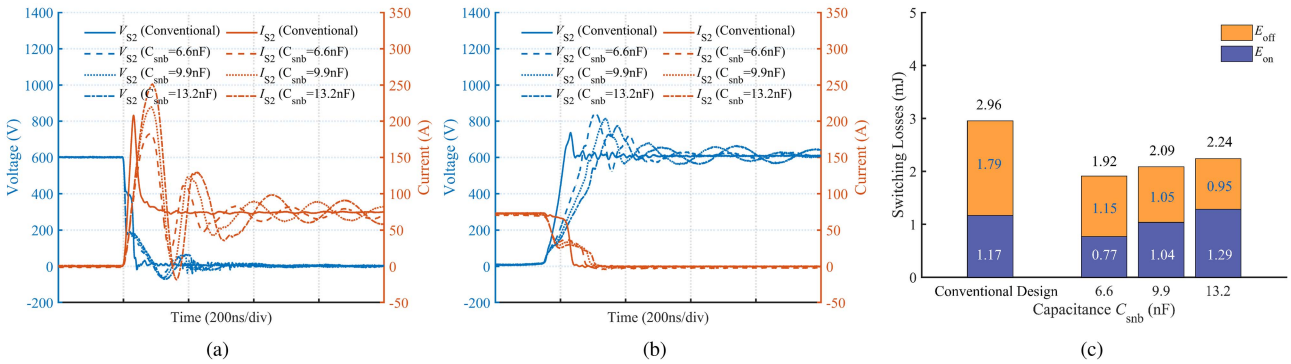


Fig. 24. Switching transient waveforms and losses with various C_{snb} (a) Turn-ON switching waveforms of S_2. (b) Turn-OFF switching waveforms of S_2. (c) Switching losses of S_2.

proposed design incurs losses of 1.66 mJ, 2.37 mJ, 2.99 mJ, 3.61 mJ, 4.21 mJ, 4.80 mJ, and 5.42 mJ, indicating reductions of -19.36%, 3.36%, 13.04%, 18.13%, 21.25%, 24.05%, and 25.80%, respectively. Furthermore, all loss components of the proposed design exhibit lower sensitivity to load current variations compared to those of the conventional hard-switching design. Specifically, the conventional hard-switching exhibits load current sensitivities of 38.0 uJ/A for E_{sw} and 50.9 uJ/A for E_{tot}, whereas the corresponding sensitivities for the proposed design are 19.7 uJ/A and 32.8 uJ/A. These results clearly underscore the superior efficiency of the proposed design in minimizing switching losses, particularly at higher current levels.

Fig. 22 depicts the voltage and current overshoots for both the proposed design and the conventional hard-switching design. Both designs show higher peak currents with increasing load currents. The proposed design displays higher peak currents under low load conditions, while it shows lower peak currents under high load conditions compared to the conventional hard-switching design. For the conventional hard-switching design, the turn-ON di/dt increases with larger load currents, resulting in

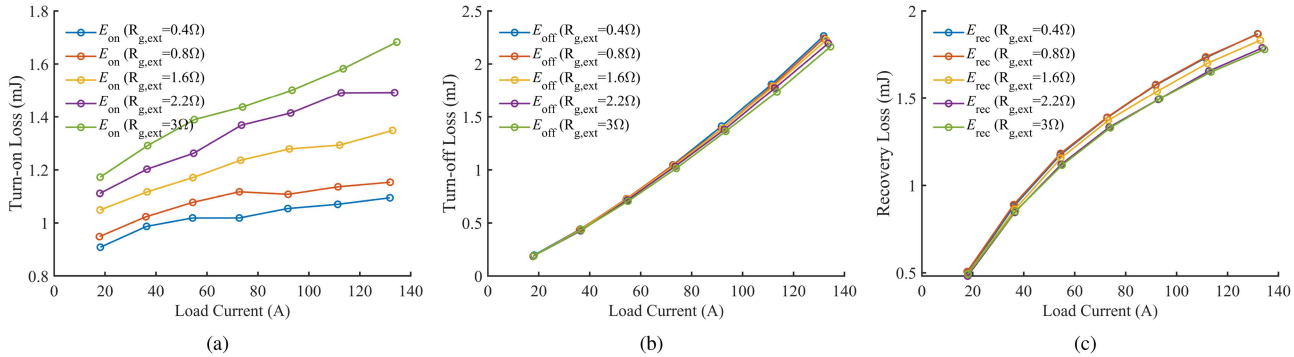


Fig. 25. Switching losses with various $R_{g,\text{ext}}$ for the proposed design. (a) Turn-ON loss of the IGBT. (b) Turn-OFF loss of the IGBT. (c) Reverse recovery loss of the FWD.

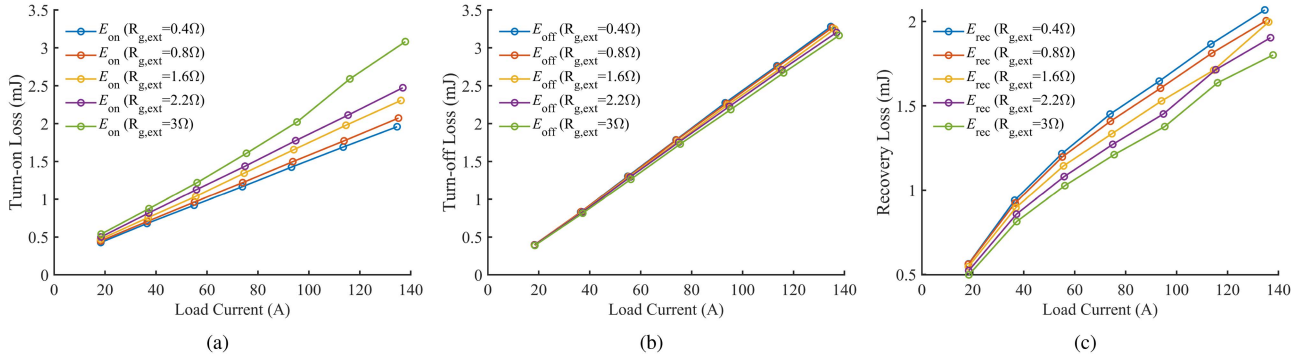


Fig. 26. Switching losses with various $R_{g,\text{ext}}$ for the conventional hard-switching design. (a) Turn-ON loss of the IGBT. (b) Turn-OFF loss of the IGBT. (c) Reverse recovery loss of the FWD.

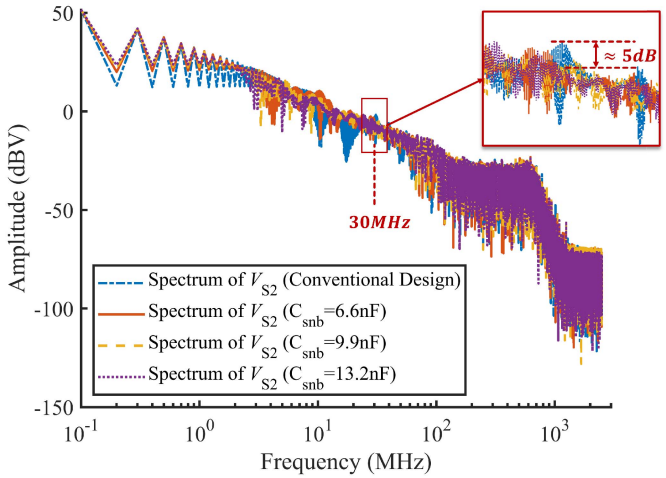


Fig. 27. Spectrum of V_{S2}.

higher reverse recovery currents on the FWD and consequently higher current overshoots on the IGBT. For the proposed design, however, the current overshoots on the IGBT are induced from the oscillation between C_{snb}, $L_{\text{sf},1p}$ and $L_{\text{sf},2p}$, which results in di/dt and current overshoots on the IGBT being less sensitive to load current. As for the voltage overshoots, the proposed design shows higher peak voltages on the IGBT when load currents exceed 60 A, which can be attributed to insufficient coupling coefficients of T_1 and T_2. Enhancing these coupling coefficients is anticipated to effectively mitigate the issue of voltage overshoots in the proposed design. The peak voltages on the FWD in the proposed design, however, are comparable to those in the conventional hard-switching design.

Fig. 23 compares the turn-ON di/dt and the turn-OFF dv/dt between the proposed design and the conventional hard-switching design. Both the di/dt and dv/dt for the proposed design are lower than those of the conventional hard-switching design across the entire range of load currents, indicating good controllability on dv/dt and di/dt of the proposed design. The smaller di/dt also contribute to reduced reverse recovery losses in the FWD.

D. Switching Losses With Various C_{snb}

The proposed design is tested with various values of C_{snb}, ranging from 6.6 to 13.2 nF, under the gate drive condition of $R_{g,\text{ext}} = 0.4\,\Omega$ and the load condition of $V_{\text{DC}} = 600\,\text{V}, I_L = 73\,\text{A}$. Fig. 24 presents the test results of the switching waveforms and losses. As the value of C_{snb} increases, the turn-ON loss of S_2 rises, while the turn-OFF loss decreases. As previously analyzed, a larger C_{snb} enhances turn-OFF performance but negatively impacts turn-ON losses due to increased current overshoots during turn-ON. The IGBT achieves a minimum switching losses of 1.92 mJ when $C_{\text{snb}} = 6.6\,\text{nF}$.

These results suggest the possibility of flexibly adjusting the turn-ON and turn-OFF performances of the IGBTs in the proposed design. For instance, in power converters with ZVS

TABLE VI
COMPARISON WITH OTHER SOFT-SWITCHING TECHNIQUES

Literature	Applicable Power Level	Snubber Type	Bidirectional Soft Switching	Main Switch Turn-on Condition	Main Switch Turn-off Condition	Magnetic Components	Theoretical Main Switch Voltage Stress	Number of High-voltage/current Auxiliary Elements for a Half-bridge
[20]	1 kW	Active	No	ZVS	ZCS	Lumped inductor with magnetic core	V_{DC}	3
[18]	2 kW	Active	Yes	ZVS	Hard		Voltage spike of hard switching-OFF	7
[38]	220 W	Passive	No	ZCS	ZVS		V_{DC}	5
[45]	200 W	Passive	No	ZCS	ZVS		V_{DC}	8
[40]	500 W	Passive	Yes	ZCS	ZVS		$1.2V_{\mathrm{DC}}$	7
[42]	350 W	Passive	Yes	ZVS	ZVS		V_{DC}	4
[43]	10 kW	Passive	Yes	ZCS	ZVS		$(n+2)V_{\mathrm{DC}}/n$	10
Proposed design	Expected to be 40 kW	Passive	Yes	ZCS	ZVS	Distributed	V_{DC}	3

characteristics, such as during normal operation of DAB and *LLC* converters, a larger C_{snb} can be employed to improve overall converter performances.

E. Switching Losses With Various $R_{g,ext}$

Figs. 25 and 26 illustrate the switching losses for various external gate resistances in the proposed design and conventional hard-switching design, respectively. In the proposed design, C_{snb} is set to 9.9 nF. As the gate resistance decreases, the E_{on} of both designs shows a significant reduction, while the E_{off} and E_{rec} remain nearly unchanged, despite only slight increases in E_{off} and slight decreases in E_{rec}. The reduction in E_{on} is attributed to the faster switching speeds associated with smaller gate resistances, which subsequently leads to a larger voltage drop on V_{S2} due to the I_{S2} rise during the turn-ON transient. In contrast, during the turn-OFF transient, a substantial portion of E_{off} is attributed to the minority carrier sweep-out process, which is relatively unaffected by the gate drive circuit.

For the conventional hard-switching design, switching performance is typically adjusted by modifying the external gate resistances, but, as demonstrated, this method has limited impact. In the proposed design, however, C_{snb}, $L_{\mathrm{sf},1p}$, and $L_{\mathrm{sf},2p}$ provide additional flexibility in optimizing switching performance. Furthermore, E_{on} is more sensitive to external gate resistance changes in the proposed design than in the conventional hard-switching design, offering enhanced flexibility.

F. EMI Spectrum and Discussion on the Switching Ringing

Fig. 27 illustrates the EMI spectrum obtained by performing a fast Fourier transform on the IGBT voltage waveform. For various values of C_{snb}, the proposed design demonstrates an EMI spectrum comparable to that of the conventional hard-switching design. However, at approximately 30 MHz, the conventional hard-switching design exhibits a slightly higher EMI level (about 5 dBV) than the proposed design. This difference is primarily attributed to the higher dv/dt associated with the conventional hard-switching design.

The waveform of the proposed design exhibits ringing with a period of approximately 150 ns (about 6.7 MHz) in Fig. 24. This ringing is primarily caused by the resonance between C_{snb} and $L_{\mathrm{sf},p}$.

The impact of this ringing can be analyzed from the following three perspectives.

1) *Influence on dead time and switching frequency:* Typically, the IGBT switching frequency is less than 20 kHz (with a switching period on the order of tens to hundreds of microseconds), and the dead time is also in the microsecond range. Since the ringing attenuates significantly within approximately 1μs, it does not affect the dead time or switching frequency.
2) *Energy loss and system efficiency:* Ideally, the energy associated with this ringing is absorbed by the ERC within one ringing cycle due to the unidirectional conduction characteristic of D_{aux1} and D_{aux2}, thereby suppressing oscillations. In a nonideal case, most of the ringing energy is still recovered by the ERC, minimizing additional losses.
3) *EMI spectrum:* As illustrated in Fig. 27, the EMI spectrum remains nearly identical to that of conventional designs, indicating that the ringing does not introduce significant EMI issues.

To further mitigate the ringing effect, the following measures can be implemented.

1) *Optimizing the design of C_{snb} and $L_{sf,p}$:* Reducing these parameters can help minimize the ringing amplitude; however, this may compromise the loss reduction benefits of the proposed design.
2) *Increasing the voltage level of C_{aux}:* This can be achieved by either reducing the capacitance of C_{aux} or increasing the voltage level of the low-voltage system. This enables the ERC to absorb the ringing energy more rapidly, thereby suppressing oscillations.
3) *Enhancing the coupling coefficient of the coupled inductors:* A higher coupling coefficient facilitates more efficient energy transfer to the secondary side of the coupled inductors, allowing the ERC to absorb the ringing energy more effectively.

G. Comparison With Other Soft-Switching Techniques

Table VI summarizes the characteristics of several representative studies on soft-switching techniques. Most existing designs are primarily suited for low-power applications (below a few kW), such as buck/boost converters and battery chargers. In contrast, high-power applications (tens of kW), including grid-connected converters and railway power supplies, pose significant implementation challenges for these designs. The main limitation stems from the reliance on lumped inductors with magnetic cores, which must conduct extremely high currents in such applications. This results in challenges such as increased magnetic losses, saturation issues, large volume, and excessive weight.

In contrast, the proposed design leverages PCB-based distributed coupled inductors, which can be seamlessly integrated into the dc busbar layout, eliminating the need for external magnetic components. In addition, the proposed design requires only three high-voltage, low-current auxiliary elements, while all other auxiliary components operate at low voltage and low current. Moreover, compared with those active snubber designs, the proposed design incorporates only passive elements, eliminating the need for complex sampling, control and gate drive circuits. This significantly simplifies implementation and enhances reliability, making it a more practical solution for high-power applications.

VI. Conclusion

This article presents an easy-to-implement flexible commutation design aimed at reducing switching losses, di/dt and dv/dt in high-speed power IGBTs for high-frequency and high-power applications. The proposed design incorporates a snubber capacitor and two PCB-based distributed coupled inductors to achieve ZVS and ZCS conditions for the main power IGBTs, meanwhile ensuring that the auxiliary diodes operate under soft-switching conditions. The design does not employ dissipative elements, facilitating a lossless operation. The proposed design requires only three high-voltage-low-current components, with all other components rated for low voltages and low currents. This simplicity is further enhanced by the exclusive use of passive components, allowing for easy implementation. This article provides comprehensive guidelines on the design of PCB-based distributed coupled inductors and details the requirements and selection criteria for other components, with comprehensive consideration and full utilization of parasitic parameters. Furthermore, the operational principles and current commutation paths are analyzed in detail.

Validation of the proposed design is conducted on a DPT platform, and comparisons are made against a conventional hard-switching design. Key characteristics of the proposed design are illustrated as follows.

1) *Switching losses:* The proposed design achieves superior loss performance to the conventional hard-switching design. The reductions in switching losses are more pronounced at higher load currents. Specifically, the proposed design exhibits lower turn-OFF losses of the IGBTs and nearly the same reverse recovery losses of the FWDs across the entire range of load currents, while also displaying reduced turn-ON losses of the IGBTs for load currents exceeding 54 A. Experimental results indicate a maximum of 35.81% reduction on the switching loss of the IGBTs and a 25.80% reduction on the total switching loss of the commutation unit, under the load current of 132 A, for the Infineon discrete IGBTs with the TO-247-4 package. All loss components of the proposed design show reduced sensitivity to load current variations.
2) *Voltage and current overshoots:* The proposed design maintains comparable levels of current overshoots on the IGBTs and voltage overshoots on the FWDs relative to the conventional hard-switching design. The voltage overshoots on the IGBTs in the proposed design at high load currents is higher than that in the conventional hard-switching design, but is still within an acceptable range. Enhancing the coupling coefficients of the PCB-based distributed coupled inductors is expected to effectively address this issue.
3) *Good controllability of di/dt and dv/dt:* The proposed design effectively reduces the turn-ON di/dt and the turn-OFF dv/dt of the IGBTs. By optimizing the self-inductance of the coupled inductors and the capacitance of the snubber capacitor, the di/dt and dv/dt can be effectively controlled. Since that there exists close relationship between EMI noise and di/dt and dv/dt, the proposed design provides further potential for optimizing the EMI characteristics.
4) *Flexibility*: The proposed design provides additional flexibility for adjusting the switching performances by adjusting the values of the snubber capacitance and the self-inductances of the coupled inductors. Increasing the self-inductances of the coupled inductors while decreasing the snubber capacitance improves the turn-ON switching losses of the IGBTs. Conversely, a larger snubber capacitance combined with decreased self-inductances of the coupled inductors enhances turn-OFF loss performance. In addition, reducing gate drive resistances can further decrease the turn-ON losses of the IGBTs, whereas the turn-OFF losses and reverse recovery losses of the FWDs exhibit lower sensitivity to the gate drive resistance.
5) *Possibility for power density enhancement:* While the proposed design requires additional space for the PCB-based inductors, potentially increasing the PCB size compared to traditional hard-switching designs, it still offers opportunities for overall power density improvement. The reduction in switching losses enables higher switching frequencies, which in turn allows for a decrease in the size of passive components, such as filter capacitors and inductors, ultimately enhancing power density. Furthermore, compared to existing snubber circuit designs that typically rely on bulky ferrite-core inductors, the proposed PCB-based inductor eliminates the need for such cores. This reduction in volume contributes to a more compact system compared to conventional snubber circuit implementations.

REFERENCES

[1] S. Cerutti, F. Musolino, and P. S. Crovetti, "Modeling and design of a zero-voltage switching battery charger for photovoltaic applications," *IEEE Access*, vol. 12, pp. 88251–88263, 2024.

[2] Y. Qin, Y. Yang, S. Li, Y. Huang, S.-C. Tan, and S. Y. Hui, "A high-efficiency DC/DC converter for high-voltage-gain, high-current applications," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2812–2823, Sep. 2020.

[3] Y.-F. Liu and D. Tan, "A discussion on ultrahigh efficiency and ultrahigh power density DC–DC converter technologies," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 3, pp. 2457–2468, Jun. 2023.

[4] D. Reusch, S. Biswas, and Y. Zhang, "System optimization of a high power density non-isolated intermediate bus converter for 48 V server applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1619–1627, Mar./Apr. 2019.

[5] C. Sun, R. Wang, Q. Sun, and H. Zhang, "A novel synchronous rectification scheme with low computational burden for LLC resonant converter in EV charger applications," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 8991–9003, Sep. 2023.

[6] T. Mishima and S. Mitsui, "A Single-stage high-frequency-link modular three-phase LLC AC–DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3205–3218, Mar. 2022.

[7] Y. Xu et al., "Impact of high switching speed and high switching frequency of wide-bandgap motor drives on electric machines," *IEEE Access*, vol. 9, pp. 82866–82880, 2021.

[8] D. Urbaneck, P. Rehlaender, J. Böcker, and F. Schafmeister, "LLC converter in capacitive operation utilizing ZCS for IGBTs–Theory, concept and verification of a 2 kW DC-DC converter for EVs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Jun. 2021, pp. 2753–2760.

[9] L. F. Pacheco, K. C. M. Nascimento, and I. Barbi, "Isolated AC/AC converter with LLC resonant converter high-frequency link and four-quadrant switches in the output stage," *IEEE Access*, vol. 8, pp. 213104–213114, 2020.

[10] O. Bhakare, K. Ghosh, S. S. Chakraborty, and K. Hatua, "Experimental study and comparison of switching loss behavior of Si IGBT and SiC MOSFET in dual active bridge series resonant converter," in *Proc. IEEE Int. Conf. Environ. Elect. Eng. IEEE Ind. Commercial Power Syst. Europe*, Jun. 2023, pp. 1–6.

[11] K.-H. Liu, R. Oruganti, and F. C. Y. Lee, "Quasi-resonant converters-topologies and characteristics," *IEEE Trans. Power Electron.*, vol. PE-2, no. 1, pp. 62–71, Jan. 1987.

[12] G. Hua and C. F. Lee, "An overview of soft-switching techniques for PWM converters," *EPE J.*, vol. 3, no. 1, pp. 39–50, 1993.

[13] U. Mumtahina and P. Wolfs, "A comparison study between series resonant and zero-voltage-resonant-transition DC-DC converters," in *Proc. Australas. Universities Power Eng. Conf.*, Sep. 2015, pp. 1–6.

[14] S. Tian, F. C. Lee, and Q. Li, "A simplified equivalent circuit model of series resonant converter," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3922–3931, May 2016.

[15] H. Jin, W. Chen, S. Shao, and L. Shu, "A quasi-square-wave modular multilevel resonant DC/DC converter with ZCS and current-shaping capacity for high step-ratio application," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 548–565, Jan. 2023.

[16] W. Cui, S. Shao, T. Wu, W. Chen, and J. Zhang, "A bidirectional modular multilevel resonant DC–DC converter for wide voltage range medium-voltage power conversion," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12743–12756, Oct. 2023.

[17] A. H. A. Biglo, S. Farhangi, and H. Iman-Eini, "A novel zero voltage transition soft-switching PWM boost converter with low voltage stress," in *Proc. 12th Power Electron., Drive Syst., Technol. Conf.*, Feb. 2021, pp. 1–5.

[18] Y. Wei, M.-C. Chen, C.-S. Yeh, and J.-S. Lai, "A novel auxiliary resonant snubber inverter using wide bandgap devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2019, pp. 2759–2765.

[19] W. Lee, D. Han, C. Morris, and B. Sarlioglu, "Minimizing switching losses in high switching frequency GaN-based synchronous buck converter with zero-voltage resonant-transition switching," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, Jun. 2015, pp. 233–239.

[20] N. Altintaş, A. F. Bakan, and İ. Aksoy, "A novel ZVT-ZCT-PWM boost converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 256–265, Jan. 2014.

[21] J. Han, C.-S. Lim, J.-H. Cho, R.-Y. Kim, and D.-S. Hyun, "A high efficiency non-isolated bidirectional DC-DC converter with zero-voltage-transition," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2013, pp. 198–203.

[22] H. Bodur, S. Cetin, and G. Yanik, "A new ZVT-PWM boost converter with active snubber cell," in *Proc. 8th IEEE Symp. Diagnostics Elect. Mach., Power Electron. Drives*, Sep. 2011, pp. 139–144.

[23] Z. Hu, B. Zhang, and W.-H. Deng, "Study on novel ZVZCT PWM DC-DC converter family," in *Proc. 4th Int. Power Electron. Motion Control Conf.*, Aug. 2004, vol. 1, pp. 154–159.

[24] H. Yu, B.-M. Song, and J.-S. Lai, "Design of a novel ZVT soft-switching chopper," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 101–108, Jan. 2002.

[25] R. Lin and F. Lee, "Novel zero-current-switching-zero-voltage-switching converters," in *Proc. PESC Record. 27th Annu. IEEE Power Electron. Specialists Conf.*, Jun. 1996, vol. 1, pp. 438–442.

[26] D.-Y. Lee, M.-K. Lee, D.-S. Hyun, and I. Choy, "New zero-current-transition PWM DC/DC converters without current stress," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 95–104, Jan. 2003.

[27] X. Jing and D. Boroyevich, "Comparison between a novel zero-switching-loss topology and two existing zero-current-transition topologies," in *Proc. 15th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2000, vol. 2, pp. 1044–1048.

[28] T. Ching, K. Chau, and C. Chan, "A novel two-quadrant zero-current-transition converter for DC motor drives," in *Proc. 24th Annu. Conf. IEEE Ind. Electron. Soc.*, Aug. 1998, vol. 2, pp. 715–720.

[29] G. Hua, E. Yang, Y. Jiang, and F. Lee, "Novel zero-current-transition PWM converters," *IEEE Trans. Power Electron.*, vol. 9, no. 6, pp. 601–606, Nov. 1994.

[30] B. Zhang, W. Han, B. Cao, W. Hu, and Y. Hu, "Optimum design of wireless power transfer-based snubbers for SiC MOSFET switching oscillations," *IEEE Trans. Power Electron.*, vol. 39, no. 9, pp. 10710–10715, Sep. 2024.

[31] K. Yatsugi, K. Nomura, and Y. Hattori, "Analytical technique for designing an RC snubber circuit for ringing suppression in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4736–4745, Jun. 2018.

[32] M. Xu, X. Yang, and J. Li, "C-RC snubber optimization design for improving switching characteristics of SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12005–12016, Oct. 2022.

[33] Y. Wang, J. Wang, F. Liu, Q. Liu, and R. Zou, "An RLL current sharing snubber for multiple parallel IGBTs in high power applications," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7555–7560, Jul. 2022.

[34] W. K. Thong, "A novel low-cost RCD snubber for Bifilar-wound motors," *IEEE Trans. Ind. Appl.*, vol. 38, no. 3, pp. 688–694, May/Jun. 2002.

[35] W. McMurray, "Selection of snubbers and clamps to optimize the design of transistor switching converters," *IEEE Trans. Ind. Appl.*, vol. IA-16, no. 4, pp. 513–523, Jul. 1980.

[36] W. Xu, A. Vetrivelan, Z. Guo, R. Yu, and A. Q. Huang, "Efficiency optimization of dual active bridge converter based on dV/dt snubber capacitors," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Jun. 2021, pp. 647–653.

[37] J.-M. Kwon, W.-Y. Choi, and B.-H. Kwon, "Cost-effective boost converter with reverse-recovery reduction and power factor correction," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 471–473, Jan. 2008.

[38] T. Shamsi, M. Delshad, E. Adib, and M. R. Yazdani, "A new simple-structure passive lossless snubber for DC–DC boost converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2207–2214, Mar. 2021.

[39] R. Faraji, H. Farzanehfard, M. Esteki, and S. A. Khajehoddin, "A lossless passive snubber circuit for three-port DC–DC converter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1905–1914, Apr. 2021.

[40] M. R. Mohammadi, H. Farzanehfard, and E. Adib, "Soft-switching bidirectional Buck/Boost converter with a lossless passive snubber," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8363–8370, Oct. 2020.

[41] M. Mohammadi, E. Adib, and M. R. Yazdani, "Family of soft-switching single-switch PWM converters with lossless passive snubber," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3473–3481, Jun. 2015.

[42] Y. Zhang, X.-F. Cheng, C. Yin, and S. Cheng, "A soft-switching bidirectional DC–DC converter for the battery super-capacitor hybrid energy storage system," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7856–7865, Oct. 2018.

[43] Z. Zhang, X. Yang, T. Q. Zheng, and J. Zhang, "A passive soft-switching snubber with energy active recovery circuit for PWM inverters," *IEEE Access*, vol. 8, pp. 100031–100043, 2020.

[44] J.-W. Kim, J.-M. Choe, and J.-S. J. Lai, "Nonisolated single-switch two-channel LED driver with simple lossless snubber and low-voltage stress," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4306–4316, May 2018.

[45] R. T. H. Li and H. S.-H. Chung, "A passive lossless snubber cell with minimum stress and wide soft-switching range," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1725–1738, Jul. 2010.

[46] X. Yu, J. Su, S. Guo, S. Zhong, Y. Shi, and J. Lai, "Properties and synthesis of lossless snubbers and passive soft-switching PWM converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3807–3827, Apr. 2020.
[47] K. Smith and K. Smedley, "Lossless passive soft-switching methods for inverters and amplifiers," *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 164–173, Jan. 2000.
[48] K. Smith and K. Smedley, "Properties and synthesis of passive lossless soft-switching PWM converters," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 890–899, Sep. 1999.
[49] H. Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE Trans. Parts, Hybrids, Packag.*, vol. 10, no. 2, pp. 101–109, Jun. 1974.
[50] F. W. Grover, *Inductance Calculations: Working Formulas and Tables* (Dover Books for Engineers). New York, NY, USA: ISA, 1982.
[51] E. B. Rosa, *The Self and Mutual Inductances of Linear Conductors*, vol. 4. Washington, DC, USA: U.S. Government Printing Office, Aug. 1907.

Yikang Xiao (Student Member, IEEE) received the B.S. degree in electrical engineering in 2020 from the Department of Electrical Engineering, Tsinghua University, Beijing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include simulation of power electronics systems, modeling and characterization of power semiconductor devices, gate drive, and snubber circuit design for Si IGBTs and SiC MOSFETs.

Shiqi Ji (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2010 and 2015, respectively.

Since 2015, he joined the Ultra-Wide Area Resilient Electric Energy Transmission Networks (CURENT), The University of Tennessee, Knoxville, TN, USA, and became a Research Assistant Professor in 2019. Since 2020, he has been with Tsinghua University, as an Assistant Professor, and then became an Associate Professor in 2021. He has authored or coauthored more than 80 technical papers in top journals and conference proceedings. His research interests include semiconductor device modeling, medium-voltage and high-power converter design, high-voltage SiC device characterization and application techniques, and grid-connected converter design.

Mingyu Yang (Student Member, IEEE) received the B.Eng. degree in electrical engineering and the B.Sc. degree in mathematics and physics both in 2024 from Tsinghua University, Beijing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include power semiconductor devices, packaging and integration, and high-frequency power converters.

Zhengming Zhao (Fellow, IEEE) received the B.S. and M.S. degrees in electrical engineering from Hunan University, Changsha, China, in 1982 and 1985, respectively, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 1991.

He is currently a Professor with the Department of Electrical Engineering, Tsinghua University. His research interests include high-power conversion, power electronics and motor control, and solar energy applications.