A Variable Parameter Series Compensation Method Featuring Fast Dynamic Response for Dual Active Bridge Converter in Battery Charging/Discharging Applications

Feng Wang, *Student Member, IEEE*, Xuehua Wang, *Member, IEEE*, Jialing Yuan, and Xinbo Ruan, *Fellow, IEEE*

***Abstract*—The extended-phase-shift (EPS) modulated dual-active-bridge (DAB) converter has become prevalent in battery charging/discharging systems, where low overshoot and short settling time are critically required. However, wide variations in battery voltage and current and abrupt operating mode transitions tend to challenge the dynamic performance of the converter. In this article, a small-signal model is developed, the potential challenge due to the wide-range variations or abrupt mode transitions is evaluated, and a variable parameter series compensation (VPSC) method is proposed. The proposed method can adjust its parameters in real time according to the variations in battery voltage and current, making the dynamics of the EPS-DAB converter immune to the variations. For practical implementation, a polynomial-fit approximation is conducted to minimize the computational complexity. An execution-optimized flowchart is also provided. Experimental results on a 45-kW prototype demonstrate the effectiveness of the VPSC method. Even under the worst case when the battery voltage is 107 V and the battery current steps from 100 to −100 A, no overshoot arises and the settling time is less than 6 ms.**

***Index Terms*—Dual-active-bridge (DAB) converter, extended-phase-shift (EPS), fast dynamic response, variable parameter series compensation (VPSC).**

I. Introduction

THE dual-active-bridge (DAB) converter was proposed in 1988 for aerospace applications [1], [2], featuring bidirectional power flow, galvanic isolation, and high power density with a low number of passive components. Recently, it has gained much attention in various industrial applications, such as renewable energy integration [3], [4], energy storage systems [5], [6], [7], and electric transportation systems [8], [9]. With the exponential growth of electric vehicles (EVs) and hybrid electric vehicles in recent decades, the DAB converter has emerged as a promising solution for battery energy management systems [10], [11], [12].

Numerous modulation schemes have been developed for the DAB converter. The simplest single-phase-shift (SPS) [2] can achieve zero voltage switching (ZVS) for all power switches (termed ZVS expectation hereinafter). However, this requires a unity voltage-conversion ratio. Otherwise, ZVS may be lost at certain operating points, increasing turn-OFF losses and conduction stresses of the switches. Advanced schemes, such as extended-phase-shift (EPS) [13], dual-phase-shift (DPS) [14], and triple-phase-shift (TPS) [15], can address this limitation by utilizing extra control variables. Specifically, the EPS modulation achieves optimal complexity-performance tradeoffs, demonstrating a 37.8% reduction in peak current and a 26.8% reduction in root-mean-square (RMS) current compared to SPS modulation [16], enabling 20% light-load efficiency improvement [17]. However, the EPS modulation has multiple operating modes, which complicates dynamic optimization and risks magnetic biasing [18], [19].

In high-power battery applications, fast dynamic response is critically required. Particularly, sudden current reversal between charging and discharging (e.g., 100 A steps down to −100 A or vice versa in vehicle-to-grid scenarios) occasionally occurs [20]. It usually demands zero overshoot, especially for high-power industrial applications (e.g., 45 kW EV chargers), as minor overshoot or delay can lead to components failure. Fast and smooth current response can reduce electrical and thermal stresses, significantly enhancing the reliability of the system. Furthermore, fast response can facilitate precise current shaping (e.g., multistage charging, pulsed protocols) for battery health under extreme conditions, and prolonging battery lifespan [21].

Extensive research has focused on both small-signal modeling [22], [23], [24], [25] and control methods [26], [27], [28] to improve the dynamic performance of DAB converters. A feedforward current control (FFCC) method was proposed in [26], which achieved fast dynamic response through a simplified nonlinear feedforward function. However, it is prone to

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The authors are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: wang_ff@hust.edu.cn; wang.xh@hust.edu.cn; yjl_hust@hust.edu.cn; ruanxb@nuaa.edu.cn).

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switching noise, particularly when some power switches lose ZVS. A virtual direct power control (VDPC) method introduced in [27] improved the dynamic response. However, it performs poorly under light-load conditions. The sliding mode control (SMC) method was also applied to the DAB converter [28]. However, its sensitivity to parameter fluctuations (e.g., inductance variations) degrades the dynamic performance. Critically, the methods in [26], [27], [28] were originally designed for SPS modulation and they commonly face challenges when being applied to EPS modulation. For instance, the EPS modulation inherently involves two or more operating modes [13], with unavoidable mode transitions. Such multimode operation and transitions can adversely impact the dynamic response [18] and induce magnetic biasing [19]. To mitigate these issues, compromises such as reducing the controller bandwidth [29] are often required, resulting in sluggish dynamic responses.

Moreover, wide variations in battery voltage and current exacerbate these challenges. The system must maintain fast dynamic responses across the full operating range without hardware reconfiguration for battery stacks. To reach this goal, the methods [26], [27], [28] require piecewise linear parameter adaptation to accommodate these variations, at the cost of difficult parameter optimization. The moving discretized control set-model predictive control (MDCS-MPC) method [30] can enhance robustness against these variations, but its high implementation complexity limits scalability to high switching-frequency applications.

To address these challenges, this article proposes a variable parameter series compensation (VPSC) method for the EPS-DAB converter. The VPSC method incorporates a series compensator with dynamically adjusted parameters based on the real-time operating conditions, and the advantages are as follows.

1) Zero-overshoot response and less than 6 ms settling time are achieved within the full operating range (i.e., 100−450 V, ±100 A).
2) The implementation is simple, where the execution time on a digital signal processor (DSP) is 3.6 μs, thus enabling deployment on low-cost microcontrollers.

These two advantages ensure that the EPS-DAB converter with the proposed VPSC method can be applied for EV fast chargers, grid-scale storage, and renewable energy integration. In fact, the VPSC method, originally developed for EPS modulation, can be extended to DPS and TPS modulations with little computational overhead.

The rest of this article is organized as follows. In Section II, the system architecture and minimum-RMS-current EPS modulation are presented. The small-signal model of the EPS-DAB converter is then established to facilitate the dynamic analysis. In Section III, the dynamic challenges arising from wide variations in battery voltage and current are unfolded, and the inherent mode-switching transitions in the EPS-DAB converter are analyzed. The proposed VPSC method is subsequently presented, with a polynomial-fit approximation and an execution-optimized flowchart. In Section IV, experiments are conducted on a 45-kW prototype to verify the VPSC method. Finally, Section V concludes this article.

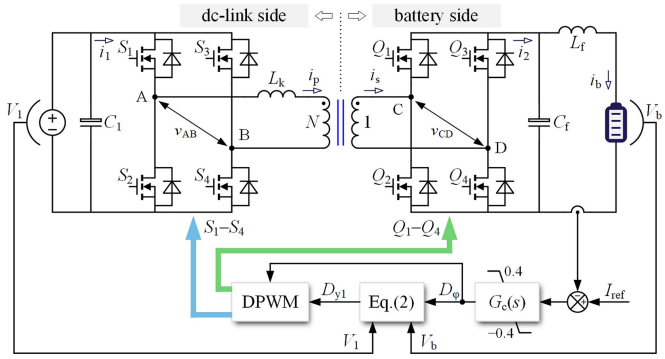

Fig. 1. Configuration of the battery charging/discharging system based on DAB converter.

II. Modeling of EPS-DAB Converter

A. System Description

Fig. 1 depicts the configuration of a DAB converter for battery charging/discharging applications. This converter is comprised of two H-bridges, with eight power switches S_1-S_4 and Q_1-Q_4. The two H-bridges are connected through a series inductor L_k and a high-frequency transformer. i_p and i_s are the transformer currents in the dc-link side and the battery side, respectively. N denotes the transformer turns ratio between the dc-link side and the battery side. On the dc-link side, a single capacitor C_1 serves as the filter; while on the battery side, a combined C_f-L_f filter is used to smooth the battery current and prolong the battery lifespan.

In the control unit, the battery current i_b is fed back and regulated by a current controller $G_c(s)$ to track its reference I_{ref}, ensuring a constant battery current. The output signal of $G_c(s)$ is the phase shift ratio between v_{AB} and v_{CD}, denoted as D_φ. Substituting D_φ, the dc-link voltage V_1, and the battery voltage V_b into (2) (derived in Section II-B), yields the duty ratio of v_{AB}, denoted as D_{y1}, where $D_{y1}\in[0, 1]$. Then, sending both D_φ and D_{y1} into the digital pulse-width modulator (DPWM), the control signals of all eight switches are generated.

B. EPS Modulation With Minimal RMS Current

In this work, energy is transferred bidirectionally between the dc-link source V_1 and the battery V_b, modulated by the ac voltages v_{AB} and v_{CD} from the dc-link- and battery-side bridges, respectively. The battery voltage V_b operates within a wide range (100–450 V), as specified in Table II in Section IV-A. To ensure the ZVS expectation, the EPS modulation is adopted. Considering the ZVS expectation of the EPS modulation has been elaborated in [13], it is briefly introduced here.

The DAB converter operates in both forward and reverse conditions with identical operating principles. For conciseness, only the forward operation is hereinafter analyzed in detail. Fig. 2 shows the operating principle, where T_s denotes the switching period. It was reported in [31] that noticeable circulating energy may arise when $D_\varphi > 0.5$. In view of this, $D_\varphi \le 0.5$ is commonly limited in practical applications.

TABLE I
ZVS CONSTRAINTS OF POWER SWITCHES

Mode a			Mode b		
Switches	ZVS condition	D_{y1} vs D_φ	Switches	ZVS condition	D_{y1} vs D_φ
S_1, S_2	$i_p(t_0)\le 0$	$D_{y1}\ge \frac{-2mD_\varphi}{1-m}$	S_1, S_2	$i_p(t_0)\le 0$	$D_{y1}\ge \frac{-2mD_\varphi}{1-m}$
S_3, S_4	$i_p(t_2)\le 0$	$D_{y1}\ge \frac{2mD_\varphi}{1-m}$	S_3, S_4	$i_p(t_1)\le 0$	$D_{y1}\ge \frac{2m(1-D_\varphi)}{1+m}$
Q_1–Q_4	$i_p(t_1)\ge 0$	$D_{y1}\le m$	Q_1–Q_4	$i_p(t_2)\ge 0$	$D_\varphi\ge \frac{1-m}{2}$

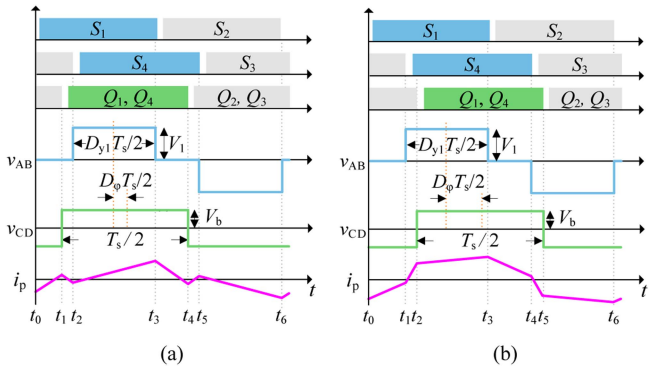

Fig. 2. Key waveforms of the EPS modulation in forward operation. (a) Mode a: $0\le D_\varphi<(1-D_{y1})/2$. (b) Mode b: $(1-D_{y1})/2\le D_\varphi\le 0.5$.

Depending on the relative position of the rising edges of v_{AB} and v_{CD}, the forward operation has the following modes.

1) *Mode a [see* Fig. 2(a)*]*: The rising edge of v_{AB} lags behind v_{CD} in a switching period. Accordingly, D_φ and D_{y1} satisfy the relation of $0\le D_\varphi<(1-D_{y1})/2$.
2) *Mode b [see* Fig. 2(b)*]*: Inversely, the rising edge of v_{CD} lags behind v_{AB}. Accordingly, $(1-D_{y1})/2\le D_\varphi\le 0.5$ holds.

In steady-state operation, the average value of i_p over one switching period is zero. Accordingly, $i_p(t_0)=-i_p(t_3)$ (see Fig. 2).

The expression of i_p can be represented via piecewise functions [13], whereby the forward transferred power of the EPS-DAB converter, denoted as P_o, is derived as

$$P_o=\begin{cases}\frac{mV_1^2}{2L_kf_s}D_\varphi D_{y1}, & \text{Mode a}\\ \frac{mV_1^2}{8L_kf_s}\left[1-(1-2D_\varphi)^2-(1-D_{y1})^2\right], & \text{Mode b}\end{cases}\tag{1}$$

where $f_s=1/T_s$ is the switching frequency, and $m=NV_b/V_1$ represents the voltage-conversion ratio.

Equation (1) indicates that for a given transmitted power, there exist many combinations of D_φ and D_{y1}. To ensure the ZVS expectation, the relations of D_{y1} versus D_φ should be derived from the operational waveforms in Fig. 2. For example, achieving ZVS of S_1 requires the current $i_p(t)$ to be negative when its gate signal is activated. This requires $i_p(t_0)\le 0$, to ensure that the body diode of S_1 conducts before S_1 turns ON. Consequently, the relation of D_{y1} and D_φ can be determined. Similarly, the ZVS conditions of the rest switches (S_2–S_4, and Q_1–Q_4) are also derived and summarized in Table I. Since the transformer turns ratio $N\le V_1/V_b$ ($m\le 1$) is designed in this work (refer to Table II in Section IV-A), $D_{y1}\ge -2mD_\varphi/(1-m)$ holds. Accordingly, S_1 and S_2 can easily achieve ZVS under all operating conditions.

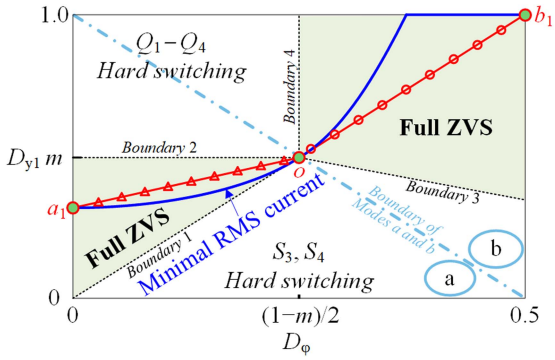

Fig. 3. ZVS regions and the optimal trajectories of I_{p_rms} under EPS modulation.

Fig. 3 illustrates the ZVS regions regarding D_{y1} versus D_φ. As can be observed, *Boundaries* 1–4 (which are plotted based on the ZVS constraints of S_3, S_4, and Q_1–Q_4 in Table I) intersect at point o ($(1-m)/2$, m), dividing the operating region into four segments, two hard switching ones and two full ZVS ones. Thanks to the intersection of the two full ZVS regions at point o, the control trajectory can be arranged to pass through the two full ZVS regions via point o. To minimize conduction losses, the minimal RMS inductor current i_p is further targeted as an additional constraint, and an optimal trajectory can be determined, as depicted in Fig. 3. It starts from point $a_1(0, m/(2-m))$, passes through point o and ends at point $b_1(0.5, 1)$. Unfortunately, this trajectory is a nonlinear curve. The nonlinearity complicates the real-time implementation. To address this issue, two straight lines (i.e., a_1o and ob_1) are selected to replace the nonlinear curve. Accordingly, the relations of D_{y1} and D_φ satisfy

$$D_{y1}=\begin{cases}\frac{m(2D_\varphi+1)}{2-m}, a_1o \text{ in Mode a } \left(0\le D_\varphi<\frac{1-m}{2}\right)\\ \frac{2(1-m)D_\varphi+2m-1}{m}, ob_1 \text{ in Mode b } \left(\frac{1-m}{2}\le D_\varphi<0.5\right)\end{cases}.\tag{2}$$

It has been examined in [13] that the maximum error of the RMS current, arising from applying the linearization shown in (2), is no more than 3% under $m\in[0.4, 0.8]$. Thus, the above-mentioned segmental linearization is reasonable.

C. Small-Signal Model of the EPS-DAB Converter

To evaluate the dynamic performance of the battery system, a small-signal model of the EPS-DAB converter is developed based on the following assumptions.

1) The switching frequency is significantly higher than the system bandwidth.
2) The semiconductors and passive components (e.g., capacitors and inductors) are assumed ideal, neglecting their parasitic resistances, losses, and magnetic saturation.

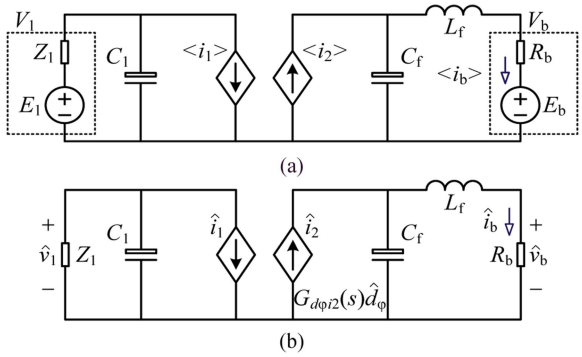

Fig. 4. Modeling of the EPS-DAB converter. (a) Averaged-switch model. (b) Small-signal model.

3) The battery is modeled as a Thévenin-equivalent circuit, which consists of an internal resistance R_b and an open-circuit voltage E_b solely depending on the static state-of-charge (SOC).

The third assumption is just to neglect hysteresis, diffusion dynamics, and SOC evolution, which prioritizes the analysis on the system-level transient interaction between the EPS-DAB converter and the battery. In fact, the neglected phenomena operate on either second-to-minute scale (hysteresis and diffusion dynamics) or hour scale (SOC evolution), all being much slower than the millisecond-scale transient response [32]. Thus, time-scale decoupling can be applied, and the complexity in the modeling process can be reduced.

Based on the abovementioned three assumptions, the averaged model of the EPS-DAB converter is derived, as shown in Fig. 4(a), where $\langle i_1\rangle$ and $\langle i_2\rangle$ represent the average values of the dc-link-side bridge current i_1 and the battery-side bridge current i_2 (see Fig. 1) in a switching period, respectively.

In fact, $\langle i_2\rangle$ can be easily derived. Considering (1) and $P_\mathrm{o} = V_\mathrm{b}\cdot I_\mathrm{b} = V_\mathrm{b}\cdot\langle i_2\rangle$, it can be derived as

$$\langle i_2\rangle = \frac{P_\mathrm{o}}{V_\mathrm{b}} = \begin{cases} \frac{NV_1}{2L_\mathrm{k}f_\mathrm{s}}\langle d_\varphi\rangle\langle d_{\mathrm{y}1}\rangle, & \text{Mode a} \\ \frac{NV_1}{8L_\mathrm{k}f_\mathrm{s}}\left[1-(1-2\langle d_\varphi\rangle)^2-(1-\langle d_{\mathrm{y}1}\rangle)^2\right], & \text{Mode b} \end{cases} \tag{3}$$

where $\langle d_\varphi\rangle$ and $\langle d_{\mathrm{y}1}\rangle$ represent the average values of d_φ and $d_{\mathrm{y}1}$ in a switching period, respectively.

Applying the corresponding perturbations to the average phase shift $\langle d_\varphi\rangle$, the average duty ratio $\langle d_{\mathrm{y}1}\rangle$ and the average battery-side bridge current $\langle i_2\rangle$, leads to $\langle d_\varphi\rangle = D_\varphi + \hat{d}_\varphi$, $\langle d_{\mathrm{y}1}\rangle = D_{\mathrm{y}1} + \hat{d}_{\mathrm{y}1}$ and $\langle i_2\rangle = I_2 + \hat{i}_2$, respectively, where D_φ, $D_{\mathrm{y}1}$, and I_2 are the quiescent values and $\hat{d}_\varphi$, $\hat{d}_{\mathrm{y}1}$, and $\hat{i}_2$ are the perturbations.

In terms of (3), I_2 and $\hat{i}_2$ can be respectively derived as

$$I_2 = \begin{cases} \frac{NV_1}{2L_\mathrm{k}f_\mathrm{s}}D_\varphi D_{\mathrm{y}1}, & \text{Mode a} \\ \frac{NV_1}{8L_\mathrm{k}f_\mathrm{s}}\left[1-(1-2D_\varphi)^2-(1-D_{\mathrm{y}1})^2\right], & \text{Mode b} \end{cases} \tag{4}$$

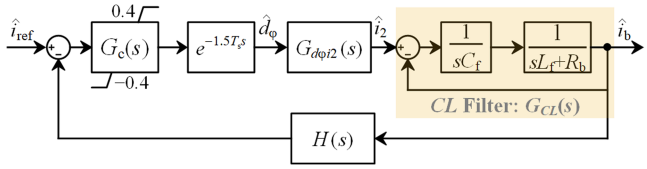

Fig. 5. Block diagram of constant current controlled EPS-DAB converter.

$$\hat{i}_2 = \begin{cases} \frac{NV_1}{2L_\mathrm{k}f_\mathrm{s}}\left(D_{\mathrm{y}1}\hat{d}_\varphi + D_\varphi\hat{d}_{\mathrm{y}1} + \hat{d}_\varphi\hat{d}_{\mathrm{y}1}\right), & \text{Mode a} \\ \frac{NV_1}{8L_\mathrm{k}f_\mathrm{s}}\left[(4-8D_\varphi)\hat{d}_\varphi + 2(1-D_{\mathrm{y}1})\hat{d}_{\mathrm{y}1}\right], & \text{Mode b.} \end{cases} \tag{5}$$

Consider that I_2 equals I_b (i.e., the quiescent value of the battery current $\langle i_b\rangle$, see Fig. 1). Substituting (2) into (4), yields

$$D_\varphi = \begin{cases} -\frac{1}{4} + \sqrt{\frac{1}{16} + \frac{L_\mathrm{k}f_\mathrm{s}(4-2m)I_\mathrm{b}}{2N^2V_\mathrm{b}}}, & \text{Mode a} \\ \frac{1}{2} - \frac{1}{2}\sqrt{1 - \frac{\frac{8m^3L_\mathrm{k}f_\mathrm{s}I_\mathrm{b}}{N^2V_\mathrm{b}} + m^2 - 2m + 1}{2m^2-2m+1}}, & \text{Mode b.} \end{cases} \tag{6}$$

The quiescent duty ratio $D_{\mathrm{y}1}$ has been derived in (2), and its associated perturbation part can be derived as

$$\hat{d}_{\mathrm{y}1} = \begin{cases} \frac{2m\hat{d}_\varphi}{2-m}, & \text{Mode a} \\ \frac{2(1-m)\hat{d}_\varphi}{m}, & \text{Mode b.} \end{cases} \tag{7}$$

By substituting (2), (7) into (5), and manipulating, yields the transfer function from $\hat{d}\varphi$ to $\hat{i}_2$, denoted as $G_{d\varphi i2}(s)$, which is

$$G_{d\varphi i2}(s) = \frac{\hat{i}_2}{\hat{d}_\varphi} = \begin{cases} \frac{mNV_1(4D_\varphi+1)}{2L_\mathrm{k}f_\mathrm{s}(2-m)}, & \text{Mode a} \\ \frac{NV_1(2m^2-2m+1)(1-2D_\varphi)}{2L_\mathrm{k}f_\mathrm{s}m^2}, & \text{Mode b.} \end{cases} \tag{8}$$

As can be observed from (8), $G_{d\varphi i2}(s)$ for the EPS-DAB converter is actually a proportional element, which is similar to the SPS-DAB converter [25].

In terms of (8), the small-signal model can be further obtained, as shown in Fig. 4(b). Accordingly, the associated block diagram is depicted in Fig. 5, and the loop gain $T_\mathrm{o}(s)$ can be derived as

$$T_\mathrm{o}(s) = G_\mathrm{c}(s)\,e^{-1.5T_\mathrm{s}s}\underbrace{G_{d\varphi i2}(s)\,G_{CL}(s)}_{G_{d\varphi i\mathrm{b}}(s)}H(s) \tag{9}$$

where the control delay of $1.5T_\mathrm{s}$ is considered. $G_{CL}(s)$ and $H(s)$ represent the transfer functions of the CL filter and the low-pass filter for suppressing noises. Their expressions are as

$$G_{CL}(s) = \frac{1}{L_\mathrm{f}C_\mathrm{f}s^2 + R_\mathrm{b}C_\mathrm{f}s + 1} \tag{10}$$

$$H(s) = \frac{1}{T_1 s + 1} \tag{11}$$

where T_1 is the time constant of the low-pass filter.

In (9), $G_{d\varphi i\mathrm{b}}(s) = G_{d\varphi i2}(s)G_{CL}(s)$ represents the control-to-output transfer function. It is provided to validate the accuracy of the derived model.

A simulation benchmark is implemented in PLECS 4.7.5, with the key parameters listed in Table II (Section IV-A). Besides, with this simulation benchmark, the simplified battery

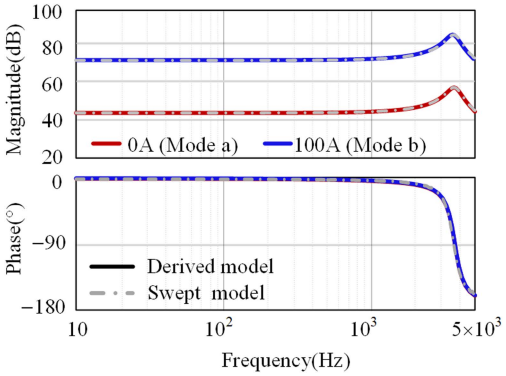

Fig. 6. Comparison between the derived model and the swept model under $V_{\rm b} = 100$ V.

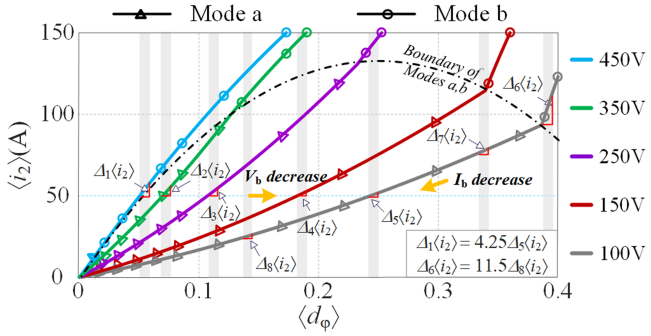

Fig. 7. Curves of the average current $\langle i_2 \rangle$ versus $\langle d_\varphi \rangle$ as the battery voltage $V_{\rm b}$ changes from 100 to 450 V for the EPS-DAB converter.

model, shown in Fig. 4(a), is concurrently examined through comparison with a second-order RC Thévenin-equivalent model developed in [33].

On the simulation benchmark, the frequency-domain ac sweeping analysis is applied, where the small-signal perturbation is injected into the phase shift ratio D_φ, and the response of the battery current $i_{\rm b}$ is measured.

Fig. 6 shows the tested frequency responses of $G_{d\varphi i{\rm b}}(s)$, including the derived model and the swept model. Here, $V_{\rm b} = 100$ V is considered under two operating points: 1) no load (i.e., $I_{\rm b} = 0$ A, operating in Mode a) and 2) full load (i.e., $I_{\rm b} = 100$ A, operating in Mode b). As can be observed, the two models keep aligned with the gain deviation of less than 0.5 dB and the phase discrepancy of 5° within the dynamic evaluation bandwidth (10 Hz−5 kHz). This result confirms the accuracy of the derived model.

III. Proposed VPSC Method

In this section, the challenges posed by wide variations in battery voltage and current, as well as abrupt operating mode transitions inherent to the EPS-DAB converter are unfolded, and a VPSC method is proposed to address these challenges.

A. Controller Challenges

As outlined in Table II, the battery voltage $V_{\rm b}$ and current $I_{\rm b}$ operate within wide ranges (i.e., 100−450 V, ±100 A). These variations directly affect the quiescent phase shift D_φ [see (6)] and then pose impact on $G_{d\varphi i2}(s)$ [see (8)]. Intuitively, the crossover frequency of the loop gain $T_{\rm o}(s)$ drifts in a wide range, posing great challenges to the dynamic performance or even the stability of the EPS-DAB converter and the design of the current controller $G_{\rm c}(s)$.

To quantify these challenges, substituting the specific parameters $V_1 = 700$ V, $L_{\rm k} = 45$ μH, and $f_{\rm s} = 10$ kHz (see Table II) into (3), the curves regarding the average current $\langle i_2 \rangle$ versus the average phase ratio $\langle d_\varphi \rangle$ under different battery voltage (450, 350, 250, 150, and 100 V) are plotted in Fig. 7. Here, the boundary of Modes a and b is also delineated.

Given the battery voltage $V_{\rm b}$ varies from 450 to 100 V, four values (i.e., 25, 50, 75, and 100 A) of $\langle i_2 \rangle$ are selected for evaluation. Using these parameters, D_φ and $D_{\rm y1}$ are calculated from (6) and (2), respectively. For example, with $V_{\rm b} = 450$ V and $I_{\rm b} = 50$ A, the steady-state values $D_\varphi = 0.045$ and $D_{\rm y1} = 0.966$ are derived. Furthermore, applying the increment (denoted as Δd_φ) to $\langle d_\varphi \rangle$, the resultant increment of $\langle i_2 \rangle$, denoted as $\Delta\langle i_2 \rangle$, can be calculated. Note that Δd_φ and $\Delta\langle i_2 \rangle$ are just the perturbations $\hat{d}_\varphi$ and $\hat{i}_2$, respectively.

For $\Delta d_\varphi = 0.01$, $\Delta_1\langle i_2 \rangle = 10.2$ A is calculated. Similarly, a fixed increment $\Delta d_\varphi = 0.01$ is continuously applied to evaluate $\Delta\langle i_2 \rangle$ at other operating points. To clarify the challenges, the following scenarios are exemplified.

1) *Scenario 1 (fixed $I_{\rm b} = 50$ A, different $V_{\rm b}$)*: According to the previous analysis, the following current increments are calculated. They are $\Delta_1\langle i_2 \rangle = 10.2$ A at $V_{\rm b} = 450$ V, $\Delta_2\langle i_2 \rangle = 8.56$ A at $V_{\rm b} = 350$ V, $\Delta_3\langle i_2 \rangle = 6.05$ A at $V_{\rm b} = 250$ V, $\Delta_4\langle i_2 \rangle = 3.92$ A at $V_{\rm b} = 150$ V, and $\Delta_5\langle i_2 \rangle = 2.4$ A at $V_{\rm b} = 100$ V, as shown in Fig. 7. As can be observed, $\Delta\langle i_2 \rangle$ decreases as $V_{\rm b}$ decreases, and the maximum decrease meets $\Delta_1\langle i_2 \rangle = 4.25\Delta_5\langle i_2 \rangle$ as $V_{\rm b}$ drops from 450 to 100 V.
2) *Scenario 2 (fixed $V_{\rm b} = 100$ V, different $I_{\rm b}$)*: Likewise, the current increments $\Delta_6\langle i_2 \rangle = 24.2$ A at $I_{\rm b} = 100$ A, $\Delta_7\langle i_2 \rangle = 3.23$ A at $I_{\rm b} = 75$ A, and $\Delta_8\langle i_2 \rangle = 2.1$ A at $I_{\rm b} = 25$ A are obtained. These current increments are also depicted in Fig. 7. As can be observed, under the lowest battery voltage of $V_{\rm b} = 100$ V, $\Delta\langle i_2 \rangle$ decreases as $I_{\rm b}$ decreases. Note that the associated current increments under $V_{\rm b} = 100$ V decrease sharply since the operating mode has switched from Mode b to Mode a. The maximum decrease meets $\Delta_6\langle i_2 \rangle = 11.5\Delta_8\langle i_2 \rangle$ as $I_{\rm b}$ drops from 100 to 25 A.

These multiples of the maximum difference pose a challenge on tuning the current controller $G_{\rm c}(s)$.

To provide an intuitive understanding of the challenge, the bode plots of the loop gain $T_{\rm o}(s)$ at these operating points are depicted in Fig. 8. As a comparison benchmark, a fixed-PI current controller serves as the baseline, expressed as

$$G_{\rm c}(s) = K_{\rm p} + K_{\rm i}/s \tag{12}$$

where $K_{\rm p} = 0.0028$ and $K_{\rm i} = 0.703$ are tuned at the rated operating point ($V_{\rm b} = 450$ V, $I_{\rm b} = 100$ A), referring to the design

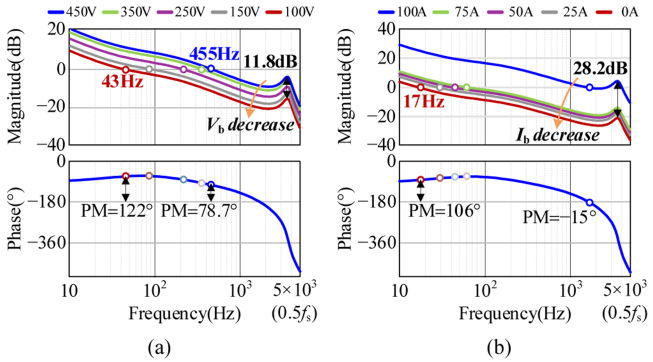

Fig. 8. Bode plots of $T_o(s)$ under different operating conditions. (a) Fixed $I_b = 50$ A with different V_b. (b) Fixed $V_b = 100$ V with different I_b.

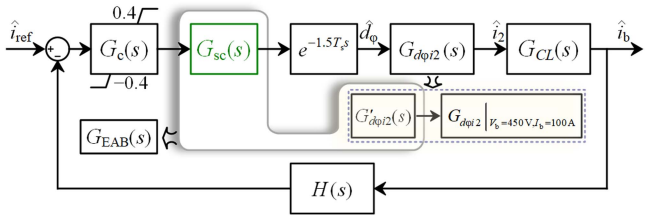

Fig. 9. Block diagram with the proposed VPSC method.

procedures presented in [34]. Correspondingly, it leads to a rated crossover frequency $f_c = 400$ Hz and a phase margin PM = 83.2°.

From Fig. 8, the following information can be obtained.

1) *Scenario 1 (fixed $I_b = 50$ A, different V_b)*: Fig. 8(a) shows that the magnitude of $T_o(s)$ drops 11.8 dB as V_b varies from 450 to 100 V. Correspondingly, f_c decreases from 455 to 43 Hz, and PM changes from 78.7° to 122°, indicating sluggish dynamic response.
2) *Scenario 2 (fixed $V_b = 100$ V, different I_b)*: In Fig. 8(b), the magnitude of $T_o(s)$ drops 28.2 dB as I_b decreases from 100 to 0 A. Correspondingly, f_c decreases to 17 Hz with PM = 106° at $V_b = 100$ V, $I_b = 0$ A. Likewise, the dynamic response is seriously deteriorated. It is worth noting that there is a sharp magnitude step between Mode a and Mode b in Fig. 8(b), and the magnitude of Mode b becomes very high, leading to PM = −15 °. It means the converter in Mode b cannot stably operate.

The bode plots of $T_o(s)$ shown in Fig. 8 demonstrate that with the fixed-PI current controller $G_c(s)$, the wide variations in either V_b or I_b inevitably pose significant impacts on the dynamic response or even the stability of the EPS-DAB converter. To address this issue, a VPSC method is proposed. Essentially, it incorporates the information of the battery voltage V_b and current I_b into the control algorithm, to ensure improved dynamic performance at all operating points.

B. Proposed VPSC Method

Fig. 9 shows the block diagram of the proposed VPSC method, where an extra compensator, denoted as $G_{sc}(s)$, is introduced and cascaded with the current controller $G_c(s)$. As shown, the two elements $G_{sc}(s)$ and $G_{d\varphi i2}(s)$ are in series in the forward path of the block diagram. Therefore, it is reasonable to regard that $G_{sc}(s)$ is designed to directly compensate the variations in $G_{d\varphi i2}(s)$. In principle, when the battery voltage V_b or current I_b varies, or the operating mode switches, $G_{d\varphi i2}(s)$ is varied. Accordingly, $G_{sc}(s)$ takes effect and dynamically adjusts its parameters to compensate for the variations of $G_{d\varphi i2}(s)$. To simplify the following analysis, $G_{d\varphi i2}(s)$ is decomposed into a normalized term $G'_{d\varphi i2}(s)$ and a static gain $G_{d\varphi i2}|_{V_b=450\text{ V},\ I_b=100\text{ A}} = 946$ calculated at the rated operating point ($V_b = 450$ V, $I_b = 100$ A) from (6) and (8).

By merging $G_{sc}(s)$ and $G'_{d\varphi i2}(s)$, the equivalent transfer function $G_{EAB}(s)$ is defined as

$$G_{EAB}(s) = G_{sc}(s)\, G'_{d\varphi i2}(s). \tag{13}$$

In the manner of (13), the primary objective of $G_{sc}(s)$ is to ensure $G_{EAB}(s) = 1$ within the full operating range, making it immune to the variations in V_b and I_b, and the operating mode transition. As a result, the dynamic performance of the EPS-DAB converter remains consistent at all operating points. To reach this goal, the expected $G_{sc}(s)$ should be derived.

By substituting (8) into (13) and performing algebraic manipulation, the ideal $G_{sc}(s)$ is obtained as

$$G_{sc}(s) = \frac{G_{EAB}(s)}{G'_{d\varphi i2}(s)} = \frac{1}{G'_{d\varphi i2}(s)} = \frac{G_{d\varphi i2}|_{V_b=450\text{ V},I_b=100\text{ A}}}{G_{d\varphi i2}(s)}$$
$$= \begin{cases} \frac{1892 L_k f_s (2-m)}{m N V_1 (4D_\varphi + 1)} & \text{Mode a} \\ \frac{1892 L_k f_s m^2}{N V_1 (2m^2 - 2m + 1)(1 - 2D_\varphi)} & \text{Mode b.} \end{cases} \tag{14}$$

By dynamically adjusting $G_{sc}(s)$ based on real-time measurements of V_b and I_b, the VPSC method is able to maintain $G_{EAB}(s) = 1$, effectively decoupling the loop gain $T_o(s)$ from operating points fluctuations. Consequently, consistent dynamic performance will be achieved within the full operating range.

However, (6) reveals that the computation of D_φ is complex in practice, due to the existence of the square root in both Modes a and b. Alternatively, a second-order polynomial approximation is applied, and the fitted expression is derived as

$$D_{\varphi_f}(V_b, I_b) = \gamma_0 + \gamma_1 V_b + \gamma_2 I_b + \gamma_3 V_b I_b + \gamma_4 V_b^2 + \gamma_5 I_b^2 \tag{15}$$

where V_b and I_b serve as the independent variables, and γ_k ($k = 0, 1, 2, 3, 4, 5$) are the fitted coefficients.

By substituting parameters $V_1 = 700$ V, $L_k = 45$ μH, and $f_s = 10$ kHz into (6), the original three-dimensional (3-D) surface showing the relation of D_φ, V_b, and I_b is depicted in Fig. 10(a). Then, applying the curve fitting toolbox of MATLAB, the coefficients in (15) are extracted as $\gamma_0 = 0.1455$, $\gamma_1 = -0.0011$, $\gamma_2 = 0.0047$, $\gamma_3 = -0.0000081$, $\gamma_4 = 0.0000018$, and $\gamma_5 = -0.0000058$. Accordingly, the fitted 3-D surface from (15) is also depicted in Fig. 10(a). As shown, the fitted surface well matches the original one. The maximum value of error ΔD_φ ($= D_{\varphi_f} - D_\varphi$) is about 0.032 at $V_b = 173$ V and $I_b = 100$ A [see Fig. 10(b), where $D_\varphi = 0.256$ and $D_{\varphi_f} = 0.288$ are calculated from (6) and (15), respectively]. This corresponds to a percentage of 12.5% relative to $D_\varphi = 0.256$, which is acceptable in practical implementations.

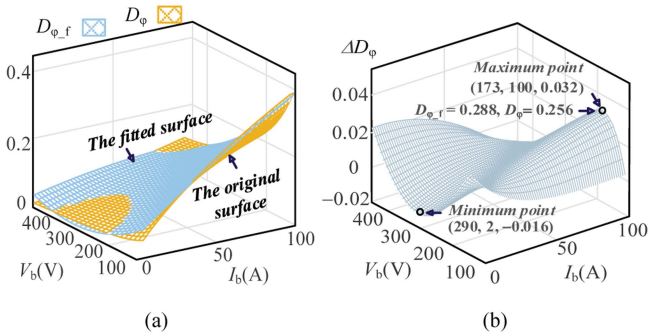

Fig. 10. Three-dimensional surface of D_φ versus V_b and I_b within the full operating range. (a) Surface plot. (b) Fitting errors.

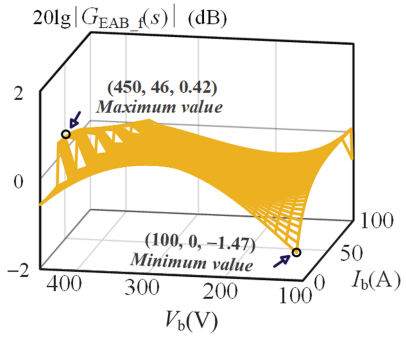

Fig. 11. Three-dimensional surface of the gain $G_{EAB_f}(s)$ within the full operating range.

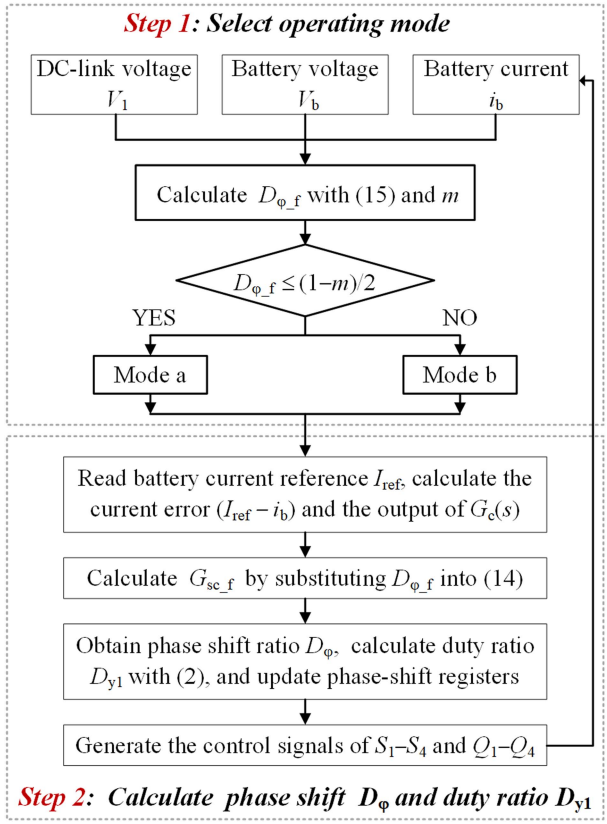

Fig. 12. Flowchart of the constant current controlled EPS-DAB converter with the VPSC method.

The fitted phase shift ratio D_{φ_f} is substituted into (14) to derive the practical compensator, denoted as $G_{sc_f}(s)$. Correspondingly, the transfer function $G_{EAB}(s)$ with $G_{sc_f}(s)$ is denoted as $G_{EAB_f}(s)$. Fig. 11 depicts the surface of $G_{EAB_f}(s)$ under $V_b = 100-450$ V and $I_b = 0-100$ A. As can be observed, the surface of $G_{EAB_f}(s)$ tightly fits the ideal $G_{EAB}(s)$ with the visible deviations of -1.47 dB and 0.42 dB. This confirms that $G_{EAB_f}(s) \approx 1$ (or 0 dB) is maintained within the full operating range.

Based on the above-mentioned analysis, a control flowchart is presented in Fig. 12, with the detailed procedures outlined as follows.

1) *Signal acquisition*: Measure and sample the dc-link voltage V_1, the battery voltage V_b, and the battery current i_b.
2) *Parameter calculation*: Calculate the voltage-conversion ratio m ($= NV_b/V_1$) and the fitted phase shift ratio D_{φ_f} using (15).
3) *Operating mode selection*: Confirm the operating mode according to the relation of D_{φ_f} and $(1-m)/2$. If $D_{\varphi_f} \le (1-m)/2$, Mode a is selected. Otherwise, Mode b is selected.
4) *Current regulation*: Read the target battery current reference I_{ref}, compute the current error Δi_b ($I_{ref} - i_b$), and feed Δi_b into the PI controller $G_c(s)$ to generate the preliminary control signal.
5) *Compensator adjustment*: Derive the practical compensator $G_{sc_f}(s)$ by substituting D_{φ_f} into (14).
6) *Phase shift ratio and duty cycle generation*: Obtain the shift phase D_φ, calculate the duty ratio D_{y1} with (2), and update the corresponding phase shift registers in the DSP.
7) *Gate signal synthesis*: Generate pulsewidth modulation (PWM) signals for switches S_1-S_4 and Q_1-Q_4 to regulate power flow. Then return to step 1) for the next control cycle.

It is worth noting that the reverse power flow operation of the EPS-DAB converter is structurally symmetrical to the forward power flow operation. Therefore, the proposed VPSC method achieves consistent performance under the reverse operation. Given this symmetry, the analysis of the reverse operation is omitted for brevity.

C. Effectiveness of the VPSC Method

To intuitively verify the effectiveness of the proposed VPSC method, the two scenarios analyzed in Fig. 8 are still compared here. Fig. 13 shows the Bode plots of the loop gain $T_o(s)$ with the VPSC method and the fitted values of γ_k ($k = 0, \ldots, 5$) extracted in Section III-B. From Fig. 13, the following observations can be made.

1) *Scenario 1 (fixed $I_b = 50$ A, different V_b)*: As depicted in Fig. 13(a), the crossover frequency f_c varies between

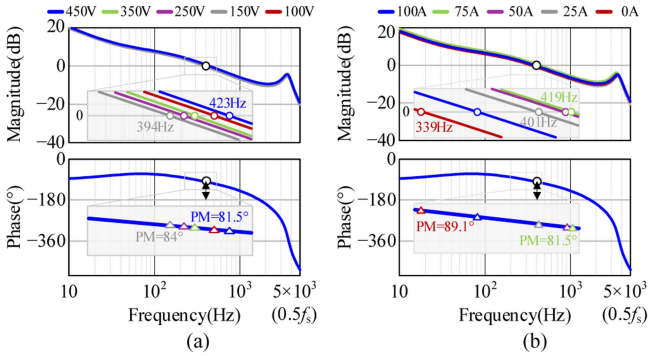

Fig. 13. Bode plots of $T_o(s)$ with the proposed VPSC method under different operating conditions. (a) Fixed $I_b = 50$ A with different V_b. (b) Fixed $V_b = 100$ V with different I_b.

394 and 423 Hz, and the phase margin PM remains within 81.5°−84°.

2) *Scenario 2 (fixed $V_b = 100$ V, different I_b)*: It can be seen from Fig. 13(b) that f_c varies between 339 to 419 Hz, and PM remains within 81.5°−89.1°.

Compared with Fig. 8, both f_c and PM exhibit smaller variations under these two scenarios when using the VPSC method. Notably, the system achieves $f_c = 423$ Hz with PM = 81.5° at the operating point (450 V, 50 A), corresponding to the maximum gain of $G_{EAB_f}(s) = 0.42$ dB (see Fig. 11). In contrast, at the operating point (100 V, 0 A), f_c decreases to 339 Hz with PM = 89.1°, matching the minimum gain of $G_{EAB_f}(s) = -1.47$ dB (see Fig. 11). The loop gains $T_o(s)$ at other operating points lie between these extremes, resulting in f_c maintaining a range of 339−423 Hz, with PM remaining within 81.5°−89.1° within the full operating range. These results confirm that the proposed VPSC method with the fitted D_{φ_f} enhances the robustness against the wide variations in battery voltage and current, ensuring consistent dynamic performance under all operating points.

Empirically, parametric drift is inevitable in practical applications. As shown in (14), the compensation function $G_{sc}(s)$ is related to the inductance L_k, which may drift in practice. To quantify this sensitivity, the normalized inductance deviation between the practical and rated values of L_k (denoted as L_{kp} and L_{kr}, respectively,) is defined as

$$\Delta L_{k(pu)} = (L_{kp} - L_{kr})/L_{kr} \times 100\%. \tag{16}$$

Accordingly, (13) is rewritten as

$$G_{EAB_f}(s) = G_{sc_f}(s)\big|_{L_{kr}} G'_{d\varphi i2}(s)\big|_{L_{kp}} = \begin{cases} \dfrac{L_{kr}\left(4D_\varphi\big|_{L_{kp}}+1\right)}{L_{kp}(4D_{\varphi_f}+1)}, \text{Mode a} \\ \dfrac{L_{kr}\left(1-2D_\varphi\big|_{L_{kp}}\right)}{L_{kp}(1-2D_{\varphi_f})}, \text{Mode b.} \end{cases} \tag{17}$$

When $L_{kp} \neq L_{kr}$ (i.e., $\Delta L_{k(pu)} \neq 0$), $G_{EAB_f}(s) \neq 1$, implying that the magnitude of $G_{EAB_f}(s)$ deviates from 0 dB. Fig. 14 illustrates the magnitude variation of $G_{EAB_f}(s)$ under $\Delta L_{k(pu)} = \pm 15\%$, which is presented to demonstrate the sensitivity to inductance tolerance. For $\Delta L_{k(pu)} = -15\%$ [see Fig. 14(a)], the maximum and minimum magnitudes of $G_{EAB_f}(s)$ are 1.93 dB and −0.06 dB, respectively; for $\Delta L_{k(pu)} = +15\%$ [see Fig. 14(b)], they are −0.65 and −2.3 dB, respectively. From the perspective of gain margin (GM), $20\lg|G_{EAB_f}| = 1.93$ dB is the worst case. Given the rated GM when $\Delta L_{k(pu)} = 0$ is set as 6 dB, the rest GM at the worst case will be 4.07 dB, indicating that the proposed VPSC method guarantees robustness to the inductance drift. In fact, an accurate inductance measurement method was pesented in [35]. Thereby, the parameter tolerance can be further optimized.

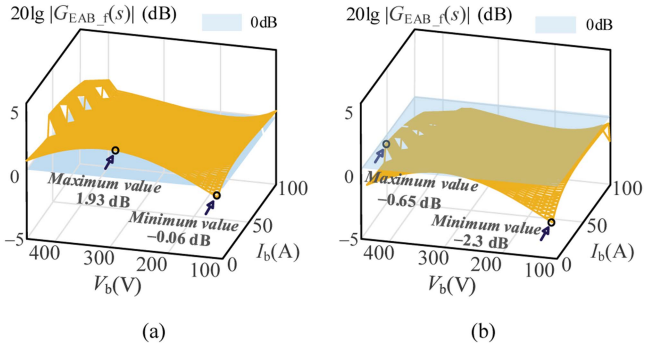

Fig. 14. Magnitude plots of the gain $G_{EAB_f}(s)$ with the VPSC method under fluctuating inductance parameters. (a) $\Delta L_{k(pu)} = -15\%$. (b) $\Delta L_{k(pu)} = +15\%$.

TABLE II
PROTOTYPE PARAMETERS

Main circuit parameters			
DC-link voltage V_1	700 V	Filter capacitor C_f	1 mF
Battery voltage V_b	100-450 V	Filter inductor L_f	1.9 μH
Rated battery current I_b	±100 A	Dead time t_{dead}	1.2 μs
Switching frequency f_s	10 kHz	Calculation period T_s	100 μs
Series inductance L_k	46.2 μH	Proportional gain K_p	0.0028
Transformer turns ratio N	3:2	Integral gain K_i	0.703
Main power components (DAB converter)			
Si IGBTs S_1–S_4	FF225R12ME4P (Infineon)		
Si IGBTs Q_1–Q_4	FF225R12ME4P (Infineon)		
Transformer	Magnetic core	EE110/56/36-PC95	
	Winding resistance	2.1 mΩ/1.2 mΩ	
	Magnetizing inductance	3.6 mH	
	Leakage inductance	46.2 μH	
Main power components (Battery)			
Internal cell voltage	3.7 V(2.5-4.2 V)	Nominal pack voltage	37 V(10S1P)
Capacity	120 Ah	Operating SOC range	10%–90%
Charge/discharge C-rate	1C (Charge), 3C (Discharge)	Internal resistance (25°C, 50% SOC)	4 mΩ

IV. EXPERIMENTAL VERIFICATION

A. Experimental Setup

Fig. 15 shows the experimental setup employed to validate the VPSC method. The main circuit parameters and components are listed in Table II. In this configuration, a front-end three-phase PWM rectifier regulates the dc-link voltage V_1 at 700 V (±1%), providing a fixed input to the EPS-DAB converter. The output of the EPS-DAB converter interfaces with the real lithium-ion battery packs, which operate from 100 to 450 V.

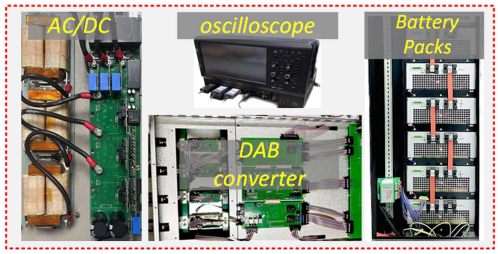

Fig. 15. Photograph of the battery charging/discharging platform.

The eight switches of the DAB converter are composed of four Infineon IGBT modules (FF225R12ME4). These modules (1200 V/225 A rating) ensure stable performance at the maximum power rating of 45 kW. The high-frequency transformer is designed with EE110/56/36 ferrite cores (PC95 material) and a 3:2 turns ratio, featuring a leakage inductance of 46.2 μH to minimize circulating currents while maintaining galvanic isolation. The control algorithm is implemented in a 32-bit floating-point DSP (TMS320F28377D). The integrated PWM modules and 16-bit analog-to-digital converters enable precise gate signal generation and low-latency feedback acquisition.

In the setup, the lithium-ion battery packs are modularized by 10 series-connected ternary lithium-ion cells (3.7 V, 120 Ah per cell), with key specifications listed in Table II as well. There are 3–12 packs (preconditioned to 40%–60% SOC) in series, and the nominal output voltages are from 100 V (3 packs) to 450 V (12 packs). This configuration facilitates the validation of the VPSC method to wide voltage ranges (100–450 V) and SOC-dependent voltage dynamics, which are critical for practical battery energy storage systems.

B. Experimental Results

For experiments, the EPS modulation with minimum-RMS-current optimization is implemented, and the performance of the VPSC method is evaluated. Fig. 16 presents the experimental results with the proposed VPSC method at $V_{\rm b} = 380$ V, where Fig. 16(a) and (b) correspond to the steady-state and dynamic waveforms, respectively. Comparing Fig. 16(a) with Fig. 2, it can be seen that the waveforms of bridge voltages $v_{\rm AB}$, $v_{\rm CD}$, and series inductor current $i_{\rm p}$ are consistent. In Fig. 16(b), a series of step changes are applied to the battery current reference $I_{\rm ref}$, where $I_{\rm ref}$ is arranged to step from 0 to 50 A, from 50 to 100 A, from 100 inversely to -100 A (reverse step), from -100 to -50 A, and from -50 to 0 A in sequence at five distinct time instants. It can be seen that no overshoot is incurred by each step, and the corresponding settling times are 2.3, 2.2, 4.3, 2.2, and 2.4 ms, respectively. The longest one (4.3 ms) does not exceed the expected 6 ms in practical applications, validating that good dynamic response at $V_{\rm b} = 380$ V is ensured by the proposed VPSC method even when the extreme transition occurs.

Figs. 17–20 are provided for evaluating the performance of the VPSC method under the above two scenarios, where Scenario 1 is exhibited in all four figures, and Scenario 2 is reflected in Fig. 20(a). It is known that the actual output voltage of the battery packs can hardly precisely operate at the above theoretical values (e.g., 450, 250, 150, and 100 V) in practice, which depends on the battery conditions such as real-time SOC. Thus, these experiments are conducted under four battery voltages: $V_{\rm b} =$ 450, 270, 162, and 107 V. Likewise, the current reference steps are set the same with those shown in Fig. 16.

Fig. 17 shows the experimental results at $V_{\rm b} = 450$ V. It can be observed that the settling times of the two cases (with and without VPSC method) at each step are equal, which are 2.1, 2.4, 3.7, 2.4, and 1.6 ms. This equality benefits from $G_{d\varphi i2}(s)$ keeping almost constant when $V_{\rm b} = 450$ V [see (8)].

Figs. 18 and 19 show the experimental results for $V_{\rm b} = 270$ V and $V_{\rm b} = 162$ V, respectively. It can be seen that without the VPSC method, the associated settling times are 4.9, 3.8, 8.2, 4.1, 4.5 ms and 11.6, 7.8, 15.1, 8.2, 11.2 ms, respectively. In contrast, with the VPSC method, they decrease to 2.1, 2.5, 5.2. 2.5, 2.1 ms and 2.3, 2.9, 5.7, 2.7, 2.3 ms, respectively. Likewise, the longest settling times at these two battery voltages are less than 6 ms. With the VPSC method, the longest settling times at $V_{\rm b} = 270$ V and $V_{\rm b} = 162$ V are reduced by 36% (from 8.2 to 5.2 ms) and 62% (15.1 to 5.7 ms), respectively.

Fig. 20 highlights the advantage of the proposed VPSC method under the extreme low-voltage condition $V_{\rm b} = 107$ V. As can be observed, without the VPSC method, the settling time is 19 ms when $I_{\rm ref}$ steps from 0 to 50 A. Unfortunately, when $I_{\rm ref}$ steps from 50 to 100 A, oscillations arise in $i_{\rm p}$ and $i_{\rm b}$, which indicates the converter is unstable. These results agree with the analysis shown in Fig. 8(b), where PM $= 112°$ and PM $= -15°$ hold. With the VPSC method, oscillations do not appear even when the battery current steps from 100 A inversely to -100 A. The settling times at each step are 2.4, 2.4, 4.5, 2.3, and 2.2 ms.

All the abovementioned waveforms shown in Figs. 16–20 come from $V_1 = 700$ V. In fact, V_1 is sometimes required to be regulated within 600–800 V in practical applications. Thus, the dynamic responses at $V_1 = 600$ V and $V_1 = 800$ V are presented in Fig. 21. Here, $V_{\rm b} = 270$ V is taken as an example. Fig. 21(a) shows that the settling times at $V_1 = 600$ V are 2.4, 2.6, 5.7, 2.7, and 2.4 ms. Fig. 21(b) shows that the settling times at $V_1 = 800$ V are 2.2, 2.4, 5.2, 2.5, and 2.3 ms. Compared with $V_1 = 700$ V, where the settling times are 2.1, 2.5, 5.2, 2.5, and 2.1 ms [see Fig. 18(b)], the dynamic responses are almost unchanged, where the deviation is no more than 0.5 ms. These results demonstrate the adaptability of the VPSC method to the different dc-link voltages, ensuring stable performance in applications with variable dc-link voltage.

The measured efficiency of the EPS-DAB converter under different battery voltages $V_{\rm b}$ and currents $I_{\rm b}$ is depicted in Fig. 22. The converter efficiency is above 95% when $V_{\rm b} = 450$ V, with the load ranges from 20% to 100%. The peak efficiency is 97.2% at $V_{\rm b} = 450$ V and $I_{\rm b} = 80$ A (36 kW, 60% of the rated power). As can be observed, the efficiency curve drops when $V_{\rm b}$ decreases since the transmitted power decreases at the same battery current.

Fig. 23 shows the longest settling times extracted from Figs. 17–20 and the code running times. The comparison results verify that the proposed VPSC method significantly improves the dynamic response of the EPS-DAB converter at cost of a little

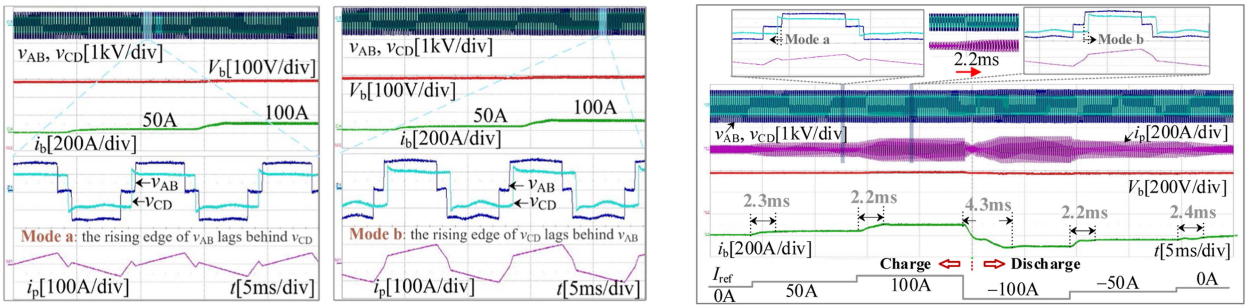

Fig. 16. Experimental waveforms under $V_b = 380$ V. (a) Steady-state waveforms. (b) Dynamic waveforms with the proposed VPSC method.

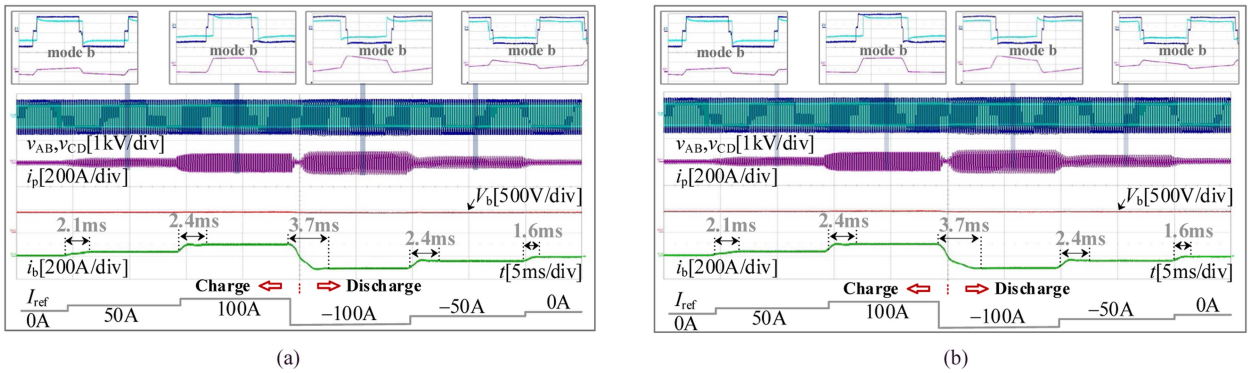

Fig. 17. Experimental waveforms under $V_b = 450$ V. (a) Without VPSC method. (b) With VPSC method.

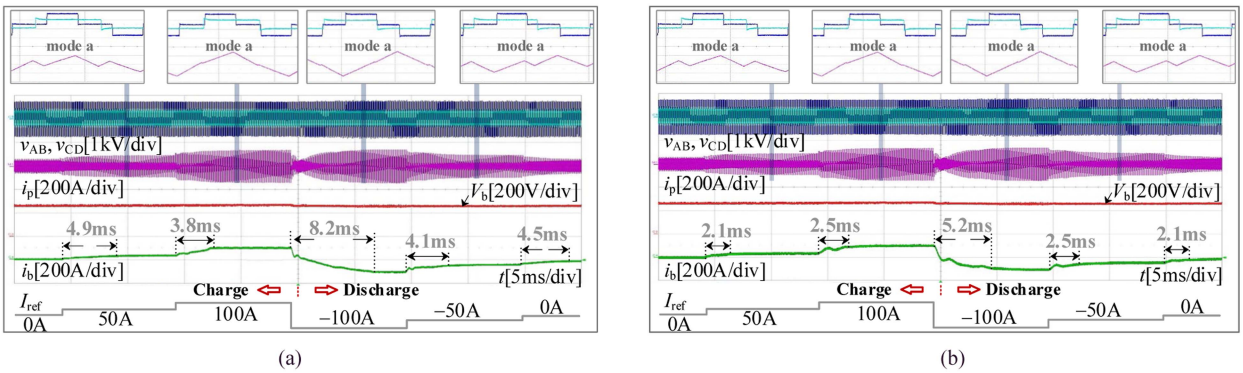

Fig. 18. Experimental waveforms under $V_b = 270$ V. (a) Without VPSC method. (b) With VPSC method.

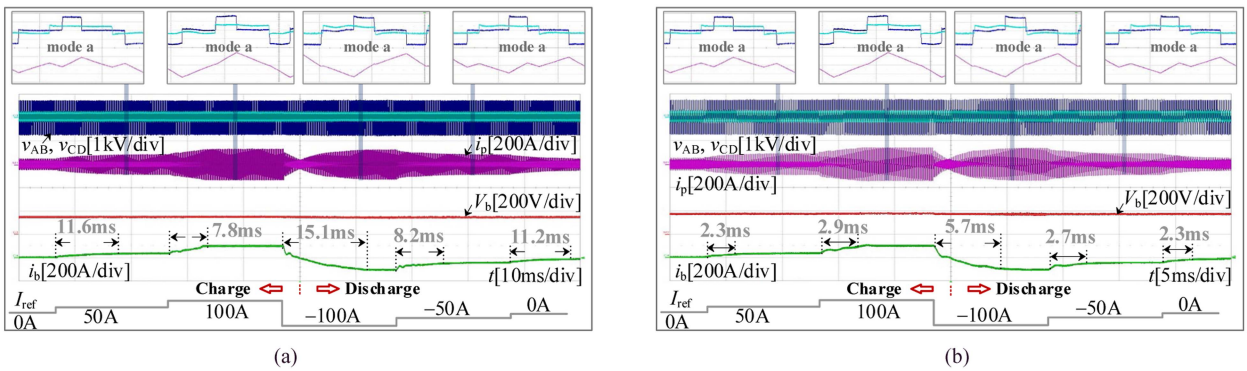

Fig. 19. Experimental waveforms under $V_b = 162$ V. (a) Without VPSC method. (b) With VPSC method.

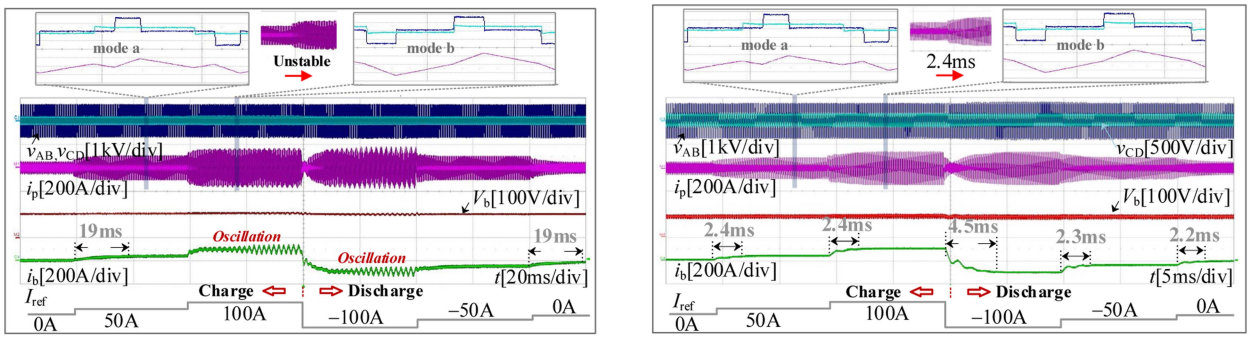

Fig. 20. Experimental waveforms under $V_b = 107$ V. (a) Without VPSC method. (b) With VPSC method.

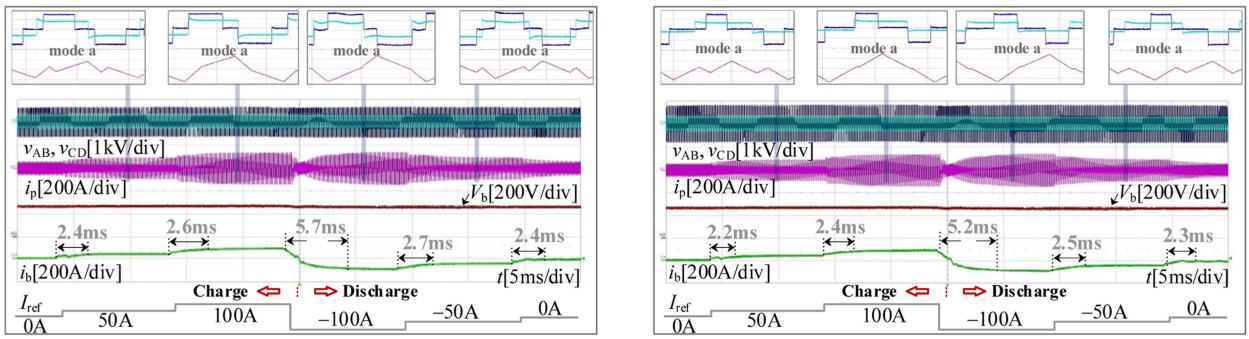

Fig. 21. Experimental waveforms under $V_b = 270$ V with different DC-link voltage V_1. (a) $V_1 = 600$ V. (b) $V_1 = 800$ V.

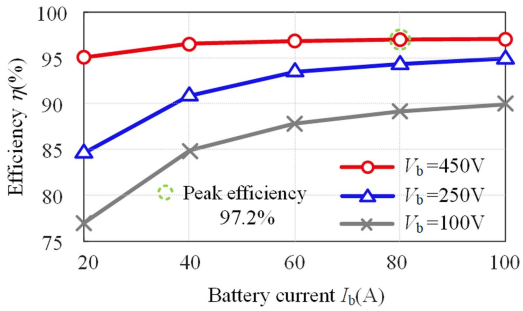

Fig. 22. Experimental efficiency curves under different battery voltages.

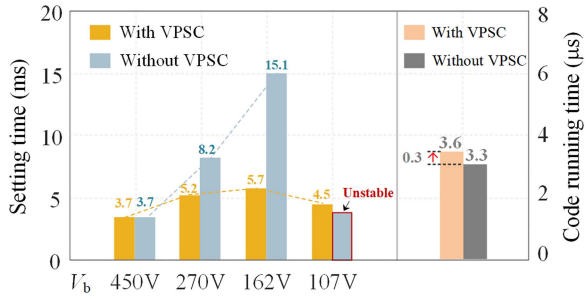

Fig. 23. Dynamic performance and code running time comparisons between the cases with and without VPSC method.

computational latency increase. In fact, the code running time of the VPSC method shown in Fig. 23 includes signal sampling and calculation of dc-link voltage V_1, battery voltage V_b, and battery current i_b; PI algorithm execution [see (12)]; VPSC execution [see (14) and (15)]; and DPWM register assignment. The VPSC method achieves a total latency of 3.6 μs, with the compensation stage adding only 0.3 μs of overhead compared to the baseline PI control. This minimal overhead is attributed to a single division operation and low-complexity arithmetic for the compensation terms in (14) and (15). Besides, the algorithm of the VPSC method avoids iterative loops and large lookup tables, thus ensuring negligible impact on code space complexity.

It is worth noting that the proposed VPSC method mitigates electrochemical stress on the battery since no current overshoot occurs, thereby enhancing the long-term reliability. On the other hand, the resultant fast dynamic response ensure rapid safety-critical current limits in both constant voltage and current limiting modes. It also enhances system reliability throughout battery charging and discharging cycles.

C. Comparison With the Existing Control Methods

The performance of the proposed VPSC method is compared with those of the existing control methods, as summarized in Table III. The key items for comparison include modulation scheme, switching frequency, rated power, dynamic response (i.e., settling time and overshoot), implementation complexity, and battery voltage adaptability. Here, implementation complexity refers to the microprocessor computational power required

TABLE III
COMPARISON OF DYNAMIC PERFORMANCE AMONG DAB CONVERTERS WITH DIFFERENT CONTROL METHOD

Control method	Modulation scheme	Switching frequency	Rated power	Load/reference step change	Settling time/overshoot	Implementation complexity	Output voltage
FFCC-LFF [26]	SPS	25 kHz	120 W	1 →6 A	0.5 ms / 10% overshoot	low	22 V
VDPC [27]	SPS	10 kHz	160 W	2.45 →3.27 A	< 1 ms / Negligible	Medium	49 V
SMC-DISM [28]	SPS	10 kHz	1.5 kW	0 →10 A	3 ms / zero overshoot	High	75 V
MDCS-MPC [30]	TPS	20 kHz	1 kW	0.7 →3.3 A	8 ms / 2% overshoot	High	260 –300 V
Proposed VPSC	EPS	10 kHz	45 kW	100 → –100 A	5.7 ms / zero overshoot	low	100 –450 V

for the control method to function. The information shown in Table III indicates the following.

1) Even in high-power applications, the proposed VPSC method can ensure the DAB converter stably operates within wide-range battery voltage.
2) Although the worst current step (100→−100 A) is provided for comparison, the proposed VPSC method can not only avoid overshoot, but also ensure only 5.7 ms settling time, which is very close to the settling times of the existing control methods.
3) The implementation of the proposed VPSC method is much easier than those of the existing control methods. The compensation function and the polynomial-fit approximation are not complex, and thus the implementation of the proposed VPSC method avoids computationally intensive operations such as square-root calculations (VDPC [27]), trigonometric functions (SMC-DISM [28]), and iterative optimization (MDCS-MPC [30]). This enables real-time execution on low-cost microcontrollers, reducing hardware costs and latency.

V. CONCLUSION

This article established a small-signal model of the EPS-DAB converter with minimum-RMS-current optimization, the impact of battery voltage V_b and current I_b variations on dynamic performance is evaluated. The key findings are as follows.

1) Although fixed-parameter PI current controller can avoid overshoot, it can hardly ensure the settling time to be less than 6 ms at all operating points. Moreover, instability may be incurred.
2) The proposed VPSC method tends to ensure the loop gain of the EPS-DAB converter dynamically adaptive to the variations in the battery voltage and current. Sufficient experimental results demonstrate that the overshoot can be avoided and the settling time can be reduced less than 6 ms even under the worst case when the battery voltage is 107 V and the battery current steps from 100 to −100 A.
3) Due to the polynomial-fit approximation, the implementation of the proposed VPSC method becomes easy, and the total code running time is only 3.6 μs.

In fact, the proposed VPSC method can also be adopted to other modulations such as DPS- and TPS-DAB converters. It is a robust solution for EV fast charging, grid-tied energy storage, and other applications requiring fast dynamic response and zero overshoot. Future work will focus on the scalability of the VPSC method to multimodule scenarios and hybrid energy systems.

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Feng Wang (Student Member, IEEE) received the B.S. degree in electrical engineering from Zhengzhou University, Zhengzhou, China, in 2019, and the M.S. degree in electrical engineering in 2022 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include bidirectional dc/dc converters and battery energy management system.

Xuehua Wang (Member, IEEE) received the B.S. degree in electrical engineering from Nanjing University of Technology, Nanjing, China, in 2001, and the M.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2004 and 2008, respectively.

Since 2008, he has been with Huazhong University of Science and Technology, Wuhan, China, where he was a Postdoctoral Fellow from 2008 to 2011 and is currently a Professor with the School of Electrical and Electronic Engineering. His main research interests include multilevel inverter and renewable energy generation system.

Jialing Yuan received the B.S. degree in electrical engineering and automation in 2022 from Huazhong University of Science and Technology, Wuhan, China, where he is currently working toward the M.S. degree in electrical engineering.

His current research interests include the soft switching technology and small-signal modeling of dc–dc converter.

Xinbo Ruan (Fellow, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively.

In 1996, he joined the Faculty of Electrical Engineering Teaching and Research Division, NUAA, where he became a Professor with the College of Automation Engineering, in 2002, and has been engaged in teaching and research in the field of power electronics. From August to October 2007, he was a Research Fellow with the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong, China. From March 2008 to August 2011, he was also with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China. He has authored or coauthored 13 books and more than 300 technical papers published in journals and conferences. His main research interests include resonant and soft-switching power converters, power converter topologies and control, grid-connected converters and system for renewable energy, modeling and stability of power converters, and envelop tracking power supply.

Dr. Ruan was a recipient of the Sustainable Energy Systems Technical Achievement Award from IEEE Power Electronics Society in 2022, the Delta Scholarship by the Delta Environment and Education Fund in 2003, and the Special Appointed Professor of the Chang Jiang Scholars Program by the Ministry of Education, China, in 2007. From 2005 to 2013, and since 2017, he has been serving as a Vice President of the China Power Supply Society (CPSS). From 2014 to 2016, he served as a Vice Chair of the Technical Committee on Renewable Energy Systems within the IEEE Industrial Electronics Society.

He currently serves as an Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS ON POWER ELECTRONICS and Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE OPEN JOURNAL OF THE INDUSTRIAL ELECTRONICS SOCIETY, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS - II. He was the General Chair of IPEMC-ECCE Asia 2020 and the General Secretary of IPEMC-ECCE Asia 2009, a Technical Program Committee Chair of the IEEE 7th Annual Energy Conversion Congress and Exposition (ECCE2015), and a Tutorial Committee Chair of the IEEE 12th Annual Energy Conversion Congress and Exposition (ECCE2020).