A Safe and Fast Closed-Loop Start-Up Strategy for Triple-Active-Bridge Converters Under DC Microgrid Application

Yuxuan Li, Lingfeng Jiang, *Student Member, IEEE*, Ziqian Wang, Linxiao Gong, *Student Member, IEEE*, and Junzhong Xu, *Member, IEEE*

***Abstract*—Triple active bridge (TAB) converters are widely adopted in dc microgrids, wherein the safe and fast start-up is a key operational requirement. Due to the integrated topology, it is difficult to establish an online and closed-loop start-up strategy to meet this requirement. A common approach is to operate the TAB converter as the dual active bridge (DAB) converter to simplify the start-up process, leading to insufficient output power and limited start-up speed. To address these issues, a closed-loop start-up strategy with dual single phase-shift (DSPS) modulation tailored for the TAB converter is proposed in this article. Major contributions include three aspects. First, a slope comparison method is proposed to quickly observe the system's maximum current point for safe operation. Second, a novel partial derivative tracing method is proposed to solve optimal phase-shift angles for online control. Finally, a safe, fast, and simplified closed-loop TAB start-up strategy based on DSPS control is developed, which maximizes output power while ensuring safe current limitation. The experimental results verify the effectiveness of the proposed strategy. With DSPS control, the start-up speed can be increased by 34% while maintaining controllable current stress compared to the direct application of the DAB start-up strategy.**

***Index Terms*—Dual single phase-shift (DSPS) control, maximum current point observation, start-up dynamics, triple active bridge (TAB) converter.**

I. Introduction

IN RECENT years, the research on dc microgrids has garnered substantial attention. dc–dc converters, as a crucial component, have increasingly become the focus of industry inquiry. Consequently, three-port converters (TPCs) have emerged [1], [2], [3], providing benefits such as improved integration, minimized system losses, high power density, and flexible energy transfer within dc microgrid systems [4], [5]. As depicted in Fig. 1, a typical TPC structure combines the dc bus, high voltage (HV) storage battery, and loads through magnetic integration, thereby enabling flexible power transmission among these components. Currently, the most extensively researched TPC topology is the triple active bridge (TAB) converter [6], [7], [8], whose power transfer is regulated through phase-shift modulation [9]. Since TAB converters are widely used in dc microgrids, a safe and fast start-up process is crucial to improve the system′s stability, especially when the operating TAB converter occurs fault event and the back-up TAB converter needs to rapidly start-up and access to the loads [10].

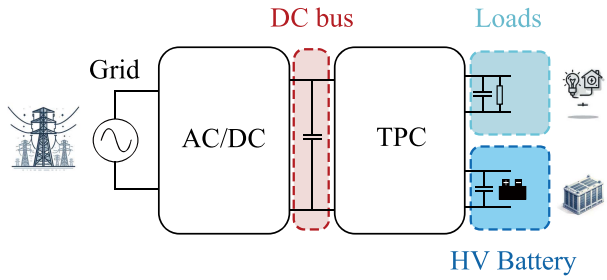

Fig. 1. Typical TPC construction under DC microgrid application.

During the start-up of TAB converters, the load port voltage must be rapidly ramped up to the desired level. However, in the initial stage of start-up, the uncharged output capacitor is equivalent to a short circuit, leading to a rapid increase in inductor current, potentially surpassing safe limits and causing damage to the switches [11]. Therefore, it is necessary to investigate safe and fast start-up strategies for TAB converters.

However, due to the complicated power model and phase-shift combinations, it is difficult to establish an online and closed-loop start-up strategy for TAB converters. Since the TAB converter is derived from the dual active bridge (DAB) converter, it is feasible to derive common start-up strategy for the TAB converters from those utilized for the DAB converters.

From the perspective of DAB converters, a straightforward engineering application is disconnecting the high-voltage battery port before the start-up process, allowing the TAB converter to operate in two-port mode. Conventional DAB start-up strategies

Received 23 December 2024; revised 27 March 2025; accepted 4 May 2025. Date of publication 9 May 2025; date of current version 30 June 2025. Recommended for publication by Associate Editor A. Davoudi. *(Corresponding author: Linxiao Gong.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3568647.

Digital Object Identifier 10.1109/TPEL.2025.3568647

are mostly open-loop and typically divide the start-up process into several steps. Giuliani et al. [12], Gammeter et al. [13], and Zhao et al. [14] proposed two-step start-up strategies: Initially, the primary inner phase-shift angle increases slowly to raise the voltage, and upon reaching a certain level, the system transitions into variable gain closed-loop control. Moreover, Pugliese et al. [15] and Liu et al. [16] proposed three-step start-up strategies to better control the inrush current and raise the start-up speed, Yao et al. [17] proposed a five-step start-up strategy to further improve the effectiveness of the start-up process. Despite the above open-loop strategy can limit the inrush current and achieve a safe start-up process, the open-loop start-up strategy require precise tuning of the ramp rate of the phase-shift angle and the reference voltage value, making the start-up process highly dependent on parameter design. Considering the low applicability of open-loop start-up strategy, contemporary research has increasingly focused on closed-loop control strategies with advanced phase-shift modulation. Hu et al. [18] proposed an extended phase-shift (EPS) —trapezoidal-current modulation (TZM) and triple phase-shift (TPS)—TZM start-up strategy, integrating EPS and TPS to limit the current to safe levels during the start-up while ensuring soft switching. Besides, a closed-loop start-up strategy based on a multimodal EPS with dc bias suppression was proposed in [19]. Moreover, Gong et al. [20] proposed a variable-frequency and phase-shift control, which significantly increases output power during the start-up process and further enhances the start-up speed.

Essentially, when applying the above strategies to the TAB converters operating in two-port operation, only two ports are employed across the whole start-up process, significantly degrading the overall power output capability of the TAB converters. Additionally, after the start-up process, the disconnected port needs to be joined to steady-state operation, adding extra steps to the overall start-up process and further restricting the start-up speed. Consequently, it is imperative for the TAB converter to operate in three-port operation to maximize the output power capability. Nevertheless, the three-port structure of the TAB converter makes it very difficult to conduct detailed model analysis as is done for the DAB converter, limiting the direct application of the DAB start-up strategies such as EPS and TPS. As a result, a safe and fast start-up control strategies that can be implemented online for the TAB converters are currently lacking.

In fact, for the TAB converters' start-up process, the SPS control can be more suitable than the aforementioned multiple phase-shift (MPS) control, as it offers high output power and simplified modulation. Furthermore, the adoption of SPS control in TAB converters differs significantly from that in DAB converters, as two external phase-shift angles can be utilized to control the start-up process. Therefore, one phase-shift angle is set to meet the output voltage requirement, while the other can be used to optimize the current stress within safe limits. In the following text, the SPS control adopted in TAB converters is referred to as dual SPS (DSPS) control.

To enhance the safety, speed, applicability and simplicity of the TAB converters′ start-up process, a closed-loop start-up strategy for the TAB converters is proposed in this article, in which the TAB converter operates in three-port operation based on DSPS. The primary contributions of this article are as follows:

1) *Maximum Current Observation Strategy Derived From Slope Comparison Method* (SCM): The core of safe start-up is to observe the current stress point among the three ports, and the real-time maximum current observation strategy based on SCM simplifies the process of observing the current stress point, reducing the computational burden of the start-up control.
2) *Optimized Phase-shifting Angles Calculated by Partial Derivative Tracing Method* (PDT): Instead of solving the Karush–Kuhn–Tucker (KKT) equations, the proposed PDT facilitates a more streamlined mathematical derivation process, thereby the online control can be implemented.
3) *Closed-Loop Start-up Control Strategy With Safe and Fast Features*: Derived from SCM and PDT, the closed-loop control strategy based on DSPS is proposed, which leverages the full power output capability of the input port to expedite the start-up process while constraining the current in the safe limits. During the start-up, both the dc bus and the battery port transfer power to the load port. Upon finishing the start-up, the system transitions smoothly into steady-state stage.

The rest of the article is organized as follows: In Section II, a concise introduction to the operating principle of the TAB is provided. Moreover, the time-domain expressions for current under DSPS control are derived. In Section III the SCM and PDT is introduced to derive the start-up strategy. In Section IV, the safe and fast start-up strategy for the TAB converter is proposed. Moreover, the control block diagram of the system is presented with simulation result verifying system characteristic. In Section V, a prototype is constructed to validate the proposed start-up strategies. Finally, Section VI concludes this article.

II. Operation Principle and Modeling of the TAB Converters

A. Analysis of the TAB Converter Under DSPS Control

The circuit schematic of the TAB converter and the DSPS control timing diagram are shown in Fig. 2, where the voltages V_1, V_2', V_3' represent the dc-bus voltage, the battery voltage, and the load voltage, respectively. The input or output currents are represented by I_1, I_2', I_3', whereas $R'_{3\mathrm{eq}}$ symbolizes the equivalent resistance of port3. Additionally, the output capacitors are represented by C_1, C_2', C_3'. Each full bridge connected to the three-port transformer through an inductor, labeled as L_1, L_2', L_3', with corresponding impedances defined as Z_1, Z_2', Z_3'. The impedance-inductance relationship is given by (1), where f_s represents the switching frequency. The number of transformer turns are designated as n_1, n_2, and n_3. The switches of each port are represented as $\mathrm{Q}_{xy,}$ where x corresponds to ports 1, 2, or 3, and y corresponds to switch numbers 1, 2, 3, or 4.

Under DSPS control, the voltage waveforms for each port are square waves. The midpoint voltages of the bridges at each port are represented by v_1, v_2', v_3'. The phase-shift angles between midpoint voltages of port 2 and port 3 are

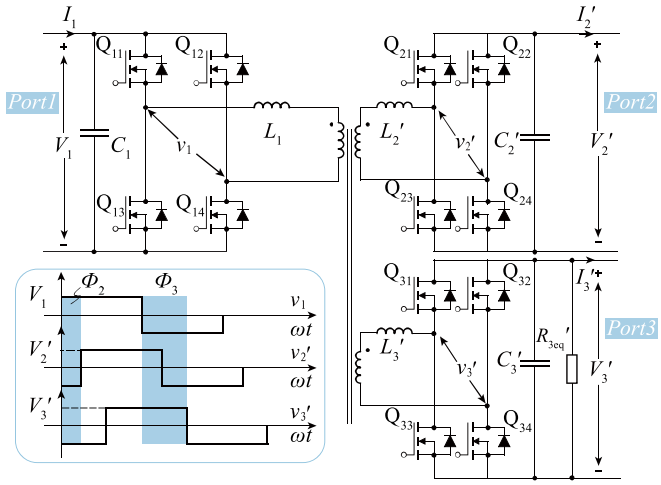

Fig. 2. Circuit topology and DSPS control timing diagram of the TAB converter.

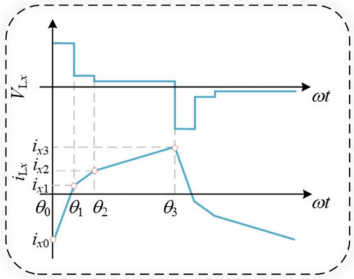

Fig. 3. Inductor voltage and current waveforms.

Φ_2 andΦ_3, respectively, taking port1 as reference. Since port 2 is connected to battery, which can operate as source or load, to maximize the output power during start-up, it is vital for both port1 and 2 to transfer power to port3 simultaneously. Consequently, the external phase-shift angles must satisfy the condition: $0 < \Phi_2 < \Phi_3 < 0.5\,\pi$. Moreover, during calculations, parameters for port 2 and port 3 are normalized to port1, with the relationship expressed in (2).

To simplify the following derivation, assumptions are made that the voltage and current of the inductor follow a strictly linear with no parasitic parameters, the transformer remains unsaturated during start-up and the on-resistance of the switch is ignored

$$\begin{cases} Z_1 = 2\pi f_s L_1 \\ Z_2' = 2\pi f_s L_2' \\ Z_3' = 2\pi f_s L_3' \end{cases} \tag{1}$$

$$\begin{cases} V_2 = \frac{n_1}{n_2} V_2', V_3 = \frac{n_1}{n_3} V_3' \\ v_2 = \frac{n_1}{n_2} v_2', v_3 = \frac{n_1}{n_3} v_3' \\ Z_2 = \frac{{n_1}^2}{{n_2}^2} Z_2', Z_3 = \frac{{n_1}^2}{{n_3}^2} Z_3' \end{cases}. \tag{2}$$

The inductor voltage (V_{xL}) and current (i_{xL}) waveforms of the TAB converter under DSPS control are illustrated in Fig. 3, with $\theta_0, \theta_1, \theta_2$, and θ_3 representing the commutation point of the

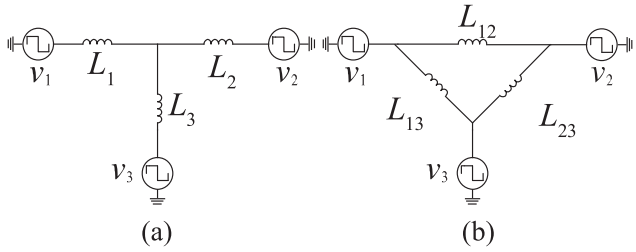

Fig. 4. Equivalent circuit of TAB. (a) T-type. (b) Δ-type.

inductor current. Since the inductor current varies linearly with its voltage, the inductor current waveform of the TAB converters manifests as piecewise linear. The slope of these segments is determined by the voltages of each port. The commutation currents are marked with i_{xy}, where x represents the port number and y represents the corresponding moment in the half cycle. According to the symmetry of the inductor current, the maximum inductor current can be controlled by solely calculating within a half cycle instead of the whole cycle.

Based on the common equivalent transformation of multi-port circuit, the TAB converters can be transformed into T-type and Δ-type circuit, as shown in Fig. 4. The impedance relationship between T-type and Δ-type is shown in (3)

$$\begin{cases} L_{12} = L_1 + L_2 + \frac{L_1 L_2}{L_3} \\ L_{13} = L_1 + L_3 + \frac{L_1 L_3}{L_2} \\ L_{23} = L_2 + L_3 + \frac{L_2 L_3}{L_1} \\ Z_{xy} = 2\pi f_s L_{xy} \end{cases}. \tag{3}$$

According to the expression of DAB transmission power under SPS control [21] and Δ-type equivalent circuit, the power expression for the port3 is given by (4). To simplify the derivation process, new variables need to be introduced and defined as

$$P_3 = \frac{V_1 V_3 \phi_3 (\pi - \phi_3)}{\pi Z_{13}} + \frac{V_2 V_3 (\phi_3 - \phi_2)(\pi - \phi_3 + \phi_2)}{\pi Z_{23}} \tag{4}$$

$$k_1 = \frac{V_1}{\pi Z_{13}}, k_2 = \frac{V_2}{\pi Z_{23}}. \tag{5}$$

B. Derivation of Inductor Current Under DSPS Control

Based on the previous analysis, the current expression can be determined by obtaining the slope of each segment, which can be realized by applying Thevenin transformation. The equivalent circuit is shown in Fig. 5. The equivalent expression is provided in (6), where v_N, L_N, Z_N represent the equivalent voltage, inductance, and impedance, respectively,

$$\begin{cases} v_N = \frac{L_1 v_2 + L_2 v_1}{L_1 + L_2} \\ L_N = \frac{L_1 L_2}{L_1 + L_2} + L_3, Z_N = 2\pi f_s L_N \end{cases}. \tag{6}$$

Herein, the derivation process of the inductor current at port 3 is given, and the same process can be applied to port1 and

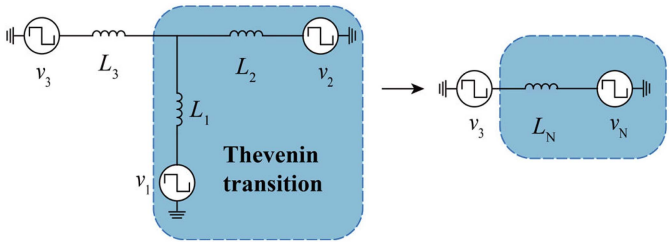

Fig. 5. Thevenin equivalence DAB of TAB.

TABLE I
SLOPE OF THE INDUCTOR CURRENT IN EACH SEGMENT AT PORT 3

Time period	slope
θ_0-θ_1	$k_{31}=(\frac{L_2V_1-L_1V_2}{L_1+L_2}+V_3)/Z_N$
θ_1-θ_2	$k_{32}=(\frac{L_2V_1+L_1V_2}{L_1+L_2}+V_3)/Z_N$
θ_2-θ_3	$k_{33}=(\frac{L_2V_1+L_1V_2}{L_1+L_2}-V_3)/Z_N$

port 2. Table I gives the slopes of the inductor currents at port 3 within different time periods, by which the relational equations corresponding to the currents at each commutation point can be derived as shown in

$$\begin{cases} i_{31}=i_{30}+k_{31}(\theta_1-\theta_0)=i_{30}+k_{31}\phi_2 \\ i_{32}=i_{31}+k_{32}(\theta_2-\theta_1)=i_{31}+k_{32}(\phi_3-\phi_2) \\ i_{33}=i_{32}+k_{33}(\theta_3-\theta_2)=i_{32}+k_{33}(\pi-\phi_3) \end{cases}. \quad (7)$$

According to the symmetry of the inductor current, the starting point and the endpoint of the inductor currents should satisfy the condition of being equal in magnitude but opposite in sign, i.e.,

$$i_{30}+i_{33}=0. \quad (8)$$

From (6) to (8) and Table I, the time-domain expression of the inductor current can be derived. To simplify subsequent calculations, the expressions for the current at each point are standardized as follows:

$$\begin{cases} i_{xy}=\frac{k_4-k_5\phi_2+k_6\phi_3}{k_3} \\ k_3=2\left(Z_1Z_2+Z_1Z_3+Z_2Z_3\right) \end{cases} \quad (9)$$

where the currents at different ports and different moments are characterized by distinct coefficients k_4, k_5, and k_6., as given in Table II. Notably, based on (9) and Table II, current expression at any commutation point in any port can be directly derived.

III. SAFE-FAST START-UP STRATEGY BASED ON DSPS

A. Limitations of the DAB Start-Up Strategy

Currently, few studies were dedicated to the start-up strategies for the TAB converters. A prevalent application is to adopt the DAB start-up strategy into the TAB converters. However, this application poses certain limitations, summarized in two aspects.

1) *Suboptimal Output Power Capability*: In the two-port operation of the TAB converters, the maximize output power capability is inaccessible. Additionally, enabling the disconnected port to join the steady-state control after start-up is an extra step, further limiting the start-up speed as well as introducing the risk of inrush current. Therefore, ensuring the TAB converter to work in three-port operation is an indispensable step during start-up.
2) *Complexity in Three-Port Operation*: In three-port operation of the TAB converter, the large amount of operation models under time-domain significantly complicates the derivation of the current expression, resulting that the advanced phase-shift modulations like EPS and TPS control are infeasible for the TAB converter.

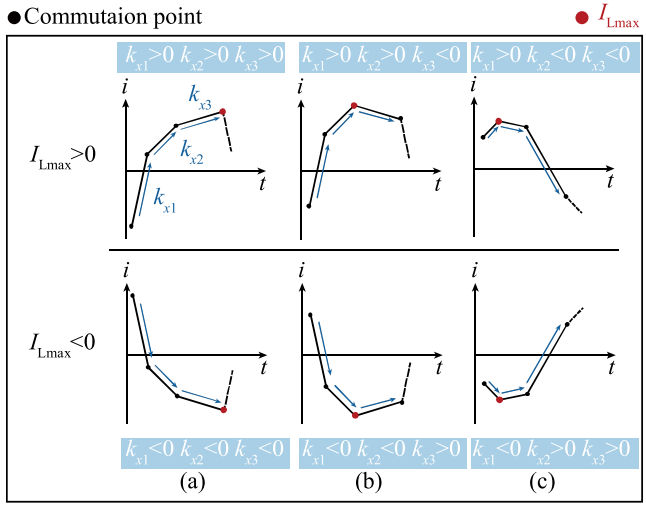

Fig. 6. Inductor current waveforms with different slope relations. (a) $k_{x1}k_{x3}>0$. (b) $k_{x2}k_{x3}<0$. (c) $k_{x1}k_{x2}<0$.

In conclusion, features of different control schemes employed in DAB and TAB converters are summarized in Table III. As can be seen, the DSPS control possess the highest output power (P_o) capability with the lowest computational burden in the DAB converters. Furthermore, when DSPS control is adopted in TAB converters, two adjustable phase-shift angles can be utilized to maximize the output power and regulate the current stress for one port. Therefore, the DSPS control is suitable for designing the closed-loop start-up strategy of TAB converters.

B. Maximum Current Point Observation Strategy Based on Slope Comparison Method (SCM)

First, to ensure safe operation, the inductor current at each port must be maintained within the safe current stress limits, which necessitates the determination of the expression for the maximum inductor current.

As shown in Fig. 3, the maximum inductor current $|I_{Lmax}|$ occurs among the commutation points of the piecewise linear current waveform, corresponding to θ_0, θ_1, θ_2, and θ_3. Therefore, in three ports there are nine current values need to be calculated and compared, significantly increasing the computational complexity.

To simplify the observation process, an SCM is proposed. As illustrated in Fig. 6, $|I_{Lmax}|$ is always located at the commutation

TABLE II
K_4, K_5, K_6 FOR DIFFERENT INDUCTOR CURRENTS AT DIFFERENT MOMENTS

i_{xy}	k_4	k_5	k_6
i_{11}	$\pi V_2Z_3-\pi V_1Z_3-\pi V_1Z_2+\pi V_3Z_2$	$-2V_1Z_2-2V_1Z_3-2V_3Z_2$	$-2V_3Z_2$
i_{12}	$\pi V_2Z_3-\pi V_1Z_3-\pi V_1Z_2+\pi V_3Z_2$	$-2V_2Z_3$	$2V_1Z_2+2V_1Z_3-2V_2Z_3$
i_{13}	$\pi V_1Z_3+\pi V_1Z_3-\pi V_2Z_3-\pi V_3Z_2$	$-2V_2Z_3$	$2V_3Z_2$
i_{21}	$\pi V_2Z_1-\pi V_1Z_3-\pi V_3Z_1+\pi V_2Z_3$	$-2V_1Z_3+2V_3Z_1$	$2V_3Z_1$
i_{22}	$\pi V_2Z_1-\pi V_1Z_3-\pi V_3Z_1+\pi V_2Z_3$	$-2V_2Z_1-2V_2Z_3$	$2V_1Z_3-2V_2Z_1-2V_2Z_3$
i_{23}	$\pi V_1Z_3-\pi V_2Z_1+\pi V_3Z_1-\pi V_2Z_3$	$-2V_2Z_1-2V_2Z_3$	$-2V_3Z_1$
i_{31}	$\pi V_3Z_1-\pi V_2Z_1-\pi V_1Z_2+\pi V_3Z_2$	$-2V_1Z_2-2V_3Z_1-2V_3Z_2$	$-2V_3Z_1-2V_3Z_2$
i_{32}	$\pi V_3Z_1-\pi V_2Z_1-\pi V_1Z_2+\pi V_3Z_2$	$2V_2Z_1$	$2V_1Z_2+2V_2Z_1$
i_{33}	$\pi V_1Z_2+\pi V_2Z_1-\pi V_3Z_1-\pi V_3Z_2$	$2V_2Z_1$	$2V_3Z_1+2V_3Z_2$

TABLE III
FEATURES OF DIFFERENT CONTROL SCHEMES EMPLOYED IN DAB AND TAB CONVERTERS

	Control scheme	Features		
		P_o	Inductor current	Burden
DAB	SPS	High	Uncontrollable	Low
	EPS	Low	Controllable	High
	TPS	Lower	Controllable	High
TAB	DSPS	High	Controllable	Low
	MPS	Low	Controllable	Higher

TABLE IV
MAXIMUM POINT OF INDUCTOR CURRENT FOR DIFFERENT SLOPE RELATIONS

Slope relationships	$\lvert I_{Lmax}\rvert$ observed by SCM
$k_{x1}k_{x3}>0$	$\lvert I_{Lmax}\rvert=\lvert i_{x0}\rvert$ (or $\lvert i_{x3}\rvert$)
$k_{x2}k_{x3}<0$	$\lvert I_{Lmax}\rvert=\lvert i_{x2}\rvert$
$k_{x1}k_{x2}<0$	$\lvert I_{Lmax}\rvert=\lvert i_{x1}\rvert$

point where the slope sign changes. At this moment, the polarity of the inductor voltage reverses, causing a change in the current slope. Therefore, within a single port, the commutation points where $|I_{L\max}|$ appears can be quickly observed by utilizing the slope relationships. This process can be realized without precise calculation of the current value by simply calculating the slope of each current segment. Based on above analysis, the maximum inductor current $|I_{L\max}|$ for different slope relationships are given in Table IV.

Therefore, by simply deriving slope polarities, $|I_{L\max}|$ within each port can be determined. Subsequently, by comparing each $|I_{L\max}|$ observing in each port, the maximum inductor current of the entire system $I_{\max}$ can be observed. The SCM significantly reduces the computational burden compared to directly calculating all commutation current values, thereby expediting the maximum current observation process. Another advantage of the SCM lies in its high parameter tolerance. In practical engineering applications, fluctuations in the port voltages and parameter deviation are possible, however, most of these fluctuations and deviation remain limited and do not alter the slope polarities, and thus the observation results of the SCM will not be affected, indicating its high applicability.

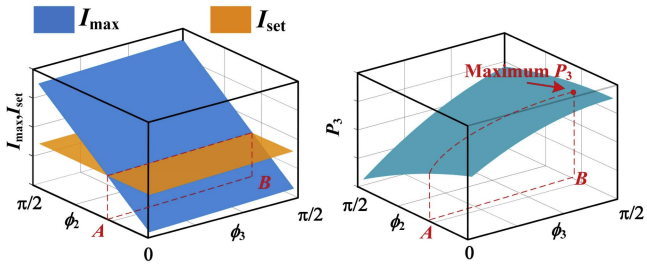

Fig. 7. Geometric interpretation of the optimization problem.

C. Derivation of Phase-Shift Angles by Partial Derivative Tracing (PDT) Method

After the observation of the maximum current, it is essential to maximize the output power while ensuring that the current stress under the safe limit for the safe and fast feature of the start-up process. This requirement can be formulated as a mathematical optimization problem subject to specified constraints, as shown in (10). Although the KKT method can be employed to determine the optimal phase-shift angles that satisfy these conditions, the excessive inequality constraints and the complexity of the expressions for the output power and inductor current pose significant challenges for the derivation of the optimal phase-shifts. Therefore, the following section would introduce the partial derivative tracing (PDT) method, i.e., utilizing partial derivative relationships to trace the optimal points under certain constraints, to solve the optimization problem

$$\max P_3(\phi_2,\phi_3)$$
$$\text{s.t.}\begin{cases} I_{\max}(\phi_2,\phi_3)\le I_{\text{set}} \\ 0\le\phi_2\le\frac{\pi}{2} \\ 0\le\phi_3\le\frac{\pi}{2} \\ \phi_2-\phi_3\le 0 \end{cases}. \tag{10}$$

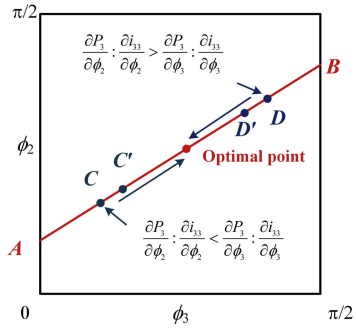

Fig. 8. Cross-sectional view of Fig. 7 when AB shows an upward trend.

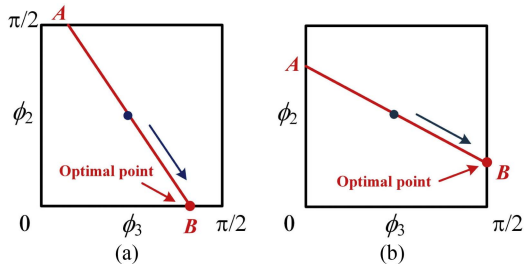

Fig. 9. Cross-sectional view of Fig. 7 when AB shows a drooping trend. (a) The boundary of Φ3 is reached first. (b) The boundary of Φ2 is reached first.

Fig. 7 provides a geometric interpretation of the optimization problem. Line AB represents the projection of the intersection line between the plane of the set inductor current value I_{set} and the maximum inductor current $I_{\max}$ onto the Φ-plane. All points on line AB can meet the safe current stress limit requirements. The essence of the optimization problem is to identify a point on line AB (Φ_2, Φ_3) that maximizes the output power P_3. According to (9), the slope of AB (k_{AB}) is determined by k_6/k_5. Based on the polarity of k_{AB}, the derivation process is categorized in two situations.

Case 1: $k_{AB} > 0$. As depicted in Fig. 8, which is a cross-sectional view of Fig. 7, AB exhibits an upward characteristic when the maximum current value is obtained at i_{33}.

Point *C* (Φ_2, Φ_3) on AB is depicted in Fig. 8 with its partial derivative relationship. *C*′ ($\Phi_2+\Delta\Phi_2$, $\Phi_3+\Delta\Phi_3$) is located in the upper right of *C*. The changes in the maximum inductor current and output power can be derived in (11) when moving from *C* to *C*′. Based on (4) and Table II, the calculation reveals that as Φ_2 increases, both P_3 and i_{33} decrease. Conversely, as Φ_3 increases, both P_3 and i_{33} increase. Moreover, since i_{33} remains unchanged when transitioning from point *C* to *C*′, (12) can be derived based on the partial derivative relationship at point *C*

$$\begin{cases} \Delta i_{33} = \frac{\partial i_{33}}{\partial \phi_2}\Delta\phi_2 + \frac{\partial i_{33}}{\partial \phi_3}\Delta\phi_3 \\ \Delta P_3 = \frac{\partial P_3}{\partial \phi_2}\Delta\phi_2 + \frac{\partial P_3}{\partial \phi_3}\Delta\phi_3 \end{cases} \tag{11}$$

$$\Delta i_{33} = 0 \rightarrow \Delta P_3 > 0. \tag{12}$$

The above deduction indicates that, compared to point *C*, point *C*′ allows port 3 to output greater power while maintaining i_{33} unchanged, which suggests that point *C*′ is a better optimal point. Therefore, the most optimal point should be searched along the direction towards upper right.

Similarly, for the gradient at point *D* (Φ_2, Φ_3) depicted in the Fig. 8, the corresponding point *D*′ located in the lower left ($\Phi_2-\Delta\Phi_2$, $\Phi_3-\Delta\Phi_3$) is a better optimal point, indicating that the most optimal point should be searched along the direction towards lower left.

Above analysis reveals that when a point satisfies the partial derivative relationship similar to point *C* or point *D*, a better optimal point can always be found. Consequently, the most optimal point must satisfy (13). By solving (13) and combining the equality constraint conditions in (10), the resulting optimal phase-shift angles can be determined, as shown in (15)

$$\frac{\partial P_3}{\partial \phi_2} : \frac{\partial i_{\max}}{\partial \phi_2} = \frac{\partial P_3}{\partial \phi_3} : \frac{\partial i_{\max}}{\partial \phi_3}. \tag{13}$$

Case 2: $k_{AB} < 0$. As depicted in Fig. 9, AB exhibits a drooping characteristic when the maximum current value is obtained at i_{13}. According to Table II, when Φ_2 increases, P_3 decreases while i_{13} increases, and when Φ_3 increases, P_3 increases while i_{13} decreases. Therefore, searching from point A to point B, where Φ_2 decreases and Φ_3 increases, ensures that the current remains constant while the power increases. The search process continues until the boundary of Φ_2 or Φ_3 is reached.

In Fig. 9, subplots (a) and (b), respectively, illustrate where the boundary of Φ_2 and Φ_3 is reached first. When one phase-shift angle is fixed at its boundary value, the value of the other phase-shift angle can be determined by the equality constraints.

Based on the aforementioned analysis, the characteristics exhibited by AB differ in two cases. However, the final results can be unified by (14), which is consistent with the results obtained by using the KKT method. During start-up the expressions for $\Phi_{2\text{set}}$ and $\Phi_{3\text{set}}$ are first computed by (15), and Φ_2, Φ_3 are determined based on (14). As can be seen from (14) and (15), the calculated phase shift angles during start-up vary with each coefficient k_{i}, which are determined solely by the voltages at the three ports. Since the voltages change continuously during start-up, the calculated phase shift angles also vary continuously, suppressing the oscillating currents

$$\begin{aligned} &a.\begin{cases} \phi_2 = \phi_{2set} \\ \phi_3 = \phi_{3set} \end{cases} \quad \left(0 < \phi_{2set} < \phi_{3set} < \frac{\pi}{2}\right) \\ &b.\begin{cases} \phi_2 = 0 \\ \phi_3 = \frac{k_3 I_{set} - k_4}{k_6} \end{cases} \quad (\phi_{2set} < 0) \\ &c.\begin{cases} \phi_2 = \frac{2k_4 - 2k_3 I_{set} + \pi k_6}{2k_5} \\ \phi_3 = \frac{\pi}{2} \end{cases} \left(\phi_{3set} > \frac{\pi}{2}\right). \end{aligned} \tag{14}$$

IV. Analysis of the System Characteristics

A. The Proposed Closed-Loop Start-Up Strategy

In this section, the DSPS closed-loop start-up strategy (DSPSS) derived from the above analysis is introduced. The overall control block diagram of the DSPSS is depicted in Fig. 10.

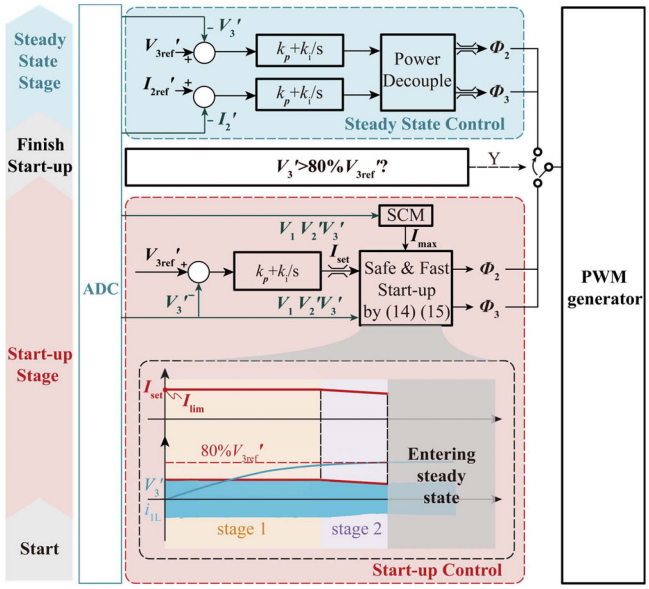

Fig. 10. Control block diagram of the DSPSS.

Fig. 10 illustrates the control procedure of the DSPSS. During the start-up stage, a single closed-loop control of the output voltage V_3' is implemented, ensuring a fast start-up while restricting $I_{\max}$ in a limit value I_{set}, which is controlled by the PI output. The upper saturation of the PI controller output is set as $I_{\lim}$, i.e., the maximum safe current limit of the entire system. By substituting I_{set}, the sampled V_1, V_2', V_3' and the observation results $I_{\max}$ by SCM into (14) and (15), the corresponding Φ_2, Φ_3 can be determined.

Based on the control procedure mentioned above, the start-up stage of the DSPSS can be divided into two substages, as shown in the timing diagram in Fig. 10, where $V_1 = 150$ V and

$$\begin{cases} \phi_{2set} = \\ \dfrac{2(k_1+k_2)k_4k_5-k_2k_6(2k_4-\pi k_6)-I_{set}[2(k_1+k_2)(2k_3-\pi k_6)k_5-2k_2k_3k_6]}{2[(k_1+k_2)k_5{}^2+k_2k_6(k_6-2k_5)]} \\ \phi_{3set} = \dfrac{2k_2k_4(k_5-k_6)+\pi k_5{}^2(k_1+k_2)-I_{set}[2k_2k_3(k_5-k_6)+2k_2k_5k_6]}{2[(k_1+k_2)k_5{}^2+k_2k_6(k_6-2k_5)]} \end{cases} \tag{15}$$

$V_2' = 100$ V, with $V_{3\text{ref}}' = 14$ V. The system′s operation in each substage is elaborated as follows:

Stage 1: At the initial stage of the start-up control, the PI output increases fast until I_{set} is equal to the upper limit $I_{\lim}$. By substituting the sampled V_1, V_2', V_3', $I_{\max}$ and $I_{\lim}$ into (14) and (15), the phase-shift angle (Φ_2, Φ_3) is obtained.

Stage 2: As V_3' gradually increases to a certain value, I_{set} progressively decreases, thereby no longer limited by the PI output saturation. The maximum current of the system gradually decreases, but the system consistently maintains maximum output power under I_{set}.

V_3' continues to increase until reaches 80% of the reference value. Subsequently, the system control stage switches from the start-up stage to steady-state stage smoothly, and the PI control is transitioned from single closed-loop to dual closed-loop. The steady state stage includes a current loop for port 2 and a voltage loop for port3 with a power decoupling unit.

TABLE V
OBSERVATION RESULTS OF THE PROPOSED SCM WHEN V_3' REACHES 10 V (1) $V_1 = 100$ V, $V_2' = 150$ V (2) $V_1 = 150$ V, $V_2' = 100$ V

Condition	(1)	(2)
k_{1y}	$k_{11}>0$ $k_{12}<0$ $k_{13}<0$	$k_{11}>0$ $k_{12}>0$ $k_{13}>0$
k_{2y}	$k_{21}>0$ $k_{22}<0$ $k_{23}<0$	$k_{21}>0$ $k_{22}>0$ $k_{23}>0$
k_{3y}	$k_{31}>0$ $k_{32}>0$ $k_{33}>0$	$k_{31}>0$ $k_{32}>0$ $k_{33}>0$
$\lvert I_{\text{Lmax}}\rvert$ Comparison	$\lvert i_{21}\rvert>\lvert i_{11}\rvert>\lvert i_{30}\rvert$	$\lvert i_{10}\rvert>\lvert i_{20}\rvert>\lvert i_{30}\rvert$
Observation results $I_{\max}$	$\lvert i_{21}\rvert$	$\lvert i_{10}\rvert$

TABLE VI
KEY PARAMETERS OF THE PROTOTYPE

Item	Parameter
DC Bus Voltage	80–160V
HV Battery Voltage	80–160V
Load Voltage	14V
Load Resistor	5Ω
Rated power	1kW
Switching frequency	100kHz
Transformer ratio	7：7：1
Inductor	L_1=4.2μH, L_2'=4.2μH, L_3'=1.6μH
C_3'	3*3.3mF in parallel
MCU	tms320f28377
$I_{\lim}$	18A

Notably, during the start-up process, the maximum current occurs at port1, which is consistent with the SCM observation result. The diagram shows that the value of I_{set} in each stage follows the variation discussed above, while the $I_{\max}$ is limited to I_{set}, ensuring a safe and fast start-up.

B. System Characteristic Analysis

To further demonstrate the effectiveness of the DSPSS, a simulation model is constructed to validate the start-up closed-loop control. The simulation parameters are consistent with the prototype parameters as given in Table VI.

1) Verification of the SCM Observation Strategy: Table V illustrates the observation result of the maximum inductor current by SCM when V_3' reaches 10 V during start-up, corresponding to conditions (1) $V_1 = 100$ V, $V_2' = 150$ V and (2) $V_1 = 150$ V, $V_2' = 100$ V. Taking (1) as an example, based on the voltages of each port, the slopes of each segment of the inductor current at port1 can be easily calculated, which are $k_{11} > 0\, k_{12} < 0\, k_{13} < 0$. According to SCM, $|i_{11}|$ can be inferred as the $|I_{\text{Lmax}}|$ for port1. Similarly, the $|I_{\text{Lmax}}|$ for ports 2 and 3 can be identified as $|i_{21}|$ and $|i_{30}|$, respectively. By comparing $|i_{11}|$, $|i_{21}|$, and $|i_{30}|$, $|i_{21}|$ is determined as the $I_{\max}$ under condition (1). The above analysis is validated by the simulation results shown in Fig. 11(a), (b), and (c). Moreover, the $I_{\max}$ under condition (2) can be observed to be $|i_{10}|$ in the same way, which is consistent with the simulation results depicted in Fig. 11(d), (e), and (f).

2) Safe Start-Up and High-Power Output Verification: The output voltage V_3' and the maximum inductor current $i_{1\text{L}}$ of the

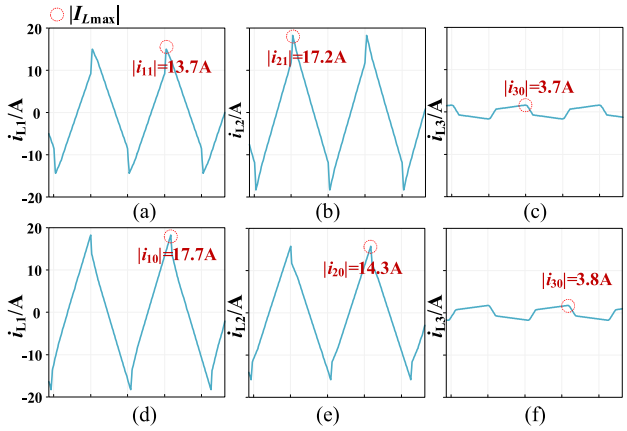

Fig. 11. Simulation results of the inductor current for two different operating conditions. (a), (b), and (c) $V_1 = 100$ V, $V_2' = 150$ V, and $V_3' = 10$ V. (d), (e), and (f) $V_1 = 150$ V, $V_2' = 100$ V, and $V_3' = 10$ V.

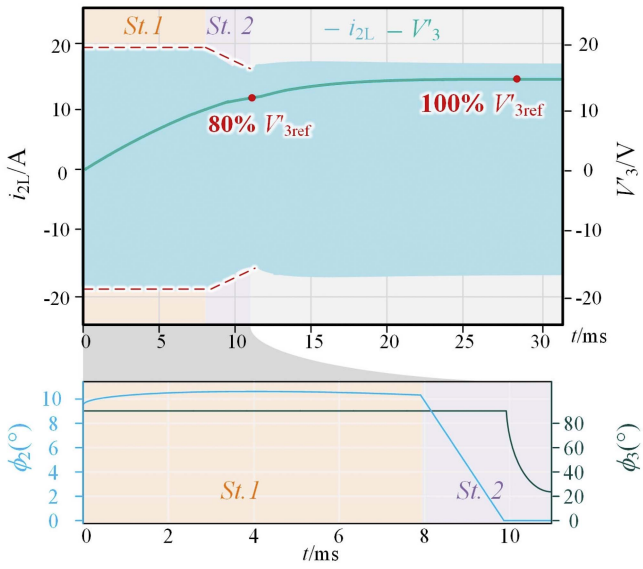

Fig. 12. Timing diagram of the output voltage V_3', inductor current i_{1L} and phase-shift angles changes during start-up under $V_1 = 150$ V, $V_2' = 100$ V.

system under conditions of $V_1 = 150$ V and $V_2' = 100$ V are depicted in Fig. 12. According to the proposed SCM, the $I_{\max}$ under this operating condition occurs at port1. The simulation results further verify that the DSPSS successfully limits the inductor current within I_{set}. Moreover, the variation trend of I_{set} is consistent with the theoretical predictions from the previous illustration that maintain the saturated value I_{lim} during the initial start-up stage and gradually decrease over time until reaches steady state stage. Additionally, Fig. 12 also demonstrates that the DSPSS facilitates a smooth transition from the start-up stage to steady-state stage. In summary, the DSPSS has proven to be highly effective in managing system current stress.

Furthermore, the trend of Φ_2 and Φ_3 during start-up is also illustrated in Fig. 12. As can be seen, throughout the start-up stage, both Φ_2 and Φ_3 change continuously without abrupt transitions, helping to suppress oscillating currents in the inductor current.

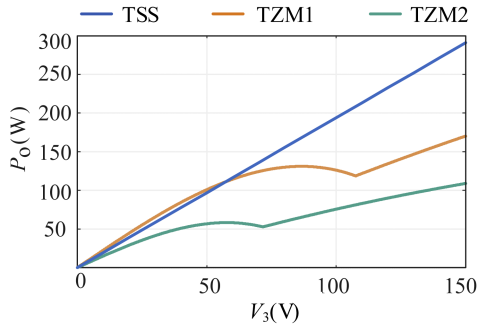

Fig. 13. Comparison of output power capability between DSPSS and TZM.

Fig. 13 presents an output power comparison between the DSPSS and the direct application of the DAB start-up strategy. In the simulation, the output power of DSPSS and two TZM strategies are compared under conditions of $V_1 = 150$ V and $V_2' = 100$ V, wherein TZM1 utilizes only port1 to transfer power to port 3, while TZM2 uses port 2.

As shown in Fig. 13, DSPSS has significant superiority in output power capability over both TZM strategies, particularly as the voltage exceeds 50 V. The output power for DSPSS is slightly lower than TZM1 before reaching 50 V, because port 2 introduces additional impedance to the converter, as shown in (3). Therefore, during the initial start-up phase, when the output voltage is still relatively low, the output capacity of the DSPSS is not fully realized. Instead, the larger equivalent inductance restricts the start-up speed. However, as the voltage gradually increases, the benefits of the DSPSS start-up in output power become increasingly significant, and the advantages over single port input become more pronounced at higher voltage levels. From a global perspective, DSPSS is undoubtedly superior to TZM in output power capability, meaning an enhanced start-up speed of the DSPSS.

3) High Applicability Performance: In practical engineering applications, the parameters′ tolerance may occur due to aging inductor or other reasons. The tolerances of the inductance can affect the applicability of DSPSS by introducing the error between the observed and actual values of the inductor current. When the inductance is overestimated, the inductor current will be less than the observed value. Conversely, when the inductance is underestimated, the inductor current will exceed the observed current, potentially causing the inductor current to surpass the safety limit I_{lim}. Fig. 14 illustrates the trend of $I_{\max}$ under different parameters′ tolerance during the start-up under $V_1 = 150$ V, $V_2' = 100$ V. It can be observed from the figure that when the inductance experiences a 20% tolerance, the actual $I_{\max}$ fluctuates from 16.2 to 20.1 A, which is consistent with the previous analysis that an overestimated inductance results in a lower $I_{\max}$. Given that the theoretical value of the $I_{\max}$ is 18 A, the maximum $I_{\max}$ overshoot caused by the tolerance is about 11.67%. To mitigate this issue without complicating the control strategy, a safety margin of 15% has already been applied to I_{lim}. Therefore, the safety characteristic of the DSPSS can hardly be affected by parameters′ tolerances.

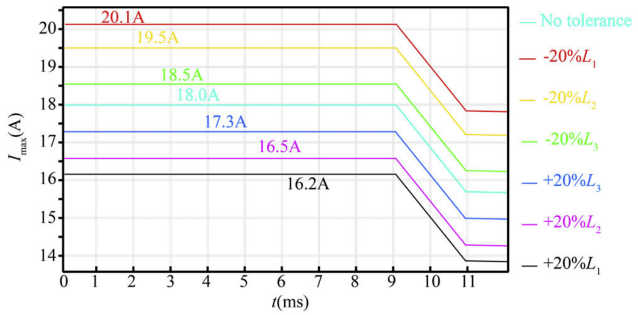

Fig. 14. Trend of $I_{\max}$ under different types tolerance under $V_1 = 150$ V, $V_2' = 100$ V.

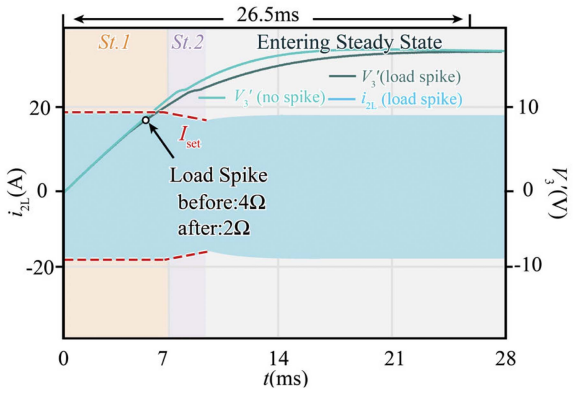

Fig. 15. DSPSS performance with load spike under $V_1 = 150$ V, $V_2' = 100$ V.

Moreover, since the calculated phase-shift angles are simply based on the three ports voltage and inductance regardless of the load, the DSPSS has high load adaptability, and load spike can hardly affect the reliability of the DSPSS. Fig. 15 depicts the DSPSS performance with load spike under $V_1 = 150$ V, $V_2' = 100$ V, where the load abruptly doubles. The output voltage exhibits a reduced rate after load spike yet still maintains a rapid start-up speed and a smooth transition from the start-up stage to steady-state. Besides, the maximum current remains effectively constrained within safe limits, demonstrating the robust applicability of DSPSS in managing load spike.

In engineering applications, dc microgrids involve various load types, including constant-power loads such as inverters or on-board charger. Due to the inability to establish power at excessively low voltage levels, a no-load start-up (NLS) is conducted during the initial stage to allow the ports to establish a certain voltage before connecting the load. The subsequent discussions regarding the constant-power loads start-up strategy are based on a two-stage process: the first stage involves NLS, which lasts for a specific duration (5 ms) to establish certain voltage, then transitions into the second stage, which is the constant-power load start-up.

Fig. 16 presents the voltage (V_3'), inductor current (i_{1L}), and output current (I_3') waveforms during the start-up of a 60 W constant-power load under $V_1 = 150$ V, $V_2' = 100$ V. The period before 5 ms represents the NLS, after which the 60 W constant

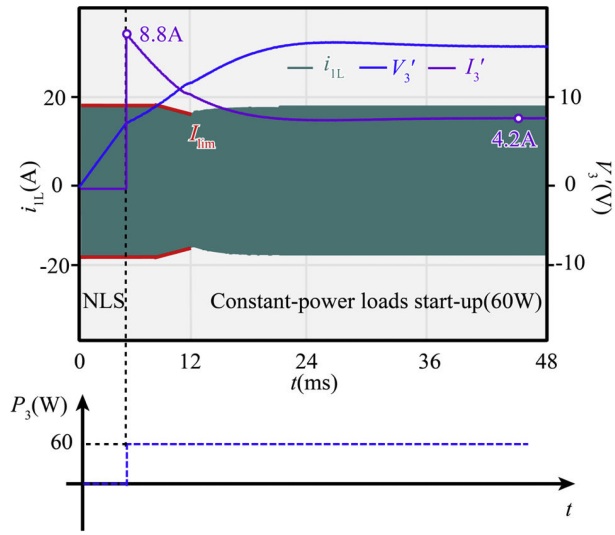

Fig. 16. Voltage and current waveforms during the start-up of a 60 W constant-power load under $V_1 = 150$ V, $V_2' = 100$ V.

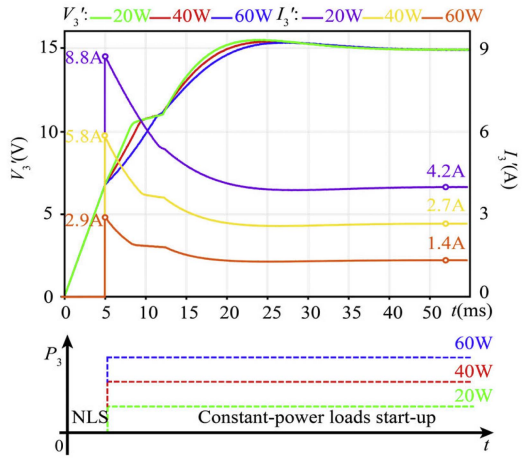

Fig. 17. Voltage waveforms during the startup of constant power loads of 20, 40, and 60 W under $V_1 = 150$ V, $V_2' = 100$ V.

power load is connected. From the figure, it can be seen that during the constant-power load start-up, DSPSS is still able to keep the current within safe limits, thereby validating its safety performance.

During the start-up, P_O consists of 2 parts, which are the charging power (P_C) and load power (P_L), where P_C determines the start-up speed. Since P_O maintains the largest during the entire start-up process under DSPSS control, Pc is consistently maximized under certain voltage conditions regardless of the load types, thereby guaranteeing the adaptability of DSPSS under constant-power loads.

Fig. 17 displays the output voltage and current waveforms during the start-up of constant-power loads of 20, 40, and 60 W under $V_1 = 150$ V, $V_2' = 100$ V, respectively. It can be observed from the figure that as the power increases, the start-up speed gradually decreases, which is because a larger load corresponds to a greater P_L. Under certain voltage conditions, the $P_{\max}$

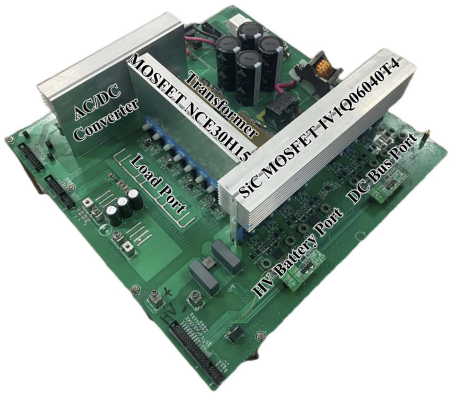

Fig. 18. Prototype of 1 kW TAB.

controlled by PDT is fixed. Therefore, as P_L increases, P_c decreases, resulting in a slower charging rate of the capacitor, which in turn limits the speed of voltage rise. Nevertheless, DSPSS can still ensure that the load receives the maximum output power throughout the start-up process, facilitating a rapid start-up. Above analysis shows that the DSPSS has a high load applicability.

Based on the above analysis, the advantages of DSPSS include the following:

1) By employing DSPSS, the maximum output power under safe current stress limits can be achieved, thereby enhancing the start-up speed and safety.
2) During the start-up stage, no sudden change in the phase-shift angle occurs, suppressing the generation of dc bias.
3) The start-up stage can smoothly transition into the steady-state control stage, ensuring a more stable start-up process.
4) High applicability under parameters′ tolerance and load spike.

V. Experiment

In order to validate the effectiveness of the DSPSS, a 1 kW/100 kHz TAB prototype based on SiC MOSFET is constructed, shown in Fig. 18. The key parameters are given in Table VI.

A. SCM Observation Strategy Validation

Fig. 19 shows the midpoint voltages of the bridges at each port and the corresponding maximum current waveforms when V_3' reaches 10 V during the start-up stage. Fig. 19(a) depicts the condition with $V_1 = 150$ V and $V_2' = 100$ V, while Fig. 19(b) depicts $V_1 = 100$ V and $V_2' = 150$ V. From the previous analysis, $I_{\max}$ occurs at port1 in case (a) and at port 2 in case (b). Fig. 19 demonstrates that the experimental waveforms align well with the simulation results displayed in Fig. 11. Additionally, the maximum current point, as indicated in the figure, is consistent with the observation results obtained by using the SCM, which validates the SCM strategy for observing the maximum current value.

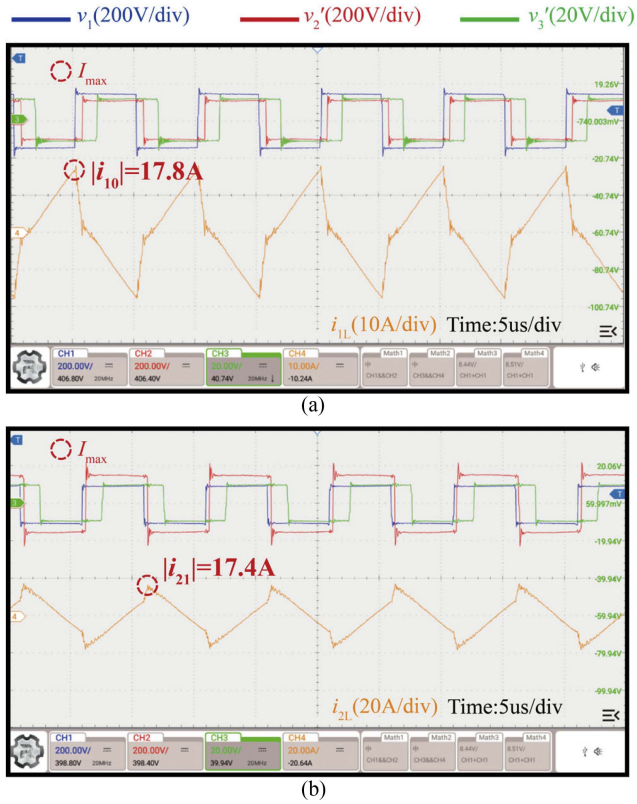

Fig. 19. Midpoint voltages of each port and the corresponding maximum current waveforms when V_3' reaches 10 V. (a) $V_1' = 150$ V and $V_2 = 100$ V. (b) $V_1 = 100$ V and $V_2' = 150$ V.

B. Safe and Fast Start-Up Features Validation

The detailed procedure of the start-up process by DSPSS is shown in Fig. 20 As depicted in Fig. 20, during the stage 1 of the start-up stage, I_{set} is equal to the PI output upper limit I_{lim} and remains unchanged during the whole stage 1. Concurrently, the inductor current is effectively limited at I_{set}, as illustrated in the zoom figure which shows the detailed waveforms when V_3' reaches 5 V. As V_3' gradually rises, the PI output decreases accordingly and is no longer constrained by the upper limit I_{lim}. Subsequently, the start-up stage transitions into stage 2, where the maximum inductor current decreases progressively while the voltage increasing continuously. The detailed waveform of stage 2 is displayed in the zoom figure when V_3' reaches 10 V. Stage 2 concludes when V_3' reaches 80% of the reference value. Since the voltage at this point is close enough to the reference value, the system transitions smoothly from the start-up stage to the steady-state stage. Moreover, the start-up speed is also depicted in Fig. 20, showing that it takes only 29.8 ms and 31.2 ms to finish the start-up in case (a) and case (b), respectively. Therefore, both the safe and fast features of the DSPSS are validated through experimentation.

To further illustrate the advantages of the DSPSS, comparison experimental results are shown in Fig. 21 which shows the start-up process of: directly apply the DAB start-up strategy to the TAB converter and directly apply the PI closed-loop control to the start-up process. As can be seen in Fig. 21(a)

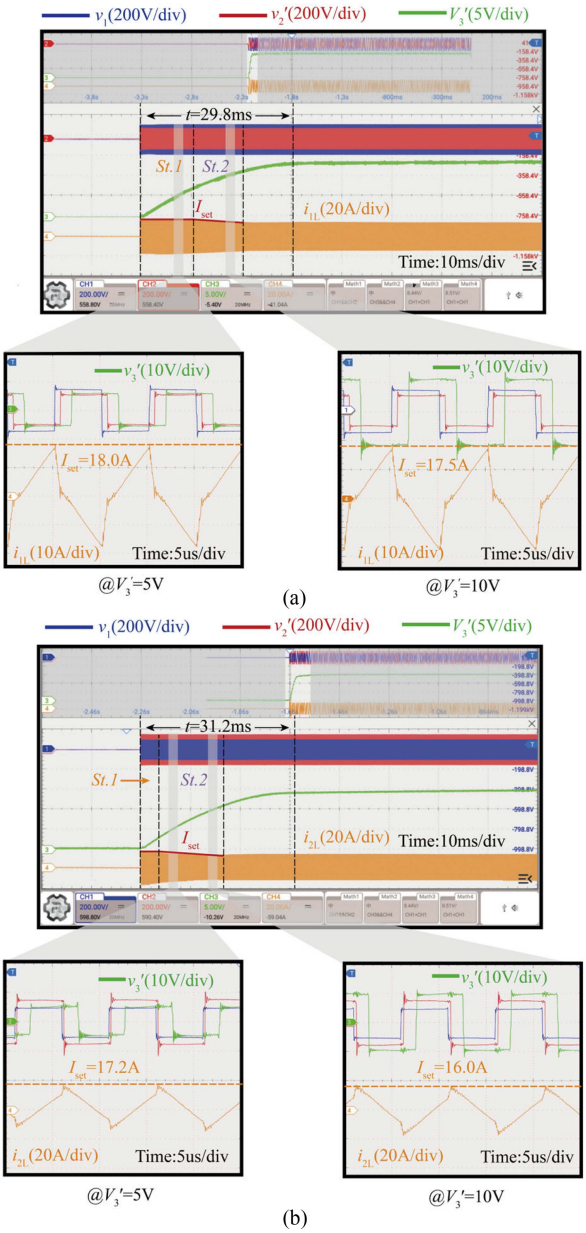

Fig. 20. Key waveforms at $V_3' = 5$ V and $V_3' = 10$ V during the start-up by DSPSS under (a) $V_1 = 150$ V, $V_2' = 100$ V and (b) $V_1 = 100$ V, $V_2' = 150$ V.

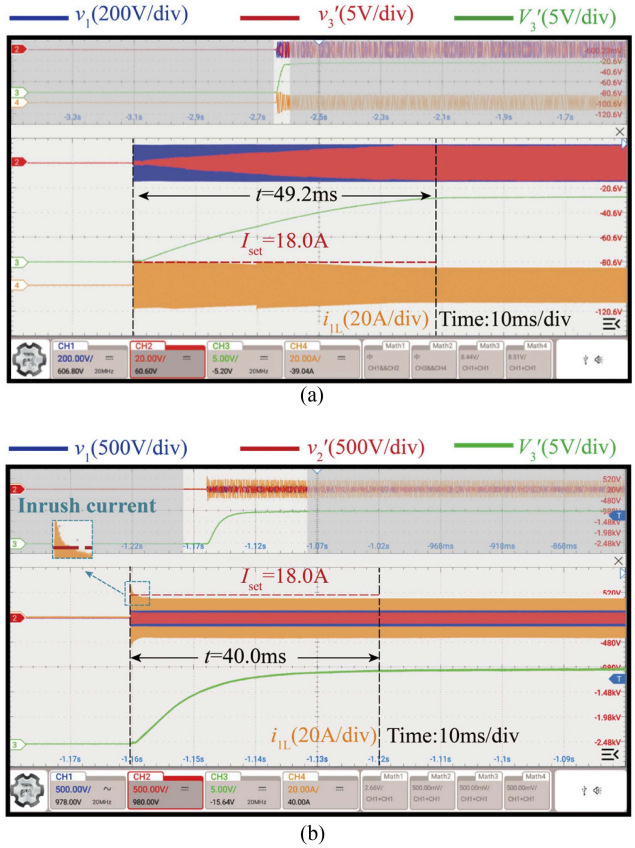

Fig. 21. Key waveforms during the start-up under $V_1 = 150$ V, $V_2' = 100$ V. (a) Directly apply the DAB start-up strategy with transferring power solely by port 1. (b) Directly apply PI control to the start-up control.

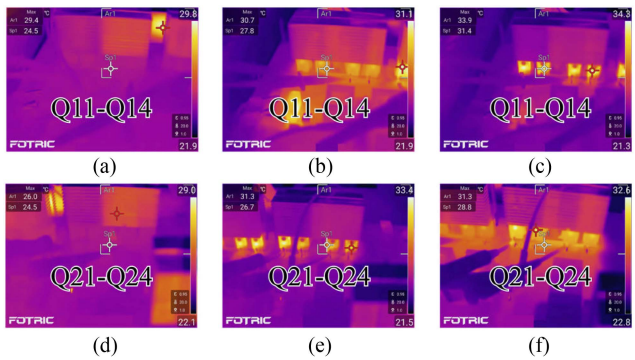

Fig. 22. Temperature variations of switches in ports 1 and 2, Port 1: (a) Before start-up. (b) $V_1 = 150$ V, $V_2' = 100$ V. (c) $V_1 = 100$ V and $V_2' = 150$ V. Port 2: (d) Before start-up (e) $V_1 = 150$ V and $V_2' = 100$ V. (f) $V_1 = 100$ V, $V_2' = 150$ V.

that within the same inductor current limits, it takes 49.2 ms to raise the output voltage to the reference value when solely transfer power by port1, which is 34% slower than the DSPSS. Considering that letting port2 join the steady-state control is an extra step, the full start-up time should be longer. Moreover, Fig. 21(b) depicts that completing the start-up process directly via the PI controller results in inrush current, which exceeds the system's safe current limit, thereby posing a risk of damaging the switches and threatening the safe and reliable operation of the system. Therefore, the critical role which the DSPSS plays in ensuring the safe and fast start-up is stressed by the comparison experiment.

To better confirm the safe operation of the DSPSS, the temperature variations of switches in ports 1 and 2 before and after start-up are depicted in Fig. 22, demonstrating that the temperature rise in both operating conditions is approximately 4 °C. This phenomenon substantiates that the proposed DSPSS does not induce rapid temperature escalation that could potentially damage switching devices during the start-up.

The applicability of the DSPSS has been experimentally validated in Fig. 23. In Fig. 23 the output voltage waveforms during the start-up process with load resistances of 2, 5, and 10 Ω are depicted, with the start-up time being 37.5, 29.8, and 24.4 ms, respectively. The results reveal that the DSPSS maintains robustness across different load conditions without

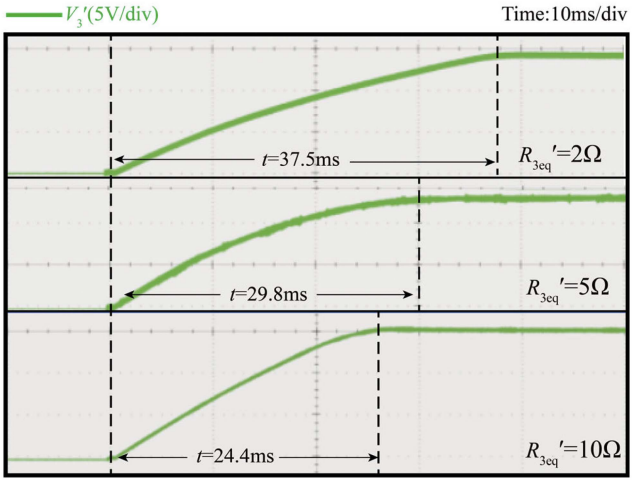

Fig. 23. Output voltage waveforms during the start-up process with different loads at $V_1 = 150$ V, $V_2' = 100$ V.

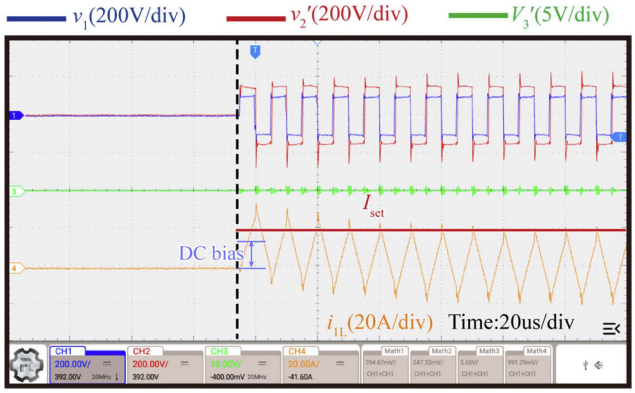

Fig. 24. DC bias phenomenon under $V_1 = 100$ V, $V_2' = 150$ V.

the dependence of strict parameter tuning, indicating its broad applicability.

C. Consideration of DC Bias Suppression

The proposed DSPSS can effectively constraint the inductor current in the safe limits and maximize the output power. However, in the first few cycles, dc bias may occur, as shown in Fig. 24, which lead to inrush current that exceed the safe limits. Such phenomenon is caused by the zero initial current at the beginning of the start-up process [22], rather than a flaw of the proposed DSPSS.

To address such an issue, Liu et al. [19] introduced a method to suppress dc bias by introducing inner phase shift angles in the DAB start-up. Due to the similar circuit, this method can also be applied to TAB converters, as illustrated below: The inner phase shift angles are introduced during the first few cycles of start-up to mitigate the dc bias, as illustrated in Fig. 25. During the first few cycles of the start-up process, MPS control is employed, which gradually increases the duty cycles of V_1 and V_2' from 40% to 100%, then transitions into DSPSS control. Notably, the time duration of the dc bias suppression by MPS lasts for 6 switching cycles, i.e., 60 us, accounting for merely 0.2% of the entire start-up process. To conclude, MPS control can effectively

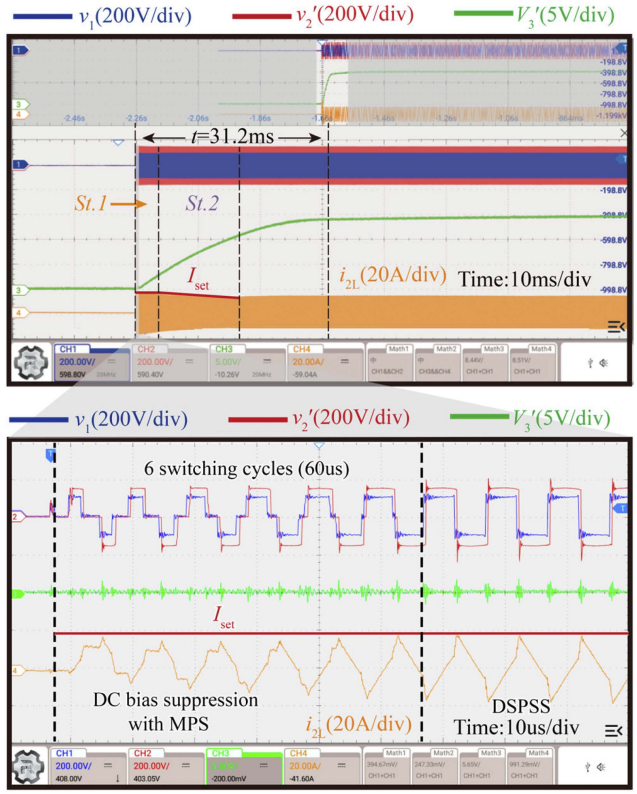

Fig. 25. DC bias suppression strategy with MPS during the first few cycles of the start-up under $V_1 = 100$ V, $V_2' = 150$ V.

TABLE VII
COMPARISON AMONG DIFFERENT START-UP STRATEGIES APPLIED IN THE TAB CONVERTERS

Strategy	Phase-shift scheme	Features		
		Speed	Safety	Applicability
PI	DSPS	High	Low	High
Ref [12]	EPS	Lower	High	Low
Ref [18]	TPS+EPS	Low	High	High
DSPSS	DSPS	High	High	High

ensure the inductor current within safe limits by suppressing the dc bias during the first few cycles without adding much time to the overall start-up. Therefore, the reliability of the DSPSS will not be affected.

Based on above analysis, the features of different start-up strategies applied to the TAB converter are summarized in Table VII. According to Section III, a comprehensive-designed start-up strategy must meet the criteria of safe and fast feature, and also demonstrate good applicability. In this section, the effectiveness of the DSPSS has been validated through experiments. During the start-up process, the maximum inductor current $I_{\max}$ is consistently constrained within I_{set}, while I_{set} initially remains constant at $I_{\lim}$ and subsequently decreases gradually, ensuring the safety during start-up. Moreover, the comparative experimental result between the DSPSS and the direct application of the DAB start-up strategy confirms that the DSPSS achieves a faster start-up speed. Furthermore, the experiments of the start-up process with different load resistances

depict the strong applicability of the DSPSS. Therefore, based on SCM and PDT, the safe and fast start-up strategy with a broad applicability can be achieved.

VI. Conclusion

In this article, a simplified online start-up strategy for the TAB converter with safe and fast feature is proposed. To completely leverage the output capability of the TAB converter, the DSPS control has been implemented. In order to accurately locate the port where the maximum inductor current occurs, this article proposes the SCM, which effectively reduces the computational burden of the control process. Secondly, in order to maximize the start-up speed while limiting the current stress, the phase-shift angles is derived to maximize the output power while limiting the inductor current based on the proposed PDT method instead of KKT conditions. On the basis of the above two works, a closed-loop TAB start-up control strategy is constructed and verified by simulation. Finally, the comparison between the proposed DSPSS in this article and the direct application of the DAB start-up strategy is illustrated by building a 1 kW prototype, which verifies the safety and rapidity of the proposed strategy as the experimental results shows the DSPSS is 34% faster compared to the DAB start-up strategy. Moreover, the applicability of the DSPSS is verified by a series of experiment with different loads. Future works will focus on the application of more dimensional phase-shifting strategies in TAB start-up.

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