A Novel Substrate-Embedded SiC Power Module With Integrated Liquid Cooling

Xinnan Sun, Min Chen, *Member, IEEE*, Jie Li, Fengze Hou, *Senior Member, IEEE*, Yifei Du, Yucheng Wu, and Bodong Li

***Abstract*—To fully leverage the advantages of silicon carbide (SiC) power devices, this study presents a substrate-embedded SiC power module with integrated liquid cooling. Four 1.2-kV SiC MOSFETs are embedded in an organic substrate and cooled via a direct-bonded microchannel heatsink, within a packaging size of 20 mm × 20 mm × 2.4 mm. This design achieves short electrical interconnection with significantly reduced parasitic parameters and eliminates the need for thermal interface material, enhancing cooling efficiency. Through careful optimization, the parasitic inductances of the power loop and driving loop are minimized to below 155 and 35 pH, respectively. The proposed module outperforms the commercial TO-247-4 packaging, exhibiting faster switching speeds with turn-ON and turn-OFF losses decreased by 12.7% and 10%, respectively. Furthermore, at a junction temperature rise of 150 °C, the die heat flux of the embedded module exceeds that of the TO-247-4 with external air cooling by 29.1% and with liquid cooling by 7.6%. In addition, due to the significant size advantage of the proposed module, the improvement in packaging heat flux is more pronounced.**

***Index Terms*—High integration, microchannel (MC) cooling, silicon carbide (SiC) MOSFET, substrate-embedded packaging, vacuum lamination.**

I. Introduction

SILICON carbide (SiC) power devices have gained significant attention owing to their exceptional material properties, including a wide bandgap, high thermal conductivity, and high breakdown electric field. These advantages allow SiC devices to operate at higher temperatures, voltages, and frequencies with enhanced efficiency compared to traditional silicon (Si) devices [1], [2], [3], [4], [5], [6]. Consequently, SiC power devices are increasingly adopted in applications such as electric vehicles (EVs), renewable energy systems, and high-power industrial equipment, where performance, power density, and reliability are particularly crucial.

However, the successful implementation of SiC power devices hinges on addressing packaging challenges, as conventional wire-bonded packaging is struggling to realize their full potential [7], [8], [9]. This is primarily due to conventional wire-bonded packaging introduces parasitic inductance challenges for SiC power devices. In standard configurations, the typical value of parasitic inductance exceeds 10 nH, which can significantly degrade the device performance by causing issues such as voltage overshoot, switching losses, and electromagnetic interference [10]. Recent innovations such as multilayer stacked design have demonstrated effective inductance reduction below 10 nH through optimizing power loop geometry, while the inductance is still at the nanohenries level [11]. These parasitic effects are especially detrimental for SiC devices, as their high switching speeds render them more sensitive to such unwanted parameters. Therefore, for high-speed SiC devices, it is crucial to modify or eliminate the bonding wires in packaging to minimize the electrical loop and mitigate parasitic effects.

In response to these challenges, various wire-bondless packaging approaches, including planar, press-pack, and 3-D packaging, have been developed [12], [13], [14]. Among the available technologies, laminate-based substrate-embedded packaging has emerged as a promising solution for SiC power modules [15]. This innovative approach integrates power devices directly into a planar multilayer structure composed of interconnection and organic polymer layers, utilizing laser drilling and microvia metallization in place of the traditional bonding wire process, achieving high interconnect density, lower parasitic inductance, and a more compact packaging size. The embedded packaging structure based on leadframe is one of the mainstream representatives. Fraunhofer IZM initially proposed a leadframe-based printed circuit board (PCB) embedded IGBT half-bridge module in 2013 [16]. A base substrate, composed of thick copper (Cu) layers and a thermally conductive prepreg layer, serves the role of direct bonded copper (DBC) in conventional modules. The dies are embedded into a prepreg layer via vacuum lamination, and electrical interconnection with outer layers is

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realized through vias and redistribution layers (RDLs), thereby achieving planar interconnection and reducing the thickness of the module. Building on this foundation, power modules based on premachined leadframes featuring cavities to aid in die positioning and improve the electroplating quality are proposed in [17], [18], and [19]. Besides, researchers from SATIE employed pressed conductive foam to establish connections of the top and bottom sides of a power die, ensuring optimal thermal performance and minimizing electrical losses [20], [21]. For easier fabrication, Bensebaa et al. [21] developed a novel process for embedding power semiconductors within PCBs. This process involves sandwiching the dies between two standard PCBs, utilizing Ag sintering and lamination of prepregs, thus enabling fabrication outside the standard PCB manufacturing line [22]. Furthermore, Hou et al. [23] introduced a symmetrical substrate embedded power module with double-sided RDLs to mitigate stress and strain of the packaging.

As previously discussed, advancements have been made in the field of embedded packaging technology; however, the majority of research has concentrated on exploring and accessing the feasibility of packaging processes, and predominantly for Si-based IGBTs. For SiC power devices with higher heat flux density and heightened sensitivity to parasitic parameters, a more comprehensive and meticulous theoretical analysis and optimization design of embedded packaging structures is imperative to harness their full potential. Moreover, despite the presence of double-sided thick copper, the high integration level of embedded packaging accompanied by the low thermal conductivity of organic polymers and solder masks make it faces substantial heat dissipation challenges, particularly in high-power applications. Consequently, effective thermal management remains a critical challenge in the evolution of embedded packaging technology, an issue that has not yet been adequately addressed.

In addition to the pursuit of better packaging materials, the integration of advanced thermal management technology represents a promising solution and has been studied in some other types of packaging. Ultrathin microchannel (MC) heatsinks based on LTCC technology have been applied in the integration of press-pack power modules, facilitated using miniature and flexible press pins called "fuzz buttons" [12]. Besides, integrated cooling technology for DBC substrates has also been proposed [24]. Stevanovic et al. [25] etched MCs on the backside of a DBC substrate to reduce the junction-coolant thermal resistivity, and Lin et al. [26] proposed a prototype of a multilayer manifold MC power module structure based on laser etching of aluminum nitride based DBC substrates. Moreover, Zhang proposed an embedded liquid cooling strategy employing a SiC substrate with micro pin fins in place of the ceramic of DBC for the thermal management of SiC power modules in EVs [27]. In addition, Iradukunda et al. [28] proposed a packaging strategy with dielectric fluid coolant for direct cooling, where the MC terminals fulfill dual roles in electrical connection and cooling to further overcome the thermal challenges faced by traditional packaging. It is evident that MC heat dissipation technology has received increasing attention from scholars and is progressively being incorporated into power module packaging to further improve their power level and integration. Nevertheless, due to the particularity of the processes involved and the nascent state of development, there remains a scarcity of reports on integrated thermal management technology in the field of embedded packaging.

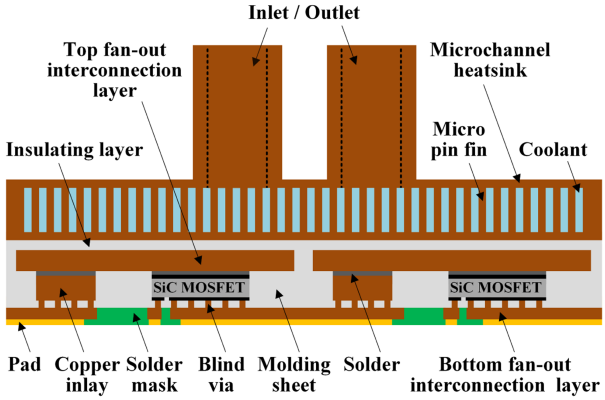

Fig. 1. Schematic diagram of the proposed integrated packaging.

This article introduces a substrate-embedded SiC power module with integrated liquid cooling, which is organized as follows. Section II details the structural configuration and fabrication flow of the module, demonstrating the integration methodology and thermal management strategies. In Section III, the comprehensive design and optimization process for the packaging is presented, including the electrical-thermal analysis of the embedded packaging, as well as the structural and dimensional design of the integrated MC cooler. Section IV presents the dynamic characteristics and thermal performance experimental results of the proposed power module, thereby validating the efficacy of the research. Finally, Section V concludes this article.

II. Liquid Cooling Embedded SiC Power Module

A. Packaging Structure

The cross-sectional structure of the proposed substrate-embedded SiC power module with integrated liquid cooling is depicted in Fig. 1, and the exploded view of the module is illustrated in Fig. 2. In the proposed power module, four 1200 V/36 A SiC MOSFET dies of CPM2-1200-0080B ($R_{\mathrm{ds(on)}}$ = 80 mΩ) from CREE are embedded to configure an H-bridge circuit, as shown in Fig. 3. The entire packaging exhibits a multilayer planar structure with thickness of each component listed in Table I.

In the lower part of the module, the SiC MOSFET dies are embedded in the molding sheet, with the electrical connections primarily established through the top and bottom fan-out interconnection layers. Copper inlays, colocated with the SiC MOSFETs, facilitate the connection between the two interconnection layers. In addition, solders and blind vias are positioned on the upper and lower sides of the MOSFETs and copper inlays, respectively, to achieve their connection with the interconnection layers. The solder mask beneath the bottom interconnection

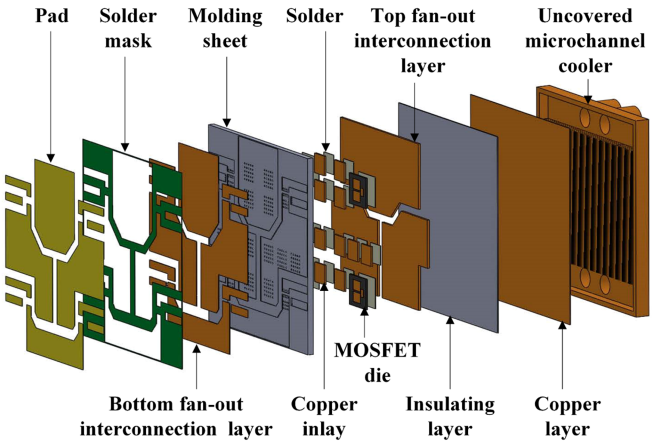

Fig. 2. Explosion diagram of the proposed H-bridge power module.

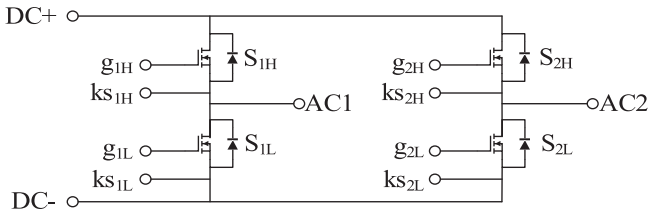

Fig. 3. Schematic of the circuit integrated in the proposed power module.

TABLE I
THICKNESS OF EACH COMPONENT OF THE PACKAGING

Component	Thickness (mm)
SiC MOSFET die	0.18
Solder	0.05
Top fan-out interconnection layer	0.25
Bottom fan-out interconnection layer	0.07
Blind via	0.075
Pad/Solder mask	0.035
Insulating layer	0.11
MC heatsink (without inlet/outlet)	1.6
Inlet/Outlet of the heatsink	3

layer serves for insulation and protection, and module pads are positioned in areas that are not covered by the solder mask.

In the upper part of the module, an MC heatsink is integrated with the die-embedded section to improve the thermal performance of the package. The MC cooler is configured with an array of uniformly spaced pin fins, enabling coolant flow and thereby enhancing heat transfer efficiency. A thin insulating layer is interposed between the MC heatsink and the top fan-out interconnection layer, serving dual roles in electrical insulation and thermal conduction.

B. Fabrication of the Integrated Power Module

The fabrication process of the substrate-embedded SiC power module with integrated liquid cooling is depicted in Fig. 4(a) and described as follows.

Step 1: The gate and source pads of SiC MOSFET dies is generally composed of aluminum (Al), which is a highly reactive metal with inferior mechanical properties. In order to make the dies compatible with processes such as laser drilling and electroplating, it is necessary to remetallize the gate and source pads [23], [29]. Thus, prior to the packaging process, about 4 μm of Cu is added onto the Al pads of the dies using physical vapor deposition technology. The outcome of die remetallization is displayed in Fig. 4(b).

Step 2: Prepare the base copper by etching, designating it as the top fan-out interconnection layer in Figs. 1 and 2. Then attach SiC MOSFET dies and copper inlays onto it by soldering.

Step 3: Laminate a sheet of molding compound (SMC) and a copper foil onto the base copper, with the copper foil serving as the bottom fan-out interconnection layer in Figs. 1 and 2.

Step 4: Utilize laser drilling to create microvias above the die pads and copper inlays, and then employ electroplating to fill the vias with copper. Subsequently, achieve the desired copper layer pattern through etching process.

Step 5: Reverse the orientation of the packaging, and laminate it with a thin SMC and a copper foil again, prepared for the integration of MC cooler.

Step 6: Apply a solder mask and perform electroless nickel/immersion gold deposition on the pads of the module to enhance their stability and solderability.

Step 7: Manufacture the uncovered MC cooler presented in Fig. 4(c) by computerized numerical control machining center and wire-electrode cutting technique. The MC cooler features a high aspect ratio in copper to ensure efficient heat transfer in the ultra-compact packaging, which is challenging for conventional manufacturing methods. Milling tools are fragile, drilling is imprecise, and etching is uneven. To overcome the limitations, the noncontact method of wire-electrode cutting is employed. Strict control of process parameters and careful selection of appropriate electrode wires ensure precise and straight MCs with high aspect ratio.

Step 8: Assemble the uncovered MC cooler with the copper layer on the top of the structure completed in step 6 to achieve the final module shown in Fig. 4(d), where the uncovered cooler and the copper layer together form the MC heatsink in Fig. 1. The size of the integrated power module is 20 mm $\times$ 20 mm $\times$ 2.4 mm (excluding the height of the inlet and outlet of 3 mm).

The abovementioned elaborates on the unique process steps of the proposed substrate-embedded integrated packaging, which form the foundation for achieving its high performance. In addition to considerations at the process level, cost factors are equally crucial for the application of a technology. The fabrication entails special processes and advanced materials, which will result in higher initial manufacturing costs. Inevitably, there will be a certain premium in small-scale production. However, benefiting from the high integration and superior performance of this technology, the proposed packaging can effectively cut down on assembly costs, decrease the quantity of dies under identical power output requirements, and reduce the lifespan cost of converters. Therefore, it has significant advantages in reducing long-term system-level costs.

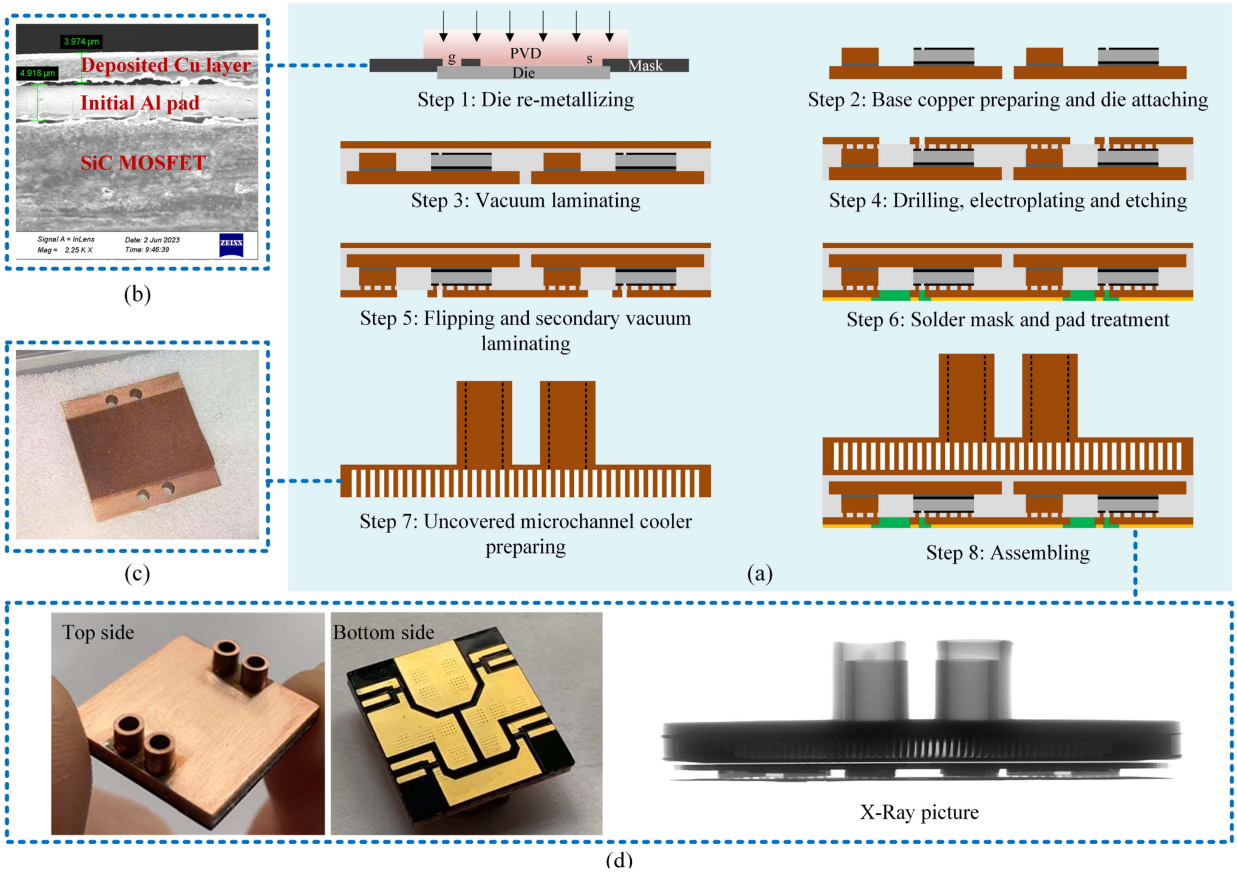

Fig. 4. Fabrication of the module. (a) Fabrication process flow. (b) Section diagram of SiC MOSFET die after remetallizing. (c) MC cooler. (d) Substrate-embedded SiC power module with integrated liquid cooling.

III. Detailed Design and Analysis of the Packaging

In Section II, a comprehensive overview of the final structure, layout, and packaging methodology of the proposed power module is presented. This section will delve into the details of the packaging design and its optimization process.

A. Orientation of the SiC mosfet Dies

As depicted in Fig. 4(a), step 5 of the fabrication process requires a flipping operation, ultimately resulting in the achievement of a face-down embedded packaging, in which the gate and source pads of the dies are oriented downwards. Correspondingly, in the absence of a flipping operation in step 5, a face-up embedded power module as illustrated in Fig. 5(a) can be obtained, leading to different electrical and thermal performance. To ascertain the optimal die orientation strategy, a comparative analysis is undertaken, focusing on the parasitic parameters and heat dissipation effects of the two structures.

Fig. 5(b) presents an enlarged view of a single MOSFET and its associated electrical circuit in both face-down and face-up embedded power modules. The MOSFET die has a vertical structure, featuring the drain pad on the lower surface, and the source and gate pads on the upper surface. Since the pads of drain and source are not in the same plane, the path length of the power loop is similar regardless of whether the dies are oriented upwards or downwards, resulting in similar power loop parasitic inductance of the two structures. However, for the driving loop, the conductive pathway of the power module with dies facing up is significantly longer than that of the module with dies facing down. This is because both the source and gate need to be connected to the module pads through copper inlays, thereby increasing the parasitic inductance of the driving circuit. Therefore, the adoption of an embedded packaging structure that employs a die face-down orientation enables the achievement of a lower overall parasitic inductance.

In terms of thermal performance, the proposed integrated power module encompasses two distinct heat dissipation pathways for the SiC MOSFET dies. One pathway involves conducting the heat to the MC for active cooling, and the other dissipates heat through the pads to the PCB located beneath the power module. Due to the MC bear the main cooling function of module, the heat transfer efficiency above the dies is particularly important. Fig. 5(c) illustrates the enlarged packaging structures of a single die and its top heat dissipation path in face-down and face-up embedded power modules, so then the thermal resistance between the die and the insulating layer within a single die area of the two types of packaging can be quantitatively assessed through

$$R_{\text{up}} = \frac{\frac{l_{\text{via}}}{\lambda_{\text{Cu}} A_{\text{via}}} \times \frac{l_{\text{via}}}{\lambda_{\text{SMC}} (A_{\text{die}} - A_{\text{via}})}}{\frac{l_{\text{via}}}{\lambda_{\text{Cu}} A_{\text{via}}} + \frac{l_{\text{via}}}{\lambda_{\text{SMC}} (A_{\text{die}} - A_{\text{via}})}} + \frac{l_{\text{Cu\_up}}}{\lambda_{\text{Cu}} A_{\text{die}}} = 0.478\ \text{K/W} \quad (1)$$

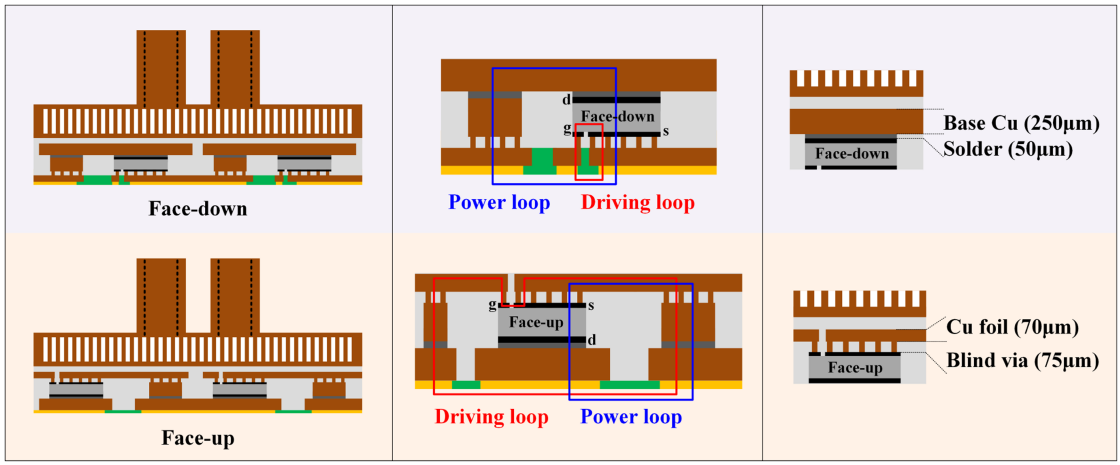

Fig. 5. Comparison of the face-down and face-up embedded packaging. (a) Complete structure. (b) Partial structure of a single die and its electrical circuit. (c) Partial structure of a single die and its top heat dissipation path.

$$R_{\text{down}} = \frac{l_{\text{solder}}}{\lambda_{\text{solder}} A_{\text{die}}} + \frac{l_{\text{Cu\_down}}}{\lambda_{\text{Cu}} A_{\text{die}}} = 0.149\ \text{K/W} \tag{2}$$

where λ_{Cu}, λ_{Solder}, and λ_{SMC} are the thermal conductivities of copper, solder and the SMC, respectively. l_{via}, l_{solder}, $l_{\text{Cu\_up}}$, and $l_{\text{Cu\_down}}$ represent the thicknesses of blind via, solder, and the top Cu layer in the face-up and face-down modules, respectively. A_{via} and A_{die} denote the areas of the blind vias and the SiC MOSFET die, respectively. It can be seen from (1) and (2) that, because of the presence of blind vias between the die and the MC in the face-up packaging, the copper content is lower compared to the face-down structure, resulting in poorer heat dissipation ability.

In summary, given that the embedded packaging with dies facing down has better performance in both electrical and thermal characteristics, the power module proposed in this study utilizes the face-down structure.

B. Packaging Layout

1) Die Spacing for Thermal Decoupling: The proposed power module integrates four SiC MOSFET dies symmetrically arranged within the package. If the spacing between the dies is not rationally designed, it can result in thermal coupling effect, leading to an increased junction temperature. To determine the proper die spacing, thermal simulations are conducted assuming a power loss of 20 W per die, which is a typical value in the target application scenarios such as an 11-kW on-board charger. Fig. 6 shows the temperature distributions of the top copper layer for edge-to-edge distance of the dies ranging from 2 to 7 mm. At a spacing of 2 mm, the temperature rise of the die is not only caused by its own heat generation, but is also influenced by the superposition effect of other dies, resulting in the most severe thermal coupling and therefore the highest die temperature. As the die spacing increases, the area of overlap in the heat flow diffusion paths between the dies decreases, consequently reducing the thermal coupling effect.

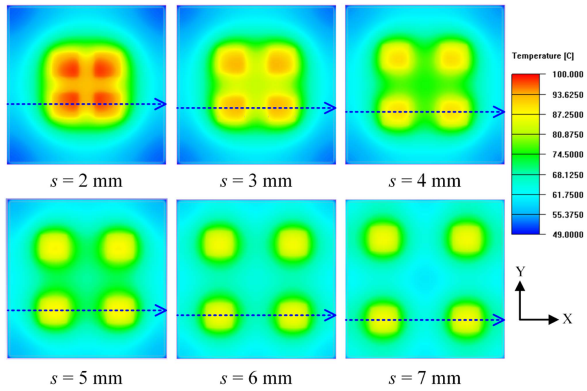

Fig. 6. Temperature distributions of the top copper layer at different die spacing.

Fig. 7(a) demonstrates the temperature variation along the line interconnecting two adjacent MOSFETs (the blue dash line in Fig. 6) at varying die spacing. When the die spacing increases to 5 mm, the die temperature does not exhibit significant further reduction with additional increases in spacing, indicating that the thermal coupling is no longer severe when the MOSFETs are spaced more than 5 mm apart. It is worth noting that simulations under different losses are also conducted. Fig. 7(b) shows the curves at 30 W, exhibiting the same trend as Fig. 7(a), which is due to the thermal coupling distance is predominantly determined by the thermal properties of packaging materials and the heat transfer mechanisms. Consequently, to mitigate the thermal coupling effect, the die spacing should be at least 5 mm in the subsequent overall layout design of the proposed packaging.

2) Parasitic Parameters Optimization: The high-speed switching characteristics of SiC MOSFETs make them particularly sensitive to parasitic parameters, which can lead to higher switching losses, device failure or even damage under severe conditions. Therefore, it is necessary to reduce the parasitic parameters caused by packaging and to minimize their detrimental effects.

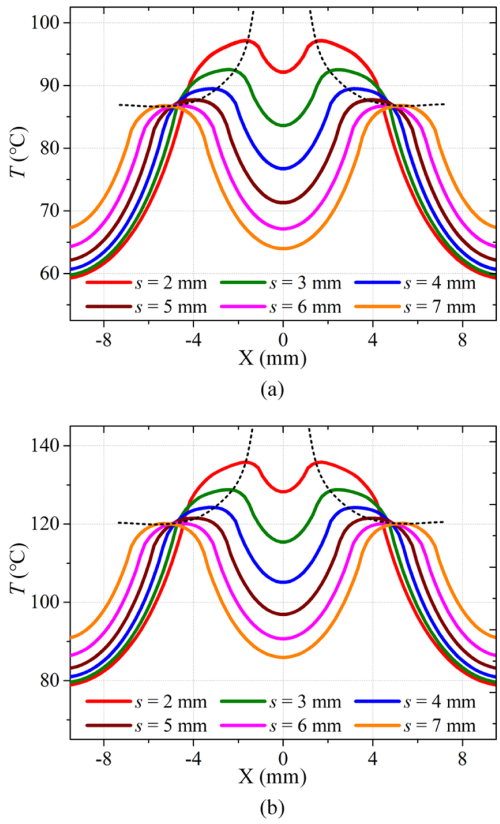

Fig. 7. Temperature variation along the line interconnecting two adjacent MOSFETs at varying die spacing. (a) 20 W. (b) 30 W.

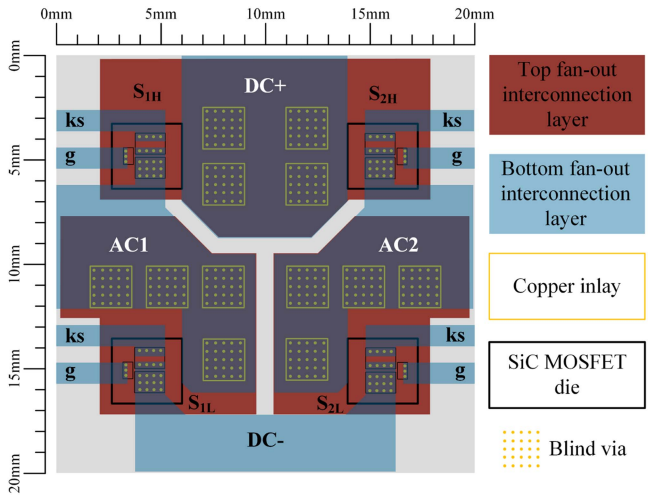

Fig. 8. Layout of the proposed H-bridge power module.

The parasitic inductances of the driving loop will retard the rise and fall time of the gate-source voltage during switching transients, thereby increasing the switching loss. And the power loop parasitic inductances will cause switching overshoot and oscillation. Through the design of face-down structure previously described, a low parasitic inductance of the driving loop can be achieved. Meanwhile, as shown in Fig. 8, the power loop parasitic inductance is minimized by reducing die spacing

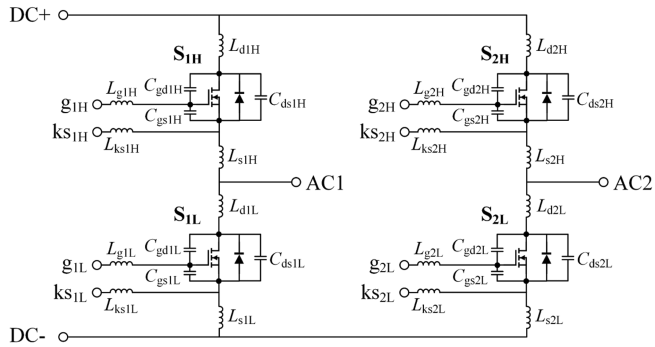

Fig. 9. Equivalent circuit model of switching transient analysis of the H-bridge SiC power module considering parasitic parameters.

while ensuring thermal coupling, optimizing the pathways of the interconnection layers, as well as strategically arranging the copper inlays around the dies. Furthermore, considering the interaction between the power loop and driving loop, a Kelvin connection is achieved for each SiC MOSFET. As illustrated in Fig. 8, the direct individual connection of both the driving loop and the power loop to the bare die allows for the achievement of nearly zero common source inductance. In addition, the power loop and driving loop are vertical to each other, so the undesired mutual effect between them can be eliminated.

Due to the ultra-thin embedded packaging structure with double-sided interconnection layers, the drain-source parasitic capacitance (C_{ds}) and the gate-drain parasitic capacitance (C_{gd}) introduced by the packaging cannot be ignored, which is determined by

$$C = \frac{\varepsilon_{\mathrm{r}}\varepsilon_0 A}{d} \tag{3}$$

where ε_{r} is the relative permittivity of molding material, ε_0 is the permittivity of vacuum, A and d are the facing area and distance of the two copper layers, respectively. The increase of capacitance can lead to a slowing down of the commutation and therefore to an increase in the switching losses [30]. To minimize the impact of C_{ds} and C_{gd} brought by the packaging, the copper facing area between the drain and source/gate of each MOSFET has been carefully reduced.

After comprehensive consideration, the packaging layout is finally designed as displayed in Fig. 8, detailing the positions of the dies, copper inlays, and blind vias, as well as the patterns of the interconnection layers. The equivalent circuit model of switching transient analysis of the H-bridge SiC power module considering parasitic parameters is presented in Fig. 9, and the parasitic parameters are extracted by Ansys Q3D Extractor, as given in Tables II and III.

As indicated in Table II, in the driving loop, the gate parasitic inductance and Kelvin source parasitic inductance of each SiC MOSFET are below 22 pH and 13 pH, respectively. Furthermore, the power loop parasitic inductances of the two half bridges are both lower than 155 pH, thereby achieving an overall low parasitic inductance of the power module. In addition, as shown in Table III, the gate-drain parasitic capacitance and drain-source parasitic capacitance of the SiC MOSFET die itself are 7.6 pF and

TABLE II
RESULTS OF THE PARASITIC INDUCTANCE EXTRACTION

	Parasitic inductance	Value (pH)	Parasitic inductance	Value (pH)
Driving loop	L_{g1H}	21.016	L_{g2H}	21.142
	L_{ks1H}	12.689	L_{ks2H}	12.726
	L_{g1L}	21.024	L_{g2L}	21.020
	L_{ks1L}	12.623	L_{ks2L}	12.628
Power loop	L_{d1H}	69.265	L_{d2H}	69.421
	L_{s1H}	12.265	L_{s2H}	12.586
	L_{d1L}	59.754	L_{d2L}	59.761
	L_{s1L}	12.504	L_{s2L}	12.505
	Power loop 1 (L_{d1H}+L_{s1H}+ L_{d1L}+L_{s1L})	153.788	Power loop 2 (L_{d2H}+L_{s2H}+ L_{d2L}+L_{s2L})	154.273

TABLE III
RESULTS OF THE PARASITIC CAPACITANCE EXTRACTION

	Parasitic capacitance of SiC MOSFET die from datasheet (pF)	Parasitic capacitances brought by packaging (pF)			
		S_{1H}	S_{1L}	S_{2H}	S_{2L}
C_{gd}	7.6	0.635	0.643	0.638	0.643
C_{ds}	72.6	3.572	3.574	3.570	3.575

72.4 pF, respectively, while those introduced by the package are about 0.64 pF and 3.57 pF, respectively. The proposed packaging only increases C_{gd} and C_{ds} of each SiC MOSFET by 8.4% and 4.9%, respectively. It can also be noted that in the proposed H-bridge power module, the parasitic parameter values of the four SiC MOSFETs are very close, which is beneficial for improving the switching consistency among the devices.

C. Integrated MC Cooler

Although substrate-embedded packaging has the advantages of low parasitic parameters, small size, and light weight, the organic materials used for die embedding and insulation have the drawback of poor thermal conductivity. In addition, the increasing power density in SiC power modules has rendered thermal management a significant challenge for substrate-embedded packaging.

To address the abovementioned challenge, this article proposes a liquid-cooled MC cooler integration method for the embedded power module, as depicted in Fig. 4. By utilizing the thermosetting properties of SMC and employing the vacuum lamination of the embedded packaging process, the SMC serves as both the carrier for die embedding and the interface for heatsink attachment. After high-temperature and high-pressure vacuum treatment, the SMC can tightly bond the MC heatsink and the die-embedded part together with a 110-μm-thick bonding layer between them, which is dense and devoid of bubbles. Compared with the traditional approach of attaching external heatsinks using thermal interface materials (TIMs) shown in Fig. 10, this method eliminates the requirement for additional TIM (such as thermal conductive adhesive) and the inevitable air

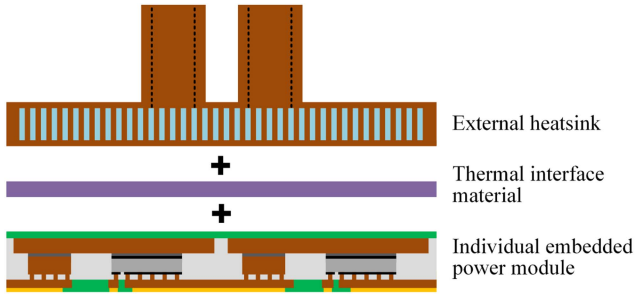

Fig. 10. Structure schematics of the embedded power module with external heatsink.

TABLE IV
THERMAL CONDUCTIVITY OF THE PACKAGING MATERIALS

Material	Thermal conductivity (W/(m·K))
SiC (MOSFET die)	490
Solder	57
Copper (Interconnection layers, heatsink)	385
SMC	4.5
Solder mask	0.17
Gold (Pad)	310
TIM	1

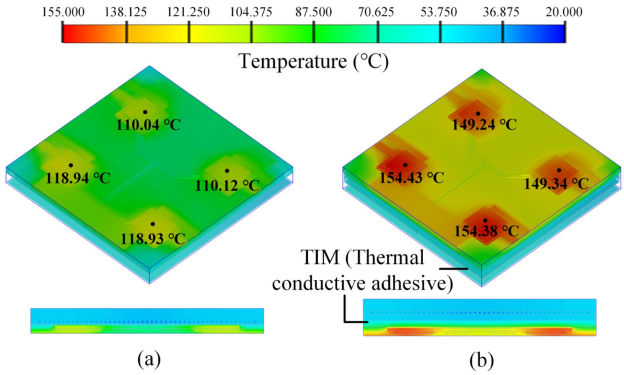

Fig. 11. Thermal steady-state simulation results. (a) Liquid-cooled integrated embedded power module. (b) Individual embedded power module with external heatsink.

they introduce, thus enhancing the thermal conductivity. Thermal simulations on integrated and external cooling solutions are conducted in Ansys Icepak, and the thermal conductivity of the packaging materials involved in the simulations is shown in Table IV. For a heat generation of 20 W per die, with a chip heat flux density of 192 W/cm^2 and a flow velocity of 0.4 m/s at each inlet, the thermal steady-state temperature distributions for the two embedded power modules are exhibited in Fig. 11. The comparative simulation results indicate that the maximum junction temperature of the SiC MOSFETs in the proposed liquid-cooled integrated embedded power module can reach a highest of 118.94 °C, which can be reduced by about 35 °C compared to that of the embedded power module with an external heatsink through thermal conductive adhesive as the TIM.

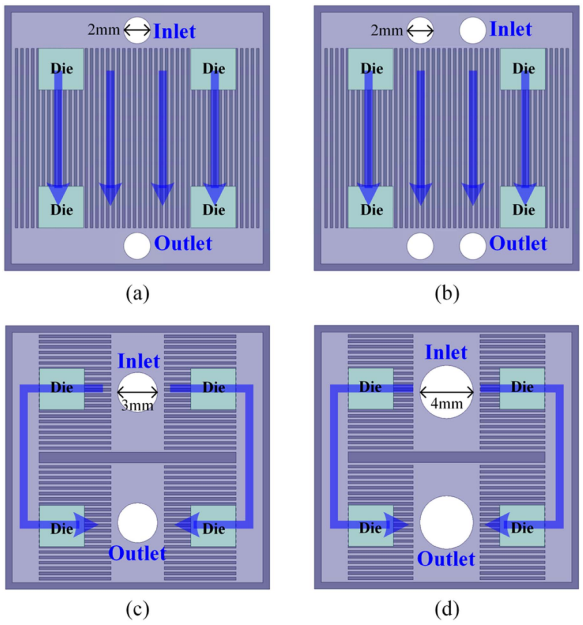

Fig. 12 Arrangements of the integrated MC cooler. (a) Type A: Straight channel with single inlet/outlet. (b) Type B: Straight channel with dual inlet/outlet. (c) Type C: Serpentine channel with d=3 mm. (d) Type D: Serpentine channel with d=4 mm.

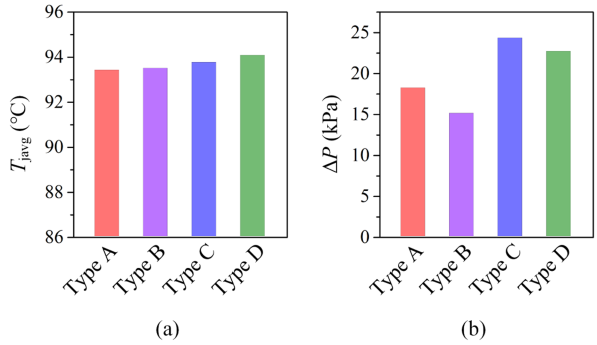

Fig. 13. Simulation results of the four types of arrangements of the MC cooler. (a) Average junction temperature. (b) Pressure drop.

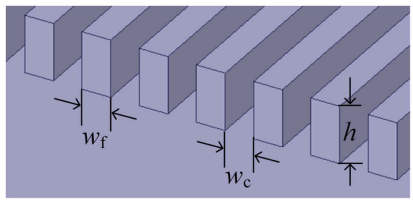

Fig. 14. Key design parameters of the micro pin fins.

To maximize the heat extraction within the limited space and thereby enhance the heat transfer performance and temperature uniformity of the module, meanwhile reducing stress and pump power, the arrangement and dimensions of the micro pin fins and inlet/outlet should be optimized. The average junction temperature of the dies T_{javg} and the pressure drop between the inlet and outlet ΔP are taken to characterize and evaluate the thermal and flow performance of the integrated heatsink in subsequent designs.

1) Arrangement of the Micro Pin Fins and Inlet/Outlet: In the power module, SiC MOSFET dies are the primary heat source, hence, micro pin fins should achieve full coverage above the dies to improve heat transfer efficiency. Based on the layout of the dies in Fig. 8, four distinct MC arrangements as shown in Fig. 12 were conceived. Among them, type A is a basic straightforward channel with a single set of inlet and outlet. Owing to constraints imposed by the die layout, the diameter of the inlet/outlet is restricted to 2 mm, suggesting that the pressure drop could be relatively high. On the basis of type A, type B adds another set of inlet and outlet to alleviate the pressure. Type C and type D adopt a serpentine channel with the inlet and outlet centrally positioned, allowing for the use of larger inlet and outlet to reduce pressure.

To compare the performance in heat dissipation as well as pressure of the four types of arrangements, fluid simulation analysis is conducted in Ansys Icepak, with the results illustrated in Fig. 13. As shown in Fig. 13(a), since all the four types of arrangements achieve full coverage above the dies, the average junction temperature T_{javg} of them are basically the same, signifying comparable heat dissipation efficiencies. Regarding the pressure drop depicted in Fig. 13(b), type B has a lower ΔP compared with type A, attributable to the inclusion of an additional set of inlet and outlet, thereby reducing packaging stress and pump power requirements. However, although type C and type D increase the inlet and outlet areas to potentially decrease pressure, the flow resistance is increased by the U-turn of the coolant during the flow process, resulting in an overall increase in pressure. Therefore, due to the superior performance in both heat dissipation and system pressure, the arrangement of type B with straight MC and dual inlet/outlet is selected in this article.

2) Optimization of the Dimensions of the Micro Pin Fins: The size of the heat exchange area exerts a direct influence on the heat dissipation capacity, so the fin width w_f, fin height h, and channel width w_c are key design parameters for each micro pin fin, as illustrated in Fig. 14. To ascertain the impact of channel dimensions on the flow and cooling performance of the cooler, a series of heatsink models featuring MCs of different sizes are established, with $w_c = w_f = w$, w and h varying between 0.1–0.3 mm and 0.1–1 mm, respectively. Fluid simulations of the embedded power modules integrated with these MC structures are conducted, while ensuring consistency in the calculation models, mesh generation, and parameter settings.

Fig. 15 dissipates the relationship between the average junction temperature of the dies and the pressure drop as a function of fin height and width. It is observed that as h increases, the average junction temperature and pressure drop both decrease. This is because a larger channel depth can result in an expanded heat dissipation area and channel volume, thereby enhancing the heat transfer efficiency and reducing the flow resistance. Consequently, the height of the channel should be designed to be large within the fabrication constraints. With the decrease of w, the cooling effect is significantly enhanced due to the increased number of micro pin fins and heat transfer area, while

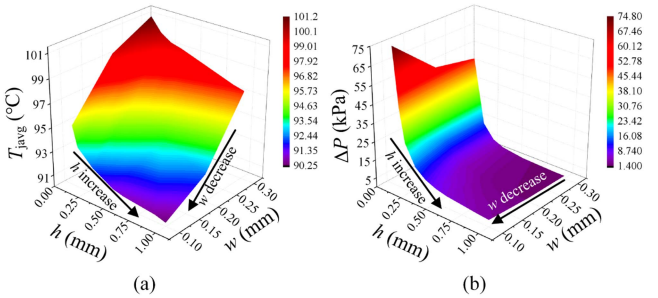

Fig. 15. Simulation results of the integrated embedded power modules with different sizes of micro pin fins. (a) Average junction temperature. (b) Pressure drop.

at the expense of a higher pressure drop. However, once the height of the MC reaches about 0.8 mm, the effect of w on the pressure drop becomes negligible, which is maintained below 5 kPa, thus allowing for the selection of a smaller w to pursue higher heat dissipation efficiency. In this study, wire-electrode cutting is utilized to process the MCs. Within the scope of its capability, the maximum aspect ratio was selected, with w and h being determined as 0.1 mm and 1 mm, respectively, ensuring that the MC design not only enhances thermal management but also maintains efficient fluid dynamics.

IV. Experimental Verification

To compare the electrical and thermal performance of the proposed integrated module with traditional commercial packaging, double pulse test (DPT) and thermal test are conducted on the proposed module and TO-247-4 packaging with identical SiC MOSFET dies (CPM2-1200-0080B).

A. Dynamic Characteristic

Fig. 16 shows the DPT circuit diagram and experimental setup for the proposed H-bridge power module and TO-247-4 packaging. As illustrated in Fig. 16(a), given that the proposed power module consists of two half bridges that exhibit a symmetrical structure, a single bridge arm is selected for the DPT. For the experimental validation regarding the TO-247-4 packaging, the half bridge in the DPT circuit is composed of two devices and the PCB traces connecting them. To fairly compare the dynamic characteristics of the two packages, the wiring, component placements, and overall circuit topology of the two DPT boards are carefully designed to be identical, as shown in Fig. 16(b).

The switching waveforms of the proposed integrated module and TO-247-4 packaging are demonstrated in Fig. 17, with the key parameters detailed in Table V. It is evident that, compared with TO-247-4 packaging, benefit by the advantage of low parasitic parameters, the proposed integrated module has a faster switching speed, resulting in shorter switching time and lower switching losses. The turn-ON and turn-OFF losses are 12.7% and 10% lower than those of SiC MOSFET in TO-247-4 packaging, respectively. In addition, despite the increased current change rate of the proposed power module, its turn-OFF voltage overshoot is still 16.9% lower than that of TO-247-4 packaging, due to the reduced parasitic inductance of the power loop.

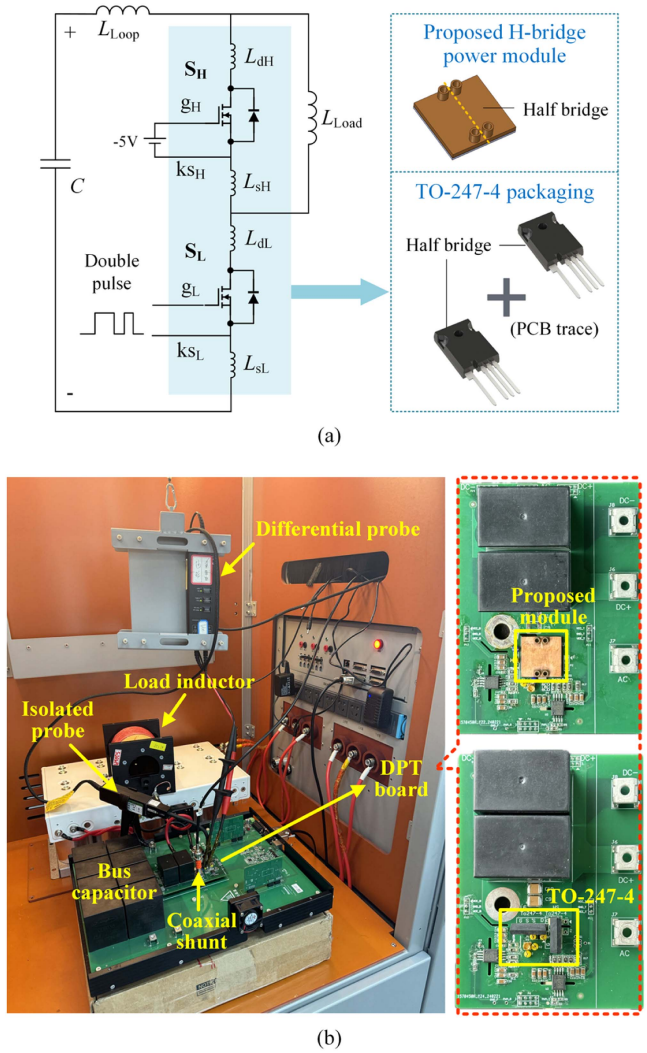

Fig. 16. DPT circuit diagram and experimental setup. (a) Circuit diagram. (b) Experimental setup.

TABLE V
Key Parameters of DPT Results

Items	Proposed module	TO-247-4
di/dt_on (A/μs)	809.984	520.227
t_{on} (ns)	51.2	75.52
E_{on} (μJ)	852.231	976.126
di/dt_off (A/μs)	808.373	578.473
t_{off} (ns)	77.12	80
E_{off} (μJ)	92.907	103.156
$V_{overshoot}$ (V)	69.684	83.861

Furthermore, due to the turn-OFF voltage oscillation caused by resonance between the output capacitor of the SiC MOSFET and the parasitic inductance of the power loop, the parasitic inductance can be calculated according to the following equation:

$$f = \frac{1}{2\pi\sqrt{LC_{OSS}}} \tag{4}$$

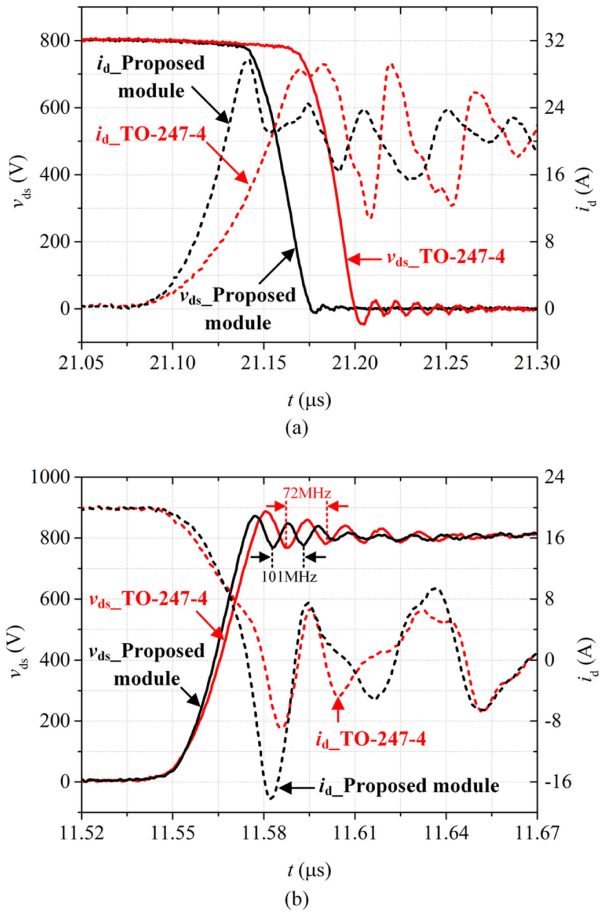

Fig. 17. Switching waveforms of the proposed integrated module and TO-247-4 packaging. (a) Turn ON. (b) Turn OFF.

where f is the oscillation frequency of v_{ds}, L is the parasitic inductance of the power loop, and C_{oss} is the output capacitance of the device. C_{oss} of the SiC MOSFET is 80 pF reading from the C-V curve at 800 V of the datasheet. It should be noted that L calculated by (4) includes both the parasitic inductance of the DPT board as well as that of the packaging. As shown in Fig. 17(b), the power loop parasitic inductance of the TO-247-4-based half bridge on PCB is estimated as 61.1 nH at 72-MHz oscillation, which includes inductances of two TO-247-4 devices as well as that of the PCB interconnections; and the parasitic inductance of the proposed module is estimated as 31.0 nH at 101-MHz oscillation. Due to the DPT boards of the two packages being designed to be nearly identical, it is therefore concluded that the power loop parasitic inductance of per half bridge of the proposed integrated module is approximately 30.1 nH less than that of the half bridge composed of TO-247-4 devices on PCB. This reduction in parasitic inductance contributes significantly to the improved electrical performance of the proposed module.

B. Thermal Performance

The thermal experiment is conducted utilizing the Power Tester 1500 A from Mentor Graphics, which can monitor the junction temperature of SiC MOSFETs through thermal sensitive electrical parameter extraction technique and achieve the thermal transient testing of the power devices.

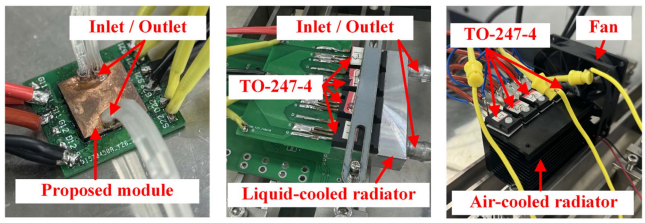

Fig. 18. Thermal experimental measurement setup. (a) Proposed integrated liquid-cooled embedded power module. (b) TO-247-4 packaging with external liquid cooling. (c) TO-247-4 packaging with external air cooling.

TABLE VI
DETAILED SETTINGS FOR THE THERMAL TESTS

Items	Proposed module	TO-247-4	
Cooling mode	Integrated liquid cooling	External liquid cooling	External air cooling
External radiator	/	➢ Material: Al ➢ Size: 40×80×12mm^3	➢ Material: Al ➢ Size: 50×80×50mm^3
Cooling medium	Deionized water	Deionized water	Air
Flow rate	0.47 L/min	0.47 L/min	51.44 CFM

As shown in Fig. 18, a comparative thermal performance analysis is undertaken between the proposed substrate-embedded SiC power module with integrated liquid cooling, as well as the traditional commercial TO-247-4 packaging with air and liquid cooling. Because the proposed power module contains four SiC MOSFET dies, four devices are used for the testing of the TO-247-4 packaging. All the thermal tests are executed under simultaneous heating of four SiC MOSFETs to simulate the operation of the H-bridge circuit. The specific settings for the thermal tests are denoted in Table VI, wherein the settings for the TO-247-4 packaging are configured based on its typical cooling conditions that are commonly used.

The process of the thermal experiment is as follows: First, a heating current is applied to the SiC MOSFETs for a certain period of time, during which the junction temperature rises and reaches thermal equilibrium. Subsequently, the heating current is terminated, and the junction temperature is continuously monitored throughout the cooling phase of the SiC MOSFETs, thereby obtaining the transient temperature response curve that characterizes the thermal characteristics of the packages.

Fig. 19 presents the transient temperature response curves under different heating powers for the proposed integrated module and TO-247-4 packaging with liquid and air cooling. By connecting the curves under identical packaging and heat dissipation conditions into three-dimensional surface plots, it can be observed that the green surface, representing the proposed integrated module, is at the lowest position, indicating the minimum junction temperature. The blue surface for TO-247-4 with liquid cooling is intermediate, and the red surface for TO-247-4 with

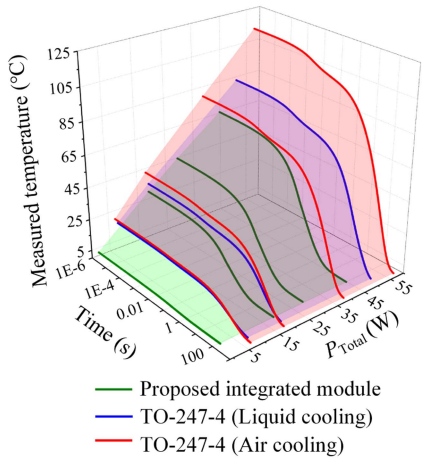

Fig. 19. Transient temperature response curves.

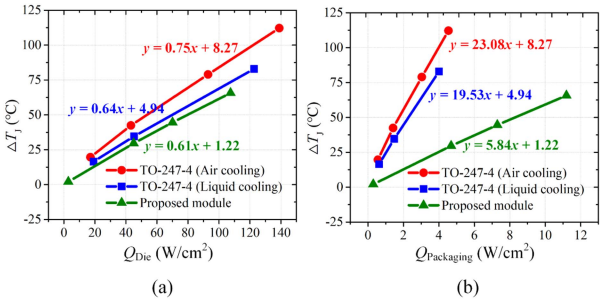

Fig. 20. Junction temperature rise under different heat flux. (a) Die heat flux. (b) Packaging heat flux.

air cooling is at the highest, signifying the maximum junction temperature.

The starting points of the curves in Fig. 19 represent the junction temperature rise ΔT_J of the SiC MOSFETs under specified heating powers. Thus, the relationship between ΔT_J and the heat flux can be further extracted as shown in Fig. 20. Q_{Die} and $Q_{\mathrm{Packaging}}$ are the heat flux of the SiC MOSFET die and the heat flux of the packaging respectively, which can be expressed as

$$\begin{cases} Q_{\mathrm{Die}} = \dfrac{P_{\mathrm{Total}}}{4A_{\mathrm{Die}}} \\ Q_{\mathrm{Packaging}} = \dfrac{P_{\mathrm{Total}}}{A_{\mathrm{Packaging}}} \end{cases} \tag{5}$$

where A_{Die} and $A_{\mathrm{Packaging}}$ are the area of the SiC MOSFET die and that of the packaging respectively, and $A_{\mathrm{Packaging}}$ of TO-247-4 is the area of four TO-247-4 devices.

As seen in Fig. 20, ΔT_J exhibits an approximately linear increase with both Q_{Die} and $Q_{\mathrm{Packaging}}$, from which the heat flux at a junction temperature rise of 150 °C can be inferred as shown in Table VII. For SiC MOSFETs with $\Delta T_J = 150$ °C, the die heat flux could go up to 243.90 W/cm^2 in the proposed integrated module, which is respectively 29.1% and 7.6% greater than those of TO-247-4 with air cooling and liquid cooling, reflecting the excellent heat dissipation performance of the proposed packaging structure. Moreover, from the perspective of packaging heat flux, for SiC MOSFETs with $\Delta T_{\mathrm{J}} = 150$ °C, $Q_{\mathrm{Packaging}}$ of the proposed integrated module is 25.48 W/cm^2,

TABLE VII
HEAT FLUX OF THE DIE AND PACKAGING AT $\Delta T_{\mathrm{j}} = 150$\°C

Packaging	Q_{Die} (W/cm^2)	$Q_{\mathrm{Packaging}}$ (W/cm^2)
Proposed module	243.90	25.48
TO-247-4 with liquid cooling	226.66	7.42
TO-247-4 with air cooling	188.97	6.14

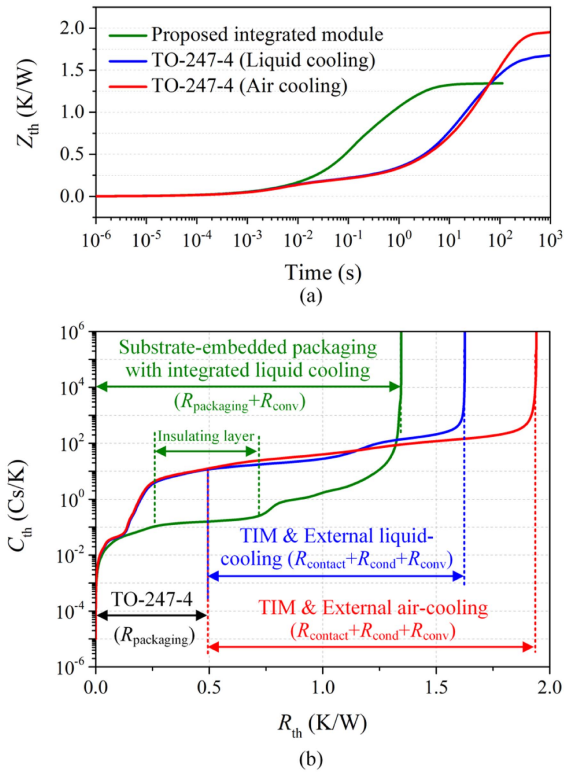

Fig. 21. Heat transfer characteristics of the different packages. (a) Thermal impedance curves. (b) Structure function curves.

which is 315.0% and 243.4% higher than those of TO-247-4 with air cooling and liquid cooling, respectively. This result underscores the advantage of the integrated MC design, enabling the proposed power module to dissipate higher power within a more compact packaging size.

To further analyze the heat transfer characteristics and provide a more comprehensive understanding of the thermal behavior, the thermal impedance curves as well as the structure function curves are included in Fig. 21(a) and (b), respectively. It is evident that although TO-247-4 packaging inherently features a low junction-to-case thermal resistance, the proposed packaging solution showcases distinct advantages. This is due to the integrated MC thermal management architecture characterized by a high aspect ratio, as well as the elimination of the contact and conduction thermal resistances associated with additional TIM. Consequently, the overall junction-to-flow thermal resistance of the proposed packaging is substantially lower compared to that of the TO-247-4 packaging employing conventional external air cooling and liquid cooling strategies. It is worth mentioning that the thermal conductivity of the insulation material employed in

the proposed module is not particularly high, which increases the thermal resistance to a certain extent. However, the feasibility and enhanced cooling efficiency of the proposed packaging concept have still been verified through the above-mentioned experiments, suggesting that it is a promising development direction. Therefore, in future research, there is a great opportunity to further improve the thermal performance of substrate-embedded packaging significantly through advancements in insulation materials and processing techniques, which aligns with our ongoing study.

V. Conclusion

This study explores the design, fabrication, and evaluation of a substrate-embedded H-bridge SiC power module with integrated liquid cooling, demonstrating enhanced performance in dimensional, electrical, and thermal metrics. The main innovations of this research can be summarized as follows.

1) Through the application of thermosetting organic polymer materials and vacuum lamination technology, the solution achieves the embedding of SiC MOSFET dies as well as the compact integration of the MC cooler, with an overall packaging size of only 20 mm $\times$ 20 mm $\times$ 2.4 mm. The integrated method creates a seamless bond, which eliminates air gaps for better thermal conductivity and mechanical stability. Moreover, it is compatible with existing substrate-embedded packaging production, reducing the need for major equipment changes.
2) Benefit from the optimization design of the multilayer planar structure without bonding wires, the driving loop and power loop parasitic inductances of the module extracted by Ansys Q3D Extractor are below 35 pH and 155 pH, respectively, thereby improving the switching performance of SiC power devices. The DPT results show that, in comparison with the commercial TO-247-4 packaging with Kelvin connection, the turn-ON and turn-OFF losses of the proposed power module are reduced by 12.7% and 10%, respectively.
3) The integration of MC cooler eliminates the TIM with poor thermal conductivity from the die heat dissipation path, enhancing the cooling efficiency of the proposed power module within a compact size. Thermal experiment indicates that when $\Delta T_J = 150$ °C, die heat flux of the proposed module is 29.1% and 7.6% higher than those of TO-247-4 packaging with external air and liquid cooling, respectively.

Due to the superior characteristics previously discussed, the substrate-embedded SiC power module with integrated liquid cooling is expected to advance the capabilities of power electronic systems in various high-performance and high-power-density applications, thus holding broad development prospects.

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