A New Control Method to Operate Isolated MLI as a Fast Fault-Tolerant Configuration for Handling a Wide Variety of Open Circuit Failures

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***Abstract*—This article describes the design of a fully fault-tolerant inverter configuration specifically for grid-connected and constant speed drive applications. The approach focuses on maintaining fault tolerance without increasing the device count in existing isolated configurations. The proposed topology employs a common cell and standard cells, each divided into operational and redundant half-bridge legs. Under normal operating conditions, the output voltage generates from operational legs. But, in the event of a switch fault, the corresponding switch in the redundant leg activates and replacing the fault switch. Besides, the proposed fault-tolerant control scheme operates within a single fundamental cycle of the output voltage waveform. During this cycle, each switch undergoes four rounds of scrutiny before any isolation occurs which significantly reducing the chances of misidentifying faults or triggering gate misfires. The fault detection and response are managed using only two output sensors (one for voltage and one for current), which streamlines the system and enhances its efficiency. The article includes a comparative study that demonstrates the effectiveness and practicality of this fault-tolerant approach compared to similar topologies and techniques. The proposed fault-tolerant topology and method will be validated through MATLAB Simulink simulations and confirmed with a hardware prototype.**

***Index Terms*—Fault diagnosis method, isolated fully fault tolerant multilevel inverter (MLI), open circuit faults, postfault operation.**

I. Introduction

MULTILEVEL inverters (MLIs) have been at the forefront, emerging as an innovative solution to address the demands of high-power applications. Owing to high quality output voltage with lower switch ratings [1], [2], [3], MLIs are extensively used in wide variety of applications such as traction, grid integration, high voltage dc transmission (HVDC), flexible ac transmission (FACTs), electric vehicles (EV), renewables, and drives [4], [5], [6]. These applications need a reliable operation of the MLIs for uninterrupted performance. Conventionally, MLI topologies based on their structural configuration are classified as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [7], [8], [9]. Among these, CHB-MLIs have gained significant attention due to their modular design, symmetrical structure, and ease of control [10]. CHB-MLIs require more number of dc sources and photovoltaic systems can provide easily as per the requirement of the topology [11]. However, Major PV-grid connected industries are recommending the isolated configurations for the safety reasons and resilient operation. Thereby, many transformer-based CHB-MLIs are introduced in the literature and most popular topology [12] is depicted in Fig. 1 where secondaries of the transformers are connected in series with the load.

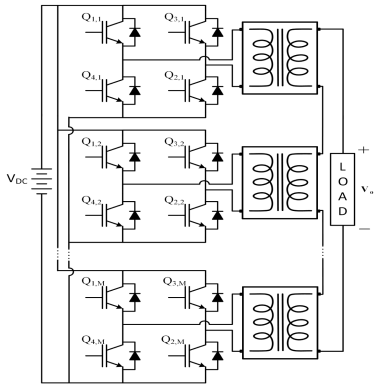

Fig. 1. Conventional Isolated CHB-MLI.

Based on findings from an industry-based survey [13], semiconductor switches and capacitors are identified as the most susceptible components to faults among all power electronic components. Therefore, to get resilient operation under any fault condition is becoming a challenging job. Among all the possible converter faults, switch faults are the most likely to happen due to the scalable nature of converter to obtain high voltage levels. More broadly, switch faults can be categorized as OCF and SCF. SCF causes sudden effects to the system and thus, requires quick diagnosis. To protect the converter against SCFs, hardware solutions such as di/dt feedback and

Received 4 October 2024; revised 14 March 2025; accepted 2 May 2025. Date of publication 27 May 2025; date of current version 30 June 2025. This work was supported in part by the Science and Engineering Research Board (SERB), Empowerment and Equity Opportunities for Excellence in Science under Grant SERB-EEQ/2021/000839 and in part by the SVNIT, Surat. Recommended for publication by Associate Editor Z. Chen. *(Corresponding author: Jammala Venkataramanaiah.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3571474.

Digital Object Identifier 10.1109/TPEL.2025.3571474

desaturation methods are adopted [14], [15]. In OCF, current path gets broken and neglecting it over a longer period turns out to be dangerous as dc current starts flowing in the converter. Various software solutions are provided for OCFs where additional components are not required. A fault is generally identified based on sensing output quantities. The method described in [16] detects and locates a single-switch OCF by inspecting the current path during zero-voltage switching and analyzing it's slope. But, it requires more than two fundamental cycles for diagnosis the fault. Similarly, authors in [17] reported about the behavior of inner and outer switch performance when the OCF occur in the semiconductor switch. On other hand, voltage-based methods extract fault features from terminal voltages, such as frequency harmonic analysis in [18] and PCA in [19], where complicated mathematical analysis are involved. The authors in [20] proposed the fault operation techniques based on SPWM through single voltage sensor at grid side by compromising the magnitude of the output voltage. A hybrid approach taking both voltage and current for single-switch fault detection in CHB was proposed in [21]. In [22] and [23], the authors presented an advanced fault detection and diagnosis approach for asymmetric CHB-MLIs and 3L-NPC systems, respectively, employing artificial neural networks (ANNs) within binary and trinary network architectures. Although the strategy is efficient for fault identification, the first paper does not address postfault operation, while the second is specific to NPC converters. In [24], authors introduced a phase shift PWM (PS-PWM) based fault-tolerant approach for the CHB battery energy storage system, enabling resilience to single switch faults. Upon fault detection, the faulty cell is initially bypassed, followed by compensation of the missing voltage levels from the remaining healthy cells to maintain balanced line-to-line voltages. Nevertheless, certain configurations do not maintain the same rated voltage in post-fault conditions, [25] provides only two-thirds of the output rated voltage. To retain the output voltage effectively without increasing the dc link, auxiliary modules are used which can be a switch, group of switches [26], or a two-level voltage source inverter with a capacitive bank [27]. In [28], postfault operations were implemented using an auxiliary CHB cell and in [26], the output voltage was preserved with the help of auxiliary switches. However, many popular topologies incorporate auxiliary cells that offer fault tolerance (bypass the entire faulty cell) for either a single or multiple faults within the same cell. This becomes problematic when the fault occurs in different cells, leading to low output voltage levels that disrupt the overall system. To address aforesaid issues, the article proposes an inverter that is designed to operate with the same number of switches as required in conventional fault-tolerant inverter topology and effectively preserves the output voltage by managing multiple OCFs located on any combination of the switch/cell of the converter. The key contributions of this article are as follows:

1) The proposed inverter topology necessitates a comparable number of cells to that of existed fault-tolerant configurations.
2) Fault tolerance operation is set up to address multiple switch faults.
3) Fault diagnosis procedure is fast and an independent of switching technique.

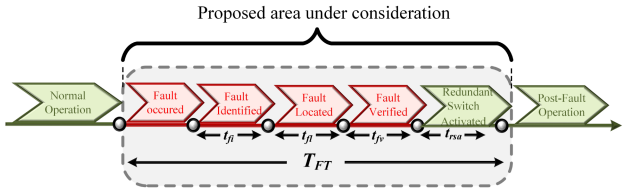

Fig. 2. Generalized fault-tolerant behavior of inverter.

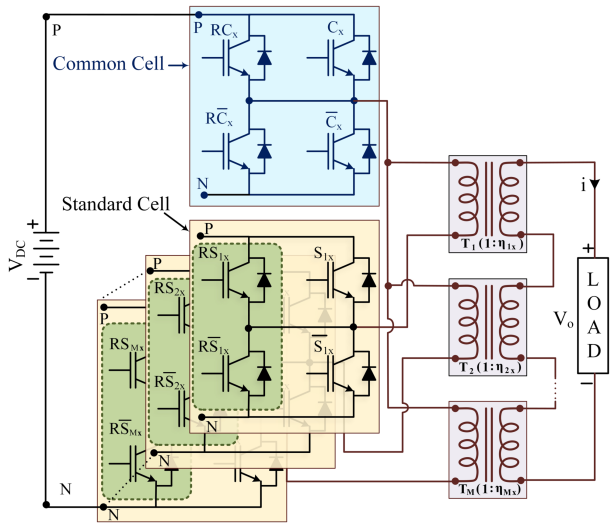

Fig. 3. Proposed isolated fully fault tolerant topology (IFFT).

4) Fault verification (FV) is done to ensure the inverter doesn't interpret gate misfires as faults.

Herein, the generalized timeline illustrating fault-tolerant power inverter circuits is depicted in Fig. 2, wherein, T_{fi} represents the fault identification time, T_{fl} indicates fault localization time followed by T_{rsa} denotes the activation time for redundant switch fault identification. The rest of this article is organized as follows, In Section II, the working topology of the converter is explained in detail. The proposed fault-tolerant methodology is given in Section III, followed by experimental results in Section IV. Finally, Section V concludes this article.

II. Working Topology

The proposed isolated fully fault tolerant topology (IFFT) consists of H-bridge cells and internal midpoint of each cell is shorted between the legs (see in Fig. 3). The configuration consists of (M+1) H-bridge cells per phase, where one is a common cell and the rest of M are standard cells. Herein, the legs of each cell are specifically named as operating leg and redundant leg since operating leg is contributing the output voltage under normal conditions whereas redundant leg will be activated under fault conditions or vice versa. The upper switch in operational leg of a common cell is denoted as C_x and its complementary switch as $\overline{C}_x$ while the switches of redundant leg are represented by RC_x and $R\overline{C}_x$. Similarly, operating and redundant leg switches of the standard cells are denoted as S_{kx} and $\overline{S}_{kx}$, RS_{kx}, and $R\overline{S}_{kx}$, respectively. The subscript x

TABLE I
NOMENCLATURE

FC :	Fundamental Cycle	SPWM :	Sinusoidal Pulse Width Modulation	FS :	Faulty Switch
η_{kx} :	Transformer Turns Ratio	PS-PWM:	Phase Shifted Pulse Width Modulation	FV :	Fault Verification
CHB :	Cascade H-bridge	GRC :	Gate pulses of redundant common switch	τ :	Tolerance
MLI :	Multilevel Inverter	T_{fi} :	Fault identification time	PGM :	Possible Gate Misfire
HVDC :	High Voltage DC transmission	T_{fl} :	Fault localization time	Nop :	Normal operation
FACTS :	Flexible AC transmission	T_{rsa} :	Activation time for redundant switch	GS_k :	Gate pulses of standard switch
EV :	Electric Vehicle	M :	Number of standard cell	GRS_k :	Gate pulses of redundant switch
NPC :	Neutral Point Clamped	N :	Number of output voltage level	FI :	Fault Identification
OCF :	Open Circuit Fault	FL :	Fault Localization	GC :	Gate pulses of common switch
SCF :	Short Circuit Fault	FDP :	Fault Detection Pulses	PCA	Principal Component Analysis
ANN :	Artificial Neural Network	a :	Variable depends upon voltage level	m:	Number of transformers

represents the phase in which the corresponding switch resides and *k* denotes the serial number of a standard cell.

In addition, the presented topology is having single dc supply and cascaded on the grid with the help of M injection transformers. Herein, one primary terminal of the each transformer is connected to the common cell and the other terminal is connected to the corresponding standard cells and all secondary windings are cascaded at the load to obtain the required output voltage. The kth transformer turn ratio is $1{:}\eta_{kx}$, where x represents the phase. According to the above nomenclature, the output phase voltage of the proposed inverter is

$$v_e(t) = \sum_{k=1}^{M} \left(C_x \overline{S}_{kx} - \overline{C}_x S_{kx} \right) * \eta_{kx} * V_{DC}(t). \quad (1)$$

The levels of the output voltage (N) is depending upon the number of standard cells M and the turn's ratio of the transformers η_{kx} (secondary turn's) and it is expressed as follows:

$$N = 2 * \left(\sum_{k=1}^{M} \eta_{kx} \right) + 1. \quad (2)$$

Table I displays promising number of levels of the proposed configuration for both symmetrical and asymmetrical turn's rations of the transformers. Table I considers only four transformers and it confirms that the maximum number of output voltage levels can be achieved when the transformers turn's ratio are selected in the binary nature and the same is generalized for *M* transformers in the following equation:

$$N_{\max} = 2^{m+1} - 1. \quad (3)$$

III. Proposed Methodology

The proposed inverter's switching table as shown in Table II is considered for establishing the presented methodology. Herein, IFFT maintains seven-level (symmetrical) output voltage under normal operating conditions where as in the event of an OCF, the output waveform cannot be maintained at seven levels and the deviation will occur based on the location of the faulty switch. There are switches for providing the positive and negative cycle of the output voltage waveform, when the fault occurs in a positive cycle then the corresponding positive level contributing switches may have the fault and similarly the fault in a negative cycle occurs due to the negative cycle contributing switches. The proposed scheme starts in the sequence of A) Fault identification, B) Fault localization, and C) Fault Verification.

TABLE II
OUTPUT VOLTAGES LEVELS WITH COMBINATIONS OF TRANSFORMER TURNS RATIO

Cells	Transformer Ratios				O\P Levels
	T_{1x}	T_{2x}	T_{3x}	T_{4x}	
2	$1:\eta$				3
3	$1:\eta$	$1:\eta$			5
	$1:\eta$	$1:2\eta$			7
4	$1:\eta$	$1:\eta$	$1:\eta$		7
	$1:\eta$	$1:\eta$	$1:2\eta$		9
	$1:\eta$	$1:\eta$	$1:3\eta$		11
	$1:\eta$	$1:2\eta$	$1:2\eta$		11
	$1:\eta$	$1:2\eta$	$1:3\eta$		13
	$1:\eta$	$1:2\eta$	$1:4\eta$		15
5	$1:\eta$	$1:\eta$	$1:\eta$	$1:\eta$	9
	$1:\eta$	$1:\eta$	$1:\eta$	$1:2\eta$	11
	$1:\eta$	$1:\eta$	$1:\eta$	$1:3\eta$	13
	$1:\eta$	$1:\eta$	$1:\eta$	$1:4\eta$	15
	$1:\eta$	$1:\eta$	$1:2\eta$	$1:2\eta$	17
	$1:\eta$	$1:\eta$	$1:2\eta$	$1:3\eta$	19
	$1:\eta$	$1:2\eta$	$1:2\eta$	$1:2\eta$	15
	$1:\eta$	$1:2\eta$	$1:2\eta$	$1:3\eta$	17
	$1:\eta$	$1:2\eta$	$1:2\eta$	$1:4\eta$	19
	$1:\eta$	$1:2\eta$	$1:2\eta$	$1:5\eta$	21
	$1:\eta$	$1:2\eta$	$1:2\eta$	$1:6\eta$	23
	$1:\eta$	$1:2\eta$	$1:3\eta$	$1:3\eta$	19
	$1:\eta$	$1:2\eta$	$1:3\eta$	$1:4\eta$	21
	$1:\eta$	$1:2\eta$	$1:3\eta$	$1:5\eta$	23
	$1:\eta$	$1:2\eta$	$1:3\eta$	$1:6\eta$	25
	$1:\eta$	$1:2\eta$	$1:3\eta$	$1:7\eta$	27
	$1:\eta$	$1:2\eta$	$1:4\eta$	$1:4\eta$	23
	$1:\eta$	$1:2\eta$	$1:4\eta$	$1:5\eta$	25
	$1:\eta$	$1:2\eta$	$1:4\eta$	$1:6\eta$	27
	$1:\eta$	$1:2\eta$	$1:4\eta$	$1:7\eta$	29
	$1:\eta$	$1:2\eta$	$1:4\eta$	$1:8\eta$	31

A. Fault Identification

During this operation, the estimated voltage ($v_e(t)$) will be compared with the measured voltage ($v_o(t)$), and any nonzero

TABLE III
SWITCHING STATES OF THE PROPOSED SEVEN-LEVEL CONFIGURATION

C	S_1	S_2	S_3	Output Voltage
1	0	0	0	$+3V_{DC}$
1	0	0	1	$+2V_{DC}$
1	0	1	1	$+V_{DC}$
1	1	1	1	0
0	0	0	0	0
0	1	0	0	$-V_{DC}$
0	1	1	0	$-2V_{DC}$
0	1	1	1	$-3V_{DC}$

TABLE IV
OUTPUT VOLTAGE DEVIATION WHEN OCF OCCURS

Fault Location	i	$[C_x\ S_x]$ [1 0]	$[C_x\ S_x]$ [0 0]	$[C_x\ S_x]$ [1 1]	$[C_x\ S_x]$ [0 1]
C_x	$i+$	$+aV_{DC}$	–	$+aV_{DC}$	–
	$i-$	–	–	–	–
$\overline{C_x}$	$i+$	–	–	–	–
	$i-$	–	$-aV_{DC}$	–	$-aV_{DC}$
S_{kx}	$i+$	–	–	–	–
	$i-$	–	–	$-V_{DC}$	$-V_{DC}$
$\overline{S_{kx}}$	$i+$	$+V_{DC}$	$+V_{DC}$	–	–
	$i-$	–	–	–	–

deviation will confirm that a fault has occurred. The proposed technique needs an output voltage and current sensors to operate effectively. Herein the current sensor is required only to identify the direction of current in an each switch. The voltage deviation of the output voltage waveform due to the OCF at the switch is presented in Table III. Suppose the OCF occurs in C_x (which is conducted only for positive current) then the deviation will become $+aV_{DC}$. Similarly, if the OCF occurs in $\overline{S}_{kx}$ then the deviation voltage will be become $+V_{DC}$ since it is allowing positive current through it. At the same time, $\overline{C}_x$ and S_{kx} provide the deviation $-aV_{DC}$ and V_{DC} sequentially under the faulty conditions. In the Fig. 4, the detailed identification procedure is explained by considering the following equations:

$$i(t) > 0\ \&\ v_o(t) - v_e(t) + a * V_{DC}(t) < \tau \tag{4}$$

$$i(t) < 0\ \&\ v_o(t) - v_e(t) - a * V_{DC}(t) < \tau. \tag{5}$$

A tolerance voltage drop, τ, is defined as half of the minimum voltage level to prevent fault misidentification. Eq. (4) confirms a fault in the positive switches, while (5) confirms a fault in the negative switches. If neither equation is satisfied, the system operates normally without any faults.

TABLE V
SIMULATION PARAMETERS

Parameters	Values
Input dc Voltage (V_{dc})	(50V for 7-level),(62V for 11-level)
Number of cells ($M+1$)	4
Transformer Turns Ratio	1: 1, 1: 1, 1: 1 (for 7-level); 1: 1, 1: 1, 1: 3 (for 11-level);
Sampling Time	50 μS
Frequency	50Hz
$Load_1$	R= 9Ω; L = 21.49mH
$Load_2$	1 hp single-phase induction motor

B. Fault Localization

In this section, a faulty switch is identified from two predefined groups, the positive and negative switch groups, as illustrated in Fig. 4. A switch is randomly selected from the suspected faulty group and isolated. The remaining switches are then activated using Fault Detection Pulses (FDP) and it will generates new $v_e^*(t)$. Now, if $(v_e^*(t) - v_o(t)) < \tau$, it confirms either gate misfiring of the switch or locating a faulty switch. Otherwise, another switch is selected, and the process is repeated until the defective switch is found. For an M+1 cell IFFT, the maximum number of FDP applied is M+1.

C. Fault Verification

At this stage, the faulty switch undergoes a second time FI and FL process. If the same switch is not identified in the FI stage for the second time, then it will be treated as gate misfiring, and then the system will go into normal operation. If the same switch is identified and, it will be forwarded from FI stage to FL stage. If it successfully completes the FL process and confirms the fault switch, it will be isolated. Once the faulty switch is isolated immediately, the corresponding redundant switch will be activated. Most of the switches can complete the whole FI, FL, and FV process within a quarter cycle of the output voltage waveform. However, a few switches take more than a quarter cycle of the output voltage waveform since they are working with high voltage levels.

IV. SIMULATION RESULTS

The proposed IFFT is validated using MATLAB/Simulink software. The simulation parameters such as input supply, number of cells, transformer turns ratio, sampling time, operating frequency, and loads are shown in Table V. The simulation results are confirming the robustness of the proposed configuration with novel control technique as follows by considering symmetrical (seven-level) and asymmetrical (11-level) operation.

Fig. 5 illustrates the characteristics of the load voltage, load current, and gate pulses of the switches when a fault occurs in a cell. A switch fault occurs in S_1 at 0.033 s as shown in Fig. 5(a). The proposed fault-tolerant methodology initiates the Fault Identification (FI) procedure to pinpoint the faulty switch. Once identified, the Fault Localization (FL) procedure is

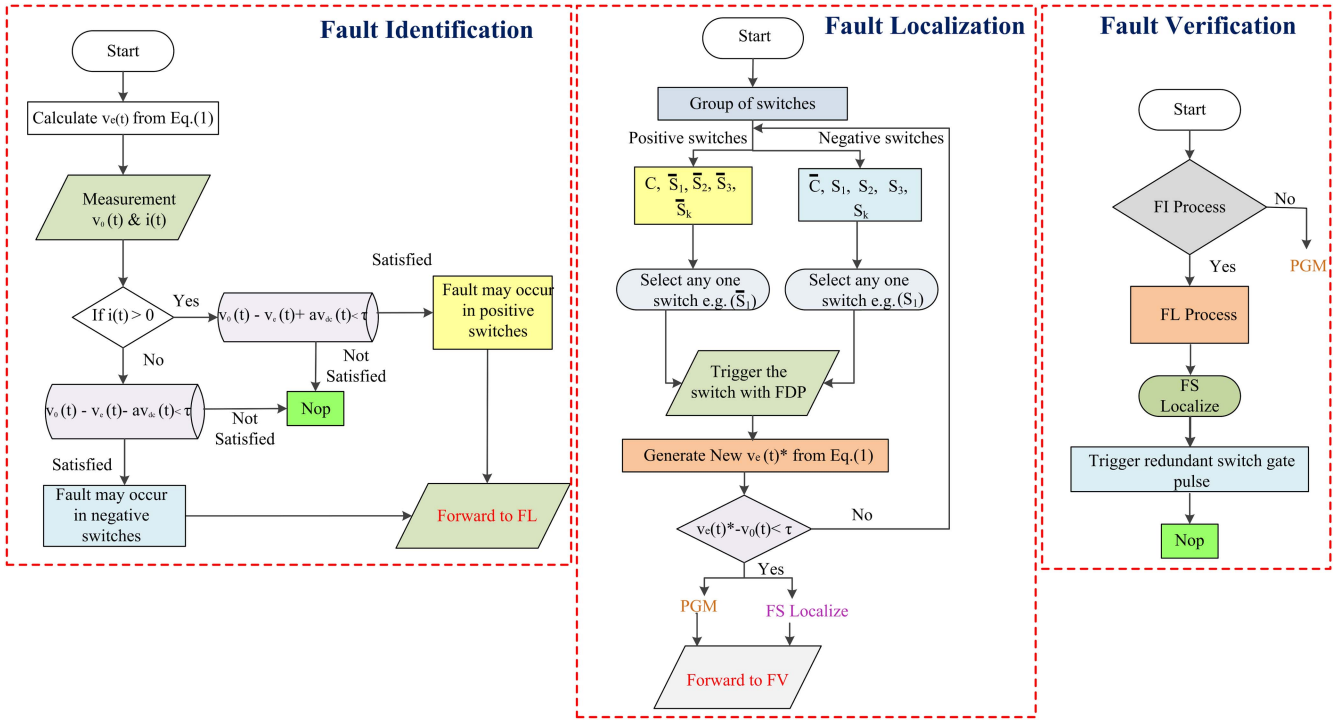

Fig. 4. Flowchart of the proposed methodology.

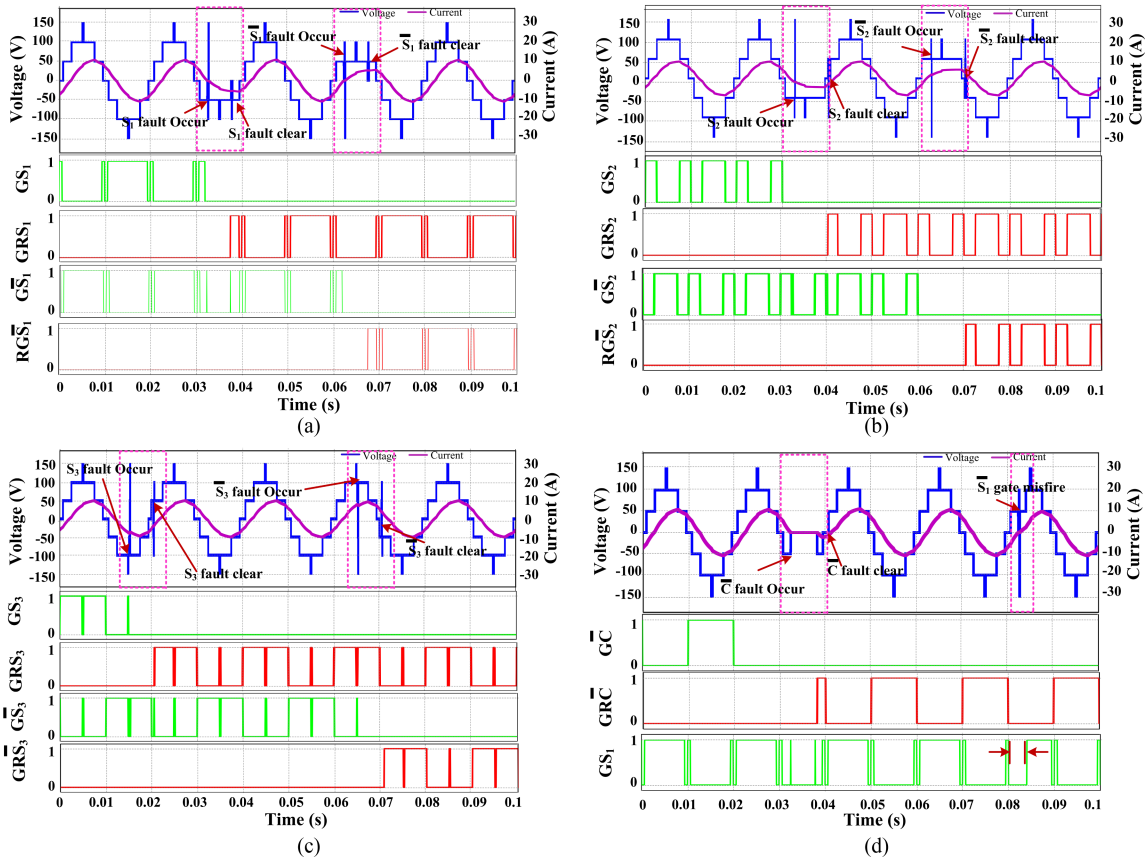

Fig. 5. Characteristics of the load voltage, load current of the proposed topology when fault occurs in (a) S_1, and $\overline{S_1}$, (b) S_2, and $\overline{S_2}$,(c) S_3, and $\overline{S_3}$,(d) when the fault occur in $\overline{C}$, and gate misfire occurs at $\overline{S_1}$.

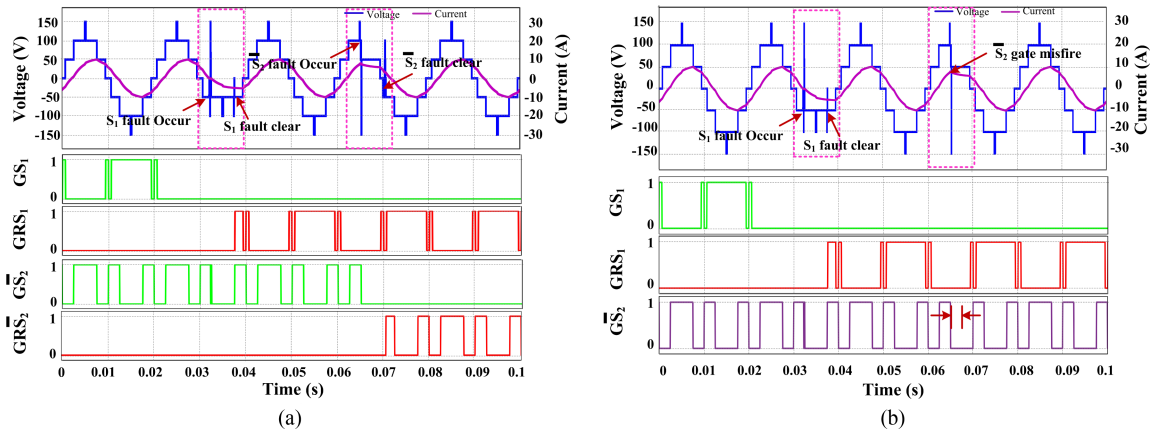

Fig. 6. Characteristics of the load voltage, load current when fault occur in different cell (a) S_1, and $\overline{S_2}$when the fault occur in S1 and gate misfire occurs at $\overline{S_2}$. (a) when fault occur in different cells S_1, and S_2, (b) when the fault occur in $_1$ and gate misfire occurs at $_2$

triggered. A test pulse (FDP) is activated in place of GS_1, and the FI and FL procedures are repeated to verify the fault location. Upon confirmation, the corresponding redundant switch RS_1 gate pulses GRS_1 are activated at 0.038 s. Similarly, Fig. 5(b) and 5(c) depict fault events and their clearance for the remaining switches (S_2, $\overline{S_2}$, S_3, and $\overline{S_3}$). Fig. 5(d) presents fault scenarios and their mitigation for the common cell, including gate misfire cases.

Fig. 6 illustrates the characteristics of the load voltage, load current, and gate pulses of the switches when a fault occurs in different cells. A switch fault occurs in S_1 at 0.033 s and is cleared at 0.038 s and the second fault occurs at switch $\overline{S_2}$ at 0.064 s which is cleared at 0.068 seconds. As stated in the previous cases, the redundant switches RS_1, $R\overline{S_2}$ will be activated once the faults are confirmed as depicted in Fig. 6(a). Similarly, Fig. 6(b) presents fault scenarios and their mitigation for the a cell, including gate misfire cases.

Fig. 7 illustrates the characteristics of the load voltage, load current, motor speed, torque and gate pulses of the switches pre and postfault conditions as similarly to the previous cases. Herein, the single phase induction motor is treated as load, 62 V is considered as input voltage, and turns ratios of transformers are considered as 1:1, 1:1, 1:3. At instant of 0.45 the motor is loaded and faults are occurred at different intervals like 0.6 s and 1.05 s. From speed waveform, it may be observed that the speed is maintained constant at pre and postfault conditions.

V. Experimental Results

The experimental validation of the proposed work is verified with the hardware parameters as mentioned in Table VI. In this work, Programmable dc Source (IT6006C-800-25(800 V,25 A)) is used for the dc power supply, and OP4510 serves solely as the controller. The proposed fault-tolerant technique is demonstrated using the 11- level asymmetrical configuration. However it can be validated with any level of the proposed topology. Fig. 8 illustrates the hardware characteristics of the load voltage,

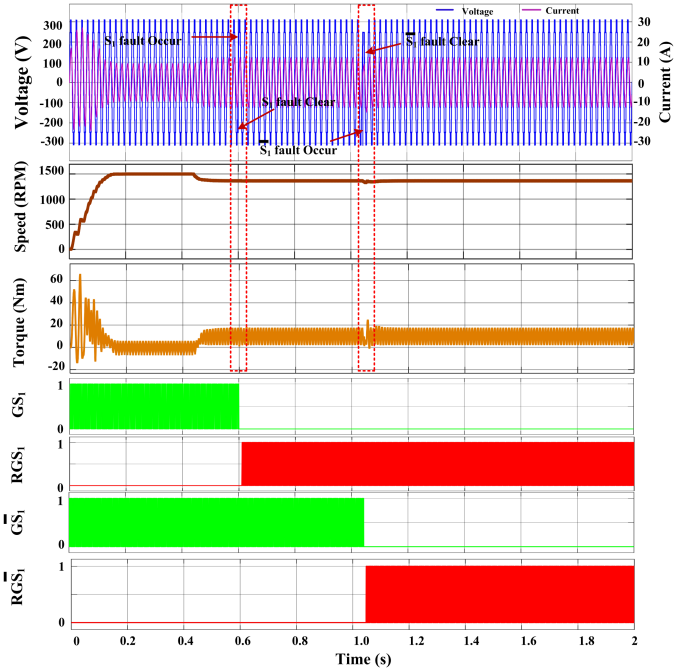

Fig. 7. Characteristics of the load voltage, load current, motor speed, and torque of the proposed topology when fault occur in S_1, and $\overline{S_1}$.

TABLE VI
Hardware Parameters

Parameters	Quantity
IT6006C-800-25(800V,25A)	1
Transformers (167VA, 230V)	3
SKM75GB12T4(75A, 1200V)	8
Voltage Sensor (LV25P-723159)	1
Current Sensor (LA55-P17229)	1
Optocoupler (TLP350)	16
$Load_1(300W)$	R= 170Ω
$Load_2(150W)$	R= 170Ω; L = 575mH
$Load_3(75W)$	Standard ceiling fan

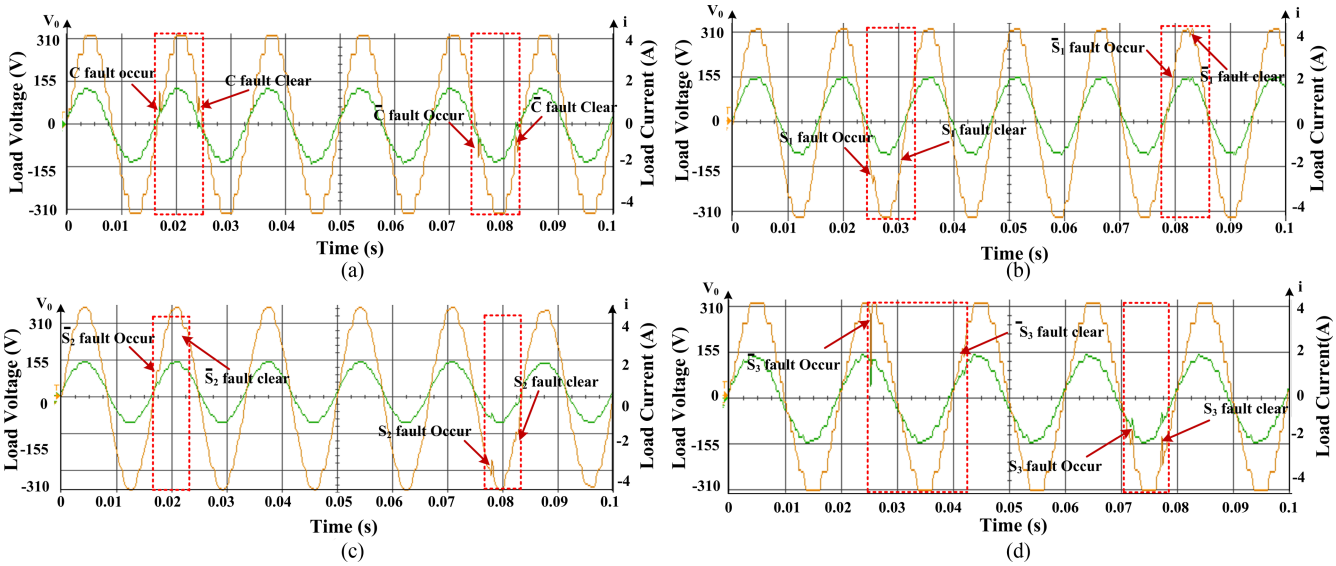

Fig. 8. Hardware Characteristics of the load voltage, load current of the proposed topology with R-load when fault occurs in(a) C, and $\overline{C}$,(b) S_1, and $\overline{S_1}$, (c) S_2, and $\overline{S_2}$,(d) S_3, and $\overline{S_3}$.

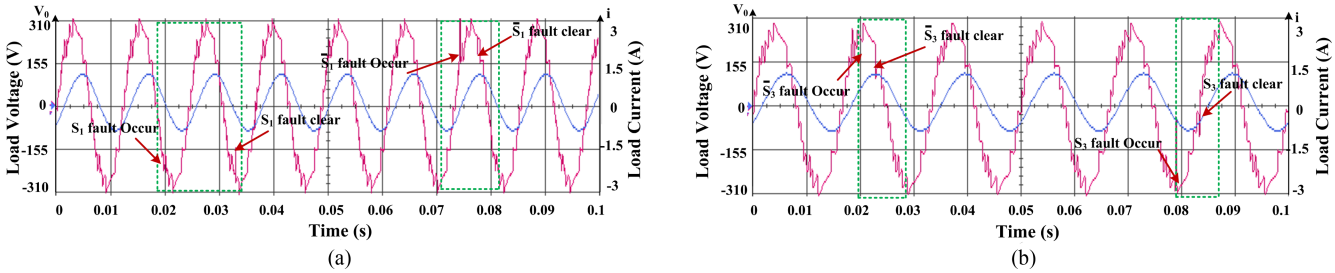

Fig. 9. Hardware Characteristics of the load voltage, load current of the proposed topology with RL-load when fault occurs in(a) S_1, and $\overline{S_1}$, (b) S_3, and $\overline{S_3}$.

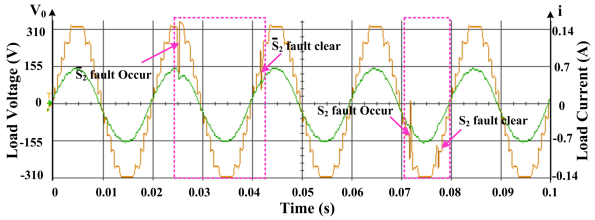

Fig. 10. Hardware Characteristics of the load voltage, load current of the proposed topology with Fan load when fault occurs in S_2, and $\overline{S_2}$.

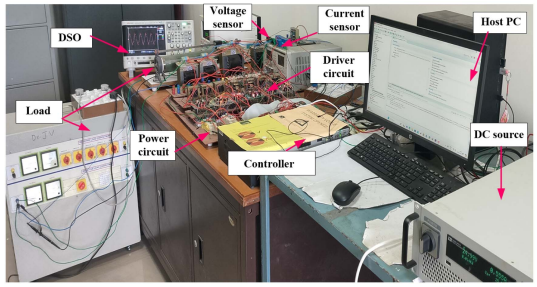

Fig. 11. Experimental setup of the proposed configuration.

load current of the proposed topology with R-load. The fault in C occurred at 0.017 s and cleared at 0.025 s and second fault occur in $\overline{C}$) at 0.075 s and cleared at 0.082 s as shown in Fig. 8(a).

Similarly, Fig. 8(b), (c), and (d) depict fault events and their clearance for the remaining switches (S_1, $\overline{S_1}$, S_2, $\overline{S_2}$, S_3, and $\overline{S_3}$).

Fig. 9 illustrates the hardware characteristics of the load voltage, load current of the proposed topology with RL-load. The fault in S_1 occurred at 0.02 s and cleared at 0.032 s and second fault occur in $\overline{S_1}$) at 0.072 s and cleared at 0.078 s as shown in Fig. 9(a). Similarly, Fig. 9(b) depict fault events and their clearance for the switches S_3, $\overline{S_3}$. Fig. 10 presents the experimental voltage and current waveforms of standard ceiling fan load under pre and postfault conditions as similarly to the previous cases.

Table VII is describing the superiority of the proposed method over existing methods interms of the fast detection, addressing multiple faults without any deviation in input voltage and modulation signal, and fault verification. The experimental prototype is depicted in Fig. 11.

TABLE VII
COMPARATIVE ANALYSIS OF THE PROPOSED METHODOLOGY WITH WELL-ESTABLISHED FAULT TOLERANT TECHNIQUE IN THE LITERATURE

Ref.	SPP		Detection Time	Detection Capability	Post Fault Discussion	DC voltage increases	Modulation signal modification	Carrier phase shifted angle modification	Complex	FV
	V	i								
[16]	1	1	$<$ 3FC	single switch	No	No	No	No	Moderate	No
[18]	1	-	$<$1 FC	Cell	No	-	Yes	-	High	-
[19]	3	-	$<$3 FC	multiple switch	No	-	-	-	High	-
[20]	1	-	$<$1 FC	Multiple switch	Same as a pre-fault rating but not level	Yes	Yes	Yes	Moderate	-
[21]	1	1	$<$1 FC	Single switch	Same as pre-fault voltage	No	No	No	Low	Yes
[25]	1	1	3FC	Single switch	2/3 of pre-fault voltage	No	Yes	No	Low	-
[26]	-	-	5FC	Multiple switch	Same as a pre-fault rating but not level	No	Yes	No	Moderate	-
[29]	-	-	3FC	Multiple switch	Same as a pre-fault rating but not level	No	Yes	No	Moderate	-
[30]	-	-	Not specified	Single switch	Same as a pre-fault rating but not level	No	Yes	No	Moderate	-
PM	1	1	$<$1 FC	Multiple switch	Same as pre-fault voltage	No	No	No	Low	Yes

VI. CONCLUSION

This article presented an isolated fully fault-tolerant configuration for single phase grid connected and constant speed applications with an optimized device count. The proposed fast fault-tolerant methodology is validated using the proposed (symmetrical and asymmetrical) configuration. The performance of the proposed work is simulated with a RL-load and Motor load using MATLAB simulink. The experimental validation is done with different power ratings and loads such as R, RL, and standard ceiling fan. The simulation results, experimental results and comparative analysis are confirmed that the fault identification, localization, verification, prefault and postfault operation were executed more quickly compared to existing literature irrespective. Moreover the methodology is independent of the switching technique.

ACKNOWLEDGMENT

Thanked by the authors for providing support.

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