A High-Efficiency Dual-Mode DC–DC Converter With a Low-Cost Seamless Transition Scheme

Yun Hao, Xukun Wang, Zhigang Han, Chunli Huang, Huikai Xie, *Fellow, IEEE*, and Bo Zhou

***Abstract*—A low-complexity pulsewidth modulation/ pulse skipping modulation (PWM/PSM) dual-mode buck dc–dc converter is proposed. The converter operates in PWM with a 1.5-MHz switching frequency in heavy load scenarios and switches to PSM with a sliding switching frequency under light load conditions, ensuring a high efficiency over a wide load range. Based on peak current mode control, only one simple voltage detector is required to regulate the converter for different loads, which significantly reduces the circuit complexity for a seamless mode transition. Fabricated in 180-nm BCD technology, the total chip area is less than 0.28 mm^2 and the quiescent current is lower than 90 μA. The converter achieves the efficiencies up to 93.65% for PWM scheme and more than 80.61% in PSM mode, respectively, with the input voltage of 4.0–5.5 V and the load current up to 1.2 A. Additionally, the presented design achieves a line regulation less than 0.18% and a load regulation lower than 0.98%, and also accomplishes a voltage variation of 3.49%/A for load current transient response and gets an attractive figure of merit.**

***Index Terms*—Buck, dc–dc converter, high efficiency, low complexity, pulse skipping modulation (PSM), pulsewidth modulation (PWM), seamless mode transition.**

I. Introduction

With the growth of the Internet of Things in the intelligent life, dc–dc converters with small size, high efficiency, and wide load range, are an attractive prospect for applications such as portable and wearable electronic devices, and are also used in power management for SoC [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. The traditional pulsewidth modulation (PWM) operation of dc–dc converters [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12] is extensively used in heavy loads, but lacks of the benefits in light load scenarios due to the dominant switching losses. The pulse frequency modulation (PFM) scheme [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14] improves the conversion efficiency in light load scenarios by reducing the switching frequency F_{SW}, however, it necessitates complicated control circuits. The constant on-time scheme is also helpful to lower the switching frequency for light loads, but suffers from subharmonic oscillations and electromagnetic interference (EMI) problems [14], [15], [16]. The pulse skipping modulation (PSM) mechanism is widely employed in commercial dc–dc converters, which utilizes the constant F_{SW} and skips cycles during a clock period in light load cases to avoid harmonic oscillations and EMI issues, but still requires a complicated control circuit [6], [17], [18].

To achieve a high conversion efficiency over a wide load range, a combination of multiple control methods is needed. Dynamic load current variations present in all practical systems require a seamless transition in dual or multiple modes [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. Therefore, dual- or multimode operation is utilized by the mainstream converters, which automatically adjusts the F_{SW} according to the load current I_{Load}. The existing buck converters [6], [7], [8], [9], operate in PWM mode with a fixed F_{SW} for heavy loads, and PSM / double clock time (DCT) / PFM / advanced burst mode (ABM) for light ones, to obtain high conversion efficiency over a wide load range. However, the additional mode controllers that are totally different from the PWM ones, inevitably cause an ultrahigh hardware complexity. Besides, due to the delay time caused by the mode swapping, the seamless mode transition is difficult to achieve and the probability of switching glitches is increased.

The comparator reused scheme proposed in [1] makes the automatic regulation under various load conditions. However, the switching of comparison voltages is prone to the undesired glitches. In the converters [3], [5], an adaptive on-time (AOT) control is widely employed to reduce the switching losses by automatically switching to PFM mode when the load current decreases. It also allows a seamless transition between PWM and PFM mode, while another challenge is the difficulty in maintaining high efficiency at light loads, where the quiescent current of the control circuitry becomes dominant. Besides, additional control circuitry such as a complex sleep-time detector or an AOT generator, is required to extends the AOT operation into light load range with high efficiency and good ripple performance, which inversely complicates the control algorithm. The converter [4] with a load current prediction scheme achieved by an extra mode selector, conducts a load-dependent seamless mode transition among PWM, PFM, and multiple-sawtooth PWM (MSPWM). While MSPWM mode uses relatively low and

Received 2 February 2025; accepted 25 February 2025. Date of publication 3 March 2025; date of current version 30 June 2025. This work was supported by the National Natural Science Foundation of China under Grant 62474020. Recommended for publication by Associate Editor H. H.-C. Iu. *(Corresponding author: Bo Zhou.)*

Yun Hao, Xukun Wang, Chunli Huang, Huikai Xie, and Bo Zhou are with the School of Integrated Circuits and Electronics, Beijing Institute of Technology, Beijing 100081, China (e-mail: 3120231366@bit.edu.cn; 3220231937@bit.edu.cn; 3120241404@bit.edu.cn; hk.xie@bit.edu.cn; zhou bo07@bit.edu.cn).

Zhigang Han is with the Shanghai TX Semiconductor Sci.-Tech. Company Ltd., Shanghai 201210, China (e-mail: zhghan@txsemi.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3547857.

Digital Object Identifier 10.1109/TPEL.2025.3547857

fixed switching frequency to obtain high efficiency, but degrades output ripple, and the additional control circuitry is required. The semi-digital converter [11] based on triple comparators is indeed regarded as low-cost low-power implementation, with a high light-load efficiency and simplified control operation, but has a limited load current. Additionally, digitalized dc–dc converters [19], [20], [21], [22], [23] utilize digital modulators to improve conversion efficiency with the optimized control algorithm. However, an analog-to-digital and a digital-to-analog converters, or a delay-locked loop, are necessary in these converters.

In conclusion, the majority of the reported converters, either utilize multiple controllers for the dynamic F_{SW}, or rely on additional modules for seamless mode transition. To aim at the low-complexity and high-efficiency application scenarios, the buck converter needs a simplified multi-mode controller with a dynamic switching technique and a seamless transition scheme, which is focused on here.

A low-cost dual-mode buck dc–dc converter with only a single mode controller, is proposed to save silicon area and obtain a high efficiency over a wide load range. In heavy loads, the switching frequency can be quasi-fixed in the continuous conduction mode (CCM) as PWM control. And under light ones, the proposed scheme works in discontinuous conduction mode (DCM) and behaves as PSM control with skipping clock cycles for a dynamic switching frequency. Based on the peak current mode control (PCMC), the output voltage of the error amplifier (EA) is monitored to enable the seamless mode transition between PWM and PSM. The proposed converter not only avoids a complicated multi-mode controller, but eliminates the additional complex unit for mode transition.

The rest of this article is organized as follows. Section II shows the proposed dual-mode structure with a low-complexity seamless transition scheme for dynamic F_{SW}, and Section III presents the detailed circuit implementations and the mode-switching mechanism, followed by experimental results in Section IV. Finally, Section V concludes this article.

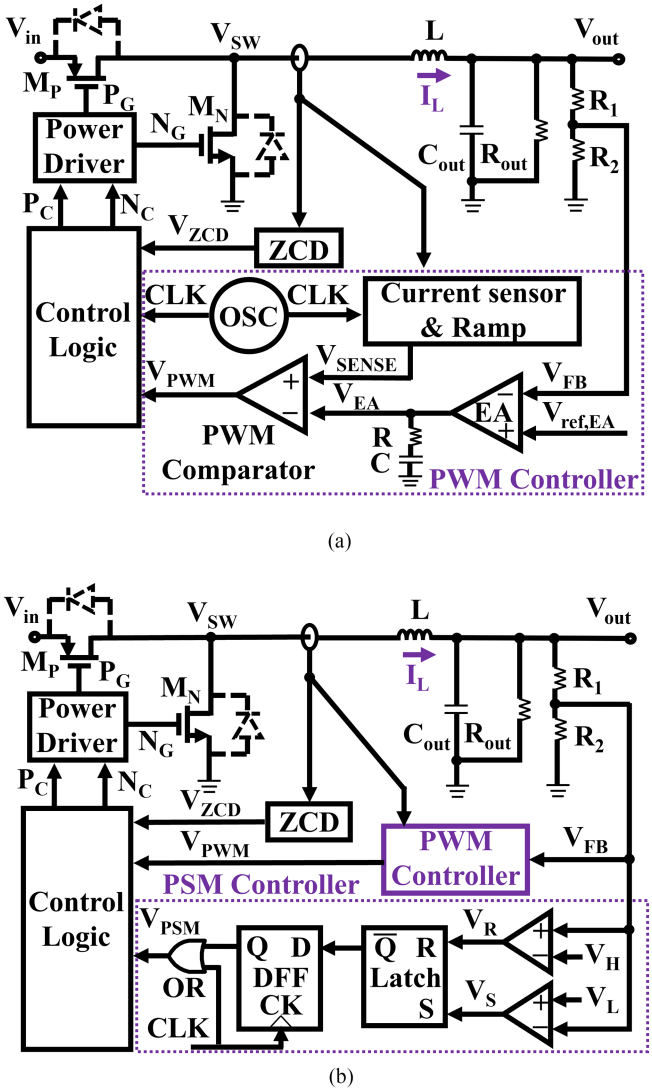


Fig. 1. Conventional buck converter structures. (a) PCMC buck with PWM mode. (b) Dual-mode buck with PWM/PSM operations.

II. Converter Architecture

A. Existing Structures

The conventional PCMC based buck converter with PWM mode is shown in Fig. 1(a). A current sensor with slope (ramp) compensation, and a voltage loop mainly consisting of a PWM comparator and an EA, which make up a PWM controller, conduct the PCMC operation to regulate the converter. The essence of PCMC is to ensure that the output voltage V_{EA} of the EA tracks the inductor current I_L well, by comparing V_{SENSE} with V_{EA} to generate V_{PWM}. The oscillator (OSC) provides the clock signal (CLK) and initiates the switching period, which combines with the comparator output V_{PWM} to periodically turn on/off the high-side and low-side power transistors M_P/M_N.

However, the single PWM mode is not attractive to light loads. Therefore, the traditional dual-mode buck converter is illustrated in Fig. 1(b). In addition to the PWM controller for heavy loads, an additional PSM controller is adopted for light loads. When the output voltage V_{out} rises so that the feedback voltage V_{FB} is higher than the reference voltage V_H, the output voltage V_R of the hysteresis comparator goes high, and the control signal V_{PSM} is high to skip the CLK cycles. Conversely, when V_{out} decreases and V_{FB} is lower than the reference voltage V_L, the output voltage V_S of the hysteresis comparator is high, as a result, the power stage is driven at a constant CLK frequency. That is, the hysteresis comparators with the output voltage detection, conduct the PSM operation. When the inductor current I_L is close to zero, the zero-current detector (ZCD) disables the power stage until the next clock cycle. The dual-mode converter needs dual (PWM and PSM) controllers, which complicates the hardware implementation. In addition, the hysteresis window inevitably degrades mode-transition continuity between PWM and PSM.

B. Proposed Architecture

PWM and PSM modes maintain high efficiencies at heavy and light load scenarios, respectively. Dynamic variations in load

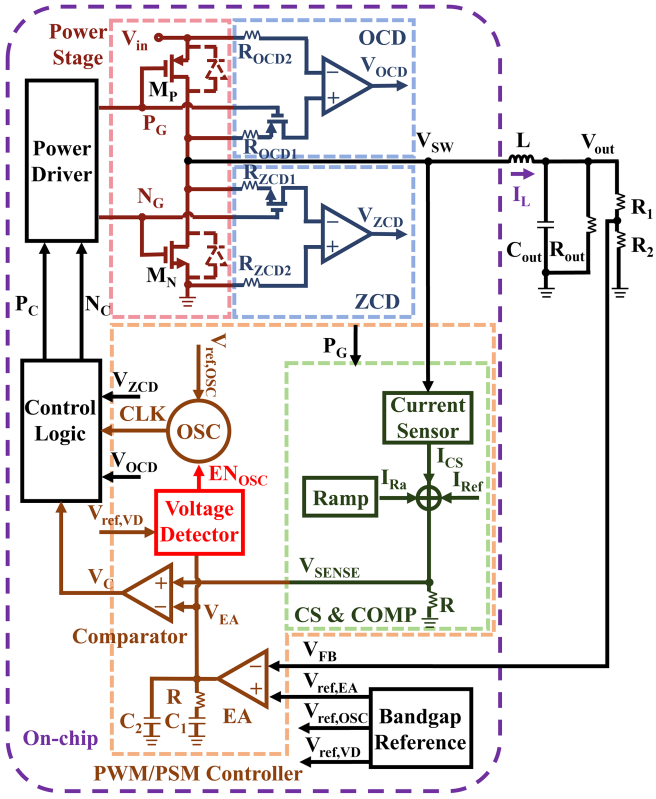


Fig. 2. Proposed PWM/PSM dual-mode architecture with low-cost seamless transition scheme.

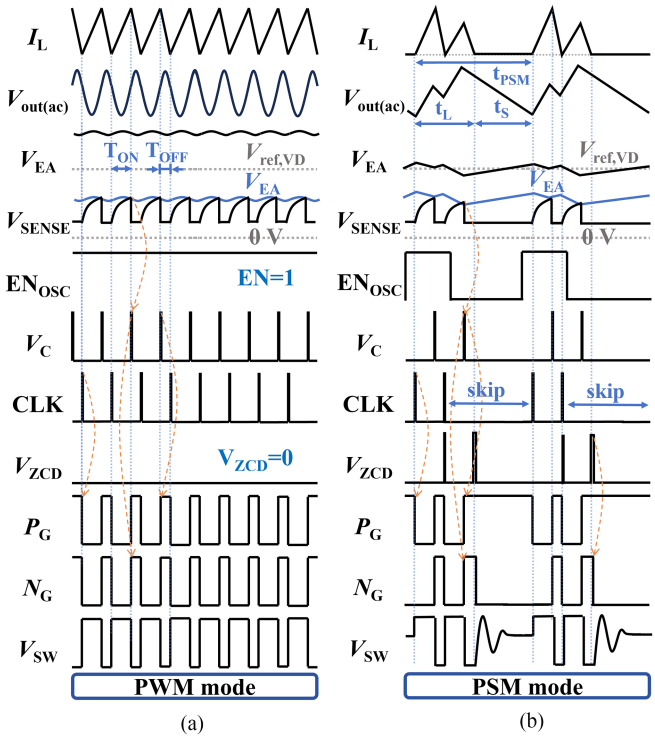


Fig. 3. Operation principles of the proposed converter. (a) Pulsewidth modulation. (b) Pulse skipping modulation.

current also necessitate the seamless mode transition between PWM and PSM. Fig. 2 illustrates the proposed architecture of the dual-mode buck converter based on the PCMC operation, to implement a load-dependent seamless mode transition. Considering the converter output voltage $V_{\rm out}$ under heavy loads is slightly lower than that in light loads, which means the EA output voltage $V_{\rm EA}$ is higher than or close to $V_{\rm ref,VD}$ under heavy or light loads, respectively. Therefore, $V_{\rm EA}$ is monitored and compared to $V_{\rm ref,VD}$ via a simplified comparator based voltage detector (VD), to generate a digital control signal $\rm EN_{OSC}$, which achieves the seamless mode transition by activating or disabling the OSC. Thus, only a single controller is required for dual-mode operation, and the VD conducts auto-switching between PWM and PSM modes, which obviously differs from the existing literature.

Compared to the traditional structure as depicted in Fig. 1(a), only a VD module is added for multi-mode control, and an over-current detector (OCD) serves as a protection module. In comparison to the conventional topology as shown in Fig. 1(b), the single-comparator-based VD module functionally replaces of the complex PSM controller with dual comparators, and determines the operation modes in accordance with the status of $V_{\rm EA}$, as well as enables / disables the OSC for the load-dependent switching frequency. Therefore, the mode transition is optimized from discreteness to continuity and no additional control circuit is required. Moreover, dual feedback (inner current and outer voltage) loops ensure that the output ripple and voltage accuracy of the converter are not sacrificed in different load condition.

The proposed architecture comprises of a control logic, a power driver, a power stage, a PWM/PSM controller, a ZCD, and an OCD, followed by the external resistive-feedback and lowpass LC filtering networks. The mode controller consists of the controller core (an EA with frequency compensation components $(R/C_1/C_2)$, a comparator, a VD, an OSC) and a current sensor with a ramp generator for slope compensation. The sawtooth voltage $V_{\rm SENSE}$ representing of both the inductor current I_L and the slope (ramp) compensation, is compared to the EA output voltage $V_{\rm EA}$ that is inversely proportional to the feedback voltage $V_{\rm FB}$, to determine the appropriate duty cycle operation of the power stage. Besides, $V_{\rm EA}$ is compared to the threshold voltage $V_{\rm ref,VD}$ via the VD, to determine the OSC operation between continuous and intermittent statuses and thus perform PWM or PSM mode. The ZCD detects the approximate zero inductor current and disables the power stage for DCM, to prevent the reverse conduction current of M_N parasitic body diode. The OCD serves as a protection module to avoid the on-time pulse current being extended to the inductor saturation current at the damaging levels, during short-circuit or over-current cases

$$V_{\rm out,CCM} = d_{\rm CCM} V_{\rm in} = V_{\rm in} T_{\rm ON}/(T_{\rm ON} + T_{\rm OFF}). \quad (1)$$

The operation principles of the proposed converter are illustrated in Fig. 3, with PWM and PSM modes, respectively. In PWM mode, I_L is large enough for the converter to operate in CCM. Both the power-stage duty cycle $d_{\rm CCM}$ and the output

voltage V_{out} are depicted in (1). Here, T_{ON} and T_{OFF} are the rising and falling slots of the inductor current. V_{EA} is not less than V_{SENSE} that is proportional to I_L during T_{ON} period. Under heavy loads, V_{EA} is higher than $V_{\text{ref,VD}}$ (0.46 V), the OSC remains activated and the converter continuously works in PWM mode. The CLK pulse makes M_P ON and M_N OFF, which increases I_L during T_{ON} slot. As a result, V_{SENSE} goes up with I_L and is compared to V_{EA}, to generate a narrow pulse signal V_C to turn M_P OFF and M_N ON, which makes the power stage enter T_{OFF} period. That is, both CLK and V_C periodically manage the power stage via the control logic. Since there is always current through the external inductor L (=4.7 μH), the switching node voltage (V_{SW}) is negative in T_{OFF}, V_{ZCD} remains logic low. The power stage operates at a constant frequency with a typical value of 1.5 MHz, which is a tradeoff between conversion efficiency and output ripple.

Under light loads, the converter will get into DCM from CCM, and V_{out} follows (2) with a duty cycle of d_{DCM}. Initially assuming $V_{\text{EA}} < V_{\text{ref,VD}}$ in the light loads, as shown in Fig. 3(b), the VD disables the OSC, the converter thus enters the pulse skipping state and then the power stage is OFF, which inversely reduces F_{SW}. During skipping period t_S, V_{out} and V_{FB} decrease to make V_{EA} more than $V_{\text{ref,VD}}$ and activate the OSC again. As a result, V_{out} and V_{FB} grow up and V_{EA} is smaller than $V_{\text{ref,VD}}$ again. That is, once I_L drops to cause V_{EA} close to $V_{\text{ref,VD}}$, V_{EA} fluctuates around $V_{\text{ref,VD}}$. Once I_L decreases to zero, to avoid the inverse current of I_L, the ZCD is introduced to disable the power stage. Thus, within t_S period, M_P-M_N are OFF and I_L is damped to zero, and C_{out} is discharged to provide I_{Load}

$$V_{\text{out,DCM}} = 2V_{\text{in}} \Big/ \left(1 + \sqrt{1 + (8LF_{\text{SW}})/(R_{\text{out}} {d_{\text{DCM}}}^2)}\right). \tag{2}$$

$$F_{\text{SW}} = \begin{cases} 1.5\,\text{MHz} & \text{PWM} \\ \frac{1}{t_{\text{PSM}}} = \frac{1}{t_L + t_S}, t_S \propto \frac{1}{I_{\text{Load}}} & \text{PSM} \end{cases}$$

$$\Delta V_{\text{out}} = \frac{1}{C_{\text{out}}} \int_0^{T_{\text{ring}}} I_L dt \propto \frac{1}{C_{\text{out}}} \int_0^{1/I_{\text{Load}}} I_L dt. \tag{3}$$

The PSM period t_{PSM} is defined as the summary of the inductor-charging/discharging time t_L and the pulse-skipping time t_S. The t_S is decided by I_{Load} and thus the switching frequency F_{SW} varies with the load condition. The output ripple voltage ΔV_{out} is also affected by the I_L ring duration T_{ring}, which is related to I_{Load}. The relationship between F_{SW}, ΔV_{out}, and I_{Load}, is given in (3). Here, C_{out} (= 15 μF) is the output capacitor. The power stage operates at the PSM mode with a varying F_{SW} less than 1.5 MHz, and conducts at the PWM mode with a fixed F_{SW} of 1.5 MHz. ΔV_{out} increases and F_{SW} decreases, as I_{Load} goes down, and vice versa.

Fig. 4 gives the state diagram of the proposed converter, to reflect the detailed function of the control logic. In each ripple period, the power stage has three alternate work statuses: charging; discharging; and pulse-skipping, where M_P and M_N are ON or OFF sequentially controlled by P_G/N_G from the power driver, and are thus determined by four paths of digital signals (CLK/V_C/V_{ZCD}/V_{OCD}). The charging status (M_P ON and M_N OFF) is triggered by CLK and ended by V_C. The discharging one (M_P OFF and M_N ON) is enabled by V_C and ended by CLK or V_{ZCD}. The pulse-skipping one (M_P OFF and M_N OFF) is activated by V_{ZCD} and disabled by CLK. During short-circuit or over-current conditions, ahead of V_C, V_{OCD} turns M_P OFF.

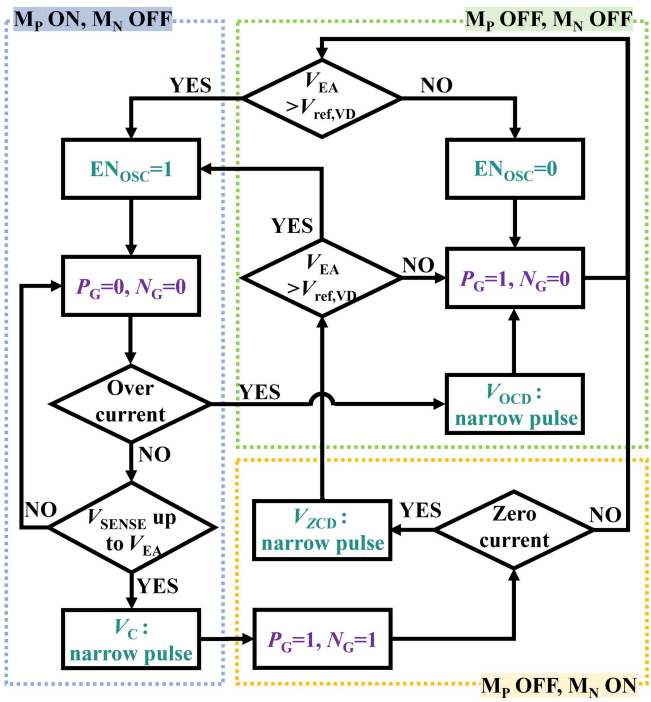


Fig. 4. State diagram of the proposed converter.

C. Architecture Merits

Based on a single controller, the structure only introduces a simplified VD to control the OSC, to achieve dual-mode operation and conduct a load-dependent seamless mode transition, with low-cost high-efficient features, which avoids the traditional multi-mode controllers or complex units.

III. Circuit Implementation

The main modules include a mode controller core, a current sensor with the slope compensation, zero- and over-current detectors, and a power driver followed by a power stage, which are clearly clarified below. Additionally, the mode-switching scheme is addressed.

A. Controller Core for PWM/PSM

The proposed mode controller is shown in Fig. 5, which consists of an EA, a comparator, a VD, and an OSC. To ensure the loop stability and enhance the transient response feature, the EA is followed by a type-II network ($R/C_1/C_2$) serving as the frequency compensation. The converter loop transfer function is expressed in (4). Here, $g_{m,\text{EA}}$, C_{EA}, R_{EA} are the transconductance, output capacitance and output resistance of the EA, respectively. A_0, f_z, f_{p1}, and f_{p2} are the dc gain, zero

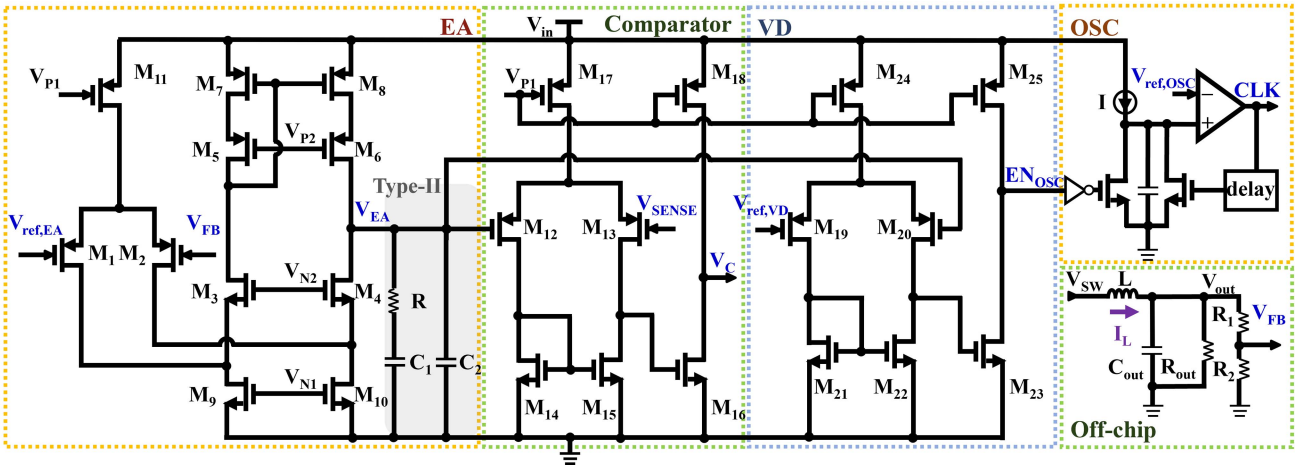


Fig. 5. Proposed controller core for PWM/PSM modes.

and poles of the voltage loop, respectively,

$$\frac{V_{\rm EA}}{V_{\rm out}} = -A_0 \frac{1+s/(2\pi f_z)}{[1+s/(2\pi f_{p1})][1+s/(2\pi f_{p2})]}$$
$$A_0 = \frac{A_{\rm EA}R_2}{R_1+R_2} = \frac{g_{m,\rm EA}R_{\rm EA}R_2}{R_1+R_2} = 47\text{dB}$$
$$f_{p2} = -1/[2\pi(R//R_{\rm EA})(C_2+C_{\rm EA})] = -1.05\ \text{MHz}$$
$$f_{p1} = -1/(2\pi R_{\rm EA}C_1) = -200\ \text{Hz}$$
$$f_z = -1/(2\pi RC_1) \quad = -31\ \text{kHz}. \tag{4}$$

The EA employs the conventional fold-cascode structure to get a high dc gain for good line and load regulations (LDRs). $V_{\rm FB}$ is compared to the reference voltage $V_{\rm ref,EA}$ (0.6 V) to generate an error voltage $V_{\rm EA}$, which is then fed into the sequent comparator and VD for mode control. The comparator employs the traditional two-stage structure to minimize the propagation delay, and compares $V_{\rm SENSE}$ to $V_{\rm EA}$ to generate a pulse signal V_C. The VD also uses the two-stage structure and compares $V_{\rm EA}$ to $V_{\rm ref,VD}$ (0.46 V) to generate the digital control signal $\rm EN_{OSC}$. When $\rm EN_{OSC}$ is high, the OSC is activated and the embedded capacitor starts charging and discharging to generate CLK signal. Once $\rm EN_{OSC}$ is low, the embedded capacitor is bypassed and the OSC stops oscillating until the next $\rm EN_{OSC}$ rising-edge arrives.

B. Current Sensor With a Ramp Generator

Considering the inductor current I_L whose average value corresponds to multiple peak ones with different duty cycles, sub-harmonics oscillation or circuit instability is prone to occurrence. To avoid this, a ramp generator is added to the current sensor circuit, as depicted in Fig. 6. With an aspect ratio k (=1000), the current sensor utilizes a matched PMOS transistor M_{P1} that is much smaller than M_P in the power stage. In order to achieve an accurate current sensing, the negative feedback loop formed by M_1-M_6 is employed to make V_A equal to V_B. As a result, $I_{\rm CS}$ is directly proportional to I_L or set to zero when the control signal P_G is 0 or 1, respectively.

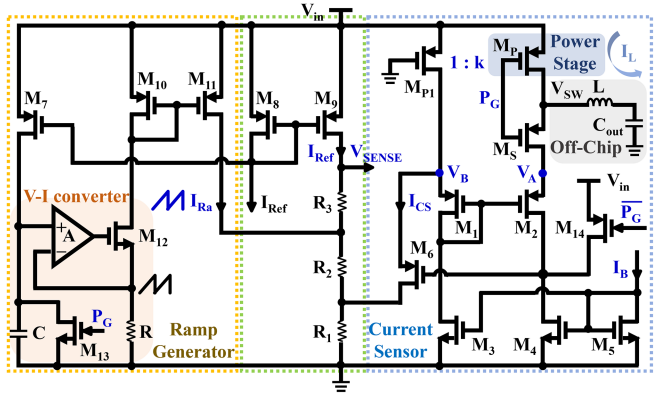


Fig. 6. Proposed current sensor with a ramp generator.

The ramp generator based on a voltage-to-current (V-I) converter and a capacitor charging-discharging unit, is used to produce a slope current $I_{\rm Ra}$. As shown in Fig. 6, three groups of currents, including the sensing current $I_{\rm CS}$, the slope current $I_{\rm Ra}$, and the constant current $I_{\rm Ref}$, are injected into the resistor network (R_1-R_3) for the output voltage $V_{\rm SENSE}$ of the current sensor, which is depicted in (5) and decided by the power-stage control signal P_G. Here, ΔI_L is the inductor ripple current. Besides, the mode-switching points of the inductor and load currents between PWM and PSM are obtained from (5). By choosing the appropriate inductor threshold current $I_{L,\rm threshold}$ (0.12 A) and the perfect load threshold current $I_{\rm Load,threshold}$ (50 mA), the mode threshold voltage $V_{\rm ref,VD}$ (0.46 V) is thus determined

$$\begin{aligned} V_{\rm ref,VD} &= V_{\rm EA,threshold} = V_{\rm SENSE,peak} \\ &= I_{\mathbf{Ref}}(R_1+R_2+R_3)+\overline{P_G}\,[I_{\rm Ra,max}(R_1+R_2)+I_{\rm CS,peak}R_1] \\ &= I_{\mathbf{Ref}}(R_1+R_2+R_3)+I_{\rm Ra,max}(R_1+R_2)+I_{L,\rm threshold}R_1/\text{k} \\ &= 2.2\mu\times(2k+28k+54k)+1.2\mu\times(2k+28k)+\frac{120m\times 2k}{1000} \\ &\approx 0.46\text{V} \\ \Delta I_L &= \frac{V_{\rm out}}{L\times F_{\rm SW}}\times\left(1-\frac{V_{\rm out}}{V_{\rm in}}\right) = \frac{3.38}{4.7\mu\times 1.5M}\left(1-\frac{3.38}{4.75}\right) \\ &= 140\ \text{mA} \\ I_{\rm Load,threshold} &= I_{L,\rm threshold}-0.5\Delta I_L = 120\ m-0.5\times 140\ m \\ &= 50\ \text{mA}. \end{aligned} \tag{5}$$

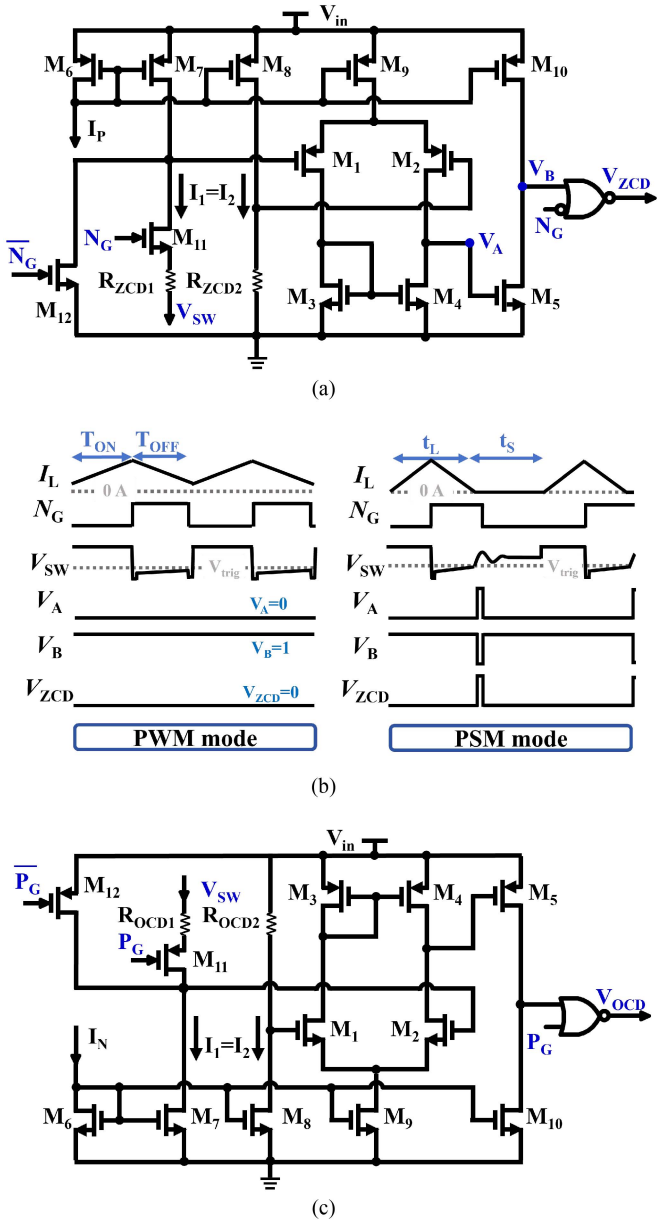


Fig. 7. Protection modules. (a) ZCD schematic. (b) ZCD signal waveforms in PWM and PSM modes. (c) OCD schematic.

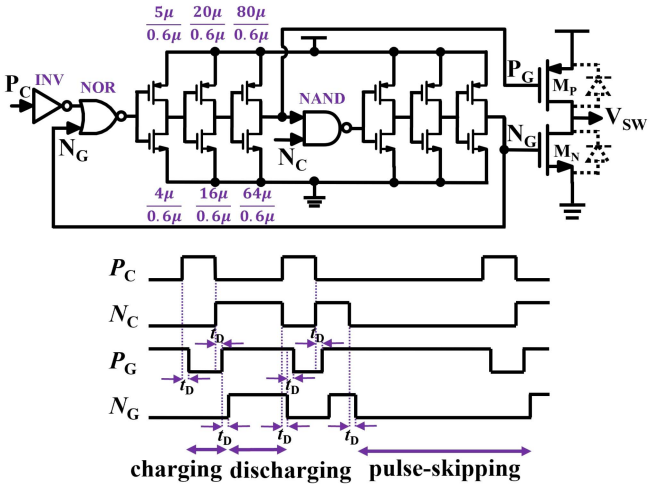


Fig. 8. Proposed power driver and power stage.

C. ZCD and OCD

Since the converter is a synchronous switching operation, the ZCD is essential to block the reverse inductor current in light loads by turning M_N OFF. As shown in Fig. 7(a), the comparator-based ZCD is controlled by the signal N_G. The ZCD is shut down during both the rising time (T_{ON}) and the skipping period (t_S) of inductor current, with the output voltage V_{ZCD} close to zero.

During the falling slots of the inductor current, M_{11} is turned ON and M_{12} is turned OFF by the signal N_G, and the biasing current I_1 is injected into R_{ZCD1} to enable the circuit rapidly. The ZCD begins to detect the inductor reverse current. Two terminal voltages (V_{SW} and GND) of M_N are compared to a trigger window of $V_{\text{trig}} = I_1(R_{\text{ZCD1}} - R_{\text{ZCD2}}) \approx 150\,\text{mV}$, which is inserted to avoid erroneous detections when V_{SW} slightly changes, that is, the hysteresis window improves the detection robustness. As shown in Fig. 7(b), since I_L is greater than zero in PWM mode, V_{SW} is negative in T_{OFF} that makes V_B high, and V_{ZCD} thus maintains logic low. However, when I_L falls below zero in PSM mode, V_{SW} becomes positive to pull V_{ZCD} to logic high, which can turn OFF M_N, and the signal N_G changes to logic low simultaneously. Therefore, the switch M_{11} is turned OFF and the switch M_{12} is turned ON, which inversely disables the ZCD. The output of ZCD is pulled to logic low again to generate a pulse signal V_{ZCD}.

Furthermore, in short-circuit or over-current cases, the on-time pulse current must be prevented from being extended to the inductor saturation current at the damaging levels. Thus, the OCD is implemented by comparing V_{SW} to V_{in} as the on-time being extended. As shown in Fig. 7(c), the OCD based on a two-stage comparator is controlled by the signal P_G. This module is shut down under the falling time (T_{OFF}) and the skipping period (t_S), with the output voltage V_{OCD} close to zero. During the rising slots of I_L, the switch M_{11} is turned ON and M_{12} is turned OFF by the signal P_G, and the OCD is activated. When the inductor current is overshoot, the voltage ($V_{\text{in}} - V_{\text{SW}}$) across the M_P increases and the V_{SW} decreases. Once $V_{\text{in}} - V_{\text{SW}}$ is higher than the value of $I_1(R_{\text{OCD1}} - R_{\text{OCD2}}) \approx 150\,\text{mV}$, V_{OCD} is set to high to turn the power transistor M_P OFF, which inversely makes P_G high to disable the OCD. Therefore, V_{OCD} is also a narrow pulse signal or always zero.

D. Power Driver and Power Stage

As depicted in Fig. 8, the proposed power driver employs two same inverter chains with transistor-size scaled-up by four, to generate the driving signals P_G and N_G for the power stage consisting of large-size transistors M_P-M_N. The dead-zone time t_D with a typical value of 1.5 ns between N_G and P_G, is achieved by these two chains based on three-stage cascaded inverters, to avoid synchronous conduction of M_P and M_N. The

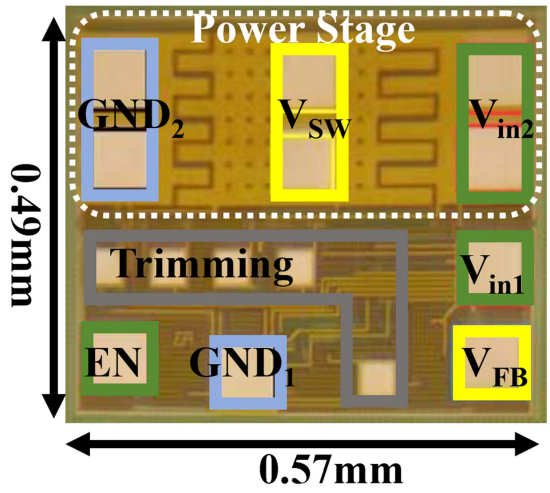


Fig. 9. Chip micrograph in 180-nm BCD.

input signals P_C and N_C from the control logic reflect three alternate statuses as depicted in Fig. 4: charging; discharging; and pulse-skipping.

The power stage only consists of push-pull transistors M_P and M_N, which are driven by the P_G and N_G signals as shown in Fig. 8. The power transistors M_P with the size ratio of 59.9 mm/0.6 μm and M_N with the size ratio of 24.85 mm/0.6 μm, to achieve conduction impedances ($R_{\rm ON}$) less than 0.12 Ω and 0.08 Ω, respectively, which benefit high conversion efficiency.

E. Mode-Switching Mechanism

As depicted in (5), with the inductor ripple current of 140 mA, when the load current is larger or smaller than 50 mA, the inductor peak current is higher or lower than 120 mA, which means the peak value of $V_{\rm SENSE}$ is more or less than 0.46 V. That is, $V_{\rm EA} = V_{\rm SENSE,peak}$ is higher or lower than $V_{\rm ref,VD}$ (0.46 V), so the VD output signal $\rm EN_{OSC}$ is always or no longer always at high level, which inversely makes the OSC always activated or alternately enabled / disabled. Therefore, the converter conducts mode switching between PWM and PSM, based on 50-mA load current threshold.

IV. Experimental Results

The proposed PWM/PSM dual-mode converter with a low-complexity seamless transition scheme is fabricated in 180-nm BCD technology. The converter quiescent current is lower than 90 μA. Fig. 9 gives the chip micrograph of the prototype buck dc–dc converter, where all the pads of the power and IO are clearly demonstrated, with the silicon size of 0.49 mm $\times$ 0.57 mm. The power stage occupies nearly 50% of hardware size. There are two sets of power supplies $V_{\rm in2}$ and $V_{\rm in1}$, and grounds $\rm GND_2$ and $\rm GND_1$, which are used for the power stage and the rest sub-modules of the converter, respectively. The trimming pads are used for the bandgap circuit to ensure high-precision reference voltages. The $V_{\rm SW}$ are connected to the off-chip *LC* low-passed filter, $V_{\rm FB}$ is the resistive subvision of $V_{\rm out}$, and EN is for chip enable signal and connected to $V_{\rm in}$.

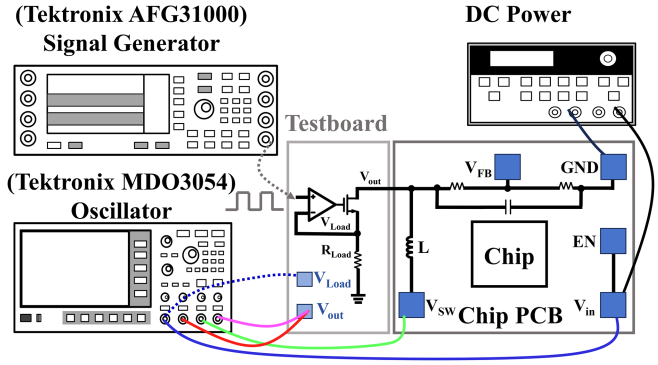


Fig. 10. Experimental setup for testing the DC–DC converter chip.

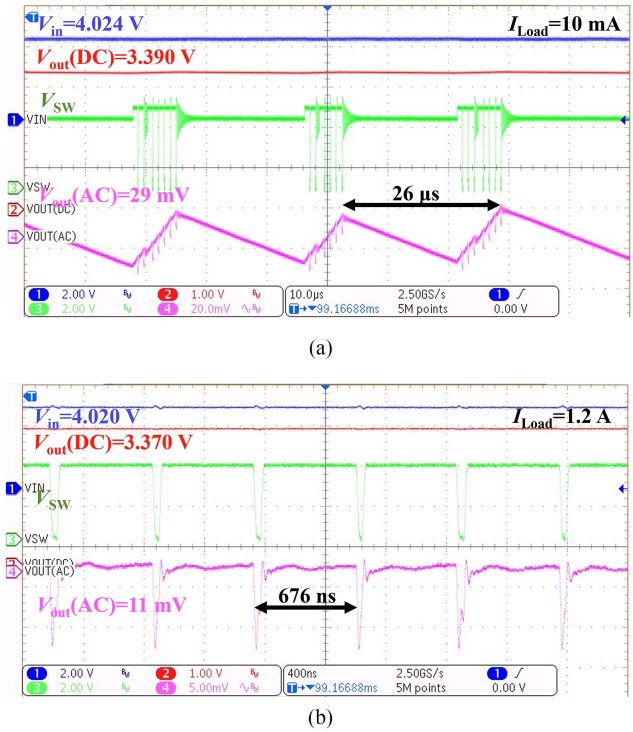
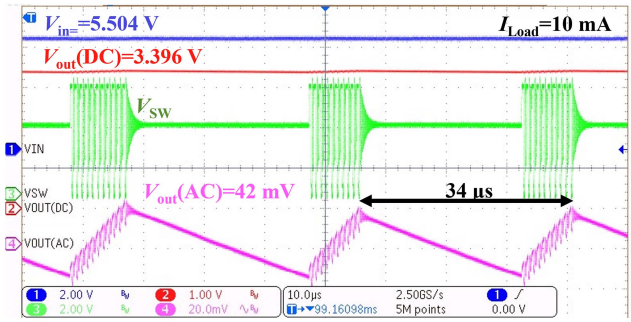


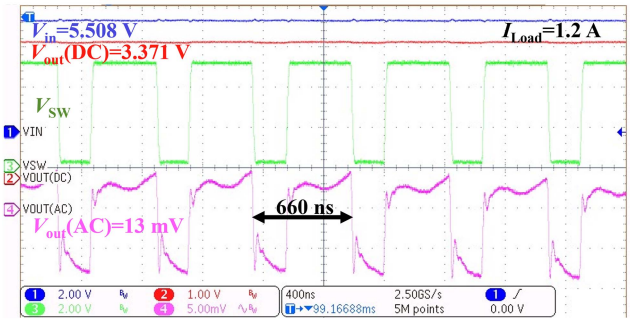
Fig. 11. Measured steady-state behaviors with 4.0-V $V_{\rm in}$ under different loads. (a) 10 mA. (b) 1.2 A.

Fig. 10 shows the experimental setup for testing the dc–dc converter chip, with the detailed connection relationship. A Tektronix MDO3054 oscilloscope is used to observe the signal waveforms. A Tektronix AFG31000 signal generator is used to generate a square wave signal to control the switching between heavy and light loads via the external voltage-to-current generator, as an electronic load. The printed circuit board for the measured chip is supplied by a dc power.

To verify the ability to adapt to a wide range of operating scenarios, the prototype converter is measured under multiple load currents and input voltages. Oscilloscopes use the default (DC) coupling mode to track the real-time signal waveforms and



(a)



(b)

Fig. 12. Measured steady-state behaviors with 5.5-V V_{in} under different loads. (a) 10 mA. (b) 1.2 A.

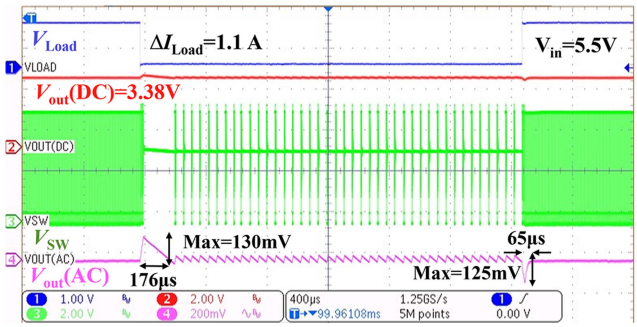
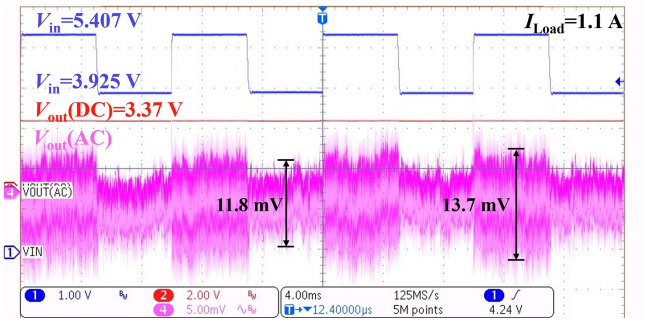
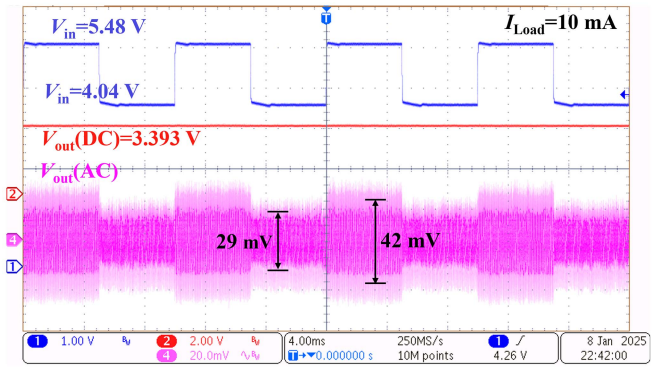


Fig. 13. Measured load transient behavior.



(a)



(b)

Fig. 14. Measured line transient behaviors. (a) Heavy load. (b) Light load.

utilize the ac coupling one to observe the ripple voltages. Figs. 11 and 12 give the measured steady-state behaviors, with V_{out} centered at 3.38 V, V_{in} variation of 4.0–5.5 V, and I_{Load} range of 0.01–1.2 A. It is observed that V_{out} varies from 3.370 to 3.396 V, and achieves a peak-to-peak ripple voltage with the minimum value of 11 mV for heavy loads and the maximum value of 42 mV for light ones, respectively. The measured switching frequency is automatic sliding from 29.4 kHz to 1.5 MHz for the I_{Load} values of 10–1200 mA, which conforms to (3). V_{SW} waveforms in accordance with Fig. 3, are also observed in Figs. 11 and 12, under different load conditions.

In order to verify the mode transition, Fig. 13 shows the measured load transient response between 1.0 mA and 1.1 A, with 5.5-V V_{in} and 3.38-V V_{out}. By employing an external voltage-to-current converter (V_{Load}/R_{Load}) as the load for the load current step, the measured overshoot and undershoot voltages are 130 mV and 125 mV, while the recovery time for load transition is 176 μs and 65 μs, respectively. The output voltage variation less than 3.49%/A (=0.13/(3.38 $\times$ 1.1)) for the load current transient response, is also observed. Fig. 14(a) gives the measured line transient response between 3.925 and 5.407 V, with 3.37-V V_{out} and 1.1-A I_{Load} for heavy loads. It is observed that V_{in} has the tiny effect on V_{out} and the slight influence on the ripple voltage from 11.8 to 13.7 mV. Fig. 14(b) gives the measured line transient behavior between 4.04 V and 5.48 V, with 10-mA light load current and 3.39-V V_{out}. V_{in} has the ignored effect on V_{out} and the little influence on the ripple voltage from 29 to 42 mV. The measured recovery time for line transition is small enough to be invisible and thus considered as zero.

Figs. 15 and 16 show the measured line regulation (LNR) and LDR features. The converter with V_{out} centered at 3.38 V achieves the LNR of 0.03%–0.18% and the LDR less than 0.98%, under 4.0–5.5-V V_{in} and 1-1200-mA I_{Load}. Fig. 17(a) gives the measured conversion efficiencies with 3.38-V V_{out}, under wide V_{in} and I_{Load} variations. The minimum and maximum efficiencies of 80.61% and 93.65%, are achieved, respectively, for PSM and PWM modes. As depicted in Fig. 17(b), for PWM mode with a fixed F_{SW}, the conduction loss dominates and scales ahead of I_{Load}, which causes the conversion efficiency slightly decreases as I_{Load} rises. While in PSM mode with a varying

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Reference		This article	Huang et al. [3]	Hong and Lee [4]	Zeng et al. [7]	Kim et al. [8]	Yuan et al. [9]
Process (nm)		180 BCD	180 CMOS	180 CMOS	180 CMOS	65 CMOS	180 CMOS
Architecture		PWM/PSM	AOT	MSPWM/PWM/PFM	PWM/DCT	PWM/PFM	PWM/ABM
Input Voltage (V)		4.0–5.5	2.1–5.5	2.0–3.3	2.0–5.0	1.8	3.0–5.0
Output Voltage (V)		3.38	1.80	1.20	3.00	1.50	1.40
Max. I_{Load} (A)		1.2	0.3	0.2	0.05	1.0	5.0
Max. F_{SW} (MHz)		1.5	2.0	7.4	2.6	10.0	3.0
Output Inductor L (μH)		4.7	2.2	1	2.2	0.22	0.33
Output Capacitor C_{out} (μF)		15	10	2.2	4.7	4.7	47
Min. Efficiency (%)		80.61	80.00	40.00	80.00	80.00	80.00
Max. Efficiency (%)		93.65	95.80	91.00	94.70	90.00	91.00
I_{Load} Trans.	ΔI_{Load} (A)	1.10	0.29	0.08	0.05	0.40	0.80
	Recovery time T_R (μs)	176	30	125	60	1.8	5
	Variation (%/A)	3.49	9.20	141.67	160.00	6.67	10.87
Total Area (mm^2)		0.28	1.09	0.85	1.10	1.50	3.20
Controller Number		1	1	1	2	2	2
FoM*		0.1306	0.1063	0.0039	0.0150	0.1040	0.0375

* Larger value is better.

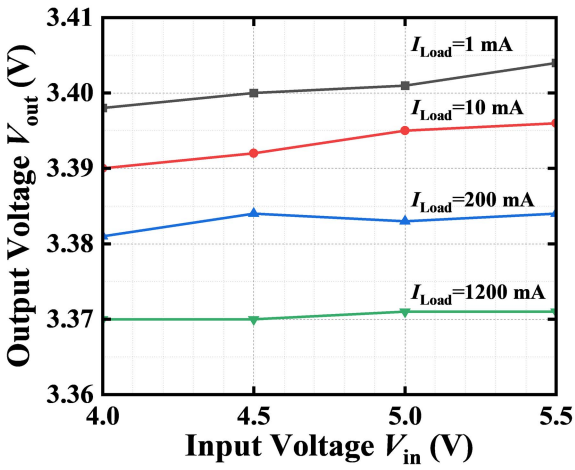


Fig. 15. Measured LNR performances with different I_{Load} values.

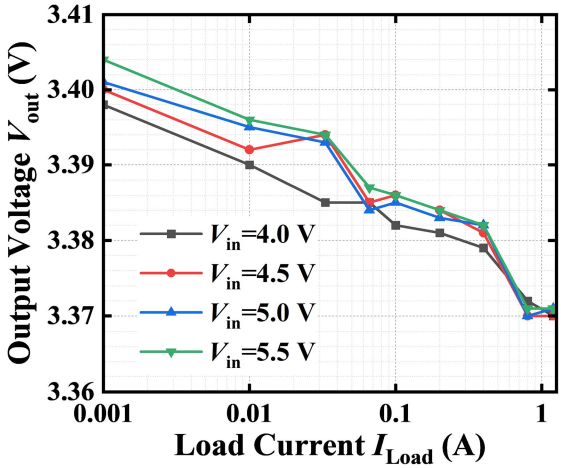


Fig. 16. Measured LDR performances with various V_{in} values.

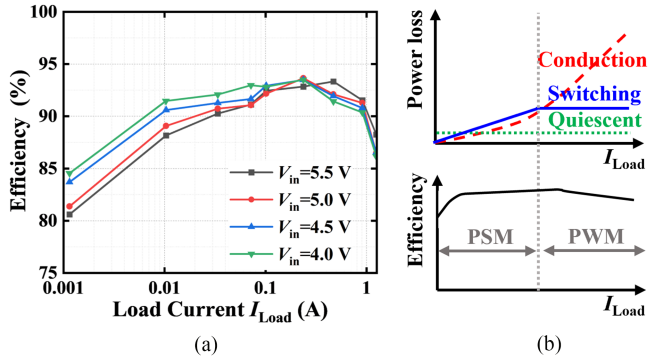


Fig. 17. Conversion efficiencies. (a) Measured values under V_{in} and I_{Load} variations. (b) Theoretical analysis.

F_{SW} that is related to I_{Load}, the switching loss dominates and is also proportional to I_{Load}, which thus holds a nearly constant efficiency. However, at extremely small load currents, quiescent loss dominates and is constant, which inversely makes the efficiency goes up with I_{Load}. The measured results of Fig. 17(a) are in accordance with the theoretical analysis in Fig. 17(b).

It is concluded that V_{out} and the ripple voltage slightly decrease, the switching frequency evidently increases, and the conversion efficiency obviously varies, as I_{Load} goes up, and vice versa. In addition, the conversion efficiency slightly grows up as V_{in} decreases.

The presented converter performances are summarized and compared to the existing designs in Table I. The figure of merit (FoM) [16] is given in (6) and defined to reflect the dynamic performance. A larger FoM value stands for a faster load transient response. Here, ΔI_{Load} and T_R are load current step (=1.1 A) and step-response recovery time (=176 μs) during the load transient

behavior between PWM and PSM modes, respectively,

$$\text{FoM} = \frac{L \times \Delta I_{\text{Load}} \times 10^2}{C_{\text{out}} \times F_{\text{SW}} \times T_R}. \quad (6)$$

In comparison to the traditional structures, the proposed design only utilizes a simplified VD for a single mode control to conduct a load-dependent seamless transition between PWM and PSM. This benefits the low-complexity implementation with a smaller silicon area, a better FoM value, a smaller voltage variation of load current transient response, and a high conversion efficiency.

V. Conclusion

By introducing a simplified mode controller, a buck dc–dc converter with a load-dependent seamless mode transition, is fabricated in 180-nm BCD with a chip size of 0.28 mm^2 and the quiescent current lower than 90 μA. The efficiencies up to 93.65% for PWM and larger than 80.61% for PSM are achieved over a wide load range, respectively. A peak-to-peak ripple voltage with the minimum value of 11 mV for heavy loads and the maximum value of 42 mV for light ones, are obtained. Both LNR and LDR less than 0.18% and 0.98% are observed, respectively. The voltage variation of 3.49%/A for the load current transient response, is also achieved. All these are fit for low-cost applications of SoC power management and portable / wearable electronic devices, such as cellular and smart phones, wireless and DSL modems, PDAs and so on.

The prototype converter has the following merits.

1) Low-complexity dual-mode structure with a single and simplified controller, to eliminate complicated mode-switching operation and additional submodules for mode transition, which is fully different from the existing mechanisms.
2) A load-dependent seamless mode transition between PWM and PSM.
3) A small silicon size and a high conversion efficiency with a good FoM value for a fast transient response.

The further study on high robustness of mode-switching current / voltage thresholds over process, voltage, and temperature variations, will be considered as a future work.

References

[1] X. Lai, J. Zhao, and B. Wang, "A current-mode DC-DC buck converter with accurate current limit using multiplex PWM comparator," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12739–12749, Dec. 2022.

[2] J.-D. Suh, J. Seok, and B.-S. Kong, "A fast response PWM buck converter with active ramp tracking control in a load transient period," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 3, pp. 467–471, Mar. 2019.

[3] W. Huang, L. Liu, X. Liao, C. Xu, and Y. Li, "A 240-nA quiescent current, 95.8% efficiency AOT-controlled buck converter with A^2-comparator and sleep-time detector for IoT application," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12898–12909, Nov. 2021.

[4] W. Hong and M. Lee, "A 7.4-MHz tri-mode DC-DC buck converter with load current prediction scheme and seamless mode transition for IoT applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 4544–4555, Dec. 2020.

[5] M. Zhao et al., "An ultra-low quiescent current tri-mode DC-DC buck converter with 92.1% peak efficiency for IoT applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 1, pp. 428–439, Jan. 2022.

[6] T.-J. Lee, C.-H. Hsu, and C.-C. Wang, "High efficiency buck converter with wide load current range using dual-mode of PWM and PSM," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2019, pp. 1–4.

[7] W.-L. Zeng et al., "A 470-nA quiescent current and 92.7%/94.7% efficiency DCT/PWM control buck converter with seamless mode selection for IoT application," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 11, pp. 4085–4098, Nov. 2020.

[8] S. J. Kim, W.-S. Choi, R. Pilawa-Podgurski, and P. K. Hanumolu, "A 10-MHz 2-800-mA 0.5-1.5-V 90% peak efficiency time-based buck converter with seamless transition between PWM/PFM modes," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 814–824, Mar. 2018.

[9] B. Yuan, M.-X. Liu, W. T. Ng, and X.-Q. Lai, "Hybrid buck converter with constant mode changing point and smooth mode transition for high-frequency applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1466–1474, Feb. 2020.

[10] Y. Yao, M. Zhao, and X. Wu, "A wide-load-range tri-mode buck converter with seamless mode transition," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2022, pp. 2511–2515.

[11] B. Zhou et al., "A low-complexity pure-MOS sliding-frequency semi-digital buck DC-DC converter based on a triple-comparator structure," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5992–6002, May 2024.

[12] W. Park et al., "A 94% peak efficiency dual mode buck converter with fully integrated on-time-based mode control for implantable medical devices," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 11, pp. 4458–4462, Nov. 2022.

[13] Y.-J. Park et al., "A design of a 92.4% efficiency triple mode control DC-DC buck converter with low power retention mode and adaptive zero current detector for IoT/wearable applications," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6946–6960, Sep. 2017.

[14] H. A. Zadeh, H. R. Kooshkaki, K.-Y. Lee, and P. P. Mercier, "An adaptive constant-on-time-controlled hybrid multilevel DC-DC converter operating from Li-Ion battery voltages with low spurious output," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 5763–5776, May 2023.

[15] Q. ul Ain et al., "A high-efficiency fast transient COT control DC-DC buck converter with current reused current sensor," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9521–9535, Aug. 2021.

[16] W.-H. Yang et al., "A constant-on-time control DC-DC buck converter with the pseudowave tracking technique for regulation accuracy and load transient enhancement," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6187–6198, Jul. 2018.

[17] T.-W. Sun, K.-Y. Liao, and T.-H. Tsai, "A digital-control buck converter with dual pulse-skipping modes for Internet of Things," in *Proc. IEEE Int. Symp. Circuits Syst.*, pp. 2516–2519, Nov. 2022.

[18] S. Kapat, B. C. Mandi, and A. Patra, "Voltage-mode digital pulse skipping control of a DC-DC converter with stable periodic behavior and improved light-load efficiency," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3372–3379, Apr. 2016.

[19] K.-Y. Hu, C.-H. Tsai, and C.-W. Tsai, "Digital V^2 constant on-time control buck converter with adaptive voltage positioning and automatic calibration mechanism," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7178–7188, Jun. 2021.

[20] S.-Y. Kim et al., "Design of a high efficiency DC-DC buck converter with two-step digital PWM and low power self-tracking zero current detector for IoT applications," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1428–1439, Feb. 2018.

[21] P.-H. Liu, Y. Yan, P. Mattavelli, and F. C. Lee, "Digital constant on-time V^2 control with hybrid capacitor current ramp compensation," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8818–8826, Oct. 2018.

[22] M. Choi, C.-H. Kye, J. Oh, M.-S. Choo, and D.-K. Jeong, "A current-mode digital AOT 4-phase buck voltage regulator," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 11, pp. 244–247, Nov. 2019.

[23] K. Hariharan, S. Kapat, and S. Mukhopadhyay, "Constant on/off-time hybrid modulation in digital current-mode control using event-based sampling," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3789–3803, Apr. 2019.

Yun Hao was born in Liaoning, China. She received the B.S. degree in electronic information engineering in 2023 from the School of Information and Electronics, Beijing Institute of Technology, Beijing, China, where she is currently working toward the M.S. degree in integrated circuit science and engineering with the School of Integrated Circuits and Electronics.

Her current research interests cover dc–dc converters and instrumentation amplifiers.

Xukun Wang was born in Shandong, China. She received the B.S. degree in electronic packaging technology in 2022 from the School of Materials Science and Engineering, Beijing Institute of Technology, Beijing, China, where she is currently working toward the M.S. degree in integrated circuit engineering with the School of Integrated Circuits and Electronics.

Her current research interests include hall sensors and instrumentation amplifiers.

Zhigang Han was born in Henan, China. He received the B.S. degree from Henan University of Science and Technology, Luoyang, China, in 1993, the M.S. degree from Henan University of Science and Technology, Luoyang, China, in 1996, both in mechanical electronics engineering, and the Ph.D. degree in systems engineering from Northwestern Polytechnical University, Xi'an, China, in 2000.

After he had finished post-doctoral research with Shanghai Jiaotong University, Shanghai, China, in 2003, he joined School of Electronics and Information Engineering, Tongji University, Shanghai, China. In 2023, he was with TX Semiconductor Sci.-Tech. Company Ltd., where he focused on power management and hall sensor design. His current research interests cover high-voltage buck/boost dc–dc converters, SVPWM motor drivers, and low-power hall sensors.

Chunli Huang was born in Guangdong, China. She received the B.S. degree in electronic information engineering in 2024 from the School of Information and Electronics, Beijing Institute of Technology, Beijing, China, where she is currently working toward the M.S. degree in integrated circuit science and engineering with the School of Integrated Circuits and Electronics.

Her current research interests cover frac-N phase-locked loops and dc–dc converters.

Huikai Xie (Fellow, IEEE) was born in Chongqing, China. He received the B.S. degree in microelectronics from the Beijing Institute of Technology, Beijing, China, the M.S. degree in photonics from Tufts University, Medford, MA, USA, in 1998, and the Ph.D. degree in electrical and computer engineering from Carnegie Mellon Universiyt, Pittsburgh, PA, USA, in 2002.

He is currently a Professor with the School of Integrated Circuits and Electronics, Beijing Institute of Technology, Beijing, China. He was an Assistant Researcher/a Lecturer with the Institute of Microelectronics, Tsinghua University, Beijing, China, (1992–1996). Before joining BIT in 2020, he was an Assistant Professor (2002–2007), an Associate Professor with tenure (2007–2011) and a Full Professor (2011–2020) with the Department of Electrical and Computer Engineering, University of Florida. He has authored or coauthored more than 350 technical papers and 11 book chapters and holds 19 issued US patents and 45 issued Chinese invention patents. His current research interests include MEMS/NEMS, CMOS-MEMS, integrated power passives, acoustic MEMS, optical beam steering, optical communications, LiDAR, NIR spectroscopy, and biophotonics.

Dr. is an Associate Editor for IEEE SENSORS LETTERS AND SENSORS & ACTUATORS A. He is a Fellow of SPIE.

Bo Zhou was born in Henan, China. He received the B.S. degree in electronic engineering from Hunan University, Changsha, China, in 2002, the M.S. degree in circuits and systems from Shanghai Jiaotong University, Shanghai, China, in 2005, and the Ph.D. degree in electronic science and technology from Tsinghua University, Beijing, China, in 2012.

In 2005, he was with STMicroelectronics Company Ltd., Shanghai, where he focused on car-body electronic power design. In 2007, he was with Agere System Company Ltd. (acquired by LSI), Shanghai, China, where he focused on magnetic head read-write channel design. In 2012, he was the Faculty of the School of Integrated Circuits and Electronics, Beijing Institute of Technology, Beijing, China. From 2014 to 2015, he was a Visiting Scholar with Oregon State University, Corvallis, OR, USA, where he focused on energy harvesting and wireless data transmission. His current research interests include delta-sigma phase-locked loop, buck/boost dc–dc converter, fully-digital transmitter, polar transmitter, frequency modulated ultrawide-band transceiver.