Understanding the Role of Dislocation Defects of GaN HEMT under Short-Circuit Stress Through Transient Thermal Characterization

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***Abstract*—Gallium nitride (GaN) high electron mobility transistor (HEMT) devices are prone to rapid failure after repetitive short-circuit (SC) stress under high bus voltage conditions. The dislocation defects at the substrate interface play a critical role in inducing device degradation and thermal breakdown failure. However, the mechanisms of dislocation defect formation under SC stress and their influence on the SC capability of GaN HEMTs remain unclear. This article presents a novel method based on transient thermal resistance characterization to monitor the evolution of dislocation defects within GaN HEMT devices. Meanwhile, a thermal model is developed to illustrate the influence of dislocation defects on the thermal characteristics of the device. By analyzing the structure function of the GaN HEMT before and after SC stress, the accumulation of previously imperceptible defects is translated into observable changes in thermal resistance curves. The degradation of thermal characteristics of GaN HEMT devices under varying bus voltages and SC pulse durations are investigated. Experimental results demonstrate that the transient thermal characterization method effectively identifies regions of dislocation defect accumulation, quantifies the extent of defect accumulation, and provides a comprehensive understanding of damage evolution within GaN HEMTs under repetitive SC stress.**

***Index Terms*—Dislocation defects, gallium nitride (GaN) high electron mobility transistor (HEMT), short-circuit, thermal resistance.**

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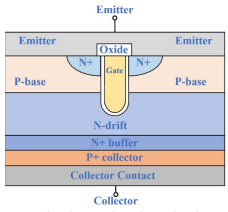
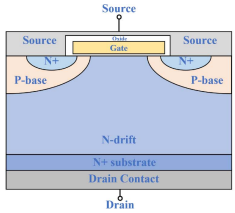
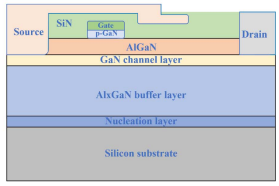
I. Introduction

GALLIUM nitride (GaN) high electron mobility transistors (HEMTs) have great potential for power electronic applications because of their high mobility, superior breakdown voltage, and fast switching capability [1], [2]. In recent years, there has been fast progress in GaN HEMT device technology [3], [4], which allowed for the production of commercial devices with better performances (power density and power efficiency) [5]. Despite these advancements, reliability concerns of GaN HEMTs such as dynamic ON-resistance ($dR_{DS(\mathrm{on})}$) degradation [6], [7] and gate instability [8], [9] remain critical challenges. Such challenges are especially problematic under harsh operating conditions, where compliance with rigorous reliability standards is required. Addressing these reliability issues is crucial to realizing the full potential of GaN HEMTs in high-performance power electronic systems.

To evaluate the limits of GaN devices under demanding operational conditions, researchers often analyze their behavior under extreme stress conditions [10], [11], [12], most commonly during short-circuit (SC) [10], and surge current scenarios [12].

GaN HEMTs generally have a weaker withstanding capability under extreme operating conditions compared to their vertical structure power device counterparts [13]. The maximum SC withstanding time of 650 V GaN HEMT devices is only a few hundred nanoseconds under 400 V dc bus voltage conditions [13], [14]. Table I provides a comparison of SC characteristics and failure mechanisms among three types of power semiconductor devices: 1) Si IGBT, 2) silicon carbide (SiC) MOSFET, and 3) GaN HEMT [15], [16], [17]. Among these devices, GaN HEMTs exhibit the shortest SC capability, typically less than 1 μs [10] under high bus voltage conditions, compared to the much longer SC withstanding time of Si IGBT ($\geq$10 μs) and SiC MOSFET ($\geq$3 μs) [16]. The shorter SC duration of GaN HEMTs is primarily attributed to their heat generation and dissipation mechanism. Specifically, a localized concentration of current and electric field forms in the channel layer of GaN HEMT under SC conditions, generating significant heat. The channel layer is located near the chip surface, which is not only smaller in volume but also has significantly lower thermal capacitance compared to its counterparts in Si IGBT and SiC MOSFET. Furthermore, the lateral conduction nature of GaN HEMTs results in reduced

TABLE I
COMPARISON OF THE SHORT-CIRCUIT CHARACTERISTICS AND FAILURE MECHANISMS OF SI IGBT, SIC MOSFET, AND GAN HEMT

Power Semiconductor Device	Si IGBT	SiC MOSFET	GaN HEMT
Device Material Carrier	Silicon Electron and Hole	Silicon Carbide Electron	Gallium Nitride Electron
Device Structure	 Vertical conduction device	 Vertical conduction device	 Lateral conduction device
Short-Circuit Capability	Longest (typically≥10 μs)	Moderate (typically≥3 μs)	Shortest (typically <1 μs at high bus voltage conditions)
Short-Circuit Failure Mechanism	1. Thermal runaway 2. Avalanche breakdown	1. Thermal runaway 2. Gate oxide breakdown	1. Thermal runaway 2. Gate heterojunction breakdown [24]
Repetitive Short-Circuit Capability	Good (typically≥1,000 cycles)	Moderate (typically>100 cycles)	Weak (>10 cycles at high bus voltage conditions)
Degradation Mechanism under Repetitive Short-Circuit	Aluminum reconstruction on chip surface	Gate oxide degradation	1. AlGaN/GaN and AlGaN/passivation interface traps 2. Dislocation defects
Short-Circuit Temperature Rise	Slow	Fast	Fast
Hotspot Region	Drift region	JFET region (Planar gate)	Channel layer (Access region)

heat spreading compared to the vertical structures of Si IGBT and SiC MOSFET. This combination of factors results in the rapid temperature rise of GaN HEMTs under SC conditions, ultimately leading to their weaker SC performance.

GaN HEMT devices not only have shorter withstand time under high bus voltage SC conditions but are also particularly vulnerable to damage under repetitive SC stress. In comparison, Si IGBTs can endure more than 1000 repetitive SC cycles without significant degradation. SiC MOSFETS show moderate SC endurance (≥100 cycles) with degradation primarily due to gate oxide defects [17]. However, GaN HEMTs typically endure only about 10 SC cycles under high bus voltage conditions (e.g., 400 V) [18], due to its susceptibility to AlGaN/GaN and AlGaN/passivation interface defects, as well as the presence of dislocation defects. Schottky-type p-GaN gate HEMTs could survive only up to 20 cycles under a 20 ns SC pulse width [18]. The GaN HEMTs show significant electrical parameter degradation when exposed to repetitive SC stress [18], [19], [20]. After enduring SC stress, the change in the GaN device's output capacitance [19] and drain leakage current [10] have been observed. The increase in interface defects within the AlGaN/GaN and AlGaN/passivation interface is thought to be one of the primary causes of degradation and rapid failure of GaN HEMTs under repetitive SC conditions [20].

Previous studies have primarily focused on electrical parameters degradation induced by charge trapping mechanisms. However, these mechanisms cannot fully explain the rapid failure observed under repetitive SC conditions. Another significant factor contributing to rapid thermal runaway failure is the extremely high temperature, which induces irreversible structural damage to the device's surface metal and generates defects within the epitaxial layers. Thermal model studies [21], [22], [23], [24] have demonstrated that device temperatures under SC conditions can exceed the thermal breakdown limits of GaN materials [23]. Thermal simulations and postfailure inspections have identified the localized hot spots in the source field plate edge region during SC conditions, leading to thermal fatigue cracks between the source field plate edge and the drain [18]. Additionally, the emergence and accumulation of defects at the substrate interface and within the buffer layer after SC stress have also been observed [24], and these defects are speculated to induce a significant increase in the device's junction temperature.

Despite these findings, several challenges remain unresolved.

1) The mechanisms underlying the formation and evolution of defects at the substrate interface under SC stress are not yet fully understood.
2) There is a lack of effective, noninvasive analytical methods to monitor the evolution of substrate interface defects in GaN HEMT.
3) The impact of defect formation at the substrate interface on the SC capability of GaN HEMTs remains unclear.

To address these challenges, this article proposes a method based on transient thermal resistance characterization to monitor the variation of dislocation defects in the GaN HEMT buffer layer and nucleation layer. The key of this approach lies in establishing a relationship between dislocation defects and the thermal characteristics of the device. To achieve this, a thermal model that incorporates the effects of dislocation defects is developed to better illustrate how these defects influence the thermal behavior of GaN HEMTs. By analyzing the thermal structure function curves of the GaN HEMT before and after SC stress, the evolution and accumulation of defects within the device can be monitored.

The main contributions of this article are as follows.

1) This study identifies dislocation defects as a key factor contributing to thermal resistance increase in GaN HEMT under repetitive SC conditions, offering a new perspective to understanding GaN HEMT's rapid failure mechanisms.
2) A novel approach utilizing thermal resistance structure function curves is proposed to detect and

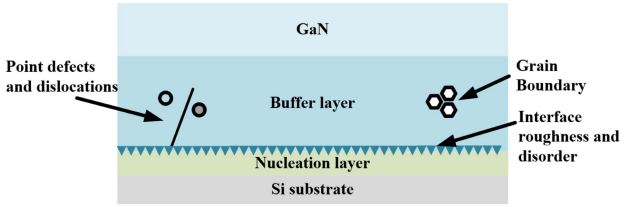


Fig. 1. Defects in the substrate interface and epitaxial layer of GaN HEMT.

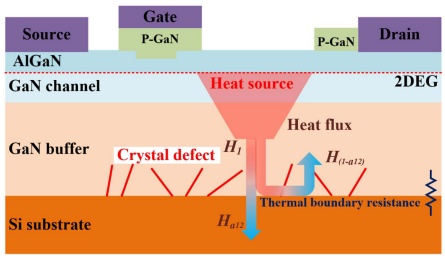


Fig. 2. Impact of dislocation defects on the thermal characteristic of GaN HEMT.

monitor the accumulation of dislocation defects in GaN HEMTs.

3) A thermal model is developed to establish a correlation between the accumulation of dislocation defects and variations in transient thermal resistance, demonstrating how these defects contribute to rapid thermal runaway failure under SC conditions.

The rest of this article is organized as follows. Section II presents the defects formation mechanism and illustrates the effects of dislocation defects on the thermal characteristic of GaN HEMT. The experimental results under repetitive SC conditions are shown in Section III, where the electrical parameters and thermal characteristic degradation after SC stress are investigated. A comprehensive analysis of electrical, thermal, and mechanical stresses under varying bus voltage conditions is performed through TCAD simulation. Section IV explains the principles underlying the defect characterization method based on the transient thermal resistance curve. Section V provides the experimental validation of the proposed method. In Section VI, potential application scenarios and challenges associated with the method are discussed. Finally, Section VII concludes this article.

II. Effects of Dislocation Defects in Thermal Characteristic of GaN HEMT

A. Dislocation Defects Formation Mechanisms in GaN HEMT

Due to the lack of available single crystal GaN substrates, the direct epitaxial growth of GaN single crystals on silicon (Si) substrates is recognized as an ideal approach due to its low cost and large wafer size compared to sapphire, SiC, and GaN substrate [3]. However, the GaN-on-Si suffers from a risk of high dislocation density or crack generation due to the tensile stress induced by the large lattice mismatch (17%) and thermal expansion coefficient difference (56%) between GaN and Si. As shown in Fig. 1, the stress accumulated during high-temperature epitaxial growth can warp the epitaxial layer, leading to a high density of dislocation defects and other extended defects, with densities in the range of 10^9–10^{10}cm^{-2} [25]. Additionally, other native defects, such as antisite and interstitial defects, also form under various growth conditions [26], [27]. These defects act as traps at different energy levels, ranging from shallow to deep levels, and contribute to unintentional doping and Fermi level pinning in the devices. Defects at the substrate interface have been reported as possible origins of excessive leakage path in reverse bias, which limits the reliability of these structures at high voltage and leads to the premature breakdown of GaN HEMT [28].

In addition to the dislocation defects arising from the epitaxial growth process, permanent degradation due to defects formation in GaN HEMTs under extreme electrical stress is another major reason hindering the device's ability to operate close to the theoretical limit [25]. Dislocation defects located at the substrate interface are prone to further evolution when GaN devices operate under stringent conditions.

This evolution is largely driven by the high temperature and high electric field within the chip under extreme electrical stress conditions. From the thermal stress perspective, the temperature gradient and uneven thermal stress across different physical layers of the device may cause deformation and irreversible strain accumulation at the interface between the substrate and the epitaxial layer, thereby leading to the expansion of dislocation defects and degradation of the GaN HEMT device. Meanwhile, since GaN HEMTs usually operate at high voltage, a high electric field is found under the channel region and gate edge. Due to the converse piezoelectric effect [29], the high electric field will increase the stored elastic energy within the material and eventually, AlGaN will relax through the formation of defects when the critical elastic energy is exceeded, resulting in pit and crack formation within the device [30].

B. Impact of Dislocation Defects On Thermal Resistance

The presence of high-density dislocation defects at the substrate interface not only contributes to substrate leakage issues but also degrades the thermal performance due to the increased thermal boundary resistance (TBR) between the GaN epitaxial layer and the silicon substrate [31], [32], [33], [34]. The thermal conductivity of effective TBR is strongly limited by the presence of dislocations, especially at densities exceeding $\sim 10^7$ cm^{-2} at room temperature, where a logarithmic relationship between dislocation density and thermal conductivity is observed [32]. These microstructural defects increase the effective TBR by enhancing phonon scattering, which reduces the effective thermal conductivity of both the interface layer and the buffer layer, thereby impeding heat transmission and diffusion [35], [36]. Therefore, it is more difficult to dissipate the heat generated within the GaN HEMT.

Dislocation defects may increase when the device is subjected to extreme electrical stress. The dislocation defects increase would weaken heat propagation within the device, leading to a nonuniform temperature distribution among the bulk of the device, as illustrated in Fig. 2.

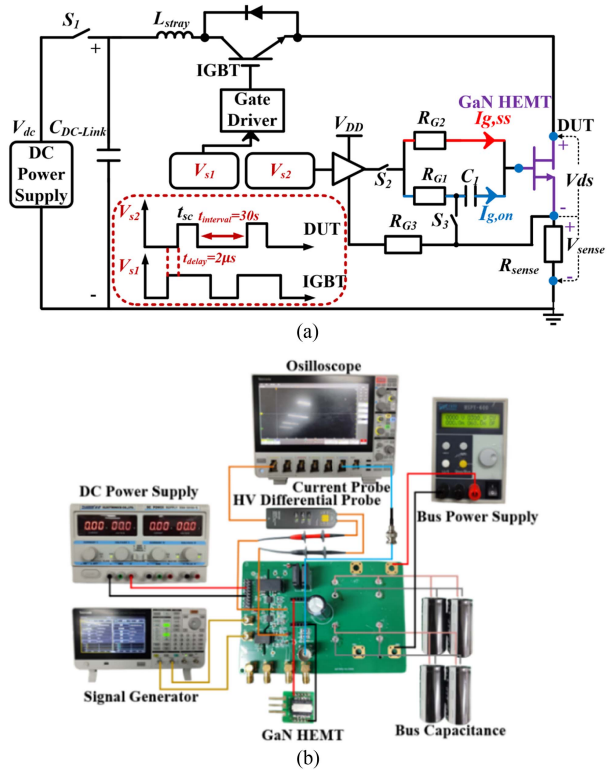


Fig. 3. (a) Schematic of the short-circuit test circuit. (b) Hardware test bench.

III. Repetitive Short-Circuit Experimental Results

This section evaluates the impact of SC pulse duration time and bus voltage on the repetitive SC capability of GaN devices. The degradation of static electrical parameters and thermal characteristics during repetitive SC stress are analyzed. Additionally, a TCAD simulation is conducted to examine the distribution of electrical, thermal, and mechanical stresses within the device under various SC bus voltage conditions.

A. SC Test Setup

In this study, a custom-developed SC testbench was developed to investigate the degradation of the GaN HEMT under repetitive SC stress conditions. A commercial ohmic gate GaN HEMT device rated at 600 V 70 mΩ was selected as the study case [37]. Fig. 3(a) shows the schematic of the SC test circuit, and the SC hardware test bench is provided in Fig. 3(b). An IGBT was employed to prevent device explosion in the case of failure. All the devices under test (DUT) were tested under hard switching fault conditions at room temperature. The applied dc bus voltage during the SC tests is 350 V and 400 V, with the SC pulse duration fixed at 1 μs and 3 μs, respectively. To prevent thermal accumulation during repetitive SC tests and allow the DUT to return to thermal equilibrium, a 30 s interval was set between each SC pulse. The detailed parameters of the DUT and SC test conditions are summarized in Table II.

B. GaN HEMT Repetitive SC Capability Characterization

Fig. 4 shows the SC waveforms of GaN HEMT devices during the first SC event and after enduring 5000 SC cycles, each with a pulse duration of 1 μs. The DUT exhibits robust repetitive SC capability under short SC pulse duration conditions, with no significant degradation observed in the SC waveforms throughout repetitive SC stress.

The maximum number of SC pulses that the DUT can withstand decreases sharply as the duration of the SC pulse increases. Fig. 5 shows the SC waveforms of GaN HEMT devices for the initial SC event and after withstanding 100 SC pulses, each with a duration of 3 μs. During the 100th SC pulse, the devices

TABLE II
Key Specifications of the DUT and Test Conditions

Parameter	Value
GaN HEMT (DUT)	IGO60R070D1
DUT voltage rating (V_{BR})	600V
DUT current rating (I_{ds})	31A@25 °C
Gate turn-on voltage/Gate turn-off voltage (V_{gs})	12 V/0 V
Gate steady-state current ($I_{gs,ss}$)	16m A
Tested bus voltage range (V_{bus})	350 V, 400 V
SC pulse duration (t_{sc})	1 μs, 3 μs
SC pulse duration ($t_{interval}$)	30 s
Tested case temperature (T_C)	25 °C

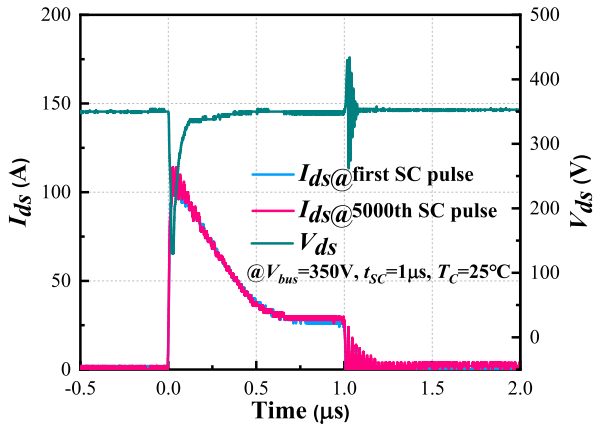


Fig. 4. SC waveforms of GaN HEMT after 5000th SC pulses at V_{dc} = 350 V, t_{pulse} = 1 μs, and Tc = 25 °C.

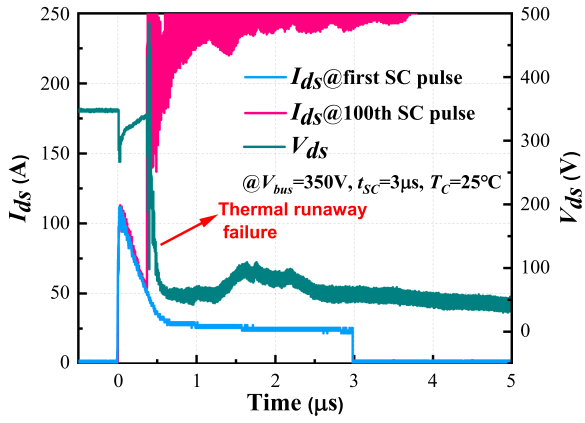


Fig. 5. SC waveforms of GaN HEMT after 100th SC pulses at V_{dc} = 350 V, t_{pulse} = 3 μs, and T_c = 25°C.

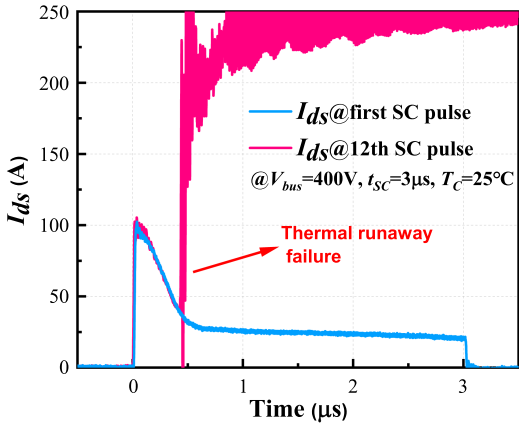


Fig. 6. SC waveforms of GaN HEMT with increasing number of SC pulses at V_{dc} = 400 V and T_c = 25°C.

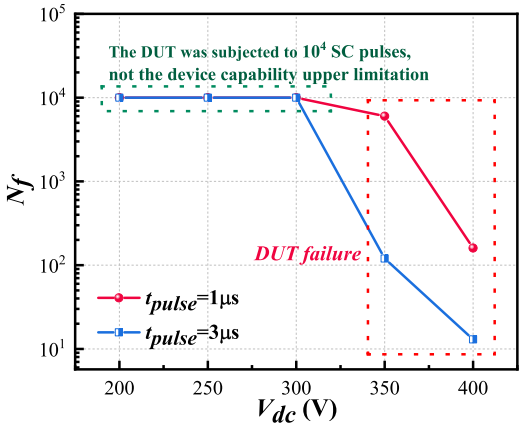


Fig. 7. Numbers of SC cycles to failure (N_f) of devices subjected to various SC pulse durations and DC bus voltage conditions.

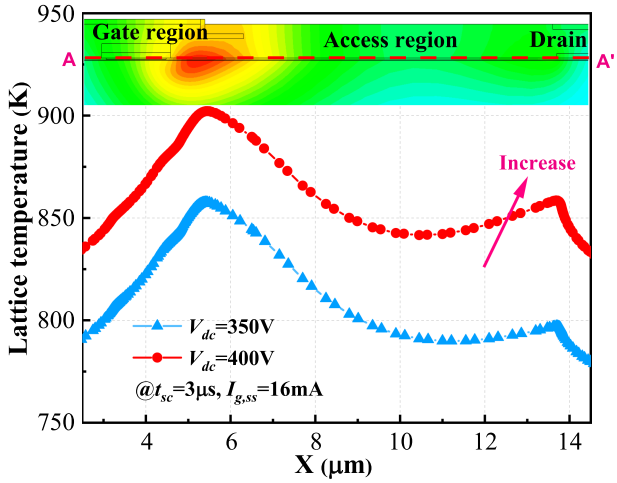


Fig. 8. Temperature distribution along the channel layer under different SC bus voltage conditions.

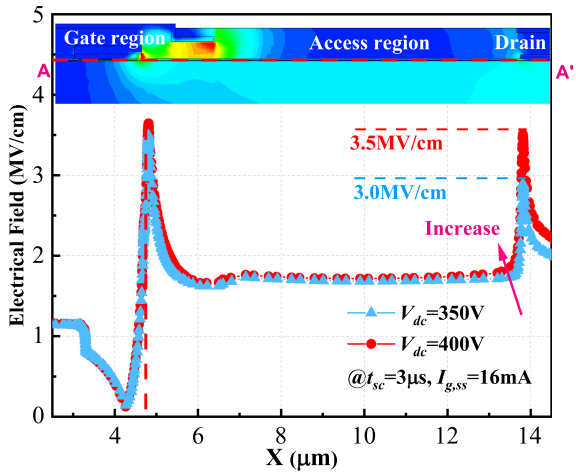


Fig. 9. Electric field distribution along the channel layer at different SC bus voltage conditions.

encountered thermal destruction when operating in the ON-state, resulting in an uncontrollable rise in drain current. This thermal runaway leads to a SC across all three terminals.

The ability of GaN HEMT devices to endure repetitive SC events is influenced not only by the duration of the SC pulses but also by the dc bus voltage. As the bus voltage increases, the number of SC cycles the device can endure quickly decreases. Under a bus voltage of 400 V, the DUT failed due to thermal runaway after withstanding only 12 SC cycles with a pulse width of 3 μs, as shown in Fig. 6. Fig. 7 summarizes the number of SC pulses that the device can withstand under various bus voltage levels and different SC pulse duration conditions. It is obvious that as both bus voltage and SC pulse duration increase, the maximum number of SC pulses that the GaN HEMT device can withstand decreases.

C. Electrical-Thermal-Mechanical Stress Analysis

An electrical-thermal-mechanical simulation was conducted using Sentaurus TCAD to analyze the distribution of electrical, thermal, and mechanical stresses within the GaN devices under different bus voltage SC conditions. The simulation model parameters were selected from the previous work presented in [24].

When the dc bus voltage exceeds a certain threshold, a composite failure mechanism is triggered in the GaN HEMT device. This mechanism involves the interaction of electrical, thermal, and mechanical stresses, which accelerates the device failure. The thermal stress in the access region of the GaN device significantly increases with the rise of dc bus voltage under SC conditions. Fig. 8 shows the temperature distribution along the channel layer after 3 μs of SC stress at cutline AA' under different bus voltage conditions. The relatively lower thermal conductivity in the buffer layer results in a localized temperature increase in the GaN channel layer.

The rapid increase in temperature in the access region can be attributed to the high electric field at the channel layer. The electric field distribution along the channel layer of the DUT at different bus voltage conditions is shown in Fig. 9. As the bus voltage increases, there is a notable increase in the electric field at the bottom of the drain P-GaN region. The high electric field, in combination with the high current density, results in increased power dissipation and temperature rise at the access region.

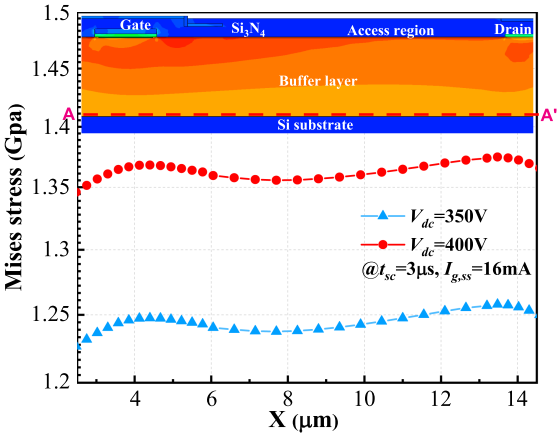


Fig. 10. Mises stress distribution among the device under different SC bus voltage conditions.

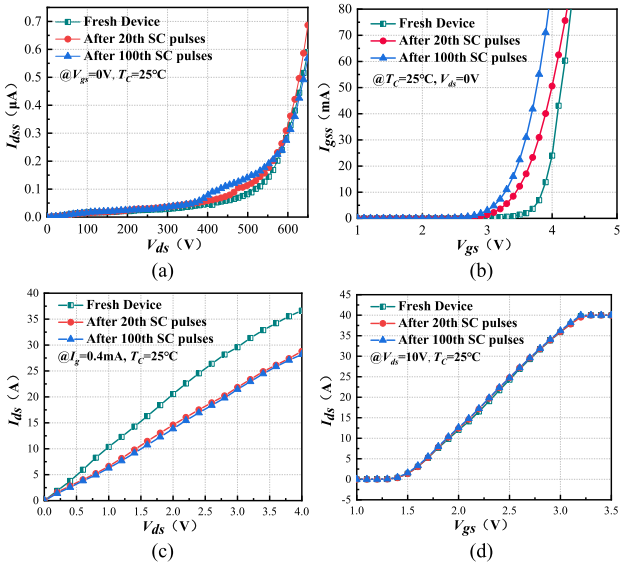


Fig. 11. Variation of the electrical parameters with increasing number of SC pulses at V_{dc} = 350 V condition. (a) Drain leakage current. (b) Gate leakage current. (c) I-V characteristic. (d) Transfer characteristic.

Similarly, the mechanical stress within the device increases rapidly with rising SC bus voltage. Fig. 10 illustrates the Mises stress distribution among the device after 3 μs of SC stress at cutline AA' under different bus voltage conditions. The simulation results show a significant difference in mechanical stress at the interface between the Si substrate and the buffer layer. Such stress can induce lattice distortion and dislocation formation, which further accelerates the device degradation.

D. Electrical Parameters Degradation Under Repetitive SC Stress

Fig. 11 shows the impact of SC pulses on the GaN HEMT's static electrical characteristics. As the number of repetitive SC stress pulses increases, a significant rise in both drain leakage current and gate leakage current is observed. This degradation is likely attributed to carrier trapping and storage at the AlGaN/GaN interface, induced by high electric field and thermal stress [19]. Additionally, a notable increase in ON-state

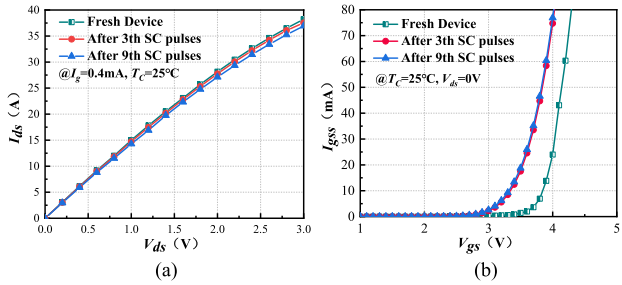


Fig. 12. Variation of the electrical parameters with increasing number of SC pulses at V_{dc} = 400 V condition. (a) I-V characteristic. (b) Gate leakage current.

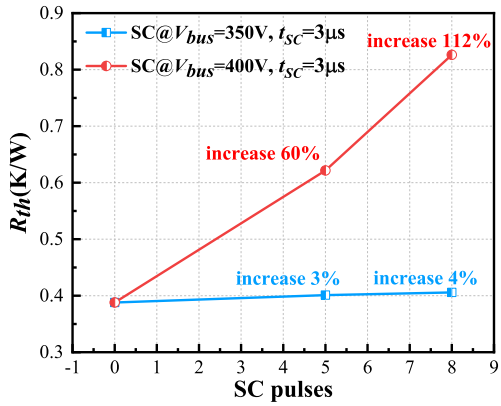


Fig. 13. Variation of GaN HEMT device's thermal resistance with increasing SC pulses.

resistance is detected after the device endures its 100th SC pulse. In contrast, the threshold voltage appears to be less influenced by the repetitive SC stress.

When the device was exposed to repetitive SC stress at a 400 V dc bus voltage, a similar degradation trend was observed, as shown in Fig. 12. The observed degradation in the device's electrical parameters is relatively minor. The degradation of electrical parameters alone cannot fully explain the premature failure of GaN HEMTs under repetitive SC stress.

E. Thermal Performance Degradation Under Repetitive SC Stress

To verify whether the thermal characteristics of the device have degraded during the SC condition, the thermal resistance of the DUT was measured after repetitive SC tests. Fig. 13 shows the thermal resistance measurement of GaN HEMTs after repetitive SC stress under varying bus voltage conditions. Two different trends can be observed. At a bus voltage of 350 V, the thermal resistance of the device showed minimal variation, increasing by only 3% after four SC pulses and by 4% after eight SC pulses. In contrast, under a bus voltage of 400 V, thermal resistance increases significantly by 60% after four SC pulses and sharply increased to 112% after eight SC pulses. The results indicate a severe degradation in the device's heat dissipation capability after repetitive SC stress under high bus voltage conditions.

The premature failure of the GaN HEMT is inferred to be caused by the increase of dislocation defects within the device,

which results in increased thermal resistance and accelerated temperature rise during SC conditions. However, the accumulation of dislocation defects is difficult to analyze directly through electrical parameter measurement. To address this issue, a dislocation defects analysis method based on the transient thermal resistance curve is proposed to investigate the evolution of dislocation defects within GaN HEMTs under repetitive SC stress.

IV. Influence of Dislocation Defects on Device Thermal Characteristic

This section explains the influence of dislocation defects on the transient thermal impedance of GaN HEMT devices using the Cauer thermal model. Furthermore, the methodology for analyzing dislocation defects through structure function curves is presented.

A. Thermal Model Considering the Influence of Dislocation Defects

As mentioned earlier, it is known that dislocation defects within the nucleation layer and buffer layer would decrease the thermal conductivity of the GaN HEMT devices. The increase in dislocation defects lengthens the heat conduction path, causing an increase in thermal resistance. Therefore, by examining the variation in the thermal resistance of GaN devices, the accumulation of dislocation defects can be inferred. The device thermal resistance formula considering the influence of dislocation defects is as follows:

$$R_{th-\mathrm{jc(degraded)}} = R_{th-\mathrm{jc(fresh)}} + \Delta R_{\mathrm{th,defect}}. \tag{1}$$

Assume that the additional thermal resistance $\Delta R_{\mathrm{th,defect}}$ caused by dislocation defects is proportional to the dislocation density ρ_{defect}

$$\Delta R_{\mathrm{th,defect}} = k \cdot \rho_{\mathrm{defect}} \tag{2}$$

where k is a constant related to the material properties.

To better understand the influence of the dislocation defects on the transient thermal characteristic of the device, a Cauer thermal model of the GaN HEMT device was built based on the actual physical structure of the device, as shown in Fig. 14. This model is divided into different stages according to the GaN device's physical structure. Each stage of the RC parameters corresponds to a specific physical layer of the GaN HEMT device. The model includes the GaN layer, buffer layer, nucleation layer, Si substrate, solder layer, and copper baseplate [38]. During device operation, heat generated at the top surface of the channel region is transmitted through these layers down to the copper baseplate at the bottom.

When the transient thermal cooling curve is measured, the thermal impedance between the junction and case $Z_{\mathrm{th-jc}}(t)$ can be extracted, they can be fitted into a finite number of exponential equations [39], [40], as shown in the following equation:

$$Z_{\mathrm{th-jc}}(t) = \sum_{i=1}^{n} R_{\mathrm{th,i}} \left(1 - \exp\left(-\frac{t}{R_{\mathrm{th,i}} \cdot C_{\mathrm{th,i}}}\right)\right) \tag{3}$$

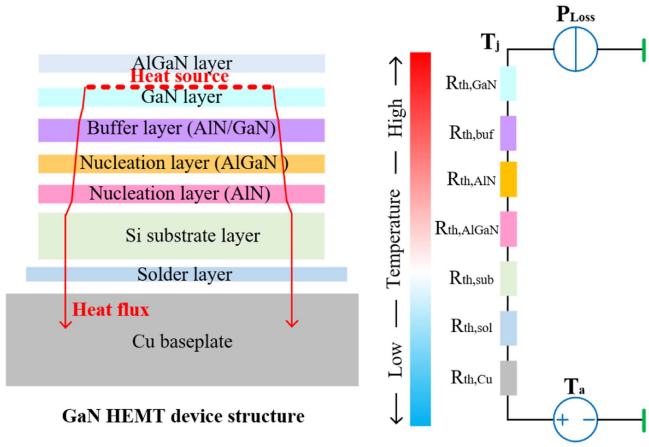


Fig. 14. GaN HEMT device structure and corresponding thermal resistance model.

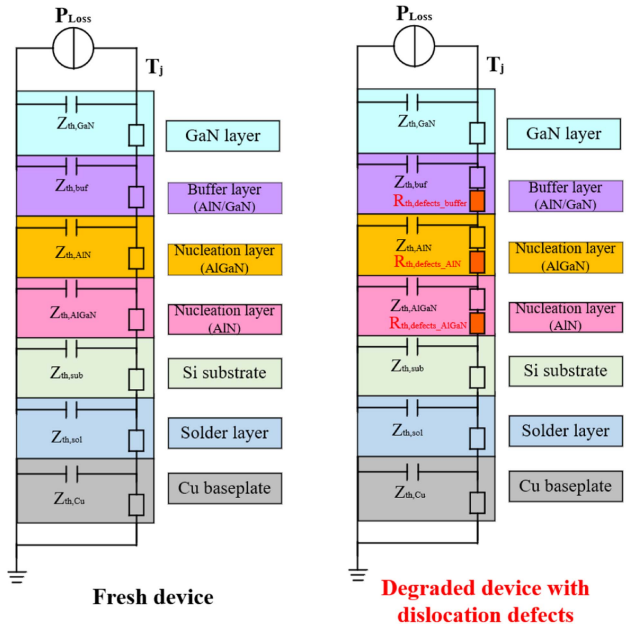


Fig. 15. GaN HEMT device thermal impedance model considering dislocation defects.

where $R_{\mathrm{th,i}}$ and $C_{\mathrm{th,i}}$ represent the thermal resistance and heat capacity of the material layer in the ith stage of the Cauer thermal model.

It is assumed that the increase in dislocation defect density within the buffer layer and nucleation layer leads to an increase in thermal resistance, denoted as $\Delta R_{\mathrm{th,defect}}$, while the heat capacity is considered unaffected by these dislocation defects, as shown in Fig. 15. The transient thermal impedance equation of degraded device can be modified

$$Z_{\mathrm{th-jc(degraded)}}(t) = \sum_{i=1}^{n} (R_{\mathrm{th,i}} + \Delta R_{\mathrm{th,defect}}) \left(1 - exp\left(-\frac{t}{(R_{\mathrm{th,i}} + \Delta R_{\mathrm{th,defect}}) \cdot C_{\mathrm{th,i}}}\right)\right). \tag{4}$$

From the abovementioned formula, it can be observed that as dislocation defects accumulate within the device, the transient thermal impedance increases due to the additional thermal resistance $\Delta R_{\text{th,defect}}$, introduced by these dislocation defects.

B. Dislocation Defects Analysis By Structure Function Curves

The thermal characteristics in the heat-flow path can be graphically represented by the cumulative structure function (CSF) and differential structure function (DSF) [40]. The differential structure function is the derivative of the cumulative structure function with respect to thermal resistance. These curves enable the analysis of thermal resistance and heat capacity distribution across the various material layers within the GaN HEMT. Both the CSF and DSF are derived through mathematical transformations of the transient thermal impedance curve.

The calculation of the structure function follows these steps: First, the measured transient thermal impedance curves are numerically differentiated. This is followed by an algebraic transformation and the introduction of an inverse convolution operation to derive the thermal time-constant spectrum. The time-constant spectrum is then discretized to obtain the *n*th-order Foster thermal network model, which is subsequently transformed into the *n*th-order Cauer thermal network model. The CSF is obtained by using the *n*th-order cumulative thermal resistance from the Cauer thermal network model as the horizontal axis and the *n*th-order cumulative heat capacity as the vertical axis, as illustrated in (5), (6), and (7). The DSF is then derived by taking the derivative of the CSF, as shown in (8). A comprehensive description of the calculation procedure can be found in [40].

The cumulative thermal resistance is defined as the thermal resistance between the nth element of the model network and the heat source

$$R_{\text{th}\sum} = \sum_{i=1}^{n} R_{\text{th,i}} \tag{5}$$

and the cumulative thermal capacitance is

$$C_{\text{th}\sum} = \sum_{i=1}^{n} C_{\text{th,i}}. \tag{6}$$

The cumulative structure function and differential structure function is obtained

$$\text{CSF} = C_{\text{th}\sum}(R_{\text{th}\sum}) \tag{7}$$

$$\text{DSF} = \frac{dC_{\text{th}\sum}}{dR_{\text{th}\sum}}. \tag{8}$$

According to the cumulative structure function, the slope of the cumulative structure function curve may change when the heat transfer area of a material layer changes or when heat transitions from one material layer to another. Therefore, a change in the slope of the cumulative structure function curve at a specific position may result in an extreme value in the differential structure function curve. Utilizing this feature, the thermal resistance and thermal capacitance of each material layer can be determined by analyzing the cumulative and differential structure function curves.

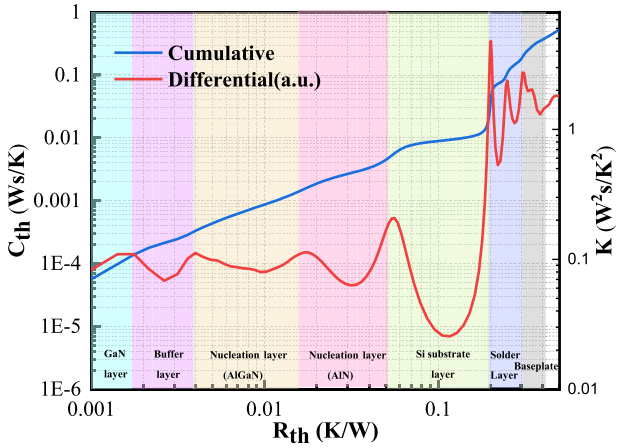


Fig. 16. Cumulative structure function and differential structure function division of GaN HEMT device.

Fig. 16 illustrates the measured cumulative and differential structure function curves of the GaN HEMT device. Based on these structure functions and the formulas for calculating material thermal resistance and heat capacity [39], [40], the thermal resistance and heat capacity of each material layer in the measured GaN device under investigation can be approximately determined.

Considering the influence of dislocation defects on the thermal characteristic of the device, the cumulative structure function and differential structure function can be modified

$$\text{CSF}_{\text{degraded}} = C_{\text{th}\sum}\left(R_{\text{th}\sum} + \Delta R_{\text{th,defect}}\right) \tag{9}$$

$$\text{DSF}_{\text{degraded}} = \frac{dC_{\text{th}\sum}}{d\left(R_{\text{th}\sum} + \Delta R_{\text{th,defect}}\right)}. \tag{10}$$

Since, the accumulation of defects within the device changes its thermal characteristics, the structure function can be used to detect these changes, identify the defect formation region, and assess the extent of defect accumulation. The above modified equations show that the slope of the cumulative structure function curve corresponding to the degraded region of the device would decrease, and the peak point of the differential structure function curve corresponding to the degraded region would shift as well.

V. Transient Thermal Characterization Validation

In this section, the defects accumulation within GaN HEMTs after repetitive SC stress were detected and tracked nondestructively through the transient thermal curve method. The transient thermal characteristic evaluation is carried out to identify the locations within the GaN devices where defects form after SC stress and how these defects evolve with increasing SC stress.

A. Transient Thermal Resistance Measurement Method

To begin the structure function analysis, transient thermal resistance characterization is conducted on the ohmic gate P-GaN

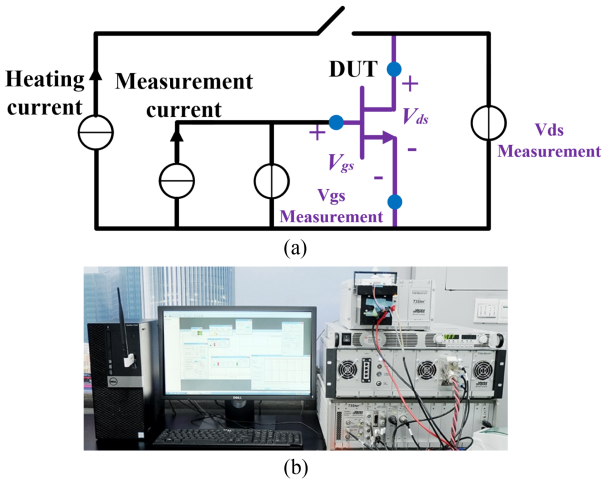


Fig. 17. (a) Schematic of GaN HEMT thermal resistance measurement circuit. (b) Semiconductor thermal analyzer.

HEMTs. This study selects the V_{gs} under constant gate current conditions as the temperature-sensitive electrical parameter for junction temperature monitoring. This evaluation utilized the negative temperature coefficient characteristic of the diode between the gate and source terminals of the Ohmic P-GaN gate GaN HEMT, where the gate is the anode and the source is the cathode. The test circuit is shown in Fig. 17(a) and (b) shows the semiconductor transient thermal tester. A T3Ster thermal resistance tester was employed to measure the thermal impedance curve. The thermal resistance test method is according to the JEDEC Standard JESD51-14 [41]. The junction temperature of the device was extracted through real-time monitoring of the variations in the gate voltage [42]. To establish a correlation between the gate voltage and the junction temperature (K-factor), the DUT was gradually heated to measure the correlation between the gate voltage and the junction temperature.

The measurement procedures were conducted as follows: Initially, a high heating current of 10 A was applied across the drain and source terminals of the GaN HEMT to induce a power dissipation of approximately 20 W, thereby heating the device to a thermally equilibrated state. Once thermal equilibrium is achieved, the drain-source heating current is switched OFF. This results in a decreasing thermal transient response curve as the device is cooling. During this cooling phase, a lower sensing current of 10 mA was applied across the gate and source terminals to measure the variation of junction temperature. The relationship between gate voltage and temperature for GaN HEMT is illustrated in Fig. 18. As the temperature increases, the gate-source voltage gradually decreases. The transient thermal resistance curve can be calculated from the cooling curve results [39]. To minimize the impact of gate degradation on the results, the K-factor is recalibrated before each transient thermal resistance measurement to avoid temperature estimation errors. In this study, the T3Ster thermal resistance tester software T3Ster Master was utilized to convert the transient thermal impedance curves into structure function curves.

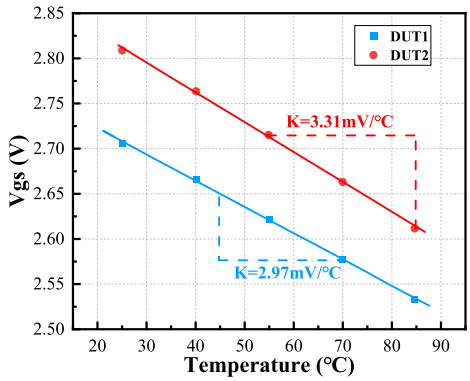


Fig. 18. Gate-source voltage and junction temperature of GaN HEMT devices exhibit a linear relationship.

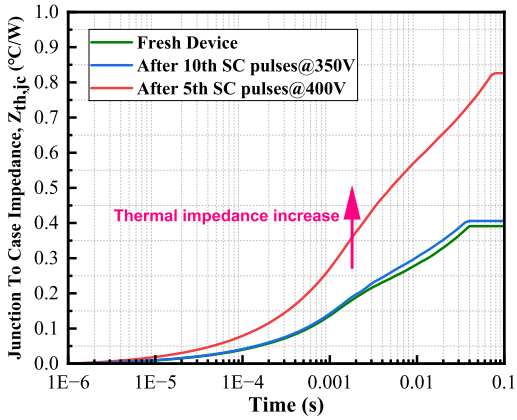


Fig. 19. Measured transient thermal resistance impedance curves before and after SC stress.

B. Transient Thermal Resistance Characteristic Test Results

To establish the relationship between the transient thermal resistance curve of the device and the presence of dislocation defects, the changes in the transient thermal resistance curve of the GaN device before and after exposure to SC stress were compared. A recalibration of the relationship between gate voltage and junction temperature is performed before each transient thermal resistance curve extraction to avoid temperature measurement error induced by device degradation during SC stress.

Fig. 19 shows the transient thermal impedance curve of the chip after repetitive SC pulses. It can be seen that the curves show an early separation with the increase of SC pulses. This early divergence in the thermal impedance curves indicates a rapid increase in thermal resistance, attributed to the accumulation of dislocation defects within the device. This is because the accumulation of dislocation defects inside the chip changes the heat transfer process, and the time required for heat to transfer from the GaN channel layer to the nucleation layer is very small. Given that the heat flow path to the silicon substrate is comparatively longer, more time is necessary for heat dissipation. As defects accumulate in the nucleation layer, the transient thermal impedance curves begin to separate at an earlier stage.

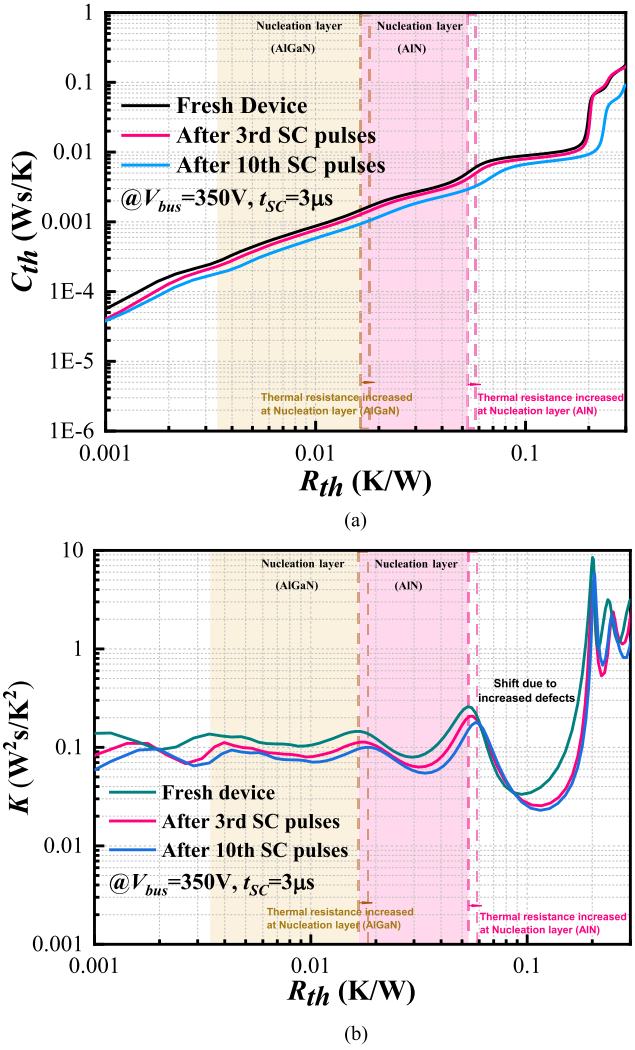


Fig. 20. Structure function curve of the GaN HEMTs after SC stress under 350 V bus voltage condition. (a) Cumulative structure function. (b) Differential structure function.

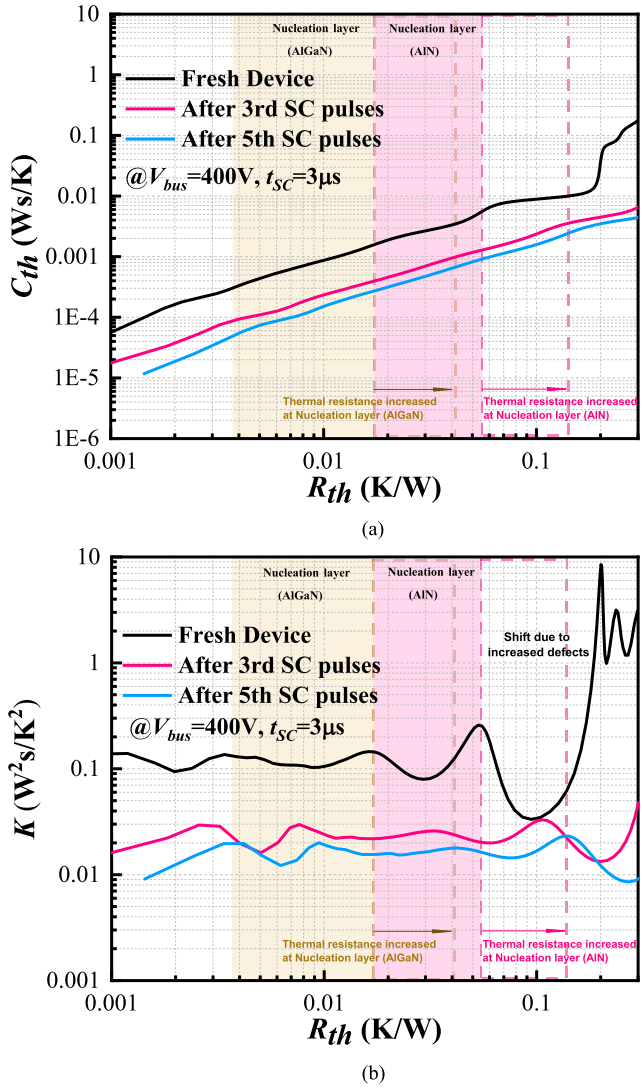
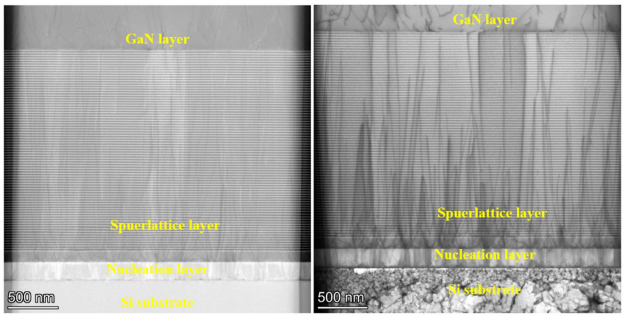


Fig. 21. Structure function curve of the GaN HEMTs after SC stress under 400 V bus voltage condition. (a) Cumulative structure function. (b) Differential structure function.

The accumulation of defects increases with the number of SC pulses and the bus voltage. Fig. 20 illustrates the cumulative and differential structure function curve of the GaN HEMTs after SC stress under 350 V bus voltage conditions. In the cumulative structure function, the flat regions on the curve indicate structures with high thermal resistance and low thermal capacitance within the device, while the steep regions indicate structures with low thermal resistance and high thermal capacitance. With the increased number of SC pulses, the slope of the cumulative structure function curve gradually decreases, and the region of the nucleation layer of the GaN device becomes wider. Simultaneously, the differential structure function after SC stress shows a clear shift in the positions of peaks and valleys. A continuous increase in thermal resistance at the nucleation layer was observed, indicating a gradual increase in dislocation defects within these regions. By analyzing the curve offset, it is found that the thermal resistance of the device's nucleation layer (including AlGaN and AlN) increases by approximately 0.0063 K/W after ten SC pulses.

Fig. 21 illustrates the cumulative and differential structure function curves of the GaN HEMTs after SC stress under 400 V bus voltage conditions. By comparing the cumulative structure function curves of the device under SC stress at 350 V and 400 V bus voltages, it is evident that the slope of the cumulative structure function curve in the nucleation layer and buffer layer region decreases significantly at the higher voltage. This reduction is attributed to the more rapid increase in dislocation defects within the nucleation layer and buffer layer under 400 V conditions. The expansion and accumulation of dislocation defects caused by SC stress result in a drastic reduction in the device's thermal conductivity. The thermal resistance of the device's nucleation layer (including AlGaN and AlN) increases by approximately 0.1139 K/W after five SC pulses under the 400 V condition, which is much larger than that observed under the 350 V condition. This degradation in thermal performance accelerates temperature-dependent failure mechanisms, ultimately resulting in the accelerated thermal breakdown of the GaN HEMT.



(a) (b)

Fig. 22. TEM view of GaN HEMTs showing dislocation defect accumulation with increasing SC stress. (a) Fresh device. (b) After 10th SC pulses at 400 V bus voltage.

C. Dislocation Defects Characterization Verification

To further confirm the accumulation of dislocation defects in GaN HEMT during repetitive SC stress, a comparative transmission electron microscopy (TEM) analysis was performed on fresh devices and devices degraded by repetitive SC stress under 400 V bus voltage conditions. Three samples were analyzed for both the fresh and degraded devices.

Cross-sectional bright-field (BF) TEM images of the degraded devices reveal the presence of dislocation defects at the substrate interface and within the buffer layer, as shown in Fig. 22. A higher density of defects is observed in the degraded GaN HEMT devices after SC stress. The BF TEM images clearly show that the density of dislocation defects in the superlattice buffer layer and nucleation layer of the GaN HEMT device significantly increases after SC stress, compared to the fresh device. These dislocation defects propagate upward from the substrate interface, penetrating through the superlattice layer, and extending into the GaN layer.

VI. Discussion

A. Implications of the Proposed Method

This study provides an in-depth analysis of the thermal degradation in GaN HEMTs under repetitive SC stress, which offers a novel perspective on the rapid thermal runaway failure mechanism of these devices. By systematically analyzing the relationship between dislocation defects and thermal resistance, this work introduces a new method for defect characterization based on transient thermal resistance curves. Through the analysis of variations in cumulative structure function and differential structure function curves before and after SC stress, the location and evolution of defects within the GaN HEMT device can be inferred. A model correlating the transient thermal resistance curve with dislocation defects in GaN HEMT devices is established to illustrate how these defects influence the thermal behavior and reliability of GaN HEMTs.

Unlike conventional defect analysis methods that rely on electrical parameters such as ON-resistance, threshold voltage, and device capacitance, the proposed method provides a direct and noninvasive means to characterize the accumulation of dislocation defects at the substrate interface and within the buffer layer. This is important because the degradation of GaN HEMTs is not limited to electrical properties but also includes thermal degradation caused by dislocation defects. By solving this problem, the proposed method overcomes the limitation of existing traditional electrical parameter-based reliability assessment techniques and expands the scope of GaN HEMT failure analysis.

B. Application Potential of the Proposed Method

The proposed dislocation defect analysis method can be applied not only under SC stress conditions but also in other reliability testing scenarios for GaN HEMT devices, such as surge current stress, where both thermal and electrical degradation may occur. Understanding the evolution of dislocation defects under varying stress conditions will provide a more comprehensive understanding of GaN HEMT failure mechanisms and facilitate the development of targeted mitigation strategies. Moreover, the findings of this study could have significant implications on the design and fabrication of GaN HEMT devices. For example, optimizing the epitaxial layer structure or implementing defect suppression techniques at the substrate interface could reduce the accumulation of dislocation defects, thereby improving the repetitive SC robustness of GaN HEMTs.

From a practical perspective, the proposed method offers a valuable tool for monitoring the health of GaN HEMT devices and predicting thermal runaway failure. It complements existing reliability assessment techniques by providing more accurate estimations of the failure boundaries for GaN HEMT devices. Combining the transient thermal resistance approach with traditional electrical monitoring techniques could establish a comprehensive and predictive reliability framework for GaN-based power electronics.

VII. Conclusion

This article provides a comprehensive analysis of the rapid thermal runaway failure mechanisms in GaN HEMTs under repetitive SC conditions. A method based on transient thermal resistance characterization is proposed to monitor the variation of dislocation defects in the GaN HEMT buffer layer and nucleation layer. Moreover, a thermal model correlating the transient thermal resistance curve with dislocation defects in GaN HEMT devices is established to illustrate the impact of these defects on transient thermal characteristics. The structure function curve of degraded GaN devices reveals that thermal resistance increases in the buffer layer and nucleation layer with an increasing number of SC pulses. The accumulation of dislocation defects is strongly related to the number of SC pulses and the dc bus voltage. The results verify that the accumulation of dislocation defects at the buffer layer and nucleation layer leads to localized overheating within the GaN device, resulting in premature thermal breakdown and limiting the repetitive SC capability of GaN HEMTs. The proposed method can also serve as a diagnostic tool to monitor dislocation defect accumulation in the buffer layer and nucleation layer of GaN HEMTs, especially under harsh operating conditions, thus supporting more accurate lifetime predictions and improving device reliability.

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