Modeling and Design of Four-Switch Buck–Boost Converter With Combined PWM and Phase-Shift Control Scheme

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***Abstract*—The four-switch buck–boost (FSBB) converter has the functions of voltage step-up and step-down as well as positive output, which is suitable for the applications with wide input voltage range. With the combined pulsewidth modulation (PWM) and phase-shift control, all the power switches can realize zero-voltage switching with minimized inductor ripple. In this article, a small-signal model of FSBB converter with the combined PWM and phase-shift control is established. The small-signal characteristics of the power stage are analyzed, and the design method of the closed-loop parameters is proposed, ensuring the stability of the converter under all the operation conditions. Finally, a 420-W prototype of the FSBB converter is fabricated and tested in the lab. The experiment results verify the correctness of the small-signal model and the closed-loop parameter design method.**

***Index Terms*—Four-switch buck–boost (FSBB) converter, small-signal model, zero-voltage switching (ZVS).**

I. Introduction

THE basic nonisolated dc–dc converters with voltage step-up and step-down include the buck–boost, Cuk, Zeta, and SEPIC converters. The buck–boost and Cuk converters output negative voltage, which are not suitable for the applications where a positive output voltage is required. The Zeta and SEPIC converters can output positive voltage, but they contain too many passive components. Besides, the power devices in these converters suffer high voltage stress, which is the sum of the input and output voltages.

The two-switch buck–boost converter features positive output voltage, lower voltage stress, and fewer passive components [1], [2], [3], [4], [5]. By replacing the two diodes with synchronous rectifiers, the four-switch buck–boost (FSBB) converter can be obtained [6], [7], [8], as shown in Fig. 1.

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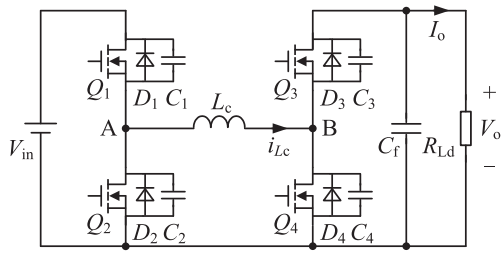

Fig. 1. Four-switch buck–boost converter.

Various control schemes have been proposed for the FSBB converter. The popular one is the two-mode control scheme, with which, the FSBB converter is operated in buck and boost modes when the input voltage is higher and lower than the output voltage, respectively, and the inductor current ripple is minimized [9], [10]. However, the power switches are hard switched. The recently developed wide bandgap (WBG) power switches such as GaN and SiC can operate at a very high switching frequency. Although the turn-OFF loss of the WBG power switches is quite small, the turn-ON loss is still large [11]. So, it is necessary to realize zero-voltage switching (ZVS) for the WBG power switches.

The FSBB converter has three control variables, i.e., the duty cycle of Q_1, denoted by D_{y1}, the duty cycle of Q_4, denoted by D_{y2}, and the duty cycle corresponding to phase-shift between the turn-ON instants of Q_1 and Q_3, denoted by D_θ. With the three available control variables, a constant-frequency quadrilateral current control is proposed [12], which is essentially the combined pulsewidth modulation (PWM) and phase-shift control. With this control scheme, all the power switches realize ZVS over the full input/output voltage and load range, and the rms value of the inductor current is minimized. Additionally, the inductor current ripple decreases with the load since the negative inductor current keeps at a fixed value, leading to an improved light-load efficiency. The implementation methods for the combined PWM and phase-shift control have been proposed [12], [13], [14], [15], [16], [17], [18], [19]. In [12], [13], [14], [15], and [16], the control scheme is implemented by lookup table to avoid complicated real-time calculations. To achieve higher control accuracy, more storage resources are acquired, leading to increased system complexity and expense.

Furthermore, due to the latency in accessing the stored data, the dynamic performance is unsatisfactory. To reduce the storage resource and realize a fast dynamic performance, a simplified real-time calculating method is proposed [17]. Nevertheless, the switching frequency varies with the load to achieve ZVS, which makes the design of EMI filter more difficult. In [18], the control scheme is implemented with constant frequency real-time closed-loop control method for avoiding complex calculation. However, the dynamic response is quite slow due to narrow control bandwidth of the phase-shift closed-loop. Based on [18], the phase-shift duty cycle is approximated in [19], which not only simplify the control circuit, but also improve the dynamic performance.

To design the closed-loop parameters, the small-signal model of the FSBB converter should be established. The small-signal model of the power stage with variable minimum negative inductor current has been established in [20]. In this article, the small-signal model of the power stage is established with fixed negative inductor current, corresponding to the feature of the combined PWM and phase-shift control. This feature is similar to the basic dc–dc converter operated under discontinuous current mode (DCM). In [21], the averaged model for the basic DCM dc–dc converters is proposed. Under DCM, with low frequency perturbation, the inductor current at any time is equal (or approximately equal) to the inductor current after one switching cycle, which implies the average inductor voltage and its small-signal ac voltage are zero. Thus, the inductor current does not appear as a state variable and the order of the power stage is reduced. However, this averaged model can only accurately predict the behavior of a converter in the low-frequency range. Incorporating the dynamic performance of the inductor current, the averaged full-order model is proposed [22], offering higher accuracy up to one-third of the switching frequency.

Different from the basic DCM dc–dc converters, which have only one control variable, the FSBB converter with the combined PWM and phase-shift control has three control variables, and the minimum inductor current is a fixed negative value rather than zero. So, a small-signal model for this FSBB converter is developed in this article, and the small-signal characteristics of the power stage are delved. After that, the small-signal model of the feedback system with the control scheme proposed in [19] is established, and the closed-loop parameter design method is proposed to ensure the stability of the converter under all the operation conditions.

The rest of this article is organized as follows. In Section II, the operating principle of the FSBB converter with the combined PWM and approximate phase-shift control [19] is briefly introduced. Then, the small-signal model of the power stage is built in Section III, and the characteristics of the model are analyzed in Section IV. After that, the small-signal model of FSBB converter with feedback system is established and the design approach of the closed-loop parameters is given in Section V. In Section VI, a prototype of a 420-W FSBB converter is fabricated and tested in the lab, and the experimental results are provided to verify the accuracy of the small-signal model and the design method of the closed-loop parameters. Finally, Section VII concludes this article.

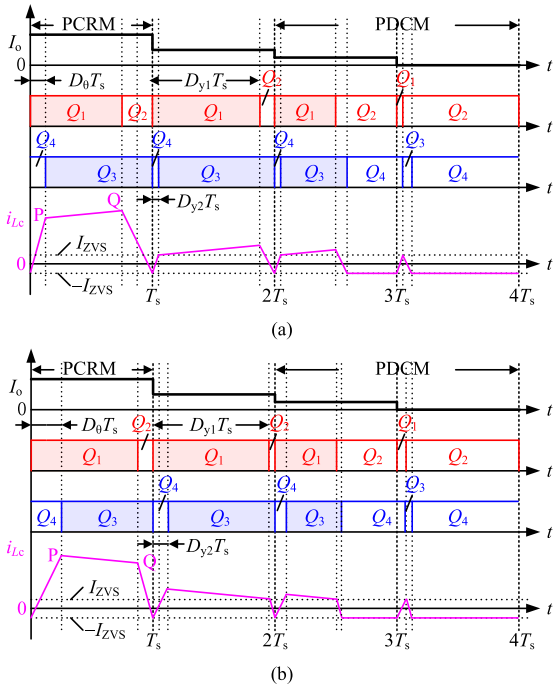

Fig. 2. Key operating waveforms. (a) $V_{in} > V_o$. (b) $V_{in} < V_o$.

II. Operating Principle of the FSBB Converter With Combined PWM and Approximate Phase-Shift Control

The operating principle of the FSBB converter with the combined PWM and approximate phase-shift control scheme has been analyzed in [19], which will be briefly presented here as the basis of establishing the small-signal model.

A. Voltage Conversion Ratio

At steady state, the voltage applied on the inductor within one switching cycle is zero according to the volt-second balance principle. Thus, we have [19]

$$\frac{V_o}{V_{in}} = \frac{D_{y1}}{1 - D_{y2}}. \tag{1}$$

B. Optimal Operating Modes of the FSBB Converter

With the combined PWM and phase-shift control, the optimal operating modes include the pseudocritical continuous current mode (PCRM) and pseudodiscontinuous current mode (PDCM), and Fig. 2 shows the key operating waveforms.

At heavy load, the FSBB converter works under PCRM, and the inductor current i_{Lc} decreases to $-I_{ZVS}$ at the end of each switching cycle, where I_{ZVS} is the minimum current to ensure ZVS for the power switches. As I_o decreases, the segment PQ is translated downward. Define the inductor current at points P and Q as I_P and I_Q, respectively. When I_P ($V_{in} > V_o$) or I_Q ($V_{in} < V_o$) decays to I_{ZVS}, Q_4 or Q_1 is turned OFF immediately to ensure

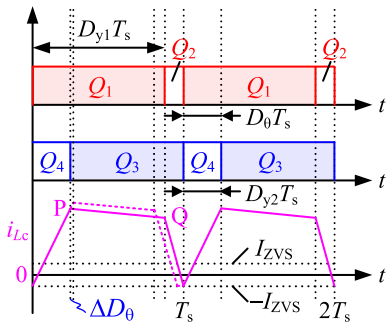

Fig. 3. Waveforms of i_{Lc} with larger approximated D_{θ_PCRM}.

ZVS for Q_3 or Q_2. When I_o further decreases, the converter enters into PDCM, where, i_{Lc} decreases to $-I_{ZVS}$ before the end of each switching cycle and then keeps at $-I_{ZVS}$.

C. Approximate Phase-Shift Control Scheme

As mentioned above, under PCRM, the inductor current decays to $-I_{ZVS}$ at the end of every switching cycle. However, this is hard to realize. If the phase-shift duty cycle is slightly larger than the theoretical one, the inductor current will decay to $-I_{ZVS}$ before the end of the switching cycle, as shown in Fig. 3. This control object can be realized with the approximate phase-shift duty cycle control method proposed in [19], and the approximate phase-shift duty cycle is expressed as

$$D_{\theta\_PCRM\_appr}(v_{in}, i_o) = av_{in} + bi_o + c \tag{2}$$

where, a, b, and c are the constants to ensure the approximated phase-shift duty cycle is larger than the theoretical one with minimized error. Thus, the PCRM changes to PDCM, denoted by PDCM1, hereinafter, and the original PDCM is denoted by PDCM2.

D. Implementation of the Combined PWM and Approximate Phase-Shift Control

Fig. 4 shows the implementation circuit of the combined PWM and approximate phase-shift control scheme [19], where CLK1 and CLK2 correspond to the turn-ON instants of Q_1 and Q_3, respectively. The implementation circuit comprises three subcircuits and are described as follows.

Subcircuit A is used to regulate the output voltage and generate the drive signals for Q_1 and Q_2.

Subcircuit B is used to generate the drive signals for Q_3 and Q_4, where CLK2 is generated in subcircuit C. When i_{Lc} decays to $-I_{ZVS}$, Comp2 outputs a high-level voltage, causing RS trigger2 to reset and turn OFF Q_3. An OR gate is intentionally added here to ensure the correct switching sequence [18].

Subcircuit C is the phase-shift duty cycle generation circuit to obtain CLK2. Under PDCM1, the approximate phase-shift duty cycle is obtained by the proportional addition, corresponding to (2). Under PDCM2, the phase-shift duty cycle is obtained by the calculation circuit, expressed as [18]

$$D_{\theta\_PDCM2} = \begin{cases} D_{y1}\frac{V_o - V_{in}}{V_o} + D_{c\_max} & V_{in} \le V_o \\ D_{c\_max} & V_{in} > V_o \end{cases} \tag{3}$$

where D_{c_max} is the duty cycle corresponding to the maximum time for i_{Lc} to decrease from I_{ZVS} to $-I_{ZVS}$ ($V_{in} < V_o$) or increase from $-I_{ZVS}$ to I_{ZVS} ($V_{in} > V_o$), expressed as

$$D_{c\_max} = \frac{2L_c I_{ZVS}}{V_o T_s} \tag{4}$$

where T_s is the switching period.

The larger one of V_{θ_PDCM1} and V_{θ_PDCM2} is sent to Comp4. An AND gate with input signals Q_θ and Q_1 is added here to ensure that Q_4 is turned OFF no later than Q_1.

III. Small-Signal Model of the Power Stage

In this section, the small-signal model of the power stage of the FSBB converter will be established.

According to Fig. 1, with the averaged switch modeling approach and considering the equivalent series resistance (ESR) of output filter capacitor C_f, the averaged model of FSBB converter is obtained, as shown in Fig. 5, where, Q_1 and Q_3 are replaced with the controlled current sources whose magnitudes are their average current during a switching cycle, and Q_2 and Q_4 are replaced with the controlled voltage source whose magnitudes are their average drain-source voltage during a switching cycle.

Note that the small-signal model of the FSBB converter is built under PDCM. According to Figs. 1–3, the average values of v_{Q2}, v_{Q4}, i_{Q1}, and i_{Q3} in a switching cycle can be expressed as

$$\langle v_{Q2}(t)\rangle_{T_s} = \langle v_{in}(t)\rangle_{T_s} d_{y1} \tag{5}$$

$$\langle v_{Q4}(t)\rangle_{T_s} = \langle v_o(t)\rangle_{T_s} (1 - d_{y2}) \tag{6}$$

$$\langle i_{Q1}(t)\rangle_{T_s} = \frac{-I_{ZVS} + I_P}{2} d_\theta + \frac{I_P + I_Q}{2}(d_{y1} - d_\theta) \tag{7}$$

$$\langle i_{Q3}(t)\rangle_{T_s} = \frac{I_P + I_Q}{2}(d_{y1} - d_\theta) + \frac{I_Q - I_{ZVS}}{2} d_{23} \tag{8}$$

where d_{23} is the duty cycle that corresponds to the time when Q_2 and Q_3 conduct simultaneously, expressed as

$$d_{23} = 1 - d_{y1} - d_{y2} + d_\theta. \tag{9}$$

According to Figs. 2 and 3, I_P and I_Q can be expressed as

$$I_P = -I_{ZVS} + \frac{\langle v_{in}(t)\rangle_{T_s}}{L_c} d_\theta T_s \tag{10}$$

$$I_Q = -I_{ZVS} + \frac{\langle v_o(t)\rangle_{T_s}}{L_c} d_{23} T_s. \tag{11}$$

Substituting (10) and (11) into (8), we have

$$\langle i_{Q3}(t)\rangle_{T_s} = -I_{ZVS}(1 - d_{y2}) + \frac{\langle v_{in}(t)\rangle_{T_s}}{2L_c} d_\theta (d_{y1} - d_\theta) T_s + \frac{\langle v_o(t)\rangle_{T_s}}{2L_c}(1 - d_{y2}) d_{23} T_s. \tag{12}$$

By imposing small-signal perturbations into (5), (6), and (12), eliminating the steady-state quantities and neglecting the high-order small-signal perturbations, we have

$$\hat{v}_{Q2} = V_{in}\hat{d}_{y1} + D_{y1}\hat{v}_{in} \tag{13}$$

$$\hat{v}_{Q4} = -V_o\hat{d}_{y2} + (1 - D_{y2})\hat{v}_o \tag{14}$$

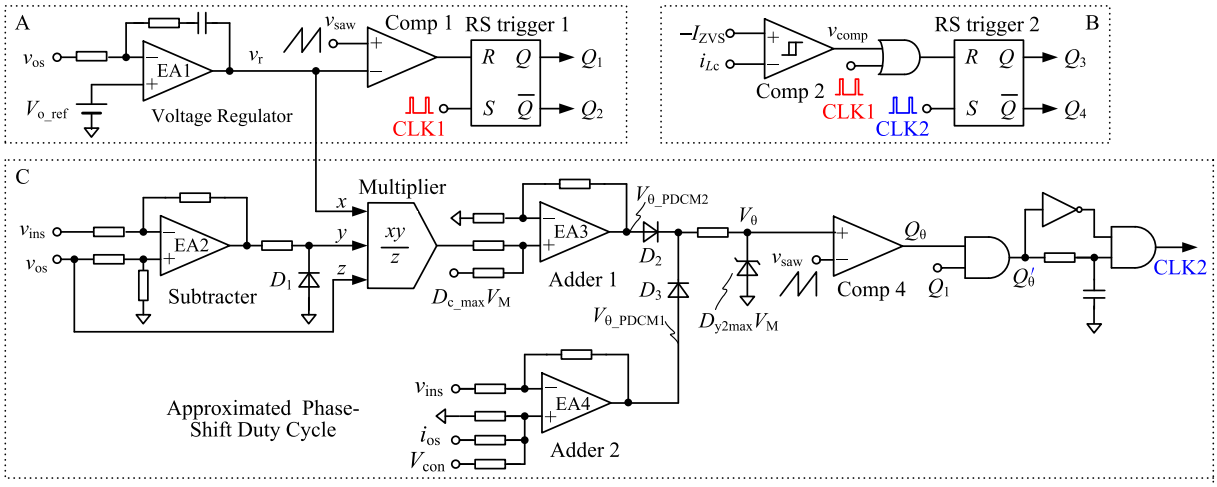

Fig. 4. Implementation circuit of the combined PWM and approximate phase-shift control scheme.

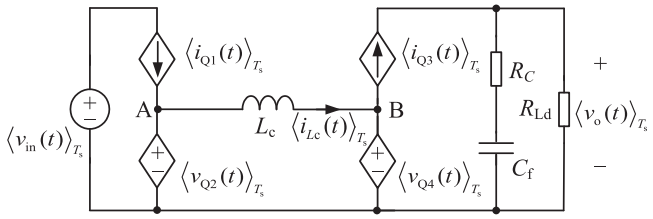

Fig. 5. Averaged model of FSBB converter.

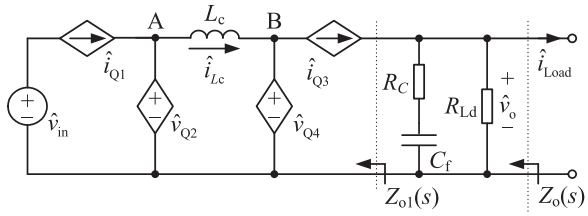

Fig. 6. Small-signal equivalent circuit of the FSBB converter.

$$\hat{i}_{Q3} = \frac{T_s}{2L_c}\left\{\begin{array}{l} V_{in}\left(D_\theta - D_{y1}\right)\hat{d}_{y1} + \left[\frac{2L_c I_{ZVS}}{T_s} - V_o\left(1 + D_{23} - D_{y2}\right)\right]\hat{d}_{y2} \\ +2V_{in}\left(D_{y1} - D_\theta\right)\hat{d}_\theta + D_{23}\left(1 - D_{y2}\right)\hat{v}_o + \left(D_{y1} - D_\theta\right)D_\theta\hat{v}_{in} \end{array}\right\}. \quad (15)$$

According to Fig. 2, the average values of i_{Lc} in a switching period can be expressed as

$$\langle i_{Lc}(t)\rangle_{T_s} = -I_{ZVS} + \frac{\langle v_{in}(t)\rangle_{T_s}}{2L_c} d_\theta d_{y1} T_s + \frac{\langle v_o(t)\rangle_{T_s}}{2L_c}\left(1 - d_{y2}\right) d_{23} T_s. \quad (16)$$

Likewise, by imposing small-signal perturbations into (16), eliminating the steady-state quantities and neglecting the high-order small-signal perturbations, we have

$$\hat{d}_{y2} = \frac{\left(D_\theta - D_{y1}\right)\hat{d}_{y1} + 2D_{y1}\hat{d}_\theta + \frac{D_{23}\left(1-D_{y2}\right)}{V_{in}}\hat{v}_o + \frac{D_{y1}D_\theta}{V_{in}}\hat{v}_{in} + \frac{2L_c}{V_{in}T_s}\hat{i}_{Lc}}{\left(1 + D_{23} - D_{y2}\right)V_o/V_{in}}. \quad (17)$$

Substituting (17) into (14) and (15), respectively, and applying Laplace transformation, lead to (18) and (19) shown at the bottom of this page.

Fig. 6 shows the small-signal equivalent circuit of FSBB converter, where $\hat{v}_{Q2}$, $\hat{v}_{Q4}(s)$, and $\hat{i}_{Q3}(s)$ are given in (13), (18), and (19), respectively. According to Fig. 6, the control-to-output transfer functions $G_{vdy1}(s)$ and $G_{vd\theta}(s)$, and the line-to-output transfer function $G_{vg}(s)$ can be, respectively, expressed as

$$\hat{v}_{Q4}(s) = \frac{1}{1 + D_{23} - D_{y2}}\left[V_{in}\left(D_{y1} - D_\theta\right)\hat{d}_{y1}(s) - 2V_{in}D_{y1}\hat{d}_\theta(s) + \left(1 - D_{y2}\right)^2\hat{v}_o(s) - D_{y1}D_\theta\hat{v}_{in}(s) + \frac{2L_c}{T_s}\hat{i}_{Lc}(s)\right] \quad (18)$$

$$\hat{i}_{Q3}(s) = \frac{1}{1 + D_{23} - D_{y2}} \times \left\{\begin{array}{l} \left(D_{y1} - D_\theta\right)\frac{V_{in}}{V_o}I_{ZVS}\hat{d}_{y1}(s) + \left[D_\theta\left(1 + D_{23} - D_{y2}\right)\frac{V_{in}T_s}{L_c} - 2\left(1 - D_{y2}\right)I_{ZVS}\right]\hat{d}_\theta(s) + \left(D_{y2} - 1\right)D_{23}\frac{I_{ZVS}}{V_o}\hat{v}_o(s) \\ +D_\theta\left[\left(1 + D_{23} - D_{y2}\right)\frac{D_\theta T_s}{2L_c} - D_{y1}\frac{I_{ZVS}}{V_o}\right]\hat{v}_{in}(s) + \left(1 + D_{23} - D_{y2} - \frac{2L_c I_{ZVS}}{V_o T_s}\right)\hat{i}_{Lc}(s) \end{array}\right\}. \quad (19)$$

TABLE I
EXPRESSIONS OF THE PARAMETERS IN (20)–(22)

Parameters	Expressions
h_1	$\dfrac{(1+D_{23}-D_{y2})V_oL_c+V_oR_{Ld}\left[\left(1-D_{y2}+\dfrac{D_{y1}-D_\theta}{1+D_{23}-D_{y2}}\dfrac{2L_cI_{ZVS}}{V_oT_s}\right)(1-D_{y2})R_CC_f+\dfrac{2L_c}{T_s}C_f+\dfrac{(1-D_{y2})D_{23}L_cI_{ZVS}}{V_o}\right]}{L_cR_{Ld}C_f\left[(1+D_{23}-D_{y2})V_o+(1-D_{y2})D_{23}I_{ZVS}R_C\right]}\approx\dfrac{1}{R_{Ld}C_f}+\dfrac{2+\dfrac{(1-D_{y2})D_{23}T_sI_{ZVS}}{C_fV_o}}{(1+D_{23}-D_{y2})T_s}$
h_2	$\dfrac{\dfrac{2L_cV_o}{T_s}+\left(1-D_{y2}-\dfrac{2L_cI_{ZVS}}{V_oT_s}\right)(1-D_{y2})V_oR_{Ld}}{L_cR_{Ld}C_f\left[(1+D_{23}-D_{y2})V_o-(D_{y2}-1)D_{23}I_{ZVS}R_C\right]}\approx\dfrac{\dfrac{2L_c}{T_s}+\left(1-D_{y2}-\dfrac{2L_cI_{ZVS}}{V_oT_s}\right)(1-D_{y2})R_{Ld}}{L_cR_{Ld}C_f(1+D_{23}-D_{y2})}$
g_1	$-\dfrac{(D_{y1}-D_\theta)V_{in}I_{ZVS}R_C}{(1+D_{23}-D_{y2})V_o-(D_{y2}-1)D_{23}I_{ZVS}R_C}\approx-\dfrac{(D_{y1}-D_\theta)V_{in}I_{ZVS}R_C}{(1+D_{23}-D_{y2})V_o}$
g_2	$-\dfrac{\left[D_\theta(1+D_{23}-D_{y2})-D_{y1}\dfrac{2L_cI_{ZVS}}{V_oT_s}\right]V_{in}V_oR_CT_s}{\left[(1+D_{23}-D_{y2})V_o-(D_{y2}-1)D_{23}I_{ZVS}R_C\right]L_c}\approx-\dfrac{V_{in}R_CT_s}{L_c}\left(D_\theta-\dfrac{D_{y1}}{1+D_{23}-D_{y2}}\dfrac{2L_cI_{ZVS}}{V_oT_s}\right)$
g_3	$-\dfrac{\left[D_\theta(1+D_{23}-D_{y2})-D_{y1}\dfrac{2L_cI_{ZVS}}{V_oT_s}\right]D_\theta V_oT_sR_C}{2L_c\left[(1+D_{23}-D_{y2})V_o-(D_{y2}-1)D_{23}I_{ZVS}R_C\right]}\approx-\dfrac{D_\theta T_sR_C}{2L_c}\left(D_\theta-\dfrac{D_{y1}}{1+D_{23}-D_{y2}}\dfrac{2L_cI_{ZVS}}{V_oT_s}\right)$
Zeros	$z_1=\dfrac{2\left(D_{23}\dfrac{V_oT_s}{L_cI_{ZVS}}-1\right)}{(D_{y1}-D_\theta)T_s}$, $z_2=\dfrac{2(D_{y1}-D_\theta)}{\left[D_\theta(1+D_{23}-D_{y2})-D_{y1}\dfrac{2L_cI_{ZVS}}{V_oT_s}\right]T_s}$, $z_3=\dfrac{2D_{y1}\left(2D_{23}-\dfrac{2L_cI_{ZVS}}{V_oT_s}\right)+2(D_{y1}^2-D_\theta^2)}{\left[D_\theta(1+D_{23}-D_{y2})-D_{y1}\dfrac{2L_cI_{ZVS}}{V_oT_s}\right]D_\theta T_s}$, $z_{ESR}=\dfrac{1}{R_CC_f}$

Note that, R_C is the ESR of the filter capacitor and is quite small. So, $\left(1-D_{y2}+\dfrac{D_{y1}-D_\theta}{1+D_{23}-D_{y2}}\dfrac{2L_cI_{ZVS}}{V_oT_s}\right)(1-D_{y2})R_C$ is much smaller than $2L_c/T_s$ and is neglected, which is applied in the approximation of h_1. Likewise, $(D_{y2}-1)D_{23}I_{ZVS}R_C$ is much smaller than $(1+D_{23}-D_{y2})V_o$ and is neglected, which is applied in the approximation of h_1, h_2, g_1, g_2, and g_3.

$$G_{vdy1}(s)=\left.\frac{\hat{v}_o(s)}{\hat{d}_{y1}(s)}\right|_{\substack{\hat{v}_{in}(s)=0\\ \hat{d}_\theta(s)=0\\ i_{Load}(s)=0}}=\frac{g_1(s-z_1)(s+z_{ESR})}{s^2+h_1s+h_2} \quad (20)$$

$$G_{vd\theta}(s)=\left.\frac{\hat{v}_o(s)}{\hat{d}_\theta(s)}\right|_{\substack{\hat{v}_{in}(s)=0\\ \hat{d}_{y1}(s)=0\\ i_{Load}(s)=0}}=\frac{g_2(s-z_2)(s+z_{ESR})}{s^2+h_1s+h_2} \quad (21)$$

$$G_{vg}(s)=\left.\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)}\right|_{\substack{\hat{d}_{y1}(s)=0\\ \hat{d}_\theta(s)=0\\ i_{Load}(s)=0}}=\frac{g_3(s-z_3)(s+z_{ESR})}{s^2+h_1s+h_2} \quad (22)$$

where, $h_1, h_2, g_1, g_2, g_3, z_1, z_2, z_3$, and z_{ESR} are given in Table I. $s^2+h_1s+h_2$ is rewritten in the form of $(s+p_1)(s+p_2)$, and p_1 and p_2 are expressed as

$$p_1=\frac{1}{C_fV_o}\left[I_o+I_{ZVS}(1-D_{y2})\left(\frac{1-D_{y2}}{2L_cI_{ZVS}}V_oT_s-1\right)\right] \quad (23)$$

$$p_2=\frac{2}{(1+D_{23}-D_{y2})T_s}=\frac{2}{2-D_{y1}-2D_{y2}+D_\theta}f_s \quad (24)$$

where $f_s=1/T_s$ is the switching frequency.

Besides, by setting $\hat{v}_{in}(s)$, $\hat{d}_\theta(s)$, and $\hat{d}_{y1}(s)$ to zero, the output impedance $Z_o(s)$ can be obtained, expressed as

$$Z_o(s)=-\left[Z_{o1}(s)//R_{Ld}//\left(\frac{1}{sC_f}+R_C\right)\right] \quad (25)$$

where $Z_{o1}(s)$ is the output impedance excluding C_f and R_{Ld}, which can be expressed as

$$Z_{o1}(s)=-\left.\frac{\hat{v}_o(s)}{\hat{i}_{Q3}(s)}\right|_{\substack{\hat{v}_{in}(s)=0\\ \hat{d}_{y1}(s)=0\\ \hat{d}_\theta(s)=0}}=\frac{1+D_{23}-D_{y2}}{\frac{(1+D_{23}-D_{y2}-\frac{2L_cI_{ZVS}}{V_oT_s})(D_{y2}-1)^2T_s}{2L_c+sL_c(1+D_{23}-D_{y2})T_s}+(1-D_{y2})\frac{I_{ZVS}}{V_o}}. \quad (26)$$

Therefore, the output voltage variation is a linear combination of the four independent inputs, i.e.,

$$\hat{v}_o(s)=G_{vdy1}(s)\hat{d}_{y1}(s)+G_{vd\theta}(s)\hat{d}_\theta(s)+G_{vg}(s)\hat{v}_{in}(s)-Z_o(s)\hat{i}_{Load}(s). \quad (27)$$

IV. SMALL-SIGNAL CHARACTERISTICS OF THE POWER STAGE

So far, the expressions for the transfer functions of the FSBB power stage have been derived. To facilitate the control circuit design, the small-signal characteristics of the power stage are discussed in this section.

By observing (20)–(22), the transfer functions have two poles and four zeros. Except z_{ESR}, the poles and zeros are related to D_{y1}, D_{y2}, and D_θ, whose expressions are given in Table II [18].

A. Characteristics of the Poles

1) Pole p_1: The expression of pole p_1 is given in (23). Since $2L_cI_{ZVS}/(V_oT_s)$, which equals to D_{c_max}, is around 0.1, the term that contains I_{ZVS} has the same order of magnitude as I_o.

TABLE II
EXPRESSIONS OF THE CONTROL VARIABLES

Operating mode	Expressions
PDCM1	$D_{y1}=\dfrac{\frac{V_o}{V_{in}}+1-\frac{L_cI_{ZVS}}{V_{in}T_s}+\sqrt{\left(\frac{V_o}{V_{in}}+1-\frac{L_cI_{ZVS}}{V_{in}T_s}\right)^2-\left[\left(\frac{V_o}{V_{in}}\right)^2+\frac{V_o}{V_{in}}+1\right]\left(\frac{2L_cI_o}{V_{in}T_s}+1\right)}}{\frac{V_o}{V_{in}}+1+\frac{V_{in}}{V_o}}$, $D_{y1}=\left(1-D_{y2}\right)\frac{V_o}{V_{in}}$, $D_\theta=D_{y2}$
PDCM2 ($V_{in}\le V_o$)	$D_{y1}=\dfrac{V_{in}}{V_o}\dfrac{L_cI_{ZVS}\left(1-2\frac{V_{in}}{V_o}\right)+\sqrt{L_c^2I_{ZVS}^2+2L_cI_o\left(V_o-V_{in}\right)T_s}}{\left(V_o-V_{in}\right)T_s}$, $D_{y2}=1-\frac{V_{in}}{V_o}D_{y1}$, $D_\theta=\frac{V_o-V_{in}}{V_o}D_{y1}+\frac{2L_cI_{ZVS}}{V_oT_s}$
PDCM2 ($V_{in}>V_o$)	$D_{y1}=\dfrac{L_cI_{ZVS}\left(1-2\frac{V_o}{V_{in}}\right)+\sqrt{L_c^2I_{ZVS}^2+2L_cI_o\frac{V_o}{V_{in}}\left(V_{in}-V_o\right)T_s}}{\left(V_{in}-V_o\right)T_s}$, $D_{y2}=1-\frac{V_{in}}{V_o}D_{y1}$, $D_\theta=\frac{2L_cI_{ZVS}}{V_{in}T_s}$

Moreover, for the output filtering requirement, $I_o/(C_fV_o)$, which is equal to $1/(C_fR_{Ld})$, should be much less than f_s. Therefore, p_1 is less than f_s.

In (23), $1-D_{y2}$ stands for the duty cycle of Q_3. To realize power transfer, the duration that Q_3 is conducting must be no less than the time that the inductor current decreases from I_{ZVS} to $-I_{ZVS}$ (see Fig. 2). Therefore, we have

$$1-D_{y2}\ge\frac{2L_cI_{ZVS}}{V_oT_s}. \tag{28}$$

At null-load, the transferred power is zero, and the equal sign of (28) is taken. Thus, according to (23) and (28), p_1 reaches its minimum value of zero only at null-load.

2) Pole p_2: The expression of pole p_2 is given in (24). Substituting the expression of D_θ under different operating conditions given in Table II into (24), we have

$$p_2=\begin{cases}\frac{2}{2-D_{y1}-D_{y2}}f_s, & \text{PDCM1}\\ \frac{2}{\frac{V_{in}}{V_o}D_{y1}+D_{c\_max}}f_s, & \text{PDCM2}\quad(V_{in}\le V_o)\\ \frac{2}{2-2D_{y2}-D_{y1}+D_\theta}f_s, & \text{PDCM2}\quad(V_{in}>V_o).\end{cases} \tag{29}$$

According to (29), we have the following conclusion.

1) Since both D_{y1} and D_{y1} are smaller than 1, p_2 under PDCM1 is higher than f_s.
2) As seen from Fig. 2(b), when $V_{in}\le V_o$, D_{y1} reaches its maximum value at the boundary of PDCM1 and PDCM2, which equal to $1-D_{c\_max}$. Meanwhile, considering $V_{in}=V_o$, thus, p_2 under PDCM2 ($V_{in}\le V_o$) is higher than $2f_s$.
3) As seen from Fig. 2(a), when $V_{in}>V_o$, we have $D_{y1}\ge D_\theta$. Meanwhile, D_{y2} are smaller than 1. So, p_2 under PDCM2 ($V_{in}>V_o$) is higher than f_s.

B. Characteristics of the Zeros

1) Zero z_1: The expression of zero z_1 is given in Table I. When $V_{in}=V_o$ and the converter is operated at the boundary of PDCM1 and PDCM2, D_{23} reaches its minimum value, which is D_{c_max}, and $D_{y1}-D_\theta$ reaches its maximum value, which is $1-2D_{c\_max}$. In this case, z_1 reaches its minimum value under all the operating conditions. Thus, we have

$$\begin{aligned}z_1&=\frac{2\left(D_{23}\frac{V_oT_s}{L_cI_{ZVS}}-1\right)}{\left(D_{y1}-D_\theta\right)T_s}=\frac{2(2D_{23}-D_{c\_max})}{D_{c\_max}\left(D_{y1}-D_\theta\right)T_s}\\&\ge\frac{2(2D_{c\_max}-D_{c\_max})}{D_{c\_max}\left(1-2D_{c\_max}\right)T_s}=\frac{2f_s}{1-2D_{c\_max}}=2.5f_s.\end{aligned} \tag{30}$$

Note that, D_{c_max} is usually designed to be around 0.1.

2) Zero z_2: In Table I, the expression of zero z_2 is given. Substituting D_θ in Table II, (4) and (9) into it, and considering (1), we have

$$z_2=\begin{cases}\frac{2\left[\left(1+\frac{V_{in}}{V_o}\right)D_{y1}-1\right]f_s}{\frac{V_{in}}{V_o}\left(1-\frac{V_{in}}{V_o}\right)D_{y1}^2-(1+D_{c\_max})D_{y1}+1}, & \text{PDCM1}\\ \frac{2\left(\frac{V_{in}}{V_o}D_{y1}-D_{c\_max}\right)f_s}{\left(1-\frac{V_{in}}{V_o}\right)\frac{V_{in}}{V_o}D_{y1}^2+D_{c\_max}^2}, & \text{PDCM2}\quad(V_{in}\le V_o)\\ \frac{2\left(D_{y1}-\frac{V_o}{V_{in}}D_{c\_max}\right)f_s}{\left(1-\frac{V_o}{V_{in}}\right)D_{c\_max}D_{y1}+\left(\frac{V_o}{V_{in}}\right)^2D_{c\_max}^2}, & \text{PDCM2}\quad(V_{in}>V_o).\end{cases} \tag{31}$$

Under PDCM1, taking the derivative of the denominator of z_2 with respect to D_{y1}, we have

$$Deri=2\frac{V_{in}}{V_o}\left(1-\frac{V_{in}}{V_o}\right)D_{y1}-(1+D_{c\_max}). \tag{32}$$

Obviously, the maximum value of the first term of *Deri* is $D_{y1}/2$, which is smaller than 0.5. So, *Deri* is always a negative value, implying the denominator is a monotonically decreasing function of D_{y1}. Meanwhile, it is easy to see that the numerator of the expression of z_2 increases with D_{y1}. So, z_2 increases with D_{y1}.

In [18], the maximum D_{y2} is given as

$$D_{y2max}=\frac{\left(\frac{V_o}{V_{in}}\right)^2+\frac{L_cI_{ZVS}}{V_{in}T_s}}{\left(\frac{V_o}{V_{in}}\right)^2+\frac{V_o}{V_{in}}+1}. \tag{33}$$

So, according to (1), the minimum D_{y1} is

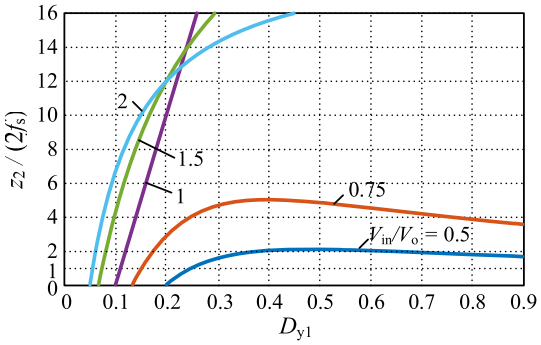

Fig. 7. Curves of z_2 as the function of D_{y1} under PDCM2 at different input voltage.

$$D_{y1\min} = \frac{V_o}{V_{in}}(1 - D_{y2\max}) = \frac{\frac{V_o}{V_{in}} + 1 - \frac{L_c I_{ZVS}}{V_{in} T_s}}{\frac{V_o}{V_{in}} + 1 + \frac{V_{in}}{V_o}}. \quad (34)$$

Substituting (34) into the expression of z_2 under PDCM1, and considering (4), the minimum value of z_2 is derived as

$$z_{2\min} = \frac{\left(\frac{V_o}{V_{in}} + 1 + \frac{V_{in}}{V_o}\right)\left(2 - \frac{V_o}{V_{in}} D_{c\_max} - D_{c\_max}\right) f_s}{\left\{\begin{array}{l} \frac{D_{c\_max}(D_{c\_max}-1)}{2}\left(\frac{V_o}{V_{in}}\right)^2 + \left(\frac{3D_{c\_max}^2}{4} - 2.5D_{c\_max} + 1\right)\frac{V_o}{V_{in}} \\ +2 - 1.5D_{c\_max} + \frac{D_{c\_max}^2}{4} \end{array}\right\}}. \quad (35)$$

According to (35), with D_{c_max} being 0.1 and V_o/V_{in} with [0.5, 2], $z_{2\min}$ is about $2f_s$.

Under PDCM2, according to (31), the curves of z_2 as the function of D_{y1} at different input voltage are depicted, as shown in Fig. 7. As seen from Table II, D_{y1} under PDCM2 increases with the load current. At about higher than 2% full load, D_{y1} will make z_2 larger than $2f_s$.

3) Zero z_3: The expression of zero z_3 is also given in Table I. Since $D_{y1} > D_\theta$, we have

$$z_3 = \frac{2D_{y1}(2D_{23} - D_{c\_max}) + 2\left(D_{y1}^2 - D_\theta^2\right)}{\left[D_\theta(1 + D_{23} - D_{y2}) - D_{y1}D_{c\_max}\right] D_\theta T_s}$$
$$> \frac{2D_\theta(2D_{23} - D_{c\_max}) + 2\left(D_{y1} - D_\theta^2\right)}{\left[D_\theta(1 + D_{23} - D_{y2}) - D_\theta D_{c\_max}\right] D_\theta T_s} = \frac{1}{D_\theta} 2f_s > 2f_s. \quad (36)$$

So far, the characteristics of z_1, z_2, and z_3 have been under all the operating conditions are discussed, and they are right half-plane zeros. According to Table I, z_{ESR} is the left half-plane zero, which is caused by the ESR of output filter capacitor and is much higher than f_s.

With the characteristics of the transfer functions, the design of the closed-loop parameters will be given in the following section. Note that, based on the control implementation circuit given in Fig. 4, the approximate error in the duty cycle is small. Therefore, the characteristics of the zeros and poles are applicable for the closed-loop parameter design.

V. Analysis and Design of the Closed-Loop Parameters

A. Small-Signal Model of the Closed-Loop

According to (27), the control block diagram of the FSBB converter can be obtained, as shown in the shadow block in Fig. 8. As seen from Fig. 4, D_{y1} is obtained by the voltage regulator, and D_θ is different under different operating modes. Under PDCM1, D_{θ_PDCM1} is obtained by the approximate phase-shift control circuit. Under PDCM2, D_θ is obtained through the calculation circuit.

By imposing small-signal perturbations into (2) and (3), respectively, eliminating the steady-state quantities and neglecting the high-order small-signal perturbations, we have

$$\hat{d}_{\theta\_PDCM1} = a\hat{v}_{in} + b\hat{i}_o = a\hat{v}_{in} + b\frac{\hat{v}_o}{R_{Ld}} \quad (37)$$

$$\hat{d}_{\theta\_PDCM2} = \begin{cases} \frac{V_o - V_{in}}{V_o}\hat{d}_{y1} + \frac{D_{y1}V_{in}}{V_o^2}\hat{v}_o - \frac{D_{y1}}{V_o}\hat{v}_{in} & V_{in} \le V_o \\ 0 & V_{in} > V_o \end{cases}. \quad (38)$$

Therefore, the small-signal model of the FSBB converter with feedback system can be obtained, as shown in Fig. 8, where $G_v(s)$ is the output voltage regulator, H_v is the output voltage sense gain; $G_{PWM}(s) = 1/V_m$ is the transfer function of PWM modulator. The part of phase-shift approximation and phase-shift calculation in Fig. 8 are based on (37) and (38), respectively.

According to Fig. 8, the voltage loop gain under PDCM1, denoted by T_1, and the voltage loop gain under PDCM2 with $V_{in} < V_o$ and $V_{in} \ge V_o$, denoted by $T_{2\_Vin\le Vo}$, $T_{2\_Vin>Vo}$, respectively, can be expressed as

$$T_1(s) = H_v G_{PWM}(s) G_v(s) G_{vdy1}(s) - \frac{1}{R_{Ld}} b G_{vd\theta}(s) =$$
$$H_v G_{PWM}(s) G_{vdy1}(s)\left[G_v(s) - \frac{b}{H_v G_{PWM}(s) R_{Ld}} \frac{g_2(s - z_2)}{g_1(s - z_1)}\right] \quad (39)$$

$$T_{2\_V_{in}\le V_o}(s) = H_v G_{PWM}(s) G_v(s)$$
$$\left(G_{vdy1}(s) + \frac{V_o - V_{in}}{V_o} G_{vd\theta}(s)\right) - \frac{D_{y1}V_{in}}{V_o^2} G_{vd\theta}(s) =$$
$$H_v G_{PWM}(s) G_{vdy1}(s)\left[1 + \frac{V_o - V_{in}}{V_o}\frac{g_2(s - z_2)}{g_1(s - z_1)}\right] \cdot [G_v(s)$$
$$- \frac{D_{y1}V_{in}}{H_v G_{PWM}(s)} \frac{g_2(s - z_2)}{V_o^2 g_1(s - z_1) + V_o(V_o - V_{in}) g_2(s - z_2)}] \quad (40)$$

$$T_{2\_V_{in}>V_o}(s) = H_v G_{PWM}(s) G_{vdy1}(s) G_v(s). \quad (41)$$

B. Design Approach of the Closed-Loop Parameters

Usually, the cut-off frequency f_c of the voltage closed-loop is set at $f_s/10$. So, according to the analysis in Section IV, under PDCM1 and PDCM2 (above 2% full load), the frequency of z_1 and z_2 is much higher than f_c, thus, we have $(s - z_2)/(s - z_1) \approx z_2 / z_1$. Therefore, (39) and (40) can be approximate as

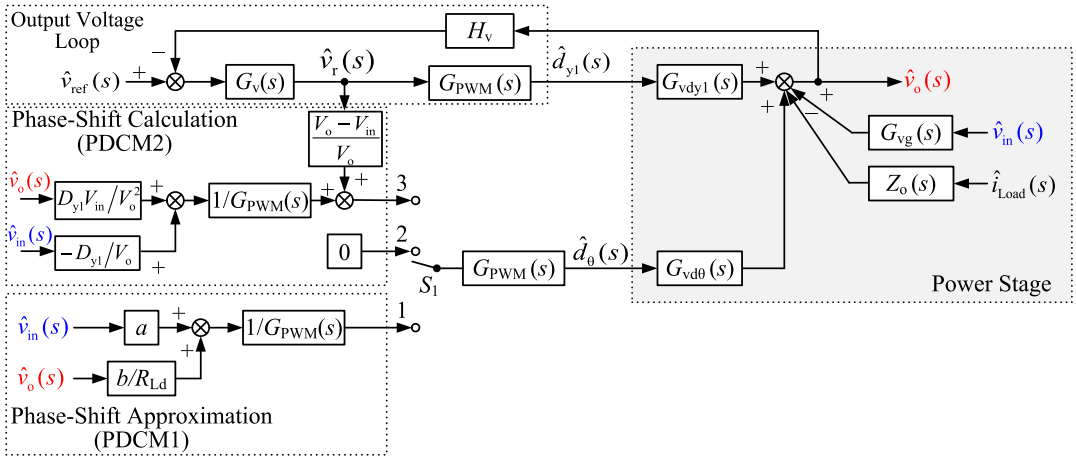

Fig. 8. Small-signal model of FSBB converter with feedback system.

$$T_1(s)=H_vG_{PWM}(s)G_{vdy1}(s)\left(G_v(s)-\frac{b}{H_vG_{PWM}(s)R_{Ld}}\frac{g_2z_2}{g_1z_2}\right) \tag{42}$$

$$T_{2\_V_{in}\le V_o}(s)=H_vG_{PWM}(s)G_{vdy1}(s)\left(1+\frac{V_o-V_{in}}{V_o}\frac{g_2z_2}{g_1z_1}\right)\cdot\left[G_v(s)-\frac{D_{y1}V_{in}}{H_vG_{PWM}(s)}\frac{g_2z_2}{V_o^2g_1z_1+V_o\left(V_o-V_{in}\right)g_2z_2}\right]. \tag{43}$$

As discussed in Section IV-B, z_1 and z_{ESR} are higher than $2f_s$. So, $s+z_{ESR}\approx z_{ESR}$ and $s-z_1\approx -z_1$ can be obtained at f_c. Thus, according to (20), $G_{vdy1}(s)$ can be approximated as

$$G_{vdy1\_appr}(s)=-\frac{g_1z_1z_{ESR}}{(s+p_1)(s+p_2)}. \tag{44}$$

As seen from (41), (42), and (43), the loop gains are different under different operating conditions. Therefore, $G_v(s)$ should be designed properly to ensure the stability requirement under all the operating conditions.

Usually, PI regulator is adopted as $G_v(s)$, expressed as

$$G_v(s)=K_p+K_i/s. \tag{45}$$

Substituting (45) into (41), (42), and (43), respectively, the loop gains can be uniformed as the product of the constant terms $G_c(s)$, transfer function $G_{vdy1\_appr}(s)$, and equivalent regulator $G_{ve}(s)$, i.e.,

$$T(s)=G_c(s)G_{vdy1\_appr}(s)G_{ve}(s) \tag{46}$$

where $G_c(s)$ and $G_{ve}(s)$ depend on the operating condition, i.e.,

$$G_c(s)=\begin{cases}H_vG_{PWM}(s), & \text{PDCM1}\\ H_vG_{PWM}(s)\left(1+\frac{V_o-V_{in}}{V_o}\frac{g_2z_2}{g_1z_1}\right), & \text{PDCM2}\quad(V_{in}\le V_o)\\ H_vG_{PWM}(s), & \text{PDCM2}\quad(V_{in}>V_o)\end{cases} \tag{47}$$

$$G_{ve}(s)=K_{pe}+K_i/s \tag{48}$$

where the expression is given in (49), shown at the bottom of this page.

It is noted that, at null load, $D_{y1}=D_\theta$, thus, z_1 is infinite. According to (40), the $G_c(s)$ and $G_{ve}(s)$ under PDCM2 when $V_{in}\le V_o$ is the same as that under PDCM2 when $V_{in}>V_o$.

In (46), since $G_c(s)$ is a constant term, the phase of $T(s)$ is the sum of $\angle G_{vdy1\_appr}(s)$ and $\angle G_{ve}(s)$.

In (44), g_1 is a negative value (see Table I). So, $\angle G_{vdy1\_appr}(s)$ is determined by the poles p_1 and p_2. Pole p_1 reaches its minimum value of 0 at null-load, which introduces a phase lag of $-90°$ across all frequencies. As discussed in Section IV-A, the minimum value of p_2 is f_s. Due to the wide operating range of the converter, f_c varies a lot as well. In this article, the maximum f_c is set at $0.1\,f_s$. At the frequency lower than $0.1\,f_s$, the maximum phase lag caused by p_2 is $-30°$. So, the minimum value of $\angle G_{vdy1\_appr}(s)$ is $-120°$.

$$K_{pe}=\begin{cases}\underbrace{K_p-\frac{bg_2z_2}{H_vG_{PWM}(s)R_{Ld}g_1z_1}}_{K_{pe1}}, & \text{PDCM1}\\ \underbrace{K_p-\frac{(1-D_{y2})g_2z_2}{H_vG_{PWM}(s)\left[V_og_1z_1+(V_o-V_{in})g_2z_2\right]}}_{K_{pe2}}, & \text{PDCM2}\quad(V_{in}\le V_o)\\ K_p, & \text{PDCM2}\quad(V_{in}>V_o).\end{cases} \tag{49}$$

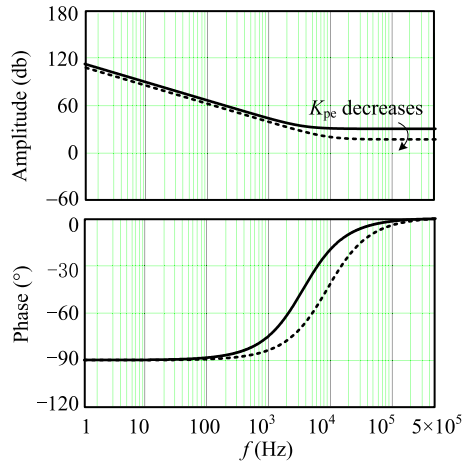

Fig. 9. Bode diagrams of equivalent $G_{ve}(s)$ with different K_{pe1} or K_{pe2}.

As seen from (48), $G_{ve}(s)$ is a PI regulator, and $\angle G_{ve}(s)$ increases from $-90°$ as the frequency increases. So, to ensure the phase margin larger than 30° under all the operating conditions, $\angle G_{ve}(s)$ at minimum f_c should satisfy

$$\mathrm{PM} = 180° + \angle G_{vdy1\_appr}(s) + \angle G_{ve}(s) = 30°. \quad (50)$$

Substituting $\angle G_{vdy1\_appr}(s) = -120°$ into (50), $\angle G_{ve}(s)$ at minimum f_c should be $-30°$. According to (48), at f_{cmin}, we have

$$\angle G_c(j2\pi f_{cmin}) = \arg\left(K_{pe} + \frac{K_i}{j2\pi f_{cmin}}\right)\frac{180°}{\pi} > -30° \quad (51)$$

where K_{pe} is designed according to the maximum $|G_c(s)G_{vdy1\_appr}(s)|$ at $f_s/10$ (f_{cmax}). With the designed K_{pe} and minimum $|G_c(s)G_{vdy1\_appr}(s)|$, f_{cmin} can be calculated. Once K_{pe} and f_{cmin} are obtained, K_i can be solved according to (51).

As seen from (49) shown at the bottom of this page, K_{pe} equals to K_p under PDCM2 with $V_{in} > V_o$. Under other operating conditions, setting $K_p = K_{pe}$, then K_{pe1} and K_{pe2} is less than K_{pe}, causing f_c to decrease, which is lower than the designed f_{cmin}. Since f_c exhibits a wide variation range, the phase lag caused by p_2 can be neglected with the further reduction of f_{cmin}. According to Fig. 9, as K_{pe1} or K_{pe2} decreases, f_c and $\angle G_{ve}(s)$ is decreased. Thus, the phase margin should be checked with minimum value of K_{pe1} and K_{pe2}.

C. Design Example

With the proposed design method, a design example is given here. The main circuit parameters of FSBB converter are listed in Table III.

According to the parameters in Table III, $I_o/(C_f V_o) = 2.9$ kHz. Combining the characteristic of p_1 in Section IV-A, we have $p_1 < f_c$. According to (44), since $f_{p2} = p_2/(2\pi) > f_c$, $|G_{vdy1\_appr}(s)|$ around f_c can be expressed as

$$|G_{vdy1\_appr}(s)| = -\frac{g_1 z_1 z_{ESR}}{s p_2}. \quad (52)$$

TABLE III
KEY PARAMETERS OF THE PROTOTYPE

Parameter	Value	Parameter	Value
Input voltage V_{in}	60~120 V	Output voltage V_o	84 V
Output power P_o	420 W	Full load current I_o	5 A
Switching frequency f_s	500 kHz	Inductor L_c	3 μH
Output capacitor C_f (ESR)	20 μF (5 mΩ)	ZVS current I_{ZVS}	2.5 A
Saw-tooth amplitude V_m	1.8 V	Voltage sense gain	0.02
Proportional factor a	−0.008	Proportional factor b	0.034

Substituting g_1, z_1 and z_{ESR} in Table I and p_2 in (24) into (52), we have

$$|G_{vdy1\_appr}(s)| = \frac{\frac{V_{in}}{L_c}D_{23}T_s - \frac{V_{in}I_{ZVS}}{V_o}}{sC_f} = \frac{V_{in}}{V_o}\frac{1}{C_f}\frac{I_Q}{s} \quad (53)$$

where I_Q is the current when Q_1 is turned OFF (see Fig. 2). As can be seen from Fig. 2, the minimum value of I_Q is I_{ZVS}, and the maximum value of I_Q can be obtained when $V_{in} = V_{inmax}$ at full-load.

The next step is to analyze the maximum and minimum values of $|G_c(s)G_{vdy1\_appr}(s)|$. As seen from (47), $|G_c(s)|$ is maximum under PDCM2 when $V_{in} \le V_o$, and $|G_c(s)G_{vdy1\_appr}(s)|$ can be expressed as

$$|G_c(s)G_{vdy1\_appr}(s)| = H_v G_{PWM}(s) \times \left(1 + \frac{V_o - V_{in}}{V_o}\frac{g_2 z_2}{g_1 z_1}\right)\frac{V_{in}}{V_o}\frac{1}{C_f}\frac{I_{ZVS}}{s}. \quad (54)$$

Substituting g_1,z_1, g_2, and z_2 in Table I into (54), we have

$$|G_c(s)G_{vdy1\_appr}(s)| = H_v G_{PWM}(s)\left[1 + \frac{V_o - V_{in}}{V_o}\frac{2(D_{y1} - D_\theta)}{(2D_{23} - D_{c\_max})}\right]\frac{V_{in}}{V_o}\frac{1}{C_f}\frac{I_{ZVS}}{s}. \quad (55)$$

Similar to the analysis for z_1 in Section IV-A, $(D_{y1} - D_\theta)/(2D_{23} - D_{c\_max}) < (1 - 2D_{c\_max})/D_{c\_max}$, which is around 8. According to the parameters in Table III, $V_{in}/V_o > 0.7$, we have

$$|G_c(s)G_{vdy1\_appr}(s)| < H_v G_{PWM}(s)\frac{1}{C_f}\frac{5.57 I_{ZVS}}{s}. \quad (56)$$

Under other operating conditions, the maximum $|G_c(s)G_{vdy1\_appr}(s)|$ can be expressed as

$$|G_c(s)G_{vdy1\_appr}(s)| = H_v G_{PWM}(s)\frac{V_{inmax}}{V_o}\frac{1}{C_f}\frac{I_{Qmax}}{s}. \quad (57)$$

According to the parameters listed in Table III, $V_{inmax} I_{Qmax}/V_o > 5.57\, I_{ZVS}$. Thus, the maximum $|G_c(s)G_{vdy1\_appr}(s)|$ under all the operating conditions is obtained when $V_{in} = V_{inmax}$ at full-load.

Besides, when $V_{in} = V_{inmin}$ at null-load, $z_2 = 0$, $I_Q = I_{ZVS}$. In this case, $|G_c(s)G_{vdy1\_appr}(s)|$ is minimum.

Fig. 10 shows the Bode diagram of $G_c(s)G_{vdy1\_appr}(s)$ when $V_{in} = V_{inmax}$ at full-load and and $V_{in} = V_{inmin}$ at null-load. As seen, when $V_{in} = V_{inmax}$ at full-load, the amplitude at 50 kHz

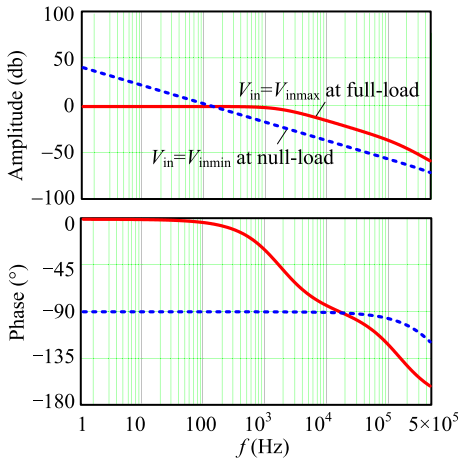

Fig. 10. Bode diagrams of $G_c(s)G_{vdy1\_appr}(s)$.

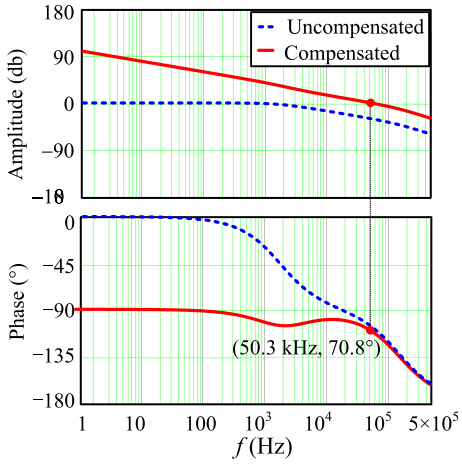

Fig. 11. Uncompensated and compensated Bode diagram of $T(s)$ in (46).

is −30 dB, then, $K_{pe} = 33$ can be calculated. With $K_{pe} = 33$, when $V_{in} = V_{inmin}$ at null-load, $f_{cmin} = 5$ kHz can be calculated. Substituting $f_{cmin} = 5$ kHz and $K_{pe} = 33$ into (51), $K_i = 6\times10^5$ can be calculated.

Setting $K_p = K_{pe}$, the minimum value of K_{pe1} and K_{pe2} is

$$\min(K_{pe1}, K_{pe2}) = K_{pe} - \frac{1}{H_v G_{PWM}(s)} \max\left(\frac{bg_2z_2}{R_{Ld}g_1z_1}, \frac{(1-D_{y2})g_2z_2}{V_o g_1 z_1 + (V_o - V_{in})\, g_2 z_2}\right). \tag{58}$$

According to the parameters listed in Table III, the minimum value of K_{pe1} and K_{pe2} is 17.6, with which, the f_c when $V_{in} = V_{inmin}$ at null-load is 4 kHz according to Fig. 10. At this time, $\angle G_{ve}(s) = -53°$. Since the phase lag caused by p_2 at 4 kHz can be ignored, the phase margin is 37°, satisfying the phase margin requirement.

With the designed $K_p = 33$, $K_i = 6\times10^5$, Fig. 11 shows the uncompensated and compensated Bode diagram of $T(s)$ in (46) when $V_{in} = V_{inmax}$ at full-load. After compensating, the cut-off frequency is 50.3 kHz, and the phase margin is 70.8°.

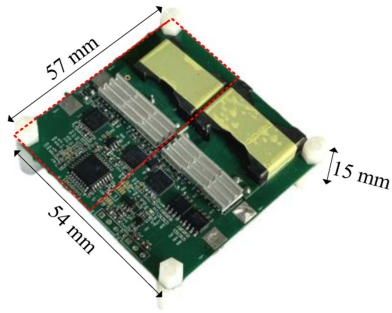

Fig. 12. Photograph of the prototype.

VI. Experimental Verification

In order to verify the correctness of the small-signal model of the FSBB and the closed-loop parameters design approach, a 420-W prototype of the FSBB converter is fabricated in the lab, as shown in Fig. 12 within the red dashed box. The parameters of the prototype have been given in Table III. The NV6128 GaN HEMT from Navitas is used as the power switches.

Fig. 13 shows the measured and theoretical Bode diagrams of $G_{vdy1}(s)$ at null-load and full-load under different input voltage. The measured results are obtained by network analyzer. As seen, the measured results are in good agreement with the theoretical ones below $f_s/3$, which prove the accuracy of the proposed small-signal model.

Figs. 14 and 15 show the measured and theoretical Bode plots of the loop gains at null-load and full-load conditions when the input voltage V_{in} is 60 V, 84 V, and 120 V, respectively, where f_{c_m} and f_{c_t} are the measured and theoretical crossover frequencies, respectively, φ_{m_m} and φ_{m_t} are the measured and theoretical phase margins, respectively. As seen, the measured results are consistent with the theoretical ones, verifying the accuracy of the closed-loop small-signal model. With the closed-loop parameters designed in Section V, the stability under all the operating conditions can be ensured.

Fig. 16 shows the experimental waveforms of the FSBB converter at full-load under different input voltages (60 V, 84 V, and 120 V), where, v_{gs_Q1} and v_{ds_Q1} are the drive signal and drain-source voltage of Q_1, respectively, v_{gs_Q4} and v_{ds_Q4} are the drive signal and the drain-source voltage of Q_4, respectively, and i_{Lc} is the inductor current. As seen, v_{ds_Q1} and v_{ds_Q4} decay to zero before Q_1 and Q_4 are turned ON, respectively. Therefore, Q_1 and Q_4 realize ZVS. In fact, Q_2 and Q_3 are also turned ON with zero-voltage.

Fig. 17(a) shows the dynamic waveforms at the nominal input voltage (84 V) when the load current is stepped changed between 10% and 90% load, and Fig. 17(b) shows the dynamic waveforms when the input voltage is stepped changed between 60 V and 120 V at full load, where i_o is output current, v_o is the output voltage, v_{in} is the input voltage. As seen, with the designed closed-loop parameters, the FSBB converter has a good dynamic response for the output voltage with small overshoot, undershoot and short recovery time.

Fig. 18 shows the measured efficiencies of the FSBB converter under different load and input voltage. As seen, the peak efficiency is 98.7% when $V_{in} = 84$ V. Moreover, the full-load efficiency at different input voltages is higher than 96.9%.

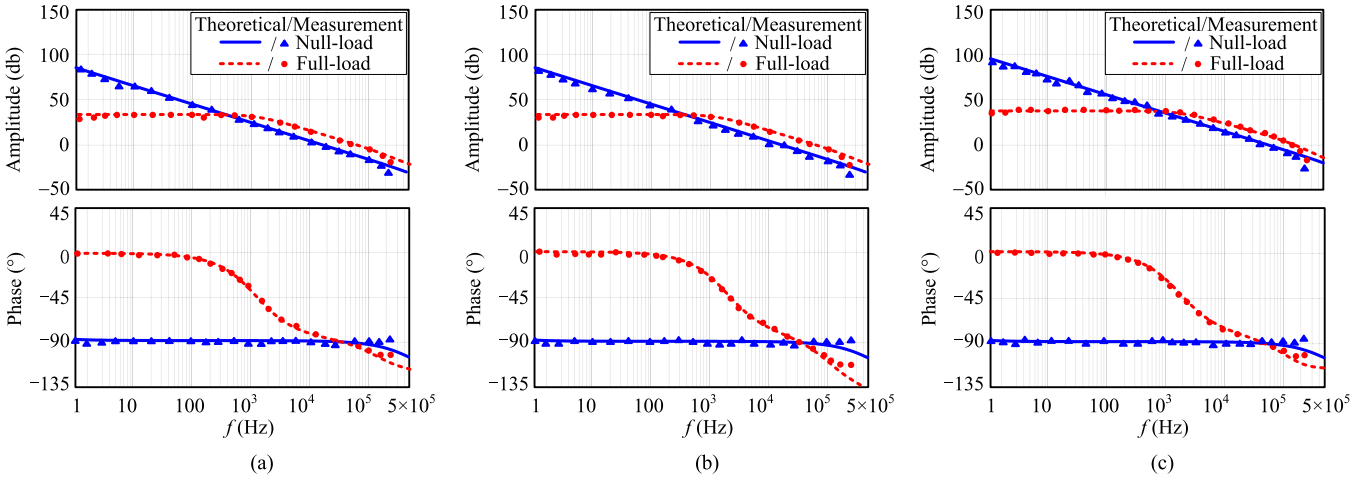

Fig. 13. Theoretical and measured Bode diagrams of $G_{vdy1}(s)$. (a) $V_{in} = 60$ V. (b) $V_{in} = 84$ V. (c) $V_{in} = 120$ V.

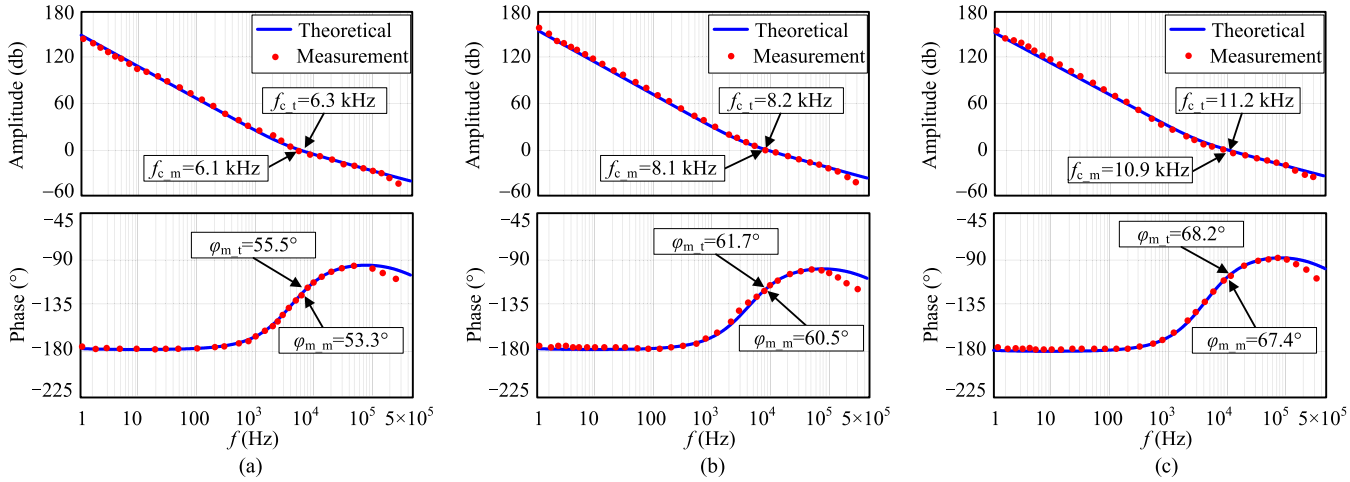

Fig. 14. Theoretical and measured Bode diagram of the loop gains at null-load. (a) $V_{in} = 60$ V. (b) $V_{in} = 84$ V. (c) $V_{in} = 120$ V.

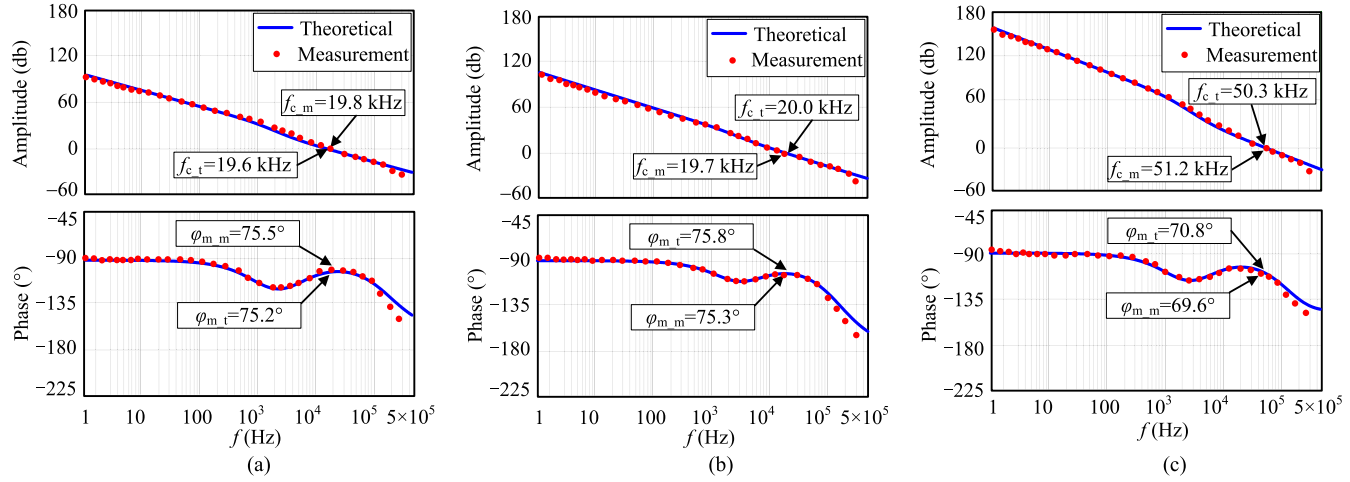

Fig. 15. Theoretical and measured Bode diagram of the loop gains at full-load. (a) $V_{in} = 60$ V. (b) $V_{in} = 84$ V. (c) $V_{in} = 120$ V.

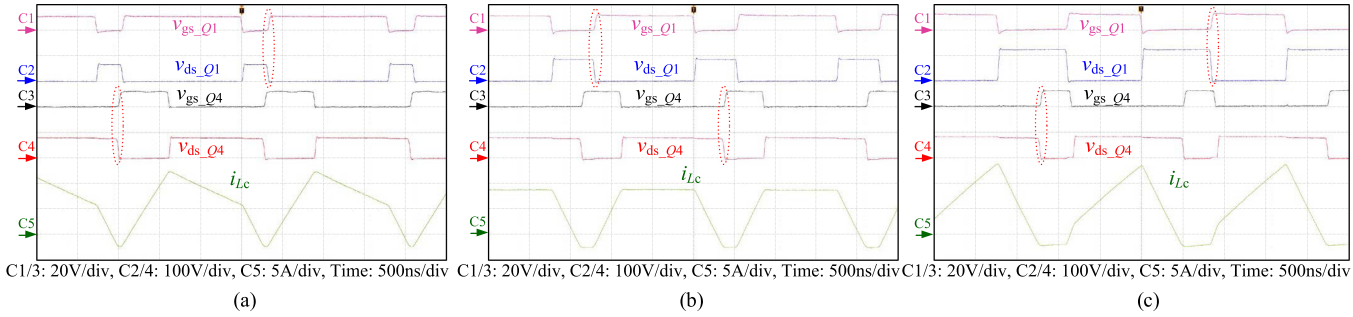

Fig. 16. Steady-state waveforms of the FSBB converter at full-load. (a) $V_{\rm in} = 60$ V. (b) $V_{\rm in} = 84$ V. (c) $V_{\rm in} = 120$ V.

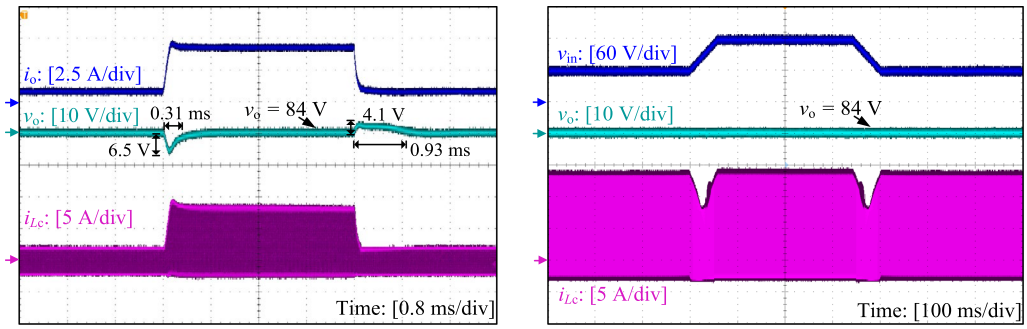

Fig. 17. Dynamic waveforms when (a) the load current is stepped changed between 10% and 90% load at rated input voltage, and (b) the input voltage is stepped between 60 V and 120 V at full-load.

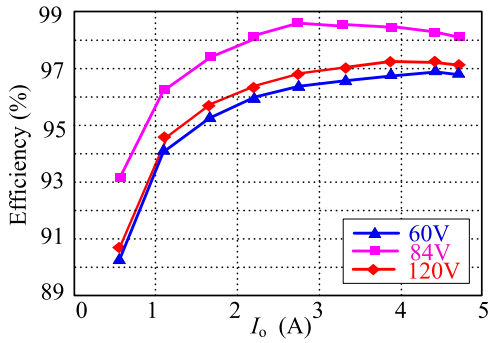

Fig. 18. Measured efficiency.

VII. Conclusion

In this article, the small-signal model of FSBB converter with the combined PWM and approximate phase-shift control is established, and the small-signal characteristics of the power stage are analyzed. After that, the parameter design approach of the closed-loop is proposed, ensuring the stability of the converter under all the operating conditions. Finally, a 420-W prototype of the FSBB converter is fabricated and tested in the lab. The experiment results verify the correctness of the small-signal model and the closed-loop parameter design approach.

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