Enhanced Single-Loop dq Control Based on Inductor Current Feed-Forward and Virtual Damping for Nonlinear Load Application

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***Abstract*—With the recent increase in demand for power electronics-based commercial products, the influx of nonlinear loads into the ac system has increased. In applications, such as standalone inverter systems or uninterrupted power supplies, ensuring sinusoidal load voltage becomes critical when such nonlinear loads are connected. This new development drives power electronics engineers to develop new techniques to mitigate the harmonic effects of these nonlinear loads. Passive filtering of the harmonics leads to costly and bulky systems. Thus, harmonic mitigation must be performed through control and modulation schemes. This article develops an enhanced single-loop direct-quadrature control scheme with inductor current feed-forward and synchronous reference frame-based active selective harmonic elimination to suppress the harmonic effects induced by the nonlinear loads on the output voltage of the standalone inverter systems. The proposed control scheme is analyzed theoretically in the frequency domain, and the design procedure for the control scheme is presented. The proposed control scheme is tested experimentally on an H-bridge-based standalone inverter system operated under different nonlinear loading conditions against its counterparts to prove its efficacy.**

***Index Terms*—Active selective harmonic elimination, inductor current feed-forward (ICF), nonlinear load, proportional–integral–resonant (PIR) control, single loop direct-quadrature (SLdq) control.**

I. Introduction

With the advancement of commercially available power electronics, nonlinear loads have become abundant in the ac load space. When such loads are connected to the standalone inverter systems or the uninterrupted power supplies (UPS), it becomes essential that the output voltage is maintained as sinusoidal. This motivates the power electronics engineers to develop inverters that can maintain the load voltage profile even under such adverse conditions. Filters are ineffective in mitigating the lower order harmonics [1], [2], [3], [4]. Thus, harmonic elimination capabilities have to be implemented in the control scheme to enhance the performance of the converter.

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In literature, multiple state-of-the-art controls have been proposed to achieve this objective. Conventionally, harmonic suppression control schemes for *LC* filter-based standalone inverter systems or UPS are majorly implemented with two cascaded loops, i.e., inner current and outer voltage loops. Within them, linear control schemes where active selective harmonic elimination [5], [6], [7], [8], [9], [10], [11] is implemented through multiple frequency-tuned controllers connected in parallel are prominent in the literature. They contain individual control blocks tuned at fixed frequencies of the desired harmonics. These individual blocks suppress the effect of the harmonics that they are tuned for. These blocks can be implemented in the stationary frame [5], [6], [7], [8], [9], [12], multiple frequency frames [10], [11], or the synchronous frame [13], [14]. The stationary frame implementation is the simplest to realize but has finite gain in the tuned frequencies due to the practical limitations in their implementation. The multiple frequency frame scheme is computationally heavy but has improved steady-state performance due to the infinite dc gain of proportional integral (PI) control. The synchronous frame adaption is an ideal middle ground with median computational burden and holistic harmonic rejection capabilities. However, they have been implemented mostly for grid-connected systems [13], [14], and their implementation has not been explored for standalone inverter systems.

Another contemporary linear control method to the multiple frequency-tuned controller scheme is the feed-forward control scheme [6], [7], [9], [15], [16], [17], where the nonideal behavior of the plant is fed into the control system through measured variables. The feed-forward control schemes can be categorized into capacitor current [9], inductor current [9], [12], load current [16], [17], or load voltage [6], [15] feed-forward methods. Feed-forward control is highly dependent on the measurement of variables, which can lead to an increase in sensor needs and, hence, the cost of the system. A variant of feed-forward control is the virtual impedance-based control scheme [7], [18], [19], where an impedance is virtually added into the system. Virtual impedance mimics the dynamic characteristics of an ideal impedance in the system without adding the thermal or parasitic effects associated with it under real-world application. This method not only reduces the stress on the controller but also helps in improving the dynamics of the system. However, the effects of the sampling and pulsewidth modulation (PWM) delay during digital implementation can negatively affect the stability of the virtual impedance-based controllers [18], [19].

Thus, these effects must be studied thoroughly when designing such controllers.

Further, linear controllers based on cascaded loops have good disturbance rejection characteristics in their inner current control loops, but they suffer from slower dynamic performance [2], [20], [21], [22], as the outer loop needs to be slower to allow the inner control loop to perform satisfactorily. Multiloop controls also take up higher controller memory and are slower to execute due to multiple cascaded controllers. In order to solve this issue, multiple single-loop control schemes [2], [12], [20], [21], [22], [23] have been proposed. However, the application of harmonic compensation has not been explored widely. proportional–resonant (PR) controllers with multiple resonant loops [12], [22] have been implemented, but they suffer from unsatisfactory steady-state performance. Single-loop controls based on state space models, such as observer-based control schemes [23], state feedback control [20], state space control [21], etc., have been proposed, but they require huge memory space and have complex digital implementation procedures. A single-loop direct-quadrature (SLdq) control scheme was presented in [2] but was shown to be ineffective in mitigating the effects of the harmonic current from nonlinear loads. In addition, Iyer and Adda [2] presented a multiple second-order generalized integrator (MSOGI)-based SLdq scheme, which improved the nonlinear load performance, but it was found to be computationally heavy.

Further, two loop-cascaded nonlinear controllers, such as repetitive control [24], [25] and Lyapunov-based control scheme [26], have been proposed to overcome the issues with the dynamic and steady-state performance of the cascaded linear control schemes. In addition, advanced single-loop nonlinear control schemes, such as feedback linearization control [27], H_∞-based repetitive control [28], iterative learning control [29], sliding mode control [30], etc., have also been proposed. However, the nonlinear controllers require advanced knowledge of nonlinear control theory and system modeling for proper implementation. They have complex implementation procedures and stringent stability requirements requiring advanced mathematical knowledge, thus hindering their widespread adaptability. Further, the aforementioned control schemes require advanced controllers with modern hardware for smooth implementation, thus increasing the cost of the system.

This article aims to extend the work presented in [2] and build an enhanced single-loop dq (eSLdq) control scheme, having inductor current feed-forward (ICF) with virtual damping (VD) and synchronous reference frame-based active selective harmonic elimination (SRFASHE) for nonlinear load application of standalone inverter systems. Contributions of this article are as follows.

1) Development of an ICF-based SLdq with VD control scheme. The ICF implemented as a VD improves the harmonic rejection ability and the dynamics of the standalone inverter system.
2) Frequency-domain analysis of the proposed ICF-based SLdq with VD is presented. Effects of sampling and PWM delays are explored, and the choice of the VD factor K_c is discussed.

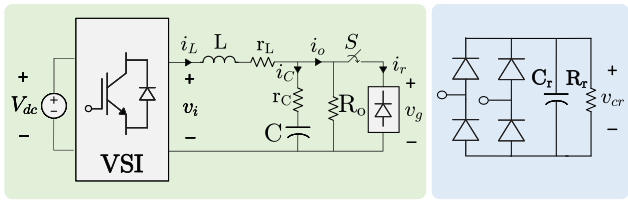

Fig. 1. Circuit diagram for (a) single-phase standalone inverter and (b) rectifier load.

3) A study of the effects of the dc-link harmonics on the output voltage of the inverter system is shown.
4) SRFASHE loops are included to improve the controller performance under nonlinear load application. The improved controller is studied in the frequency domain, and the analysis is presented.
5) A comparative experimental study of the developed ICF-based SLdq with VD and eSLdq control scheme with the existing controllers in the literature under different nonlinear loading conditions is performed on a 200-W H-bridge-based standalone inverter system.

The rest of this article is organized as follows. The design of ICF-based SLdq control with VD in the dq reference frame is presented in Section II, which also presents the frequency-domain analysis and design of the newly developed controller. Section III deals with the implementation of SRFASHE loops to further improve system performance under nonlinear load applications. Section IV presents the comparative experimental study of the proposed control schemes with state-of-the-art controllers. Finally, Section V concludes this article.

II. ICF-Based SLdq Control With VD

A. Modeling of ICF-Based SLdq Control With VD

The complete circuit diagram of the inverter system is shown in Fig. 1. It consists of a voltage-source inverter connected to a linear load, ideally resistive in nature, and a nonlinear load (diode bridge rectifier in this case). The supply to the system can either be a constant dc source (battery) or a variable dc source (renewable energy source). The synchronous dq frame model of the system shown above [2] is given as

$$v_i^e - WLi_L^e = L\frac{di_L^e}{dt} + r_L i_L^e + v_g^e \tag{1}$$

$$i_L^e = i_o^e + WCv_g^e + C\frac{dv_g^e}{dt} - Wr_cC(i_L^e - i_o^e) - r_cC\frac{d(i_L^e - i_o^e)}{dt} \tag{2}$$

where W is given by $\begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}$, ω is the system frequency in rad/s, $x^e = [x_d \quad x_q]^T$, $x \in \{v_i, i_L, i_o, v_g\}$, L and C are the filter inductance and capacitance, and r_L and r_C are their parasitic resistances, respectively.

In order to dampen the harmonic effect of the nonlinear load, VD is introduced into the system by adding $K_c i_L^e$ on both sides

of (1). The inductor current i_L^e is used as the feed-forward term to serve two purposes, i.e., 1) the nonlinearity of the load is due to the nature of the current drawn by the load and 2) the VD with i_L^e acts as a series resistor with the inductor, thus helping in dampening the resonance effect of the *LC* filter. The modified equation after the addition of VD is as follows:

$$v_i^e - WLi_L^e + K_c i_L^e = L\frac{di_L^e}{dt} + r_L i_L^e + K_c i_L^e + v_g^e \tag{3}$$

where K_c is the VD coefficient. The design of K_c is presented in the following sections.

Deriving the single-loop control logic of the system by taking the Laplace transform of (2) and (3), we get

$$\begin{bmatrix} I & -WL + K_c \\ 0 & I \end{bmatrix} \begin{bmatrix} v_i^e(s) \\ i_L^e(s) \end{bmatrix} = AT^e$$

$$T^e = \begin{bmatrix} i_L^e(s) & i_o^e(s) & v_g^e(s) \end{bmatrix}^T$$

$$A = \begin{bmatrix} (sL + (r_L + K_c))I & 0 & I \\ -\dfrac{r_c CW}{sr_c C + 1} & I + \dfrac{r_c CW}{sr_c C + 1} & \dfrac{WC + sCI}{sr_c C + 1} \end{bmatrix} \tag{4}$$

where I is the identity matrix.

Substituting $i_L^e(s)$ in the right-hand side of $v_i^e(s)$ in (4) and combining the cross-coupling and VD terms as $u_i^e(s) = v_i^e(s) - WLi_L^e(s) - W(r_L + K_c)Cv_g^e(s) + K_c i_L^e(s)$, we get

$$u_i^e(s) = BT^e$$

$$B = \begin{bmatrix} -\dfrac{r_c CW\ (sL + r_L + K_c)}{sr_c C + 1} \\ (sL + r_L + K_c)I + \dfrac{r_c CW\ (sL + r_L + K_c)}{sr_c C + 1} \\ \left(I + \dfrac{sC\ (sL + r_L + K_c)I}{sr_c C + 1} \right. \\ \left. + \dfrac{sWC\ (L - (r_L + K_c)r_c C)}{sr_c C + 1}\right) \end{bmatrix}^T. \tag{5}$$

Forming the control law using $u_i^e(s)$, we get

$$\begin{aligned} v_i^e(s) = {} & G_{cv}(s)e_v^e(s) + WLi_L^e(s) - K_c i_L^e(s) \\ & + W(r_L + K_c)Cv_g^e(s) \end{aligned} \tag{6}$$

$$u_i^e(s) = G_{cv}(s)e_v^e(s)$$

$$e_v^e(s) = v_g^{e*}(s) - v_g^e(s) \tag{7}$$

where $G_{cv}(s)$ is the controller transfer function, and $e_v^e(s)$ is the error in voltage.

The VD introduced in the inverter control scheme utilizes the inductor current as the feed-forward term. Thus, the control scheme for ICF-based SLdq with VD has been successfully built. The control block diagram is shown in Fig. 2.

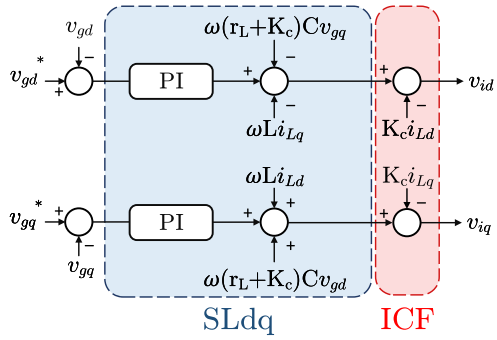

Fig. 2. Control block diagram of ICF-based SLdq control scheme with VD.

B. Frequency-Domain Analysis and Design of ICF-Based SLdq Control With VD

To analyze the proposed controller, the closed-loop frequency-domain dq reference frame transfer functions are built in terms of $v_g^e(s)$ for the inverter system. Since the aim of the proposed controller is to control the output voltage $v_g^e(s)$, thus the effects of the closed-loop system and the disturbances on the controlled parameter $v_g^e(s)$ must be studied. Due to the implementation of the system experimentally in the digital domain, the effects of the sampling and PWM delays are also explored in this section. In addition, the ability of the system to generate sinusoidal output voltage even under harmonic-rich dc-link voltage is also studied. Furthermore, the developed transfer functions are used to design the VD factor (K_c). The detailed analysis is presented as follows.

1) Effects of Delay on ICF-Based SLdq Control With VD and Frequency-Domain Model of the Delay Implemented System: In order to derive the closed-loop transfer function of the system in terms of $v_g^e(s)$, the overall control block diagram of the plant is built and represented in Fig. 3(a) using s-domain transfer function of (1) and (2) and the developed control scheme as presented in (6) and Fig. 2.

The digital implementation of the control scheme is embedded with delays associated with the sampling of the measured signals and the comparator-based implementation of the PWM. These delays can affect the stability of the system as well as the performance of the controller. Thus, in order to study the effects of the aforementioned delays, the following have been incorporated in the overall control block diagram presented in Fig. 3(a):

$$\begin{aligned} \text{Sampling delay} &= e^{-s(T_s)} \\ PWMdelay &= e^{-s(0.5T_s)} \end{aligned} \tag{8}$$

where T_s is the sampling time of the digital controller.

The sampling delay is multiplied with the VD factor (K_c), and the PWM delay is multiplied by the controller output. The overall control block diagram with the delays included can be restructured, as shown in Fig. 3(b). This restructuring leads to the formation of a new effective impedance, which is given by

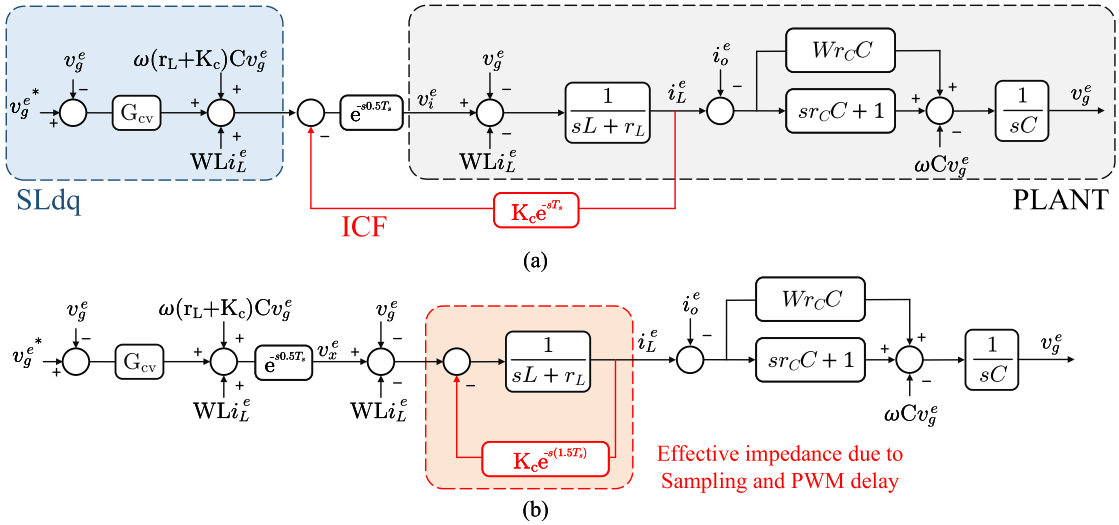

Fig. 3. (a) Complete s-domain plant block diagram of the ICF-based SLdq with VD and the *LC* filter connected standalone inverter and (b) effective s-domain plant block diagram of the ICF-based SLdq with VD and the *LC* filter connected standalone inverter.

the following equation:

$$Y_{\text{eq}}(s) = \frac{\dfrac{1}{sL + r_L}}{1 + \dfrac{K_c e^{-s(1.5T_s)}}{sL + r_L}} \tag{9}$$

where $Y_{\text{eq}}(s)$ is the equivalent s-domain admittance of the inductor with delays included in the system.

Substituting $s = j\omega$ and $e^{-jwT} = \cos(wT) - j\sin(wT)$ and simplifying (9), we get

$$\begin{aligned} Y_{\text{eq}}(j\omega) &= \frac{1}{Z_{\text{eq}}(j\omega)} = \frac{1}{R_{\text{eq}}(\omega) + jX_{\text{eq}}(\omega)} \\ R_{\text{eq}}(\omega) &= r_L + K_c\cos(\omega(1.5T_s)) \\ X_{\text{eq}}(\omega) &= \omega L - \omega K_c \sin(\omega(1.5T_s)) \end{aligned} \tag{10}$$

where $R_{\text{eq}}(\omega)$ and $X_{\text{eq}}(\omega)$ are the resistance and reactance of the equivalent impedance $Z_{\text{eq}}(j\omega)$, respectively.

Plotting R_{eq} and X_{eq} for varying ω, we get the curve shown in Fig. 4. It is observed that with an increase in K_c, the equivalent reactance reduces; however, the equivalent resistance increases in value. However, after a fixed frequency $(f_s/6)$, which is dependent on the sampling frequency(f_s), the equivalent resistance is observed to become negative. It is important to note that if the resonant frequency of the *LC* filter is kept above this frequency, the system will become unstable due to the negative resistance. Thus, the resonant frequency must be maintained below $f_s/6$ for the successful implementation of the ICF-based SLdq with VD [18], [19].

Considering the equivalent plant model, as shown in Fig. 3(b), the closed-loop transfer functions of the system can be built. In order to model the delay transfer function, e^{-sT} is replaced with its first-order Padé approximation form $\dfrac{1 - sT/2}{1 + sT/2}$. The

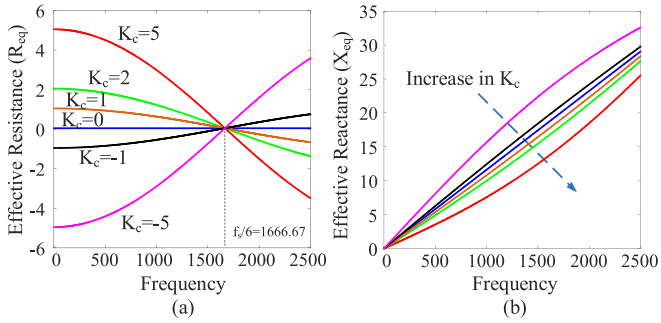

Fig. 4. Plot of change in equivalent (a) resistance and (b) reactance with change in frequency due to delay in ICF.

controller transfer function $G_{cv}(s)$ is replaced by (11). After necessary block diagram and mathematical modifications, the following closed-loop transfer functions are derived:

$$v_g^e(s) = \begin{bmatrix} G_p(s) \\ G_{io}(s) \\ G_{io}^c(s) \\ G_{iL}^c(s) \\ G_{vg}^c(s) \end{bmatrix}^T \begin{bmatrix} v_g^{e*}(s) \\ i_o^e(s) \\ i_o^f(s) \\ i_L^f(s) \\ v_g^f(s) \end{bmatrix}$$

$$G_{cv}(s) = K_p + \frac{K_i}{s} \tag{11}$$

where $G_p(s), G_{io}(s), G_{io}^c(s), G_{iL}^c(s)$, and $G_{vg}^c(s)$ are the output voltage to the reference voltage, load current disturbance, cross-coupled load current disturbance, the cross-coupled inductor current disturbance, and cross-coupled load voltage disturbance closed-loop transfer functions, respectively, G^c represents the transfer function considering the cross-coupling terms of the variable, and $x^f = \begin{bmatrix} -x_q & x_d \end{bmatrix}^T$.

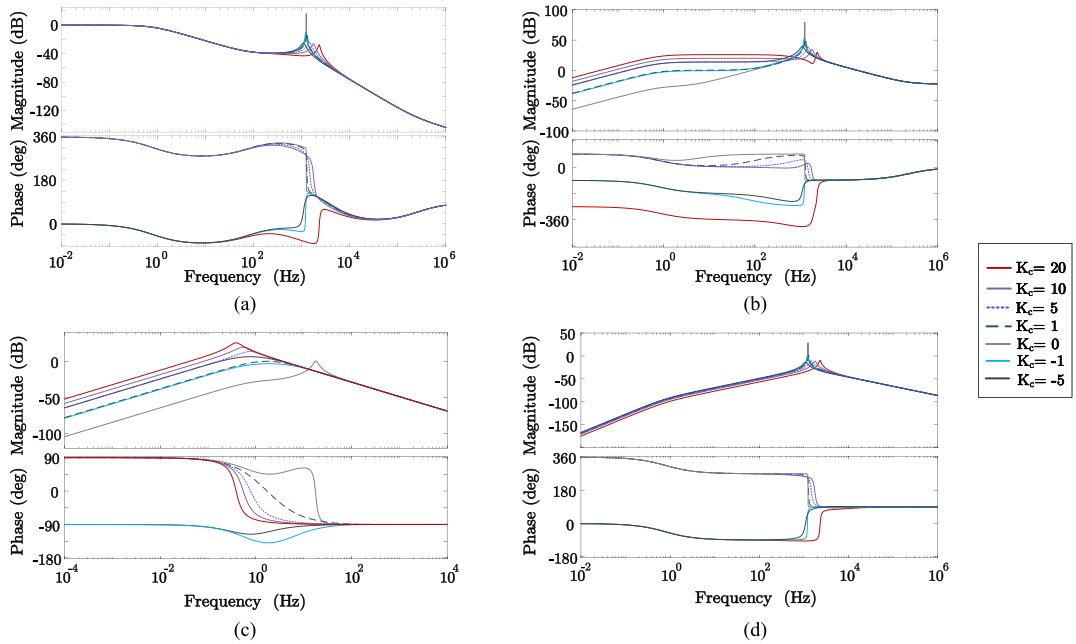

Fig. 5. Magnitude and phase plots of closed-loop transfer function of ICF-based SLdq with VD under various K_c values for load voltage to (a) reference, (b) load current disturbance, (c) cross-coupled load current disturbance, and (d) cross-coupled load voltage disturbance.

TABLE I
HARDWARE PARAMETERS

Parameter	Value
DC voltage (V_{dc})	180 V
Reference frequency (ω)	100π rad/s
Filter inductance (L)	1.85 mH
Filter capacitance (C)	9 μF
Inductor series resistance (r_L)	0.05 Ω
Capacitor series resistance (r_c)	0.075 Ω
Load resistance(R_o)	94.7 Ω
Rectifier output capacitance (C_r)	120 μF
Rectifier output resistance (R_r)	302.5 Ω
Output power (P_o)	200 W
Parameters for ICF-based SLdq (K_p,K_i,K_c)	0.01, 5, 5
Parameters for eSLdq (K_{pr2},K_2)	10, 0.05
Parameters for eSLdq (K_{pr4},K_4)	10, 0.05

2) Effects of VD Factor (K_c) on the Frequency-Domain Characteristics of the Inverter System: The derived closed-loop system is studied using the hardware parameters, as given in Table I. Fig. 5 shows the Bode plots for (11) for varying VD factor (K_c) plotted using MATLAB R2022a.

As perceived from Fig. 5(a), the resonance peak of the system dampens with an increase in the value of K_c. It is also concluded through the Bode plot of $G_p(s)$ that the frequency reference tracking ability of SLdq is dampened with increase in the VD coefficient. Further, it is observed that using a negative value for K_c makes the system unstable. Thus, K_c must be maintained positive. However, there is a limit for the maximum value of the positive K_c that can be used, as it is observed that the system becomes unstable when K_c is set to 20. Thus, based on the given system parameters, K_c must be set within the range of 0 to 20.

The frequency plots for $G_{io}(s)$ and $G_{iL}^c(s)$ are plotted in Fig. 5(b) and (c), respectively. The plot of $G_{io}^c(s)$ is omitted as its characteristics are the same as those of $G_{iL}^c(s)$ with the only variation being the negative sign in the former. The deterioration in damping of the high-frequency components in the system due to increase in VD is observable in both the plots in Fig. 5(b) and (c). The normal and cross-coupled load current disturbance rejection gain of the system increases with an increase in K_c. This is evident by the fact that, effectively, resistance is added in series with the inverter, which would further induce a voltage drop in the system. However, it should be noted that the proposed controller, as will be shown through experimentation, is able to dampen the effect of the harmonics caused by the nonlinear load system. In contrast, Fig. 5(d) suggests that the damping of cross-coupled voltage disturbance is improved with the increase in K_c. However, similar to $G_p(s)$ characteristics, $G_{io}(s)$ and $G_{vg}^c(s)$ become unstable for $K_c = 20$.

3) Effects of VD on the Load Voltage to Inverter Voltage Characteristics of the System: As observed in Section II-B-2, the VD is shown to negatively affect the overall characteristics of the inverter system. However, as would be shown experimentally, the controller is able to mitigate the effects of the nonlinear load effectively. Thus, a new approach is required for the study of the system. One such approach would be the study of the effect of VD on the load voltage to inverter voltage characteristics of the system. In order to do so, the modified load voltage to inverter voltage transfer function is obtained from Fig. 3(b) as follows:

$$G_{vx}(s) = \frac{Y_{\text{eq}}(s)\dfrac{sr_cC+1}{sC}}{1+Y_{\text{eq}}(s)\dfrac{sr_cC+1}{sC}} \tag{12}$$

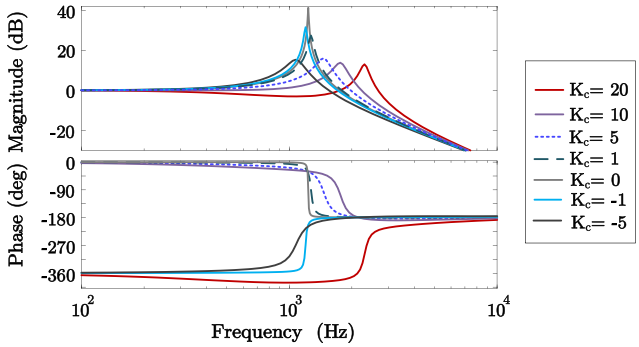

Fig. 6. Magnitude and phase plots of ICF-based SLdq with VD for load voltage to inverter voltage.

where $G_{vx}(s)$ is the modified load voltage to inverter voltage transfer function.

Fig. 6 shows the magnitude and phase plots for (12) under varying K_c. It is observed that with an increase in K_c, the effects of the harmonics in the inverter voltage on the output voltage waveform are reduced drastically due to the damping effect. Furthermore, the resonant peak of the system drops with the increase in frequency, thus improving the system's overall harmonic mitigation ability. However, with an increase in K_c to 10, the system is observed to become unstable. Thus, for the given parameters, the range of VD factor K_c is restricted further in between 0 and 10.

Hence, there must be a healthy compromise between the increased sensitivity of the system to the load current disturbance, the dynamics of the system, and the improved mitigation of the inverter voltage harmonics while making the choice of K_c. Another aspect of the practical choice of K_c is the overflowing of the result register if the value chosen is too large. In addition, considering the effects of delay further limits the choice of K_c. Thus, in this article, the choice is made through practical experimentation, and the optimal value of K_c is found to be 5.0.

4) Effects of DC-Link Harmonics on Load Voltage Harmonics: In addition to the abovepresented analysis, another aspect of the system that affects the harmonic profile of the load voltage is the dc-link harmonics. It can be shown mathematically that due to the existence of nonideal output load voltage and current, the dc-link voltage will contain harmonics other than the second-order harmonic. Considering the worst-case scenario where the load voltage contains the third harmonic and the load current contains the fifth harmonic apart from the fundamental component of each. The input–output power balance can be given as

$$V_{\rm dc}I_{\rm dc} = (V_m \sin\omega t + V_{m3}\sin 3\omega t)(I_m \sin\omega t + I_{m5}\sin 5\omega t) \tag{13}$$

where $V_{\rm dc}$ and $I_{\rm dc}$ are the dc-link voltage and current, and V_{mn} and I_{mn} are the voltage and current peaks of the nth harmonic.

Let

$$P_{\rm dc} = V_{\rm dc}I_{\rm dc}$$

$$P_m = \frac{V_m I_m}{2}$$

$$P_{m2} = \frac{-V_m I_m + V_{m3}I_m + V_{m3}I_{m5}}{2}$$

$$P_{m4} = \frac{-V_{m3}I_m + V_m I_{m5}}{2}$$

$$P_{m6} = \frac{V_m I_{m5}}{2}$$

$$P_{m8} = \frac{V_{m3}I_{m5}}{2}$$

where $P_{\rm dc}$ is the dc power of the system and P_{mn} is the power corresponding to the nth harmonic in the system.

Then, simplifying (13) using trigonometric identities, we get

$$P_{\rm dc} = P_m + P_{m2}\cos 2\omega t + P_{m4}\cos 4\omega t - P_{m6}\cos 6\omega t - P_{m8}\cos 8\omega t. \tag{14}$$

Suppose we consider a constant dc current ($I_{\rm dc}$) being drawn from the dc-link capacitor; the dc voltage is observed to have the second, fourth, sixth, and eighth harmonics. If this dc-link is used to generate a pure sine wave of modulation index M, the resulting output voltage is given as follows:

$$v_i = \left[\frac{P_m}{I_{dc}} + \frac{P_{m2}}{I_{dc}}\cos 2\omega t + \frac{P_{m4}}{I_{dc}}\cos 4\omega t - \frac{P_{m6}}{I_{dc}}\cos 6\omega t - \frac{P_{m8}}{I_{dc}}\cos 8\omega t\right] M\sin\omega t. \tag{15}$$

Through basic trigonometry, we can deduce from (15) that the inverter output voltage will contain the third, fifth, seventh, and ninth harmonics. This output voltage is highly polluted, and when combined with the dead-time effects, the harmonics in the load voltage will be further amplified. However, as shown in Section II-C and Fig. 6, the ICF-based SLdq with VD control is able to mitigate these generated harmonics due to its improved inverter voltage harmonic elimination characteristics.

III. Development and Study of eSLdq Control Scheme

The already existing harmonic elimination capabilities of the ICF-based SLdq with VD can be further enhanced to provide better harmonic profiles of the load voltage. Multiple methods have already been cited in the introductory discussion to achieve this, and the synchronous reference frame-based-active selective harmonic elimination (SRFASHE) is chosen for implementation in this article. SRFASHE [13], [14], [31], [32] is a combination of multiple proportional–integral–resonant (PIR) controllers implemented in the synchronous frame of reference. Thus, allowing it to be easily integrated with the proposed ICF-based SLdq and VD. It can be shown that a (2n+1)th-order harmonic frequency component in a stationary frame becomes a (2n)th component in the synchronous frame. This fact allows the use of resonant filters to mitigate the selective harmonics from the quantity tracked. The controller transfer function for PIR is

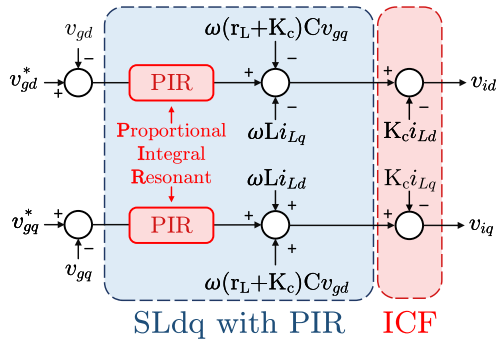

Fig. 7. Control scheme for eSLdq with ICF and synchronous reference frame-based-active selective harmonic elimination (SRFSAHE).

given as

$$G_{cv}(s) = K_p + \frac{K_i}{s} + \sum_{j=2}^{2n} \frac{jK_{prj}K_j\omega s}{s^2 + jK_j\omega s + \omega^2} \tag{16}$$

where $2n$ represents the maximum harmonic order to be eliminated in SRF.

The choice of the harmonics to be eliminated has to be made, taking into consideration the dynamic nature of the load. With the change in the load voltage, the harmonic composition of the current drawn by the rectifier varies. Thus, the choice of elimination of the third and fifth harmonics is made through experimental testing against the nonlinear load used. As previously stated, to mitigate the aforementioned harmonics in the synchronous frame, we need to implement the second and fourth harmonic resonant loops in SRF. The control block diagram of eSLdq is shown in Fig. 7. As can be observed, the PI controller in the ICF-based SLdq with VD control, as shown in Fig. 2, is replaced by a PIR controller given by (16).

The effects of the resonant loops in the proposed eSLdq can be observed by plotting the Bode plots for the closed-loop system as given in (11) with $G_{cv}(s)$ as given in (16). Fig. 8 plots the magnitude and phase plots of $G_p(s), G_{io}(s), G^c_{iL}(s)$, and $G^c_{vg}(s)$ in MATLAB R2022a. $G_p(s)$ has improved gain with respect to ICF-based SLdq with VD at the 100-Hz and 200-Hz marks, implying an improvement in the tracking ability at those frequencies. The disturbance transfer functions $G_{io}(s)$ and $G^c_{vg}(s)$ also find a drop in the gain at the 100-Hz and 200-Hz marks, indicating an improvement in the disturbance rejection ability of the system. $G^c_{iL}(s)$ has a minimum gain reduction after the inclusion of SRFASHE loops, but the natural gain of the system is low enough to damp the effects of the harmonics.

Thus, it is shown that the eSLdq not only retains the benefits of the resonant peak damping of the ICF-based SLdq with VD control but with the addition of the SRFASHE loops, the selective harmonic mitigation ability of the controller is also improved.

IV. Experimental Study of ICF-Based SLdq With VD and eSLdq

In order to experimentally verify the efficacy of ICF-based SLdq control with VD and eSLdq, it is tested against existing controllers, such as cascaded loop dq (CLdq) [33], SLdq [2], MSOGI-based SLdq [2] and single-loop proportional resonant (PR) with multiple resonant controllers (PR+MRC) [34].

TABLE II
Hardware Components

Component	Manufacturer	Part number
IGBT	ON SEMI	NGTB40N120IHLWG
Optocoupler	Fairchild	FOD3180
DSP	Texas Instruments	TMDSDOCK28335
Diode Bridge Rectifier		KBPC3510
Voltage sensor	LEM	LV-25p
Current sensor	LEM	LA-55p

The experimental setup is shown in Fig. 9 and the component list is shown in Table II. The H-bridge was chosen as the inverter for testing. The H-bridge consists of two half-bridge legs made with ON-SEMI NGTB40N120IHLWG IGBTs and driven by Fairchild FOD3180 opto-couplers. The voltage and current measurements for the controller action are performed with the LEM-manufactured LV-25p and LA-55p sensors.

The controllers are implemented using the TMS320F28335-based TI experimental kit (TMDSDOCK28335). The controllers are implemented as difference equations in the code composer studio environment. Initially, the s-domain transfer functions of the controllers are derived. The derived transfer functions are then converted to the z-domain using the bilinear transformation, after which they are further simplified to their difference form. For dq-based controllers, the second-order generalized integrator (SOGI) is implemented for the dq conversion. A brief description of the implemented controllers is as follows: the CLdq control scheme consists of PI-based inner current loop and outer voltage loop, which are implemented in the dq reference frame. The SLdq and MSOGI-based SLdq schemes both contain only a voltage control loop in the dq reference frame to control the converter's output voltage. In the case of MSOGI-based SLdq, two parallel control loops are implemented, each tuned to mitigate the third and fifth harmonics in the system, respectively. The single-loop PR+MRC control consists of multiple PR voltage controllers in parallel to control the fundamental, third and fifth harmonics, respectively.

To test the controllers for nonlinear load application, the system is tested under four different conditions (practical application) [15], [35], [36], i.e., (a) nonlinear load switching with the linear load connected (PC or UPS systems with no power factor correction (PFC) circuits implemented), (b) only nonlinear load connected (UPS powering PC and oscilloscopes without PFC circuits), (c) linear load switching with the nonlinear load connected (printer and microwave oven), and (d) rectifier load with pulsed resistance (traction load).

A. Nonlinear Load Switching With Linear Load Connected

Application: Nonlinear load switching with a linear load connected to the inverter system is commonly found in applications where multiple linear (electric pump, fans, bulb, etc.) and nonlinear loads (old chargers, led bulbs, personal computers without PFC circuits, etc.) are connected to the inverter.

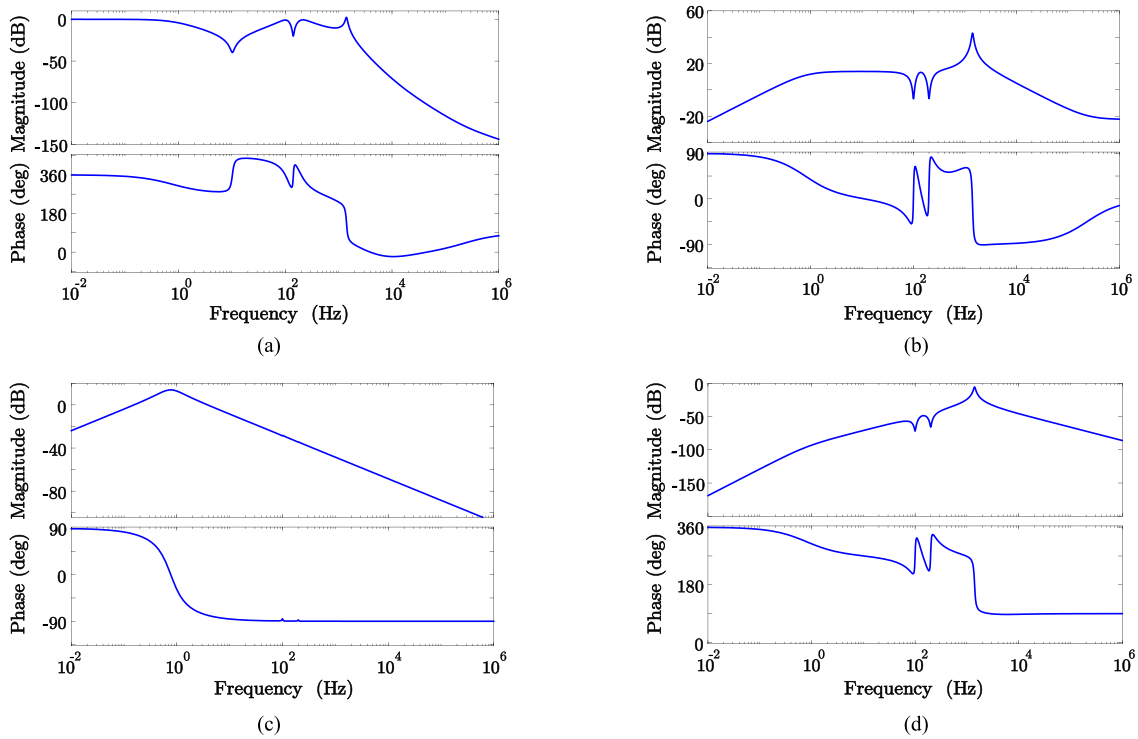

Fig. 8. Magnitude and phase plots of eSLdq, with $K_c = 5$ and resonant loops for the second and fourth harmonics incorporated, for load voltage to (a) reference, (b) load current disturbance, (c) cross-coupled load current disturbance, and (d) cross-coupled load voltage disturbance.

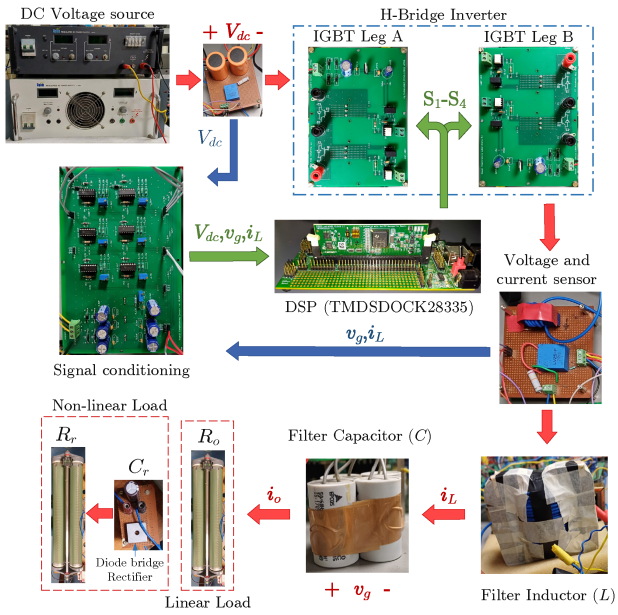

Fig. 9. Experimental setup of single-phase standalone H-bridge inverter with an *LC* filter. The power flow is shown by red arrows, blue arrows represent the measured signals, and green arrows represent signals to and from the DSP.

Implementation: The tested inverter is started with a linear load of 100 Ω connected across the filter capacitor. A nonlinear load, i.e., a single-phase diode bridge rectifier with a 120-μF capacitor and 350-Ω resistive load at the output, is switched across the linear load. The switching action is performed manually.

Key observation points: Since the inverter load switches from a linear load current to a harmonic-rich current, the controller must overcome the effects of the sudden inrush current of the rectifier load and the spiky nature of its steady-state current. Thus, this test provides insights into the ability of the controller to overcome the effects of the inrush current and its overall impact on the steady-state voltage quality.

Discussion: Table III and Fig. 10 present the results for this test condition. The eSLdq is found to have the best performance with an overall voltage total harmonic distortion (THD) of 2.85% within the tested controls. Not only have the third and fifth harmonics been mitigated compared to SLdq, but further damping of the seventh and ninth harmonics is also observed. An increase in the execution time by 60.85% from that of ICF-based SLdq with VD control can be a bottleneck in the maximum permissible operating frequency of the inverter.

ICF-based SLdq with VD is found to have a better total harmonic distortion (THD) profile than SLdq and PR controller. Due to its lower settling time compared to the CLdq and performance similarity to MSOGI-based SLdq, it can be a good alternative for systems that require faster response and improved voltage profile with lower computational burden. It is observed that the THD performance of all the controllers is the worst compared to all the other conditions due to the effects of the inrush surge current drawn by the rectifier load on its turn ON.

In addition, it is also observed that the dq frame controls are able to maintain the fundamental close to the reference due to the high dc gain of the controller. This benefit is not available with the PR+MRC as the practical implementation of the controller

TABLE III
COMPARISON OF THE CONTROL SCHEMES UNDER NONLINEAR LOAD SWITCHING WITH LINEAR LOAD CONNECTED

Parameter	Single-loop PR+MRC [34]	SLdq [2]	MSOGI-based SLdq [2]	ICF-based SLdq with VD	CLdq [33]	eSLdq	[6]	[7]	Limit as per IEEE 519-2022	Limit as per IEC EN50160
Switching frequency (kHz)	10	10	10	10	10	10	-	-	-	-
Execution time (μs)	24.41	17.40	32.28	17.55	18.01	28.23	-	-	-	-
Voltage THD (%)	4.44	3.83	3.38	3.36	3.11	2.85	6.769	3.075	8	8
Fundamental (V_{peak})	114.9	117.4	117.9	118	117.7	118.2	127.58	105.64	-	-
Third harmonic (%)	0.639	1.290	0.303	0.317	0.354	0.630	1.492	-	5	5
Fifth harmonic (%)	0.941	1.628	0.216	0.589	0.583	0.407	1.049	-	5	6
Seventh harmonic (%)	2.125	1.842	1.938	1.500	1.478	0.488	0.948	-	5	5
Ninth harmonic (%)	1.959	1.396	1.473	1.308	1.267	0.570	-	-	5	1.5
11th harmonic (%)	1.613	1.020	1.179	1.189	1.162	1.049	-	-	5	3.5
Settling time (ms)	20	20	10	40	340	40	-	-	-	-

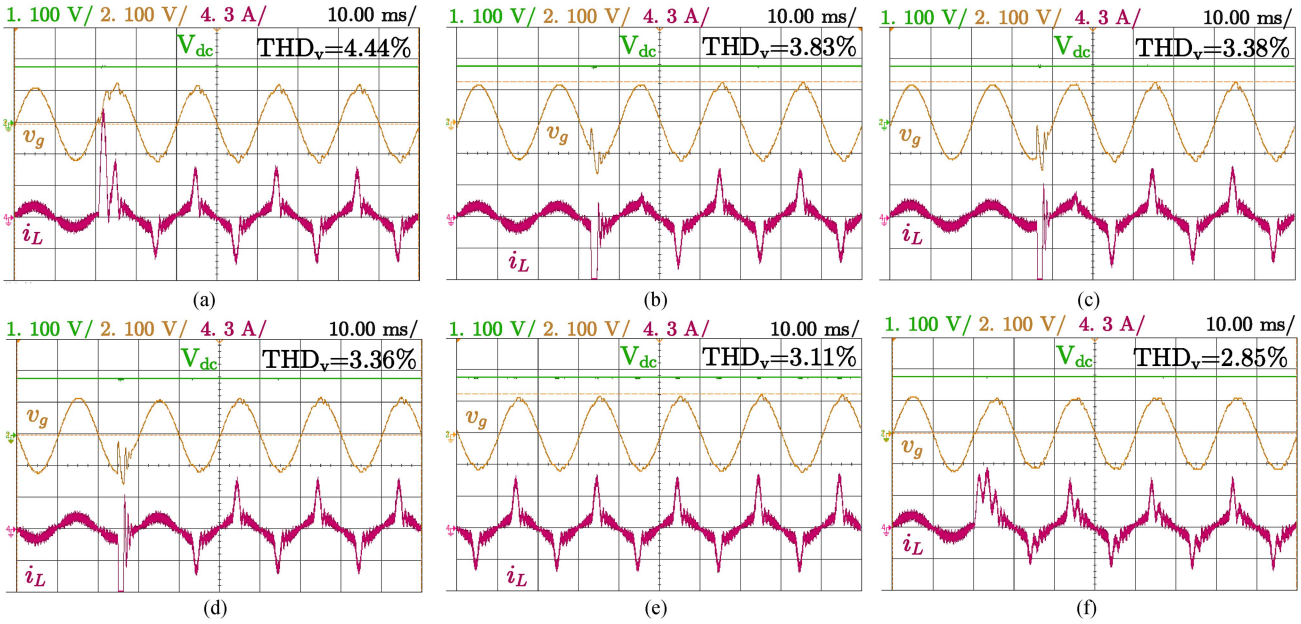

Fig. 10. Hardware results for nonlinear load switching with the linear load connected of (a) single-loop PR with MRC, (b) SLdq, (c) MSOGI-based SLdq, (d) ICF-based SLdq with VD, (e) CLdq, and (f) eSLdq control schemes.

warrants a comparatively lower gain at the resonant frequency. CLdq control is still a viable option where the response time of the system is not of much concern, but good disturbance rejection characteristic is expected with minimum computation time.

B. Only Nonlinear Load Connected

Application: The nonlinear load connected to the inverter system is commonly found in applications where the UPS system powers PC or oscilloscope loads that do not contain PFC circuits.

Implementation: The tested inverter is started with a nonlinear load connected across the filter capacitor, i.e., a single-phase diode bridge rectifier with a 120-μF capacitor and 1000-Ω resistive load at the output. A resistive load of 1000 Ω is then manually switched across the output of the rectifier.

Key observation points: Since the inverter starts directly with the harmonic rich current, the controller must overcome the effects of the spiky nature of the steady-state current only. This gives a comprehensive understanding of how the controller performs without the effects of inrush current. In addition, load transient is introduced at the output of the rectifier to analyze the impact of the dc load change on the performance of the controller.

Discussion: Table IV and Fig. 11 present the results for this test condition. In comparison to the previous test condition, the overall steady-state voltage THD of all controllers is observed to have reduced. This can be attributed to the absence of the huge inrush current that existed in the previous case. Further, similar to the previous condition, the eSLdq provides the best THD performance with an overall THD of 2.03%. It is observed that the SLdq control scheme has a similar performance to that of the PR+MRC. However, the SLdq has better reference tracking ability among the two. The ICF-based SLdq with VD control is another good alternative as it provides improved THD performance as compared to both SLdq and single-loop PR+MRC. Further, its performance is similar to that of the MSOGI-based SLdq control, with the execution time being only 54.37% of the latter. It is also observed that the initial current drawn by the rectifier load in the case of the PR+MRC

TABLE IV
COMPARISON OF THE CONTROL SCHEMES UNDER ONLY NONLINEAR LOAD CONNECTED

Parameter	Single-loop PR+MRC [34]	SLdq [2]	ICF-based SLdq with VD	MSOGI -based SLdq [2]	CLdq [33]	eSLdq	[25]	[15]	[8]	[23]	[5]	Limit as per IEEE 519-2022	Limit as per IEC EN50160
Voltage THD (%)	2.89	2.71	2.48	2.35	2.20	2.03	4	3.57	1.68	4.1	2.6	8	8
Fundamental (V_{peak})	113.59	118.13	117.94	117.82	118.35	117.65	-	16.97	164.61	-	-	-	-
Third harmonic (%)	0.706	1.092	0.843	0.153	0.752	0.386	-	-	-	-	-	5	5
Fifth harmonic (%)	0.565	1.196	0.941	0.291	0.884	0.257	-	-	-	-	-	5	6
Seventh harmonic (%)	1.682	1.257	1.176	1.465	1.044	0.454	-	-	-	-	-	5	5
Ninth harmonic (%)	1.203	0.775	0.919	1.023	0.793	0.377	-	-	-	-	-	5	1.5
11th harmonic (%)	1.281	0.748	0.851	1.027	0.949	0.843	-	-	-	-	-	5	3.5
Settling time (ms)	20	20	10	20	380	20	-	-	-	-	-	-	-

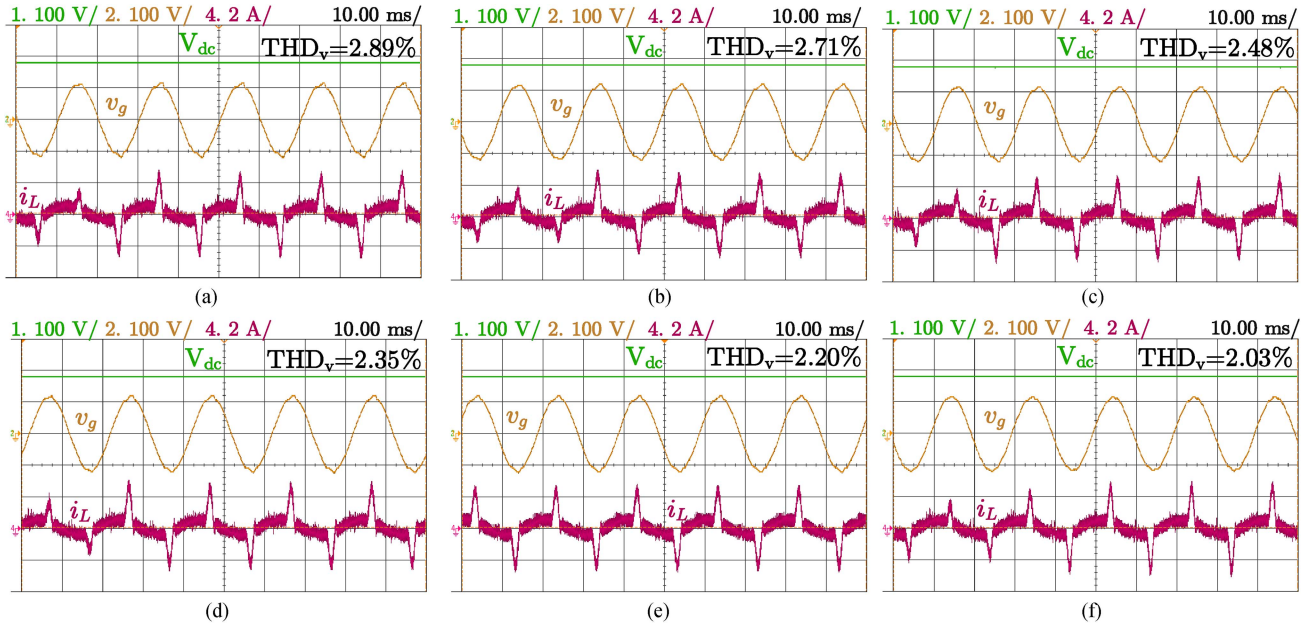

Fig. 11. Hardware results for only nonlinear load connected condition of (a) single-loop PR with MRC, (b) SLdq, (c) ICF-based SLdq with VD, (d) MSOGI-based SLdq, (e) CLdq, and (f) eSLdq control schemes.

controller is highly unsymmetrical compared to all the other controllers tested. Slight variations in the settling time of the controllers are observed compared to the previous case, but it will have no bearing on the quality of the output voltage as it is majorly dependent on the load current drawn by the system. In conclusion, both the proposed control schemes have been found to perform satisfactorily under this operating condition.

C. Linear Load Switching With Nonlinear Load Connected

Application: Linear load switching with a nonlinear load connected to the inverter system is commonly found in applications, such as printers and microwave ovens.

Implementation: The tested inverter is started with a nonlinear load, i.e., a single-phase diode bridge rectifier with a 120-μF capacitor and 1000-Ω resistive load at the output. A 100-Ω resistive load is switched across the nonlinear load. Switching is performed manually.

Key observation points: Since the inverter starts directly with the harmonic rich current, the controller must overcome the effects of the spiky nature of the steady-state current only. However, once the linear load is switched, the controller has to track an improved higher magnitude sinusoidal current. Thus, it tests the effectiveness of the controller in case of an improvement in the load current harmonics drawn and an increase in the maximum current drawn.

Discussion: Table V and Fig. 12 present the results for this test condition. Unlike the previous two conditions, the MSOGI-based SLdq control is found to be the best in terms of its voltage quality; however, the improvement in the voltage quality comes at the cost of the controller's voltage-tracking ability. The SLdq, ICF-based SLdq with VD, and eSLdq controllers were found to perform similarly in this condition. It is observed that the use of current feed-forward has no major effect on the performance of the system in the given condition. Reduction in settling time is observed when compared with the results given in Table III; however, this reduction is due to the nature of the load change and has no bearing on the steady-state performance of the controllers. The steady-state voltage quality is dependent on the nature of the load change, and as both cases (linear load switching with a nonlinear load connected and nonlinear load switching with a linear load connected) have different initial

TABLE V
COMPARISON OF THE CONTROL SCHEMES UNDER LINEAR LOAD SWITCHING WITH NONLINEAR LOAD CONNECTED

Parameter	Single-loop PR+MRC [34]	ICF-based SLdq with VD	SLdq [2]	eSLdq	CLdq [33]	MSOGI -based SLdq [2]	Plug in RC [28]	Robust RC [28]	Limit as per IEEE 519-2022	Limit as per IEC EN50160
Voltage THD (%)	2.77	2.28	2.28	2.26	2.17	2.02	1.3	0.2	8	8
Fundamental (V_{peak})	112.56	118.39	118.19	117.56	118.37	116.96	155.70	156.13	-	-
Third harmonic (%)	0.359	0.546	0.642	0.096	0.693	0.199	-	-	5	5
Fifth harmonic (%)	0.665	0.648	0.988	0.451	0.724	0.372	-	-	5	6
Seventh harmonic (%)	0.647	0.604	0.556	0.256	0.496	0.609	-	-	5	5
Ninth harmonic (%)	0.794	0.682	0.820	0.125	0.694	0.829	-	-	5	1.5
11th harmonic (%)	0.547	0.618	0.597	0.494	0.603	0.596	-	-	5	3.5
Settling time (ms)	25	10	10	10	260	10	83.33(60Hz)	16.67(60Hz)	-	-

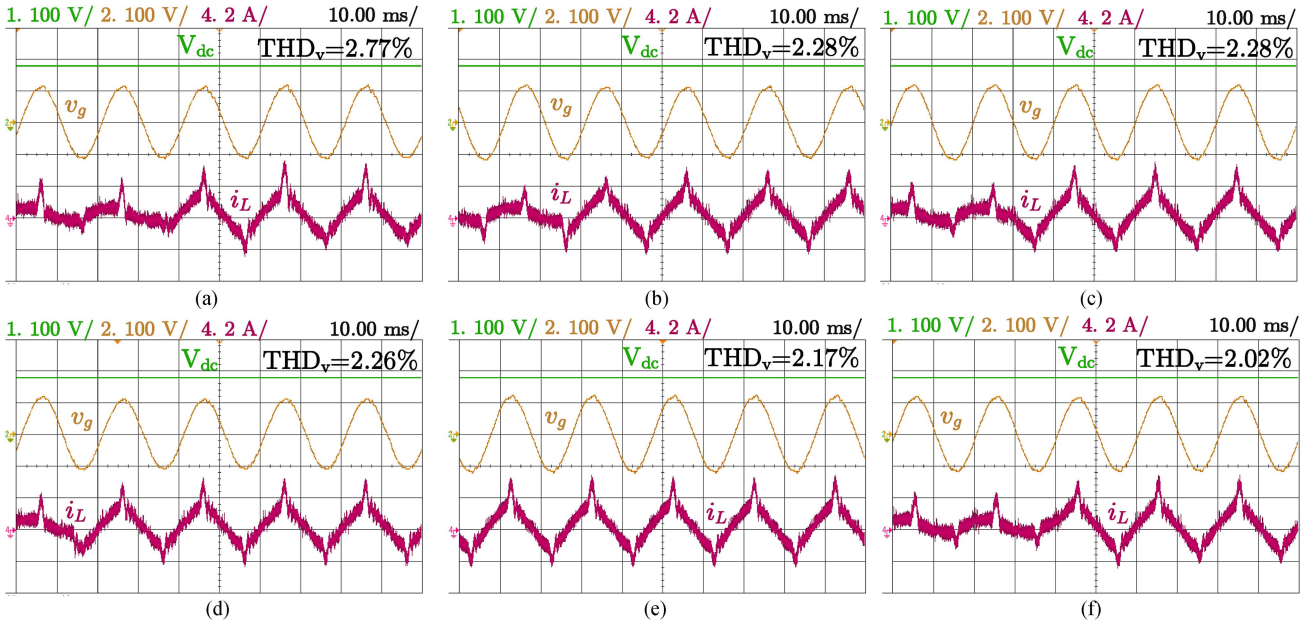

Fig. 12. Hardware results for nonlinear load connected condition of (a) single-loop PR with MRC, (b) ICF-based SLdq with VD, (c) SLdq, (d) eSLdq, (e) CLdq, and (f) MSOGI-based SLdq control schemes.

loading conditions, the steady-state voltage peak and voltage THD vary after switching. Further, the voltage THD is dependent on the harmonic rejection ability of the chosen controller. Thus, controllers having better harmonic rejection ability, as is shown for the proposed controllers, have better THD performance. The fundamental peak depends on the controller gain at the modulating frequency, where a higher controller gain leads to improved steady-state error. Hence, it is observed that the PR-based controller has the worst voltage tracking performance due to its gain limitation caused by the finite gain of the controller. PR+MRC controller is observed to be the worst in terms of voltage THD among the tested controllers. It is also observed that the CLdq control is the slowest among the tested control schemes.

D. Rectifier Load With Pulsed Resistor

Application: Rectifier loads with pulsed resistors are commonly found in traction applications.

Implementation: The tested inverter is started with a nonlinear load, i.e., a single-phase diode bridge rectifier with a 120-μF capacitor and 1000-Ω resistive load at the output. A 1000-Ω resistive load is switched across the nonlinear load at a 25-Hz switching frequency. In this case, the input dc voltage is reduced to 120 V, and the reference is set at 77 V_{peak}.

Key observation points: Since the switching of the pulsed load is periodic in nature, its effect on the input current drawn would also be periodic. Thus, this method would test the effectiveness of the controller in mitigating the effects of periodic disturbances in the nonlinear current drawn by the load.

Discussion: Table VI and Fig. 13 present the results for this test condition. It is observed that the controllers with harmonic compensation loops perform better in mitigating the effect of the pulsed nonlinear load compared to the feed-forward-based method. The eSLdq control performs the best out of all the tested controllers. ICF-based SLdq with VD control is found to perform the worst in terms of voltage quality, and the single loop PR+MRC performs the worst in terms of tracking ability. Unbalance in the current drawn by the rectifier load in the positive half and negative half is observed in all controllers except for the eSLdq and MSOGI-based SLdq.

TABLE VI
COMPARISON OF THE CONTROL SCHEMES UNDER RECTIFIER LOAD WITH PULSED RESISTOR

Parameter	ICF-based SLdq with VD	CLdq [33]	SLdq [2]	MSOGI -based SLdq [2]	Single-loop PR+MRC [34]	eSLdq	[15]	[36]	Limit as per IEEE 519-2022	Limit as per IEC EN50160
Voltage THD (%)	2.06	1.90	1.85	1.84	1.80	1.67	2.92	4.85	8	8
Fundamental (V_{peak})	77.22	77.09	77.03	77.41	74.18	76.96	16.97	-	-	-
Third harmonic (%)	0.617	0.725	0.909	0.349	0.282	0.317	-	-	5	5
Fifth harmonic (%)	0.208	0.191	0.445	0.069	0.276	0.065	-	-	5	6
Seventh harmonic (%)	0.854	0.679	0.925	0.876	0.951	0.286	-	-	5	5
Ninth harmonic (%)	0.587	0.379	0.447	0.491	0.644	0.543	-	-	5	1.5
11th harmonic (%)	0.761	0.675	0.648	0.714	0.741	0.564	-	-	5	3.5
Pulse frequency (Hz)	25	25	25	25	25	25	180	150	-	-

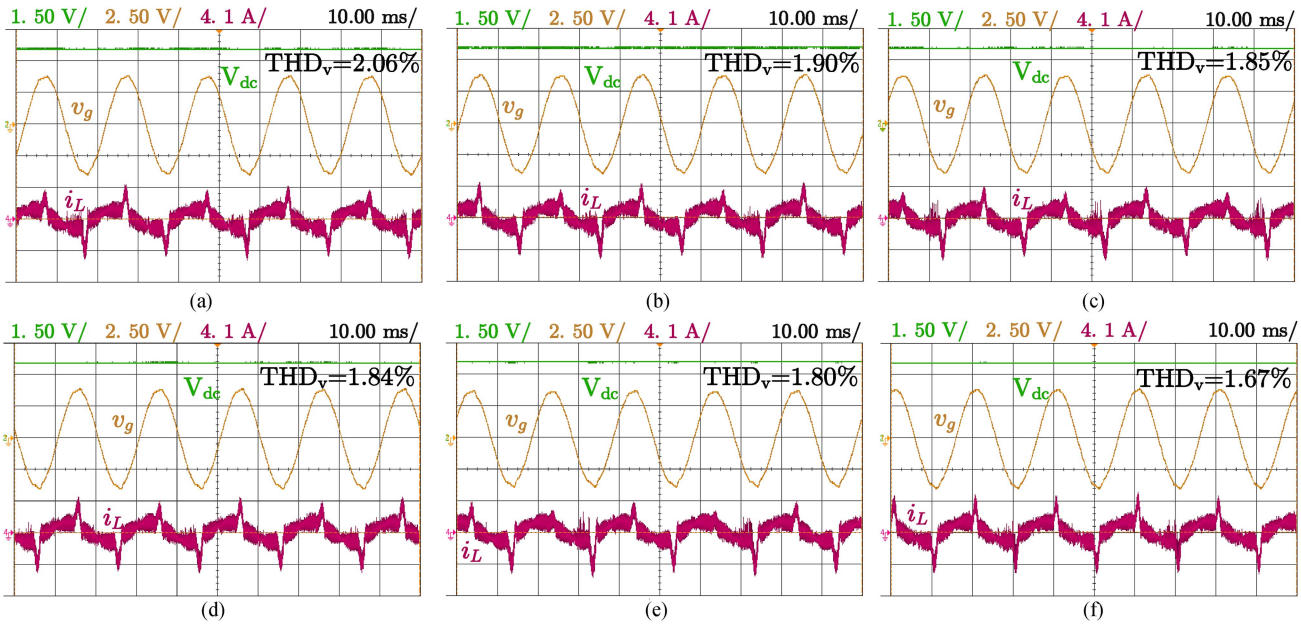

Fig. 13. Hardware results for rectifier load with pulsed resistor condition of (a) ICF-based SLdq with VD, (b) CLdq, (c) SLdq, (d) MSOGI based SLdq, (e) single-loop PR with MRC and (f) eSLdq control schemes.

V. CONCLUSION

This article successfully models and analyzes the ICF-based SLdq with VD and eSLdq control strategies for standalone inverter systems. Both the proposed controllers are found to perform better relatively within the tested controller space. It is inferred from the frequency-domain analysis of the control system that the optimal choice of the VD coefficient, i.e., K_c, can positively affect the voltage profile of the load. It is also demonstrated that the presence of the sampling and PWM delays negatively affects the ICF-based SLdq with VD control. Thus, the choice of K_c must be carefully made to ensure system stability. ICF-based SLdq with VD is shown to be a good alternative to that of MSOGI-based SLdq, where about a 45.63% reduction in computational time is observed against an increase of about 5.94% (average) in the voltage THD compared to the latter. Further addition of synchronous reference frame-based active selective harmonic elimination strategies enhances the harmonic suppression ability of the controller. The proposed controllers are tested against existing controllers in the literature under different nonlinear load conditions and are shown to perform within the IEEE 519 and IEC EN50160 standard limits. Experimental findings reveal that, holistically, eSLdq is superior to the controls tested.

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