Design and Implementation of 40-kV Active Pull-Down Pulsed-Power Modulator for Driving Plasma Reactor in Gas Abatement

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***Abstract*—This article deals with 40-kV active pull-down pulsed-power modulator for driving plasma reactor in gas abatement. Plasma reactors for industrial gas processing have capacitive load characteristics. Moreover, when a voltage of several tens of kV is applied, a corona discharge is generated that induces a decomposition reaction of the flowing industrial gas. To increase gas processing efficiency, tens of kV of pulsed-power is required with a fast-rising rate, short pulse width, and high repetition rate. In this article, a 40-kV solid-state pulsed power modulator with an active pull-down circuit that enables a submicrosecond pulse output under plasma reactor load conditions is proposed. The proposed modulator consists of a capacitor charger, a discharge circuit, and a pull-down circuit. The design of the pulsed modulator based on a modular structure, and solutions for achieving reliable operation are presented. Strategy for gate-driving, designing the integrated gate driver circuit, and efficient high voltage isolation are introduced. The pulse output performance of the implemented 40-kV active pull-down pulsed-power modulator is verified under a plasma reactor load (1000-mm, Φ100-mm) condition.**

***Index Terms*—Active pull-down, corona discharge, plasma reactor, pulsed-power modulator.**

I. Introduction

GLOBAL warming, driven by the emission of carbon dioxide (CO_2), has become a critical issue in modern society. Various abatement processes for industrial gases and odorous gases (such as NOx and VOCs) are significant contributors to CO_2 emissions, exacerbating environmental problems. Traditional methods such as carbon absorption or regenerative thermal oxidizer typically result in CO_2 emissions and secondary pollutants release, posing a substantial challenge from the perspective of environmental protection.

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Given these issues, corona discharge-based gas abatement methods have been studied as an alternative [1], [2], [3], [4], [5], [6], [7]. Corona discharge is a phenomenon in which an electric field caused by a high voltage ionizes the surrounding air molecules, inducing a low-temperature plasma state. This low-temperature plasma state uses electrons with high kinetic energy in the air to dissociate the nitrogen and oxygen. The active species generated in this process can decompose exhaust gases, therefore, they can be used in applications that process industrial gases or complex odors. Notably, this method offers an environmentally friendly solution by processing gases and odors without emitting CO_2.

To induce corona discharge, a gas reactor and a high-voltage power supply are required. Depending on the type of power supply applied, either dc corona or pulsed corona can be induced. A pulsed corona has a higher gas abatement efficiency compared to a dc corona because the short pulses prevent recombination reactions, which can occur due to subsequent oxidation reactions. Therefore, various studies for a high-voltage pulsed-power supply with plasma reactors in gas abatement applications have been conducted [8], [9], [10], [11].

Since plasma reactors exhibit capacitive characteristics, an additional pull-down circuit is required to dissipate residual reactor energy after applying a high voltage. This minimizes pulse width and enables a high repetition rate [12], [13], [14]. A pull-down circuit can be implemented by connecting pull-down resistors or an active pull-down circuit in parallel with the reactor, as shown in Fig. 1. While conventional method of connecting pull-down resistors dissipate residual energy as heat, it has limitations in minimizing pulse width, leading to bulky system designs and reduced performance [15], [16]. In contrast, the method of connecting an active pull-down circuit significantly reduces pulse width to submicrosecond levels, enabling higher pulse repetition rates and improved gas abatement efficiency by mitigating recombination reactions. Additionally, this approach

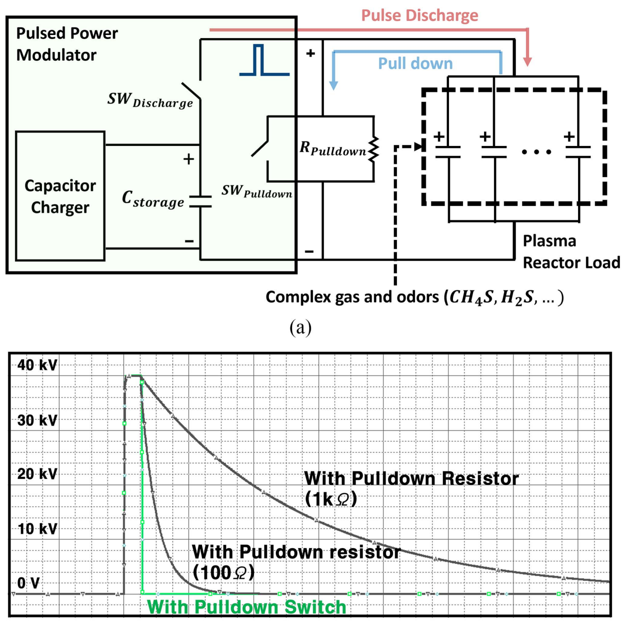


Fig. 1. Pulsed-power system for driving a plasma reactor. (a) System circuit. (b) Pulse waveform under reactor load for different types of pull-down circuits.

allows for a more compact system implementation. However, integrating an active pull-down circuit capable of withstanding tens of kilovolts presents challenges related to reliable switching control and voltage endurance.

Recent advancements in power electronics have explored pulsed-power modulators with modular structures based on series-stacked semiconductor switches [15], [16], [17], [18], [19], [20], [21], [22], [23]. Research has focused on modular structures for implementing discharging circuit, high-efficiency parallel capacitor chargers, and gate-driving methods for series-stacked switches in solid-state pulsed-power modulators. However, the implementation of a discharge circuit and an active pull-down circuit capable of withstanding tens of kilovolts has not yet been reported. Furthermore, previous studies have demonstrated feasibility at 10-kV but have primarily used resistive loads rather than plasma reactor loads.

This article presents the design and implementation of a 40-kV solid-state active pull-down pulsed-power modulator based on semiconductor switches for operating a plasma reactor. The proposed modulator consists of a capacitor charger, a pulse discharge circuit, and an active pull-down circuit, achieving a pulse width of less than 300-ns. The discharge and pull-down circuits are implemented based on a modular structure with 48 discharge switches and 48 pull-down switches, each rated at 1200-V. Additionally, experimental validation under actual plasma reactor load conditions is presented to demonstrate the modulator's practical feasibility for gas abatement applications.

The primary contributions of this article are as follows.

1) The development of a 40-kV active pull-down pulsed-power modulator achieving sub -300-ns pulse widths for improving gas abatement efficiency.
2) The design of a modular structure for implementing series-stacked discharge circuits and pull-down circuits.
3) The design of a robust gate-driving method for synchronously operating series-stacked modules and an integrated gate driver for reliable switching of discharge and pull-down switches in high-voltage environments.
4) Strategies for efficient high-voltage isolation.

The rest of this article is organized as follows. Section II contains a discussion of the design of the active pull-down pulsed-power modulator, including the gate-driving method and design of the integrated gate driver. Section III presents the implementation of the 40-kV active pull-down pulsed-power modulator. Section IV presents the experimental results under plasma reactor load conditions to verify the submicrosecond pulse output performance. Finally, Section V includes a summary of the study and confirms the performance of the proposed solid-state active pull-down pulsed-power modulator for operating a plasma reactor.

II. Design of Pulsed-Power Modulator

The pulsed-power modulator is designed for driving a plasma reactor by supplying a 40-kV output voltage with a submicrosecond pulse width. Furthermore, plasma reactors have capacitive characteristics, and an active pull-down circuit is included. The design of the 40-kV active pull-down pulsed-power modulator, module-based structure, gate-driving method for series-stacked modules, and the design of the integrated circuit for driving the discharge and pull-down switches are also discussed.

A. 40-kV Pulsed-Power Modulator Structure

The schematic of the 40-kV active pull-down pulsed-power modulator is shown in Fig. 2. The pulse modulator consists of a capacitor charger, a pulse inverter, a pulse discharge circuit, and a pull-down circuit. First, the capacitor charger is capable of 12-kW average power and is designed based on an *LCC* resonant converter. This comprises a full-bridge charger inverter, an *LCC* resonance tank and charging transformers [23], [24]. The 48 storage capacitors are charged in parallel to up to 833-V through multiwinding transformers and secondary voltage-Doubler circuits. The pulse discharge and pull-down circuits are designed as a modular structure to ensure the reliability of the series-stacked semi-conductor switches. Each module comprises two storage capacitors, discharge switches, pull-down switches, integrated gate drivers, and a voltage-doubled rectifier. Since only the voltage of a storage capacitor is applied to a discharge switch and a pull-down switch, this modular structure has reliable performance with dynamic balance. The number of modules is selected by considering the maximum output voltage, the rated voltage of the discharge and pull-down switches, and the voltage margin:

$$N_{\text{Module}} = \frac{V_{\text{OUT}}}{2 \times V_{\text{DS}_{\text{MAX}}} \times (1 - \alpha)} \tag{1}$$

where $V_{\text{DS\_MAX}}$ is 1200-V (the rated voltage of the discharge and pull-down switches), α is the voltage margin (approximately 30%), and the V_{OUT} is the pulse output voltage. Therefore, the number of modules is selected as 24 and it is designed as a 4

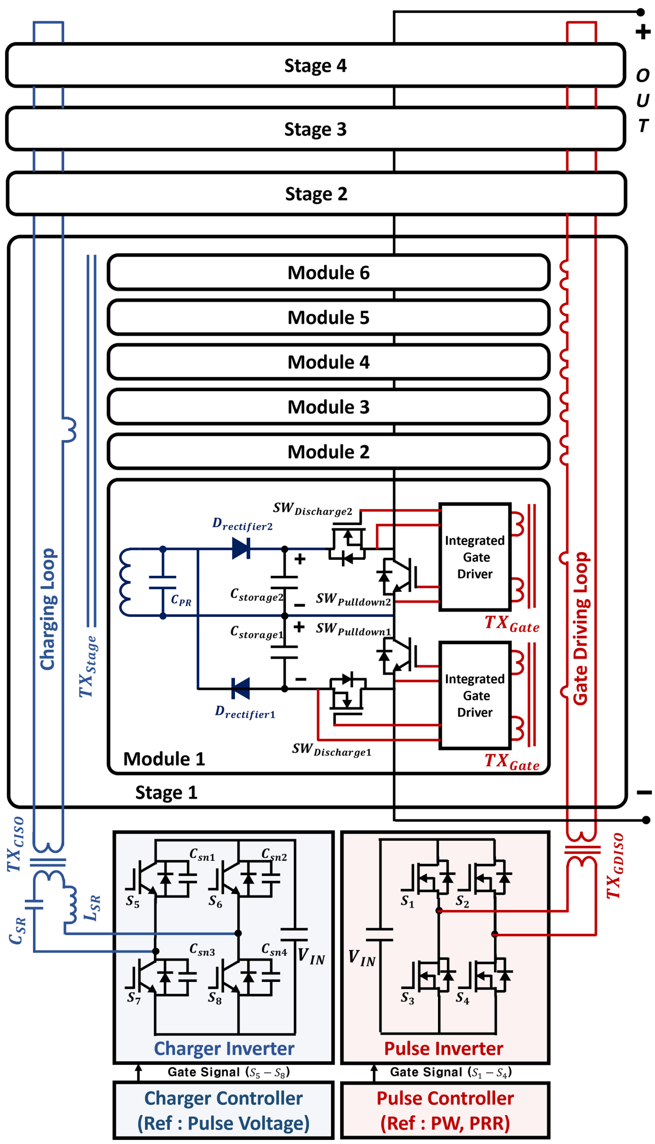


Fig. 2. Schematic of the 40-kV active pull-down pulsed-power modulator.

stage structure with 6 modules per stage. A total of 48 storage capacitors are charged in parallel to a maximum of 833-V through multiwinding transformers and secondary voltage-Doubler circuits. The pulse inverter outputs on-off pulses and supplies synchronized signals and power to each integrated gate driver through the gate-driving loop. Additionally, this structure has the advantage of reliability in terms of synchronization faults. During discharge mode, if a discharge switch fails to turn ON, the discharge current can bypass through the body diodes of the pull-down switches. Similarly, during pull-down mode, if a pull-down switch fails to turn ON, the pull-down current can bypass through the body diodes of the discharge switches.

Table I presents the specifications of the developed pulsed-power modulator for driving the plasma reactor. This has a specific pulse output of the maximum 40-kV, 200-A with a maximum pulse repetition of 3-kHz and a minimum pulse width of 250-ns. This short pulse widths have the advantage of reducing the possibility of arc occurrence from the reactor side, and

TABLE I
SPECIFICATION OF SOLID-STATE PULSED-POWER MODULATOR

Input voltage	3Ø 380 V_{AC}
Pulse Output Voltage	0–40 kV
Pulse Output Current	0–200 A
Pulse Output Power	8 MW
Maximum Pulse Repetition Rate	3 kHz
Minimum Pulse Width	250 ns
Peak Power Density	62.4 kW/L
Size (W x D x H)	450 mm × 475 mm × 600 mm
Volume	128.25 L

preventing damage to the discharging switches even when an arc occures, since the arc current does not increase significantly.

B. Gate-Driving Method

The pulse inverter outputs on-off pulses according to the commanded pulse width and repetition rate, which are defined by the controller. The output signal is applied to the integrated gate driver of each module through a current driving method and synchronously drives all 48 discharge switches and 48 pull-down switches in a series stacking structure.

The applied current loop-based gate-driving method has the advantage of being able to supply both isolated signals and power to each gate driver, in addition to satisfying the requirements of high-voltage isolation and gate synchronization.

In the gate-driving method of series stacked switches, configuring all modules in a single loop is advantageous in terms of synchronized operation of the switches. However, the equivalent inductance of the gate-driving loop is increased. Consequently, the rise and fall times of the current become longer, resulting in a limitation to shorten pulse width. Additionally, when configured as a single loop, there is a disadvantage in terms of noise induction by the power loop because the loop area is structurally increased. Therefore, considering both switch synchronization and minimizing the inductance of the conductors and loop area, the entire gate-driving loop is designed with a total of eight parallel loops, as shown in Fig. 3.

The potential of the node for gate-driving is connected to a maximum 20-kV node, which is half the potential of 40-kV. Using this method, 30-kV isolated cable can be used for the gate-driving loop, satisfying reliable high-voltage isolation.

C. Integrated Gate Driver Circuit

The integrated gate driver is designed to drive the discharge and pull-down switches simultaneously through the gate-driving loop and a multi-winding single core. Key considerations when designing an integrated gate driver include supplying sufficient gate energy to the discharge switch, securing dead time between the complementary switches, applying a parasitic turn-ON prevention circuit (by the Miller capacitance), and securing a sufficient gate signal length of the pull-down switch. The circuit of the integrated gate driver designed with these considerations is shown in Fig. 4.

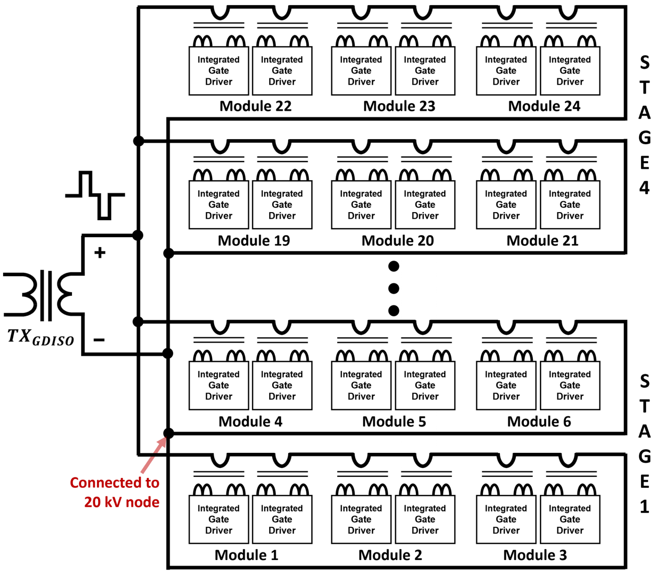


Fig. 3. Structure of the gate-driving loop.

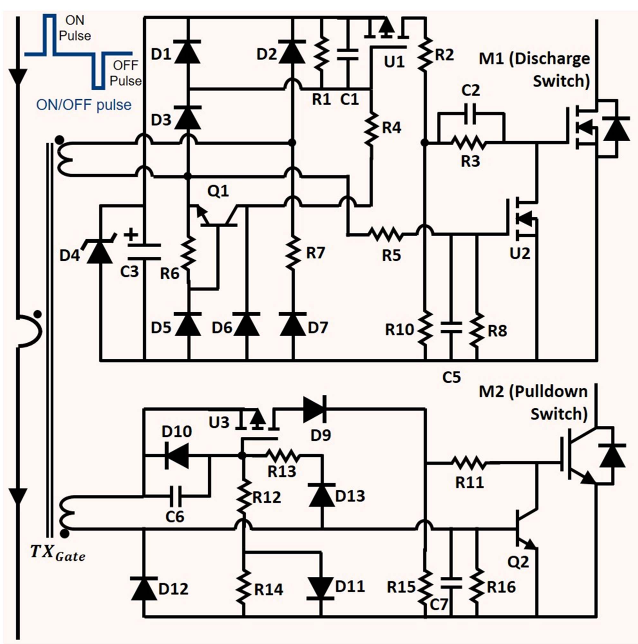


Fig. 4. Integrated gate driver for discharge and pull-down switches.

The gate signal of the discharge switch turns ON when the on pulse is applied, and turns OFF when the OFF pulse is applied. In contrast, the gate signal of the pull-down switch turns ON as the OFF pulse is applied, and slowly decreases after the OFF pulse ends. Fig. 5 shows the operation mode of the integrated gate driver according to the applied ON-OFF pulse signal.

1) Mode 1: Mode 1 is for the preparation of the turn-ON discharge switch (M1). When the on pulse is applied through the gate-driving loop, at the discharge switch gate driver, D2 conducts and the dc link capacitor (C3) is charged. In addition, current flows through D5, and the base-emitter voltage of Q1 increases.

2) Mode 2: Mode 2 is the turn-ON mode of the discharge switch (M1). When Q1 is turned ON, the gate voltage of P-MOSFET U1 is charged, U1 is turned ON, and the gate of M1 is charged by C3, thereby turning M1 on. In modes 1 and 2, at the pull-down switch gate driver, BJT (Q2) is turned ON, preventing parasitic turn-ON of the pull-down switch (M2) by the Miller capacitance when the discharge switch is turned ON, and the drain-source voltage of M2 increases.

3) Mode 3: Mode 3 is the turn-ON-hold mode of the discharge switch (M1). The turn-ON state of M1 is maintained using the energy charged in C3, while U1 is maintained in the turn-ON state. With the turn-ON-hold mode, long pulses can be output through only ON-OFF pulses with short widths, which has the advantage of solving the saturation problem of small toroidal gate cores.

4) Mode 4: Mode 4 is the dead-time mode between M1 and M2. When an OFF pulse is applied through the gate-driving loop, at the discharge switch gate driver, D1, D3, and D7 conduct, and the dc link voltage of C3 is charged. In addition, U1 turns OFF, the gate charging of M1 stops, and U2 turns ON and quickly pulls down the gate energy of M1. Meanwhile, at the pull-down switch gate driver, U3 is not turned ON by the RC time constant. Therefore, a dead time between the discharge switch (M1) and the pull-down switch (M2) are applied. The dead time can be calculated as follows:

$$T_{\text{dead}} = -R_{12} \times (C_6 + C_{GS}) \times \ln \times \left(1 - \frac{V_{TH}}{V_{TX\_IN} - 2V_F}\right) \tag{2}$$

where C_{GS} is gate-source capacitance of U3, C_{GS} is the threshold voltage of U3, and V_F is the forward voltage of D11 and D12.

5) Mode 5: Mode 5 is the turn-ON mode of the pull-down switch (M2). When the OFF pulse continues, U3 turns ON and the gate of the pull-down switch is charged. In modes 4 and 5 where the OFF pulse is applied, at the discharge switch gate driver, U2 remains turned ON. Therefore, when the pull-down switch (M2) is turned ON and the drain-source voltage of M1 increases, parasitic turn-ON by the Miller capacitance is prevented.

6) Mode 6: Mode 6 is the turn-ON-hold mode of the pull-down switch (M2). After the OFF pulse ends, the residual energy of C6 is reset through D13, and the gate voltage of M2 remains turned ON. This mode is maintained for a sufficient time to pull down all the residual energy in the reactor load with the active pull-down circuit. Fig. 6 illustrates the ideal waveforms of the active pull-down pulsed-power module, driven by an ON/OFF pulse inverter and the gate-driving loop. The drain-source voltage waveforms of the discharge switch and pulldown switch are shown under capacitive load conditions.

III. Implementation of Pulsed-Power Modulator

A. Implementation of Module

The discharge and pull-down circuits are implemented as a modular structure. Fig. 7 shows the integrated gate driver and a CAD model of the developed assembled single module. This module consists of a rectifying diode, a storage capacitor, a

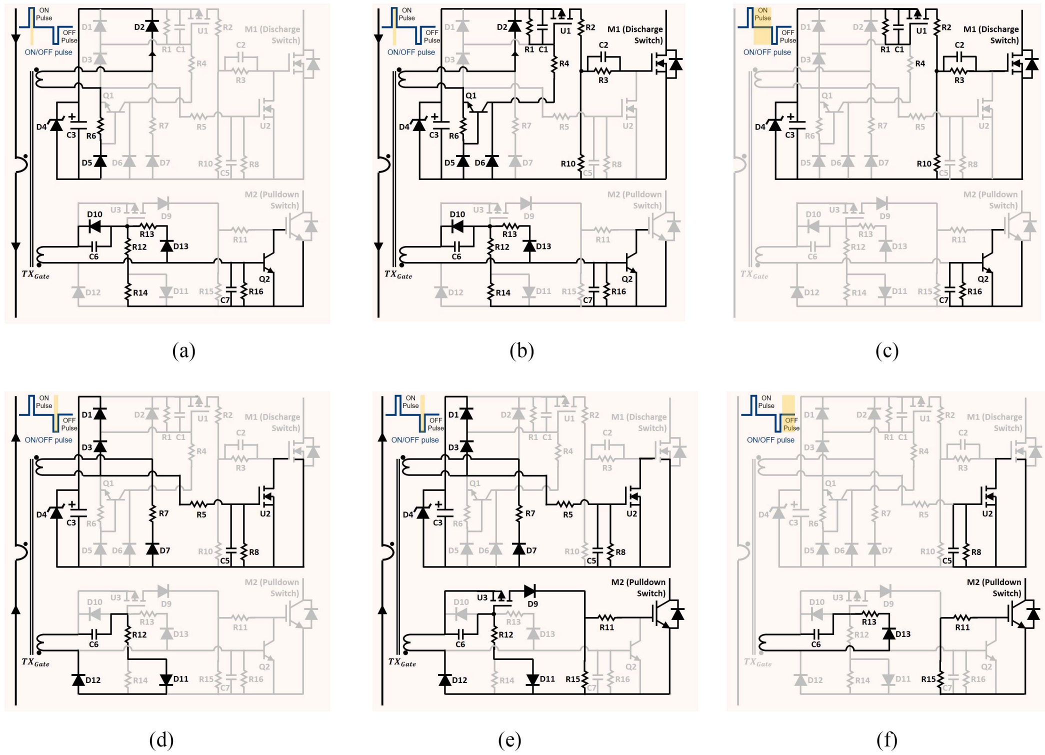


Fig. 5. Operation modes of integrated gate driver. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

parallel resonant capacitor, an integrated gate driver, a discharge switch, and a pull-down switch. Each module can output a maximum of 1.66-kV, as well as provide a pull-down path. This modular structure has the advantage of easy maintenance and enables each module to be implemented with identical parasitic components, which are important factors in improving the reliability of the series stacking method.

B. Implementation of 40-kV Pulse Generator With Active Pull-Down

The 40-kV modulator is developed based on a 24-module structure to effectively implement the series stacking structure of the discharge and pull-down circuits. Fig. 8 shows a CAD model of the pulse modulator. One stage consists of six modules and a stage transformer and can output up to 10-kV. The total output is up to 40-kV with four stages. Primary windings for the four stage transformers are wound simultaneously with a winding for the charging loop using a 100-kV insulated cable. Additionally, the gate-driving loop is configured with a total of 8 parallel loops and is designed to drive three modules per loop in series using a 30-kV insulated cable on the primary side. The secondary windings of the stage transformers and gate transformers are wound with 3-kV insulated cable. Through the proposed structure, an efficient charging and gate-driving loop structure are enabled, and the maximum potential difference between adjacent modules is 10-kV.

Table II gives the main components for implementing the 40-kV pulsed-power modulator. The isolated transformers of the charging loop and gate-driving loops prevent any parasitic malfunction of the charger inverter and pulse inverter when a high voltage pulse is output. Since high-voltage pulses have high-frequency characteristics, isolation transformers with a small parasitic capacitance are configured in the loop, resulting in high-frequency immunity and reliable operation.

TABLE II
COMPONENTS OF 40-KV ACTIVE PULL-DOWN PULSED-POWER MODULATOR

Symbol	Part	Specification
$SW_{Discharge}$	Discharge switch	CREE, C3M0021120D (1200 V, 200 A)
$SW_{Pull-down}$	Pull-down switch	Fairchild, FGL40N120AND (1200 V, 120 A)
$D_{Rectifier}$	Rectifying diode	Cree, C4D05120A (1200 V, 5 A) / 2-series
C_{SR}	Series resonant capacitor	ICEL, PMB (2000 V, 0.56 μF) / 2-parallel
C_{PR}	Parallel resonant capacitor	KEMET, R73UN13304000J (2000 V, 3300 pF) / 2-series
$C_{Storage}$	Storage capacitor	Vishay, MKP1848S55010JP4B (1000 V, 5 μF)
TX_{CISO}	Charging isolated transformer	TDK, EC120x101x30 (PC44) Turn ratio 17:14
TX_{Stage}	Charging stage transformer	TDK, EC120x101x30 (PC44) Turn ratio 4:33
TX_{GDISO}	Gate-driving isolated transformer	EPCOS, B64290L0082X087 (N87) Turn ratio 10:18
TX_{Gate}	Gate transformer	TDK, T18x6x10 (HF70) Turn ratio 1:2

IV. EXPERIMENTAL RESULTS

To verify the performance of the developed 40-kV active pull-down pulsed-power modulator, a gate-driving experiment was conducted for the 24 modules. Furthermore, a pulse output

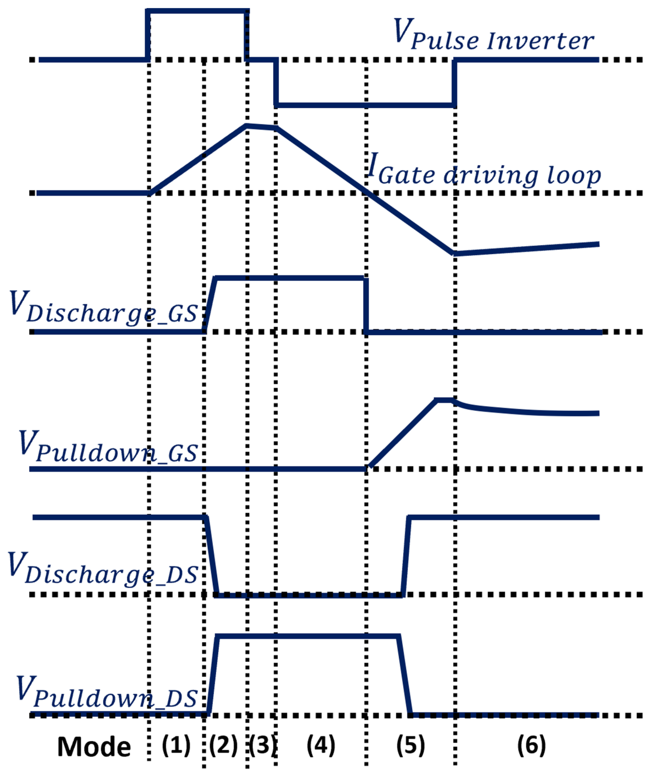
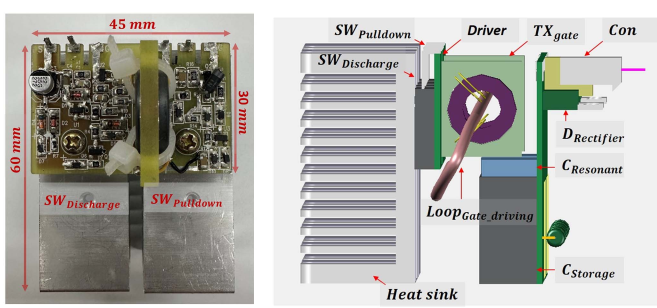


Fig. 6. Ideal waveforms of the active pull-down pulsed-power module.



(a) (b)

Fig. 7. Implementation of module. (a) Integrated gate driver.(b) CAD model of assembled single module.

experiment under a plasma reactor load was conducted. The measurement equipment comprised a Tektronics P6015A high voltage probe, a Pearson 4997 CT, and a Yokogawa 700924 differential probe. Fig. 9 shows the experimental setup for driving plasma reactor using the developed modulator.

A. Gate-Driving and Capacitor-Charging Experiment

Fig. 10 shows the experimental waveforms of the series driving 48 integrated gate drivers. An ON-OFF pulse voltage was applied to the gate-driving loop from the pulse inverter. When the on pulse was applied, the current flowing through the gate-driving loop had a rising slope when an OFF pulse was applied, the current had a falling slope. The gate voltage increases as the length of the applied ON- and OFF-pulse widths increases. However, as the on-pulse width increases, the positive peak of the gate-driving loop current increases. Therefore,

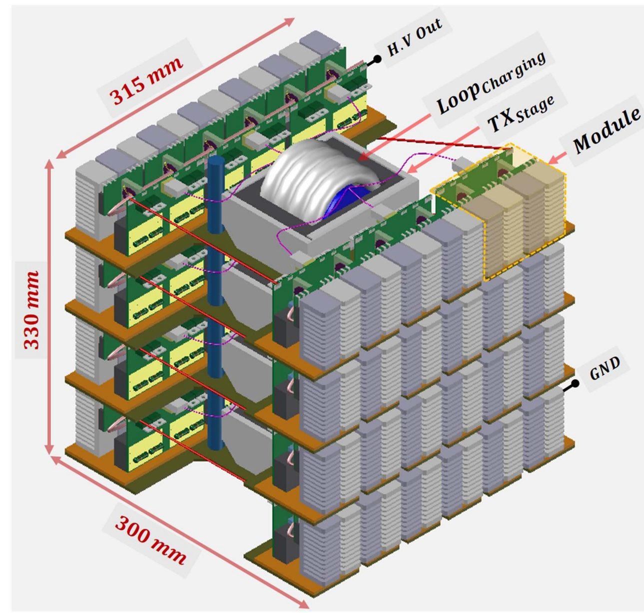
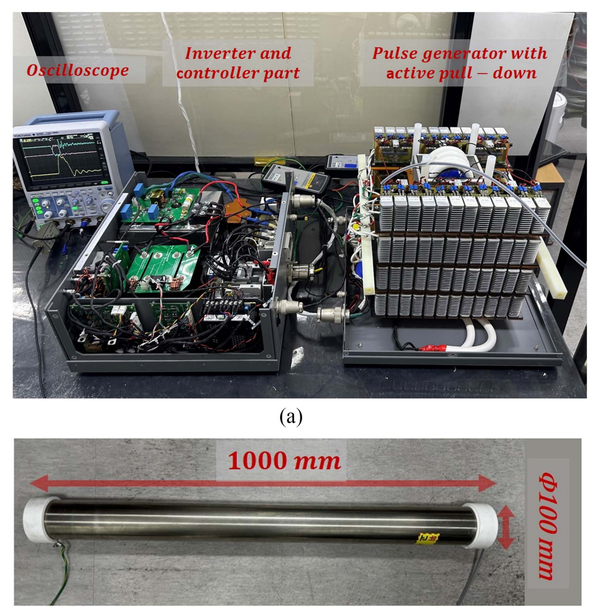


Fig. 8. Implementation of 40-kV pulse generator with active pull-down.



(a)

(b)

Fig. 9. Experimental setup for driving plasma reactor using the developed modulator. (a) Developed pulsed power modulator and oscilloscope. (b) Plasma reactor.

there is the problem that the minimum pulse width that can be output increases. Additionally, the longer the OFF-pulse width, the higher the negative peak of the gate-driving loop current. Therefore, the OFF-pulse width should be selected so as not to exceed the allowable current range of the pulse inverter switch. Accordingly, considering securing the gate voltage, controlling the minimum pulse width, and ensuring the allowable switch current, the ON- and OFF pulse widths were selected as 250-ns and 500-ns, respectively. Regarding jitter characteristics, measurements confirmed that the 24 modules exhibited a maximum synchronization error of 10 ns.

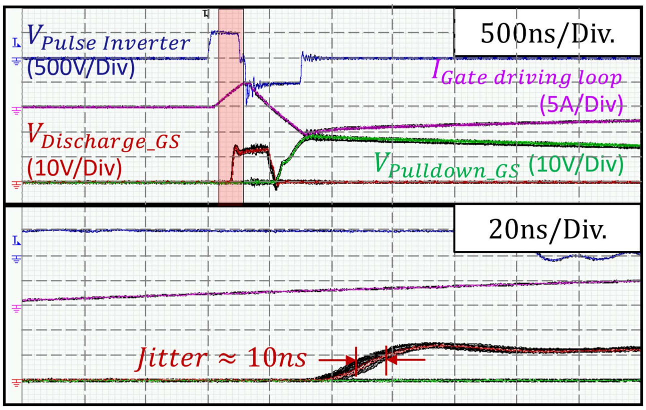


Fig. 10. Waveform of gate-driving for 24 modules.

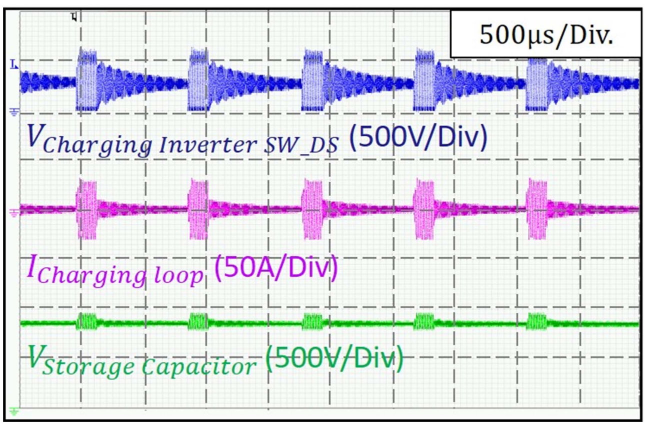


Fig. 11. Waveform of capacitor charging for 24 modules.

According to the operation mode described previously, when the on pulse was applied, the gate signal of the discharge switch was approximately 15-V. When an off pulse was applied, the gate of the discharge switch was turned OFF. Moreover, after a dead time of approximately 80-ns, the gate of the pull-down switch was charged. Even after the OFF pulse ended, the gate signal of the pull-down switch was maintained for a sufficient time of more than 10-μs. In addition, the synchronization of the 48 discharge switches and 48 pull-down switches was verified to be within less than a 10-ns error.

Fig. 11 shows the experimental waveforms of charging 48 capacitors in parallel under no-load condition. The charger controller senses the capacitor voltage of module 1 at stage 1 and performs voltage control. Each of storage capacitors was charged to approximately 840-V from the charging inverter through the charging loop and stage transformers. When the cell voltage reached the reference voltage, the charger stopped operating, causing oscillations in the drain-source voltage and resonant current waveforms due to the resonance between the resonant inductor and the snubber capacitor. When the charging voltage dropped below the reference level, the charger resumed operation. The charging voltage balancing was verified to have less than 4% tolerance.

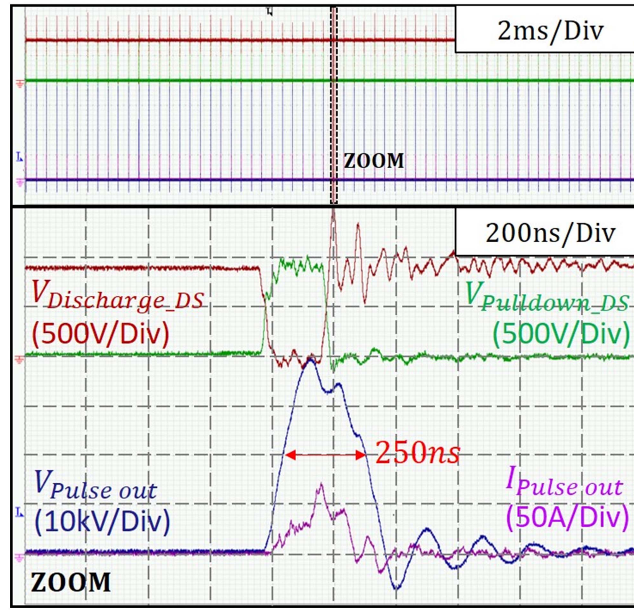


Fig. 12. Waveform of pulse output under plasma reactor load.

B. Plasma Reactor Load Experiment

The developed 40-kV pulse modulator was tested for pulse output under plasma reactor load conditions. The plasma reactor has a size of (1000-mm, Φ100-mm). Through the capacitor charger, each of the 48 storage capacitors was charged with a voltage of approximately 830-V, and as the 48 discharge switches were turned ON, a voltage of up to 40-kV was applied to the load. Fig. 12 shows the experimental waveform of the 40-kV, 73-A pulse output of at 3-kHz, which is the rated pulse repetition rate. Furthermore, a pulse width of 250-ns with a 90-ns rise time was measured. All the residual energy of the plasma reactor was dissipated through pull-down switches and no arc occurred during reactor load experiments.

Through the experimental results, the pulse output and reactor-driving performance of the proposed pulse modulator were verified. In addition, in gas processing application experiments, it is expected that the shorter pulse width output of 250-ns can suppress the recombination reaction by the subsequent oxidation reaction and achieve higher abatement efficiency, as well as high reliability from arc occurrence.

V. Conclusion

In this article, a 40-kV active pull-down pulsed-power modulator was developed to drive a plasma reactor in gas abatement. To achieve a submicrosecond pulse output with the plasma reactor, discharge and pull-down circuits were designed and implemented based on a modular structure. As a solution to operate 24 modules reliably, a gate-driving loop structure for efficient synchronous driving of the series-stacked modules was proposed. Furthermore, the integrated gate driver for driving the discharge and pull-down switches was designed in consideration of dead time application and parasitic turn-ON prevention to ensure reliability for complementary operation between the discharge and pull-down switches. Herein, implementation of the single module and entire pulsed-power modulator were presented considering high voltage isolation. The developed pulse modulator was tested for a pulse output of up to 40-kV under a plasma reactor load (1000-mm, Φ100-mm) condition, and achieved a 40-kV pulse output with a rise time of 50-ns, a pulse width of 250-ns, and a pulse repetition rate of 3-kHz. These results are expected to contribute to improving gas abatement efficiency with short pulse widths and high repetition rates. In future studies, the developed modulator will be applied to a large-capacity gas reactor and gas abatement experiments.

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