Carrier Phase Synchronization Based on Circulating Current Identification for Distributed Inverters

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***Abstract*—Distributed parallel inverters are a promising solution for large power systems due to their flexibility and reliability. However, the distributed control mode often causes carrier phase desynchronization among the control units, leading to adverse effects on high-frequency harmonics and power loss. To address this issue, this article proposes a carrier phase synchronization (CPS) method for distributed parallel inverters, leveraging circulating current identification. In the proposed scheme, circulating currents in parallel inverters directly influence high-frequency harmonics and carry carrier phase information. The peak amplitude of these currents is used to identify the CPS point and adaptively adjust the carrier phase difference. The proposed strategy leverages existing circulating currents to achieve CPS in parallel inverters, eliminating the need for additional synchronization hardware. Consequently, this solution not only reduces system costs and size but also enables CPS-based multifunctionality, such as power quality optimization and common mode reduction. Finally, both simulation and experimental results are provided to validate the effectiveness of the proposed CPS method and the associated analysis.**

***Index Terms*—Carrier phase synchronization (CPS), circulating current, distributed parallel inverter system.**

I. Introduction

In recent years, renewable energy generation has grown rapidly, and inverters have been widely used to connect renewable energy systems to the grid [1], [2], [3], [4], [5]. Over the past few decades, centralized inverters have been widely used in large-scale photovoltaic stations [6]. However, a key drawback of centralized inverters is their reliance on a single maximum power point tracking method [6], [7], [8], which prevents full utilization of the power generation potential of each PV array due to the nonuniform geographical and temporal distribution of renewable energy sources.

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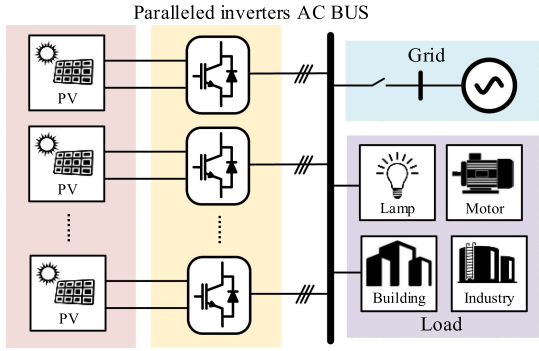

Fig. 1. Distributed paralleled inverter power generation system.

Consequently, an increasing number of PV power plants are adopting distributed paralleled inverter systems to improve control margins [9], [10], [11], [12], [13]. In a distributed generation system, each PV array is individually controlled to track its maximum power point, optimizing control to improve grid-connected performance (e.g., reducing line losses and improving converter overload protection), thereby increasing the penetration and utilization of renewable energy [14]. Fig. 1 illustrates the new energy generation system using distributed paralleled inverters, where the power generating equipment passes through the inverter and converges at the ac bus, which is connected to the grid or load.

Compared to centralized systems, distributed systems suffer from carrier desynchronization at the execution layer due to different carrier generation units. Carrier synchronization at the execution layer is essential for the system's global PWM optimization strategy, eliminating the need for expensive and complex solutions such as additional hardware or modifications to the inverter topology [15], [16], [17], [18], [19], [20]. For example, literature [21], [22], [23] proposes a method to reduce leakage current by controlling the phase shift angle; Jiang et al. [24] introduce a ZCMV modulation algorithm for common-mode voltage cancellation by strictly controlling the cancellation of the pulse signal; Liu et al. [25] introduce a PS-SPWM modulation algorithm can reduce CMV by reducing the number of different switching-state combinations. However, the high-frequency characteristics of the carrier wave make synchronization extremely challenging, requiring very high precision. Thus, achieving high-precision carrier phase synchronization (CPS) for inverter control in distributed systems has become a critical and challenging issue.

To address the issue of carrier synchronization at the execution level, several research efforts have proposed leader-follower synchronization methods that provide an external uniform synchronization signal to the system. Benaifa et al. [26] proposed a method that achieved carrier synchronization by sending carrier signals directly from an independent external synchronization unit. Bae and Kim [27] used a CAN communication channel to send and receive carrier synchronization commands and adjust the internal carrier phase (Comm-CPS). This method requires an external synchronization unit, adding additional system cost. Although some communication systems have been integrated into inverters, most are unable to meet the requirements for CPS due to unacceptable delays (ranging from 100 μs to several seconds) caused by data encapsulation or long communication distances (several hundred meters) [28], [29].

In addition to leader-follower carrier synchronization methods, several local information-based approaches have been proposed for CPS. Perreault and Kassakian [30] proposed a distributed carrier phase-shifting method, where the clock signal generators of multiple inverters are connected in parallel through an oscillating synchronization line, grounded through a resistor, ensuring that each inverter generates signals with the same frequency and amplitude. However, this method still requires complex line construction. Hu and Ma [31] proposed a carrier in-phase method based on the zero-sequence current component and a virtual oscillator to eliminate common-mode circulating current. The accuracy of this method is limited by sampling errors and the virtual oscillator. Cho et al. [32] used the zero-crossing moment of the grid voltage for carrier synchronization, which requires no additional hardware and is easily scalable. However, this method allows carrier synchronization only at the zero-crossing point of the grid voltage, and its accuracy is limited by grid voltage distortion and sampling errors. Xu et al. [33] and He et al. [34] proposed a phase-locked-loop synchronized carrier (PLL-CPS) method, but the accuracy is limited by fluctuations in the PLL results between the inverters. Moreover, all of these carrier synchronization methods rely on local information, their accuracy is limited by fluctuation errors in processing this information.

Based on the investigations above, it is evident that CPS in distributed parallel inverter systems cannot achieve high accuracy at low cost. CPS, which is critical for the execution of the global PWM strategy in distributed inverters, should be emphasized. For this reason, we propose a CPS method based on circulating current identification for distributed inverters (CICPS).

The rest of this article is organized as follows. Section II introduces the CICPS scheme and its principles within the distributed paralleled inverter system. Section III verifies the feasibility of CICPS through simulation. Section IV presents the verification and superiority of CICPS through comparative experiments. Finally, Section V concludes this article.

II. Principle of Proposed CPS for Distributed Inverter System

This section first briefly introduces the distributed parallel inverter system, and then presents the principles of the proposed CICPS scheme comprehensively.

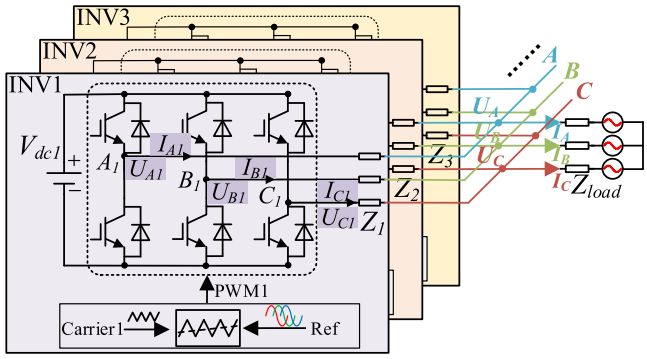

Fig. 2. Block diagram of distributed paralleled inverters system.

A. Introduction of Distributed Parallel Inverter System

Fig. 2 illustrates the topology of the typical distributed parallel two-level three-phase inverter system.

According to Kirchhoff's voltage and current law, the voltage and current equation of the inverter system can be derived

$$U_{XK} - U_X = Z_K I_{XK} \tag{1}$$

$$I_X = \sum_{K=1}^{N} I_{XK} \tag{2}$$

where $X = A,B,C$, $K = 1,2,3 \ldots N$, U_{XK}, I_{XK}, and Z_K are the X-phase output voltage, current and line impedance in INVK, U_X and I_X are the X-phase total output voltage and current of parallel inverters.

In ideal conditions, the output current of each inverter flows evenly through the load. However, due to differences in parameters and operating conditions between inverters, the output voltages of each inverter may be different, resulting in circulating currents that flow between the inverters. Taking the two-paralleled inverters as an example, the circulating current is generated and can be calculated as

$$I_{X1c} = \frac{U_{X1} - U_{X2}}{Z_1 + Z_2} = -I_{X2c} \tag{3}$$

where I_{XKc} is the circulating current of INVK. Thus, when the inverter carriers are unsynchronized, a deviation in the switching times of the power devices causes voltage differences between the inverters, resulting in high-frequency circulating currents between the parallel inverters. Based on this phenomenon, the relationship of circulating current and carrier phase difference can be utilized to realize the CPS.

B. Circulating Currents Analysis and Extraction for the Proposed CICPS

Usually, the output phase-leg voltage is related to the fundamental and switching frequencies, so the double Fourier analysis method can be utilized. The output phase-leg voltage depends on two time-variables as follows:

$$x(t) = \omega_c t + \theta_c \tag{4}$$

$$y(t) = \omega_0 t + \theta_0 \tag{5}$$

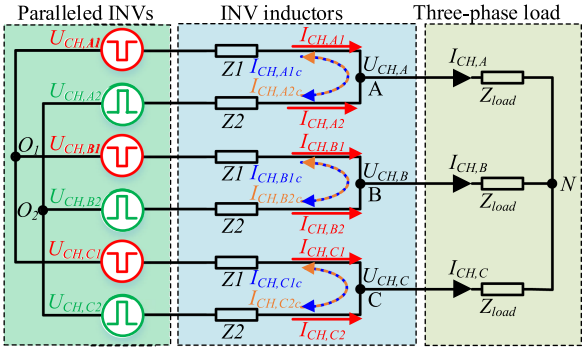

Fig. 3. Equivalent circuit of the distributed parallel two-inverters system in CH component.

where ω_c is the angular frequency of the carrier, θ_c is the initial phase angle of the carrier, ω_0 is the angular frequency of the fundamental, and θ_0 is the initial phase angle of the fundamental. Thus, by double Fourier transform, the phase-leg voltage can be decomposed as follows:

$$\begin{aligned} U_{XK}(t) &= A_{XK}^{0,0} + A_{XK}^{0,1}\cos(\omega_0 t + \theta_{XK}^0) \\ &+ \sum_{m=1}^{\infty} A_{XK}^{m,0}\cos m(\omega_c t + \theta_{XK}^c) \\ &+ \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} A_{XK}^{m,n}\cos[m(\omega_c t + \theta_{XK}^c) \\ &+ n(\omega_0 t + \theta_{XK}^0)] \end{aligned} \tag{6}$$

where θ_{XK}^0 and θ_{XK}^c are the initial phase angle of the fundamental and carrier waves, $A_{XK}^{m,n}$ is the amplitude of each component for X phase-leg voltage of INVK. In (6), the first term represents the dc component, the second term represents the baseband harmonics, the third term represents the carrier multiple harmonics (CMH), where $m = 1$ corresponds to the carrier harmonic (CH), and the fourth term represents the sideband harmonic (SH).

From (6), it can be seen that the CH components of the three phases do not vary with the fundamental phase angle. And with the identical carriers, the three phase CH components satisfy the relationship:

$$U_{CH,AK} = U_{CH,BK} = U_{CH,CK} = A_{XK}^{1,0}\cos(\omega_c t + \theta_{XK}^c) \tag{7}$$

where $U_{CH,XK}$ is the CH component of U_{XK}. In this case, an equivalent circuit of the parallel two-inverter system in carrier frequency can be established, as shown in Fig. 3.

Taking the carrier phase of INV1 as reference, i.e., $\theta_{X1}^c = 0$, the phase of INV2 can be given by φ_{X2}^c ($\varphi_{X2}^c = \theta_{X2}^c - \theta_{X1}^c$). The CH components of the paralleled phase-leg voltages for two inverters can be expressed as

$$\begin{aligned} U_{CH,A1} &= U_{CH,B1} = U_{CH,C1} \\ &= A_{X1}^{1,0}\cos(\omega_c t + \theta_{X1}^c) = A_{X1}^{1,0}\cos(\omega_c t) \\ U_{CH,A2} &= U_{CH,B2} = U_{CH,C2} \\ &= A_{X2}^{1,0}\cos(\omega_c t + \theta_{X2}^c) = A_{X2}^{1,0}\cos(\omega_c t + \varphi_{X2}^c). \end{aligned} \tag{8}$$

(9)

Therefore, the CH component of the circulating current is given by

$$\begin{aligned} I_{CH,X1c} &= -I_{CH,X2c} = \frac{U_{CH,X1} - U_{CH,X2}}{Z_1 + Z_2} \\ &= \frac{A_{X1}^{1,0}\cos(\omega_c t) - A_{X2}^{1,0}\cos(\omega_c t + \varphi_{X2}^c)}{Z_1 + Z_2} \end{aligned} \tag{10}$$

where $I_{CH,XKc}$ is the CH component of circulating current I_{XKc}. It can be observed that $I_{CH,X2c}$ is directly related toφ_{X2}^c. Therefore, the carrier phase difference can be determined by analyzing the relationship between $I_{CH,X2c}$ and φ_{X2}^c.

To extract switching frequency circulating current $I_{CH,XKc}$ in distributed inverter, the optional method is extracting from the phase-leg current $I_{CH,XK}$; whereas, $I_{CH,XK}$ primarily consists of two components: $I_{CH,XKc}$, and the other is the CH components of phase current I_X. Assuming the phase current is generally evenly distributed among the phase-leg currents of parallel inverters, the CH currents satisfy

$$I_{CH,XK} = \frac{I_{CH,X}}{2} + I_{CH,XKc} \tag{11}$$

where $I_{CH,X}$ is the CH of I_X . In addition, based on the impedance symmetry of the circuit shown in Fig. 3, and the same voltage sources according to (7), the CH phase voltage can be same. Therefore

$$U_{CH,A} = U_{CH,B} = U_{CH,C}. \tag{12}$$

From (12), it can be seen that there is no voltage difference at phase terminals (A, B, C). Therefore, there is no CH component in I_X

$$I_{CH,X} = 0. \tag{13}$$

Substituting (10) and (13) into (11), the following is obtained:

$$I_{CH,X1} = I_{CH,X1c} = -I_{CH,X2} = -I_{CH,X2c} = \frac{U_{\Delta CH,X(1,2)}}{Z_1 + Z_2} \tag{14}$$

where $U_{\Delta CH,X(1,2)}$ is the CH voltage difference between the paralleled phase-leg voltage, and can be expressed as

$$\begin{aligned} U_{\Delta CH,X(1,2)} &= U_{CH,X1} - U_{CH,X2} \\ &= A_{X1}^{1,0}cos(\omega_c t) - A_{X2}^{1,0}cos(\omega_c t + \varphi_{X2}^c). \end{aligned} \tag{15}$$

Therefore, with the determined loop impedance, $I_{CH,X1}$ and $I_{CH,X2}$ exhibit a direct relationship with $U_{\Delta CH,X(1,2)}$.

Thus, the following step is to extract $|I_{CH,XK}|$ from I_{XK}. Due to the high CH frequency and the presence of sideband signals ($\omega_c \pm\omega_0$) near the spectrum, the Q ($Q = \omega_c/B$, $B = 2\omega_0$) of the applicable bandpass filters are too large to design. Therefore, the coherent demodulation is employed to accurately extract CH information, as shown in Fig. 4. The principle is that the $I_{CH,XK}$ is frequency shifted to dc by multiplying I_{XK} with sinusoidal signal $c(t)$, which is provided with the same frequency and phase

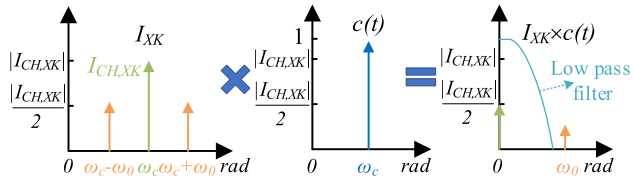

Fig. 4. Coherent demodulation in frequency domain.

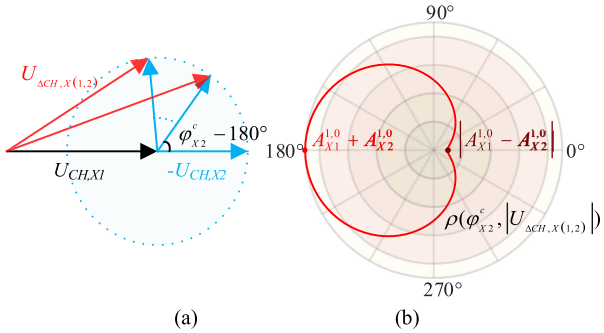

Fig. 5. $U_{\Delta CH,X(1,2)}$ generation. (a) Synthesis process of $U_{\Delta CH,X(1,2)}$. (b) Relationship between $|U_{\Delta CH,X(1,2)}|$ and φ^c_{X2}.

as the inverter's carrier; then through a lowpass filter, $|I_{CH,XK}|$ can be extracted.

C. Relationship Identification Between Phase Difference and Circulating Currents for the Proposed CICPS

From (15), the generation process of $U_{\Delta CH,X(1,2)}$ and the relation between $|U_{\Delta CH,X(1,2)}|$ and φ^c_{X2} can be obtained, as shown in Fig. 5. It can be seen that the absolute value of $U_{\Delta CH,X(1,2)}$ ($|U_{\Delta CH,X(1,2)}|$) is related to the carrier phase difference φ^c_{X2}, and $|U_{\Delta CH,X(1,2)}|$ is minimized regardless of the amplitude difference for these two inverters when $\varphi^c_{X2} = 0°$, and the minimum value is $|A^{1,0}_{X1} - A^{1,0}_{X2}|$. When $\varphi^c_{X2} = 180°$, the maximum value of $A^{1,0}_{X1}+A^{1,0}_{X2}$ can also be obtained.

For the complex N-inverter distributed system, the circulating current of CH component can be calculated as

$$|I_{CH,XKc}| = \frac{|U_{CH,XK} - U_{CH,X}|}{Z_K} \tag{16}$$

$$U_{CH,X} = \frac{\sum_{k=1}^{N} U_{CH,Xk}}{N}. \tag{17}$$

When the parameters of all inverters are identical, it can be easily deduced that the paralleled phase-leg voltage of point X satisfy

$$A^{1,0}_{X1} = A^{1,0}_{X2} = A^{1,0}_{X3} = \ldots = A^{1,0}_{XN}. \tag{18}$$

Thus, when all inverters are CPS, i.e.,

$$\varphi^c_{X2} = \varphi^c_{X3} = \varphi^c_{X4} = \ldots = \varphi^c_{XN} = 0. \tag{19}$$

Substituting (18) and (19) into (7), it can be seen that

$$U_{CH,X1} = U_{CH,X2} = U_{CH,X3} = \ldots = U_{CH,XN}. \tag{20}$$

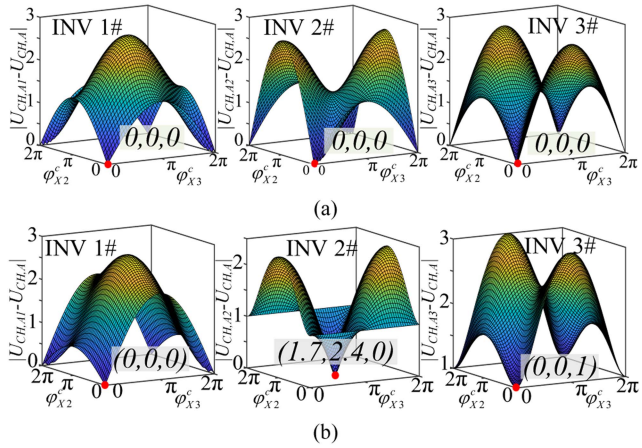

Fig. 6. Voltage of CH component between the X phase-leg in INVK and point X ($|U_{CH,XK}$-$U_{CH,X}|$) varies with the scanning of φ^c_{X2} and φ^c_{X3}: (a) while $A^{1,0}_{X1}$=$A^{1,0}_{X2}$ =$A^{1,0}_{X3} = 2$; (b) while $A^{1,0}_{X1} = 2$, $A^{1,0}_{X2} = 1$, and $A^{1,0}_{X3} = 3$.

From (17) and (20), it is obvious

$$U_{CH,XK} - U_{CH,X} = 0. \tag{21}$$

So, from (16), $|I_{CH,XKc}|$ and $|U_{CH,XK}$-$U_{CH,X}|$ will always be minimum when with CPS. Take the three-inverter system as an example, the two INVs simultaneous scanning result is shown in Fig. 6(a). The CPS point can be found at the point of minimum voltage difference.

But in most cases, the conditions of (18) cannot be achieved, i.e.,

$$A^{1,0}_{X1} \neq A^{1,0}_{X2} \neq A^{1,0}_{X3} \neq \ldots \neq A^{1,0}_{XN}. \tag{22}$$

The difference of $A^{1,0}_{XK}$ will affect the determination of the minimum value during the simultaneous scanning of multiple inverters. Also taking the three-inverter system as an example, as shown in Fig. 6(b). It can be seen that INV2 reaches the minimum value in the asynchronous point. Therefore, the simultaneous scanning method of multiple inverters is only applicable when the input parameters of inverters are nearly identical.

To solve the problem that the synchronization point is misjudged when (18) is not fulfilled, the proposed CICPS uses gradual synchronization strategy. Specifically, the system adds inverters one by one, synchronizing each inverter before proceeding to the next one. When the current $K-1$ inverters are CPS, i.e.:

$$\varphi^c_{Xk} = 0\,(k = 2, 3, 4 \ldots K-1)\,. \tag{23}$$

The CH component in the output of these $K-1$ inverters can be approximated equivalently as

$$U_{CH,XS(K-1)} = \frac{\sum_{k=1}^{K-1} A^{1,0}_{Xk}}{K-1} \cos(\omega_c t) \tag{24}$$

where $U_{CH,XS(K-1)}$ is the CH component in the output voltage of the $(K-1)$-inverter system. Therefore, the $(K-1)$-inverter system can be considered equivalent to an inverter that is synchronized with the main inverter INV1. Each time a new inverter is connected to the system, it can be treated as a system

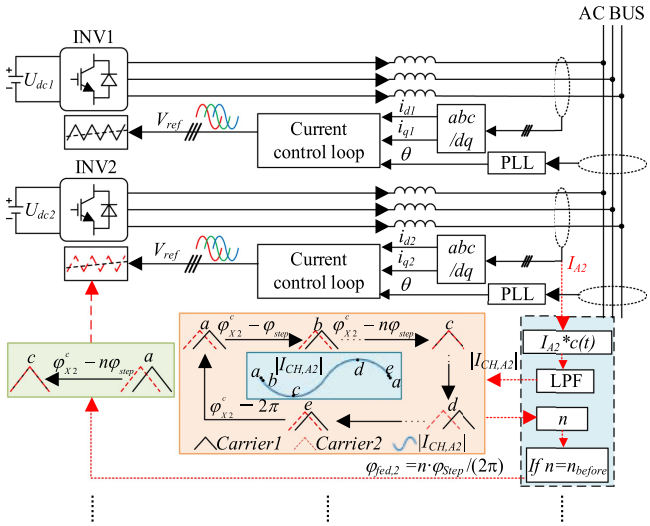

Fig. 7. Block diagram of the CICPS algorithm in distributed inverters system.

consisting of two inverters. Thus, the voltage difference, which generate circulating current, versus phase difference in the newly connected inverter is consistent with Fig. 5. The CICPS converts the synchronization of the N-inverter system into N-1 times synchronization of the two-inverter system. Each synchronization can achieve by finding the minimum point of circulating current through a phase scanning process based on the relationship in Fig. 5. Thus, the proposed CICPS is suitable for N-inverter distributed system regardless of the parameters discrepancy.

Based on the above-mentioned introduction, the block diagram of the CICPS algorithm in N paralleled inverters distributed system is shown in Fig. 7. The system control method is similar with conventional grid-connected inverters, and the proposed CICPS method is inserted into the system. The specific CICPS process for each N-1 inverter is as follows: first, measuring I_{XK} and extracting $|I_{CH,XK}|$ from it by coherent demodulation; then identify the required phase difference $\varphi_{\mathrm{fed},K}$ for synchronization based on the results of scanning $\varphi_{\mathrm{fed},K}$, which is corresponding to changes in $|I_{CH,XK}|$, where $\varphi_{\mathrm{fed},K}$ $(K = 2, 3, 4 \ldots N)$ is the normalized phase compensation of the INVK; finally, based on the identified $\varphi_{\mathrm{fed},K}$ for synchronization, ending the scanning process with fixed compensation, thereby achieving CPS. CICPS implements CPS through closed-loop control that compensates for phase differences using feedback from circulating information generated by phase differences. Compared to the open-loop control of Comm-CPS and PLL-CPS, which receive external information, it can theoretically achieve higher precision in CPS control.

III. Simulation

To validate the proposed CICPS scheme, a simulation model using PLECS is developed. The simulation parameters are listed in Table I.

First, the CPS scanning operation of two paralleled inverters are used to investigate the relationship between switching frequency circulating current $|I_{\mathrm{CH,A2}}|$ and the carrier phase

TABLE I
Parameters

Parameters	Value
DC link voltage	150 V
INV switching frequency	10 kHz
Fundamental frequency	50 Hz
INV paralleled inductors	1.4 mH
Load inductors	1.4 mH
Load resistors	5 Ω

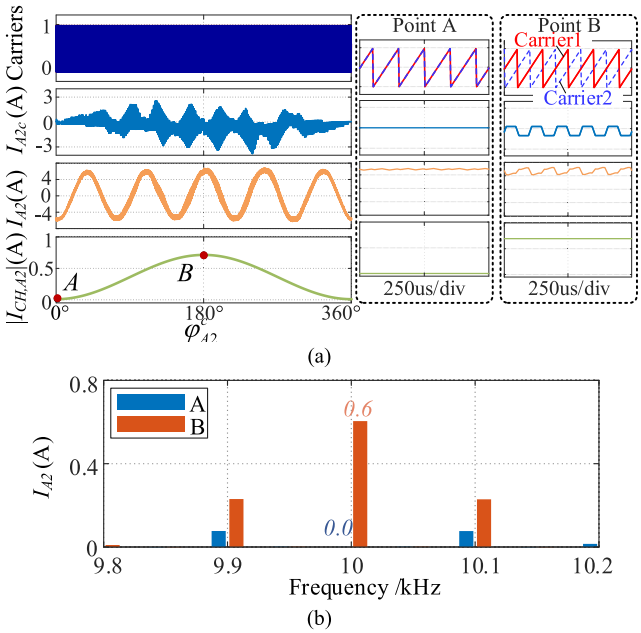

Fig. 8. Relationship of I_{XKc} and I_{XK} with carrier phase difference. (a) I_{A2c}, I_{A2}, and $|I_{CH,A2}|$ versus phase difference φ^c_{A2}. (b) Spectrum analysis of I_{A2} in point A and point B.

difference φ^c_{A2} of INV2, as shown in Fig. 8(a). It can be seen that the circulating current I_{A2c}, the phase-leg current I_{A2}, and $|I_{CH,A2}|$ extracted by the filter all vary with φ^c_{A2}. $|I_{CH,A2}|$ is minimized at $\varphi^c_{A2} = 0°$ and maximized at $\varphi^c_{A2} = 180°$, which is consistent with theory. Fig. 8(b) shows the spectral information of I_{A2} for point A ($\varphi^c_{A2} = 0°$) and point B ($\varphi^c_{A2} = 180°$). When $\varphi^c_{A2} = 0°$, $|I_{CH,A2}| = 0$, which means no switching frequency current existing in I_{A2}, and INV2 keep CPS state; and when $\varphi^c_{A2} = 180°$, $|I_{CH,A2}| = 0.6$, which means obvious switching frequency current in I_{A2} and INV2 out of CPS state.

With the relationship between φ^c_{A2} and $|I_{CH,A2}|$, the proposed CICPS algorithm can be implemented, as shown in Fig. 9. The CICPS algorithm usually consists of three steps: before CPS which INV2 is initially connected to the system; the scanning process, which the normalized carrier phase compensation value $(\varphi_{\mathrm{fed},2})$ of INV2 is scanned and the required $\varphi_{\mathrm{fed},2}$ for synchronization is identified; after CPS which the carrier phase compensation is applied based on the identified $\varphi_{\mathrm{fed},2}$ to achieve synchronization. It can be seen that after implementing the CICPS, the difference between the phase-leg voltages (U_{A12}) and the carrier signals of the two inverters approaches zero, demonstrating that the two inverters are synchronized.

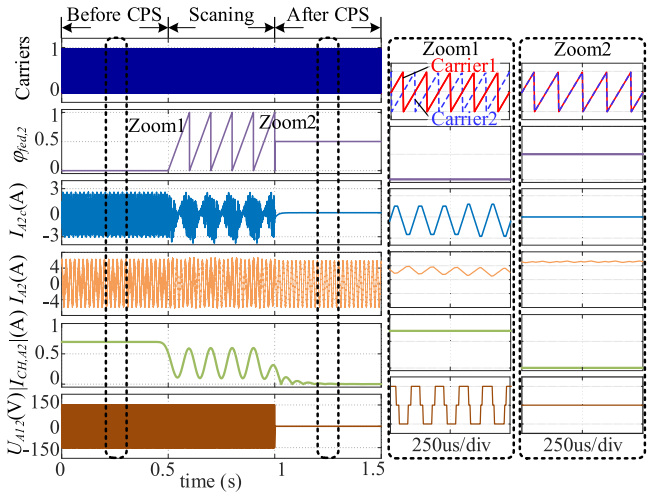

Fig. 9. Synchronization process of two paralleled inverters.

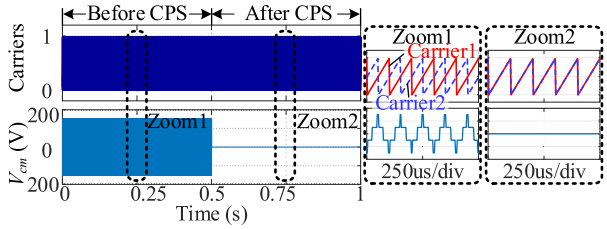

Fig. 10. CPS validation with the ZCMV algorithm for the proposed CICPS.

With the CPS for two paralleled inverters, the global PWM strategies related with carrier phase can be optimized. For example, the ZCMV modulation strategy, which require pulse precise cancelation is implemented for validation. As shown in Fig. 10, when the two inverters are not synchronized, the ZCMV modulation strategy cannot achieve the desired common-mode voltage reduction effect. After applying the proposed CICPS algorithm, the strategy works effectively, which the common-mode voltage can be canceled. This effect shows the availability of the proposed CICPS.

In addition, when the number of parallel inverters increases to three, the CICPS can be implemented sequentially. As shown in Fig. 11, INV2 is first accessed for synchronization using the CICPS algorithm, followed by INV3 for synchronization. Thus, the process of A, B, C are similar with Fig. 9, which realize the INV2 synchronization. The remaining process of D, E, F repeat the identical operation to obtain INV3 synchronization. With the CPS achieved, the difference between the phase-leg voltages U_{A12}, U_{A13} are reduced to zero.

IV. Experimental Results and Discussion

To further evaluate the performance of the proposed CICPS method and compare with other schemes, experiments are implemented in an experimental platform, as shown in Fig. 12. Three RT Boxes with three-phase two-level inverter modules are utilized to consist the distribute control system. Measured

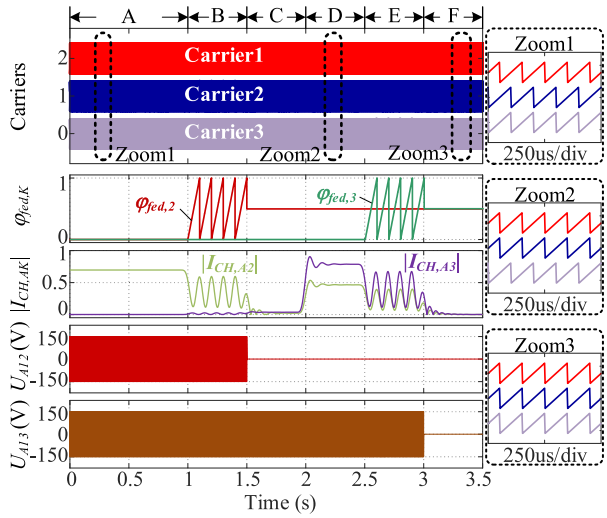

Fig. 11. CPS process of three inverters for CICPS.

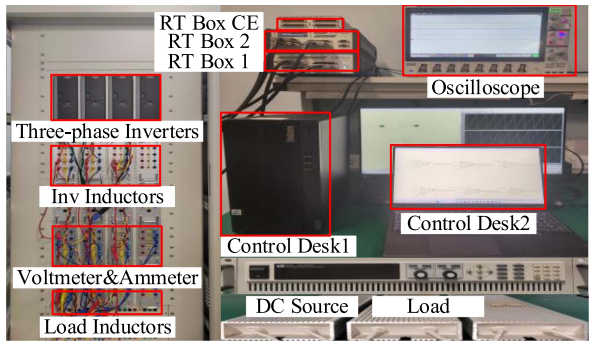

Fig. 12. Experimental test platform.

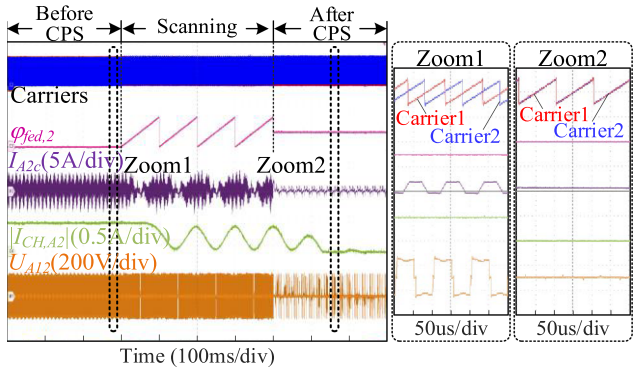

Fig. 13. Process diagram of CICPS in a distributed two-inverters system.

currents and voltages from the voltmeter and ammeter are used for observation, control, and CPS. The main experimental parameters are the same as simulation parameters listed in Table I.

A Validation of the Effectiveness of CICPS

First, the CICPS method is implemented in a two-inverter system, as shown in Fig. 13. The CICPS method is also divided

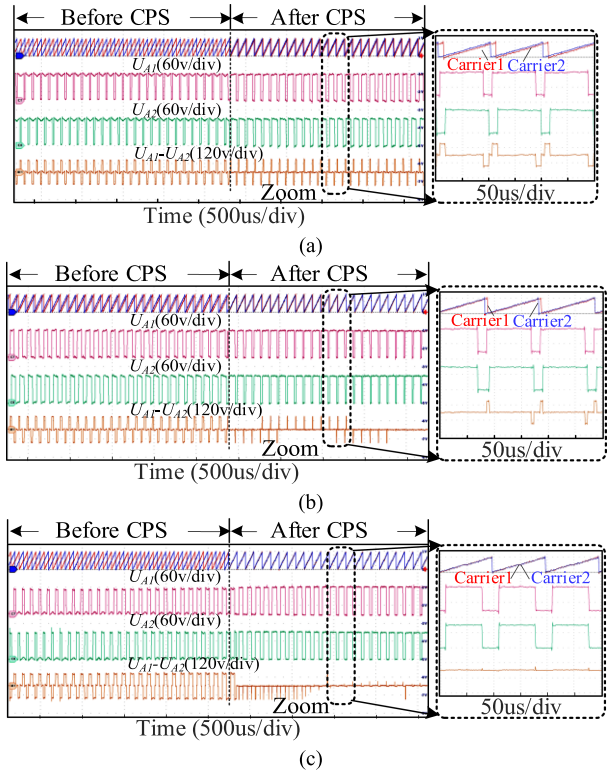

Fig. 14. Comparison of the accuracy of different algorithms. (a) Comm-CPS. (b) PLL-CPS. (c) CICPS.

into three steps. The step 1 occurs when INV2 is connected to the system, but the carrier of INV2 is not synchronized. Step 2 begins with a scan of $\varphi_{\mathrm{fed},2}$ between 0 and 1, with a period of 100 ms and a scanning step of 1/10k. Based on the scanning results, the relationship of $I_{CH,A2}$ and $\varphi_{\mathrm{fed},2}$ can be identified. However, the scanning process is influenced by the transient behavior of the filter circuit. Therefore, the scanning time is extended when the circuit reach a steady state. Experimental results show that when the scanning time exceeds four scanning cycles (400 ms), the identified phase difference stabilizes. With the identified suitable $\varphi_{\mathrm{fed},2}$, the compensation of phase difference can be implemented in step 3. It can be seen that after the CICPS, carrier1 and carrier2 are nearly identical, and the difference between the phase-leg voltages (U_{A12}) remains zero most of the time, and only less voltage spikes exist.

Moreover, the CPS effect of the CICPS is compared with different schemes, as shown in Fig. 14. For conventional Comm-CPS shown in Fig. 14(a), due to the inevitable communication delays (including transmission and signal processing delays), the CPS cannot be well achieved. The CPS error is about 0.1 (1e-5s/1e-4s), preventing complete CPS. In PLL-CPS, a fluctuating error in the carrier phase arises due to grid fluctuations and sampling errors. As shown in Fig. 14(b), the maximum CPS error can reach 0.05 (5e-6s/1e-4s). Therefore, PLL-CPS cannot achieve high-precision CPS. Moreover, the proposed CICPS is shown in Fig. 14(c), it can be seen that CICPS achieves near-complete synchronization. This effect is due to the carrier phase identification process, which can avoid the delay factors. Thus,

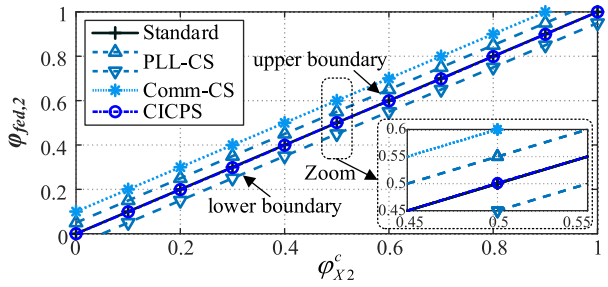

Fig. 15. CPS errors of different algorithms with varying initial phase differences φ^c_{X2}.

the proposed CICPS outperforms Comm-CPS and PLL-CPS in terms of accuracy, approaching the ideal state.

To evaluate the accuracy of the proposed CICPS in full working range, the CPS error is tested and statistics, as shown in Fig. 15. It can be seen that the CPS error of CICPS remains within 0.002, significantly smaller than the errors of Comm-CPS (0.1, 10e-6/1e-4) and PLL-CPS (-0.05 to 0.05, 5e-6s/1e-4s). Thus, the proposed CICPS have the best performance.

B Optimization Effect of CICPS on the Execution of Modulation Strategies for Distributed Inverter Systems

With CPS method, the carrier phase-sensitive PWM strategies can be implemented in the distributed system, such as ZCMV of two paralleled inverters. First, the ZCMV strategy is tested with the centralized control system, as shown in Fig. 16(a), the CMV can be effectively suppressed. For the conventional Comm-CPS and PLL-CPS schemes shown in Fig. 16(b) and (c), the effect of CMV suppression is significantly reduced with the execution of ZCMV strategy in distributed systems, which is owing to the obvious CPS error. For the proposed CICPS shown in Fig. 16(d), the CMV suppression is superior to that of the Comm-CPS and PLL-CPS algorithms and is closer to the effect achieved in a centralized system. This effect is owing to the higher CPS accuracy of CICPS method.

Moreover, the carrier phase shift PWM is also implemented to test the CPS effect. For two paralleled inverters with 180° phase shifting operation in centralized control manner, the odd switching harmonics can be eliminated in the ideal case. Thus, different CPS schemes are testes to make comparison, as shown in Fig. 17. It can be seen that with different CPS methods, the three-phase current can achieve a certain degree of optimization by effectively reducing the amplitude of odd switching harmonics. And the CICPS achieves the best current optimization with the lowest odd switching harmonics, which is owing to the accuracy CPS effect.

C Validation of CICPS in Distributed Multi-Inverter Systems

Finally, a distributed three-inverter system has been constructed for further validation with the proposed CICPS. Fig. 18 shows the gradual CPS process of INV2 and INV3. It can be seen that the carrier of INV2 is first adjusted to be synchronization with INV1 in Fig. 18(a). In this case, the INV1 and INV2 can

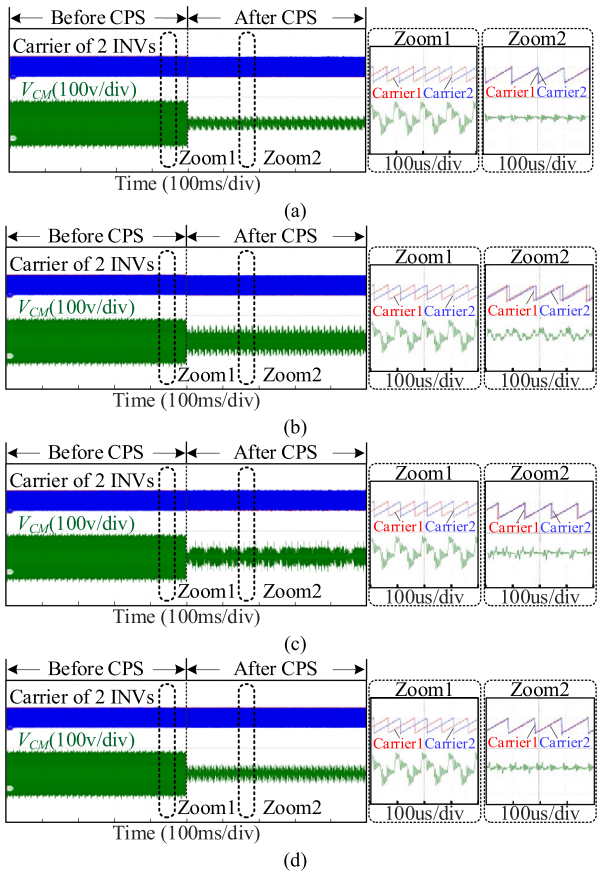

Fig. 16. Implementation of each synchronization algorithm in ZCMV modulation strategy: (a) in centralized system; (b) Comm-CPS; (c) PLL-CPS; (d) CICPS.

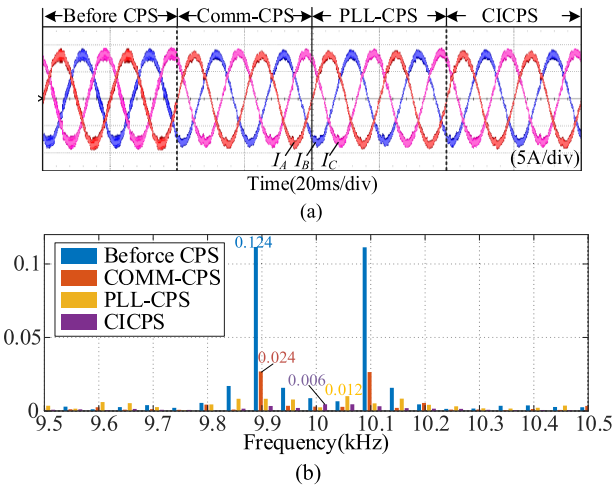

Fig. 17. Effectiveness of the 180° phase-shift algorithm in different CPS algorithms. (a) I_X of the system under different CPS algorithms. (b) Spectrum of I_X before CPS, after Comm-CPS, after PLL-CPS, after CICPS.

be regarded as an inverter, and INV3 can be CPS with the same adjusting process shown in Fig. 18(b). Thus, it is proved that CICPS can still achieve the expected CPS in a multi-inverter system.

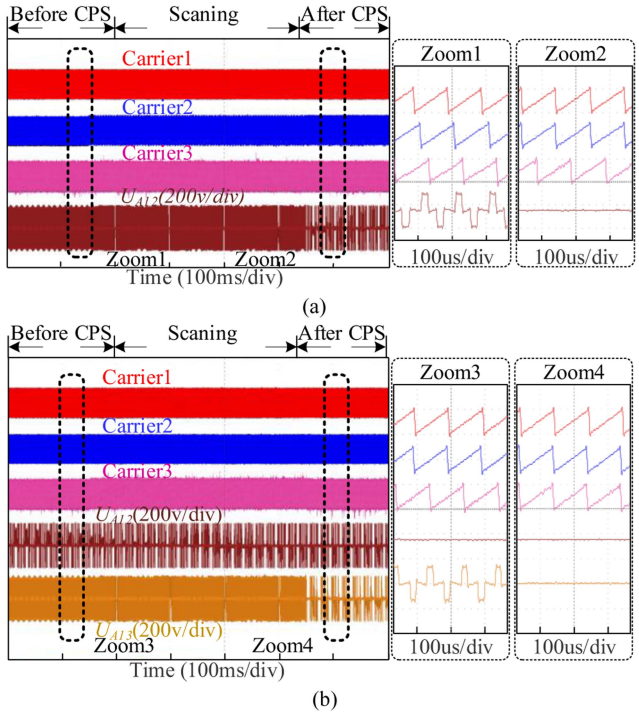

Fig. 18. Process diagram of CICPS in a distributed three-inverters system. (a) CICPS of INV2. (b) CICPS of INV3.

V. Conclusion

This article proposes a CICPS for distributed parallel inverter systems. In the proposed CICPS, the peak circulating current is used to identify the CPS point and adaptively adjust the carrier phase difference for multiple inverters. The proposed CICPS method achieves phase synchronization without the need for low-latency communication hardware. Moreover, based on the CPS function, flexible phase-shift PWM schemes with strict carrier phase requirements can be implemented to achieve multiple functions, including power quality optimization and common-mode voltage reduction. The simulation and experimental results show that the proposed CICPS achieves higher phase synchronization precision compared to conventional methods. Since CPS is crucial for the cost and performance of distributed paralleled inverter applications, the proposed CICPS is expected to be a promising CPS solution.

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