Analysis and Mitigation Methods of Gate Oscillation in Paralleled 10 kV SiC MOSFETs

Gao Liu, *Graduate Student Member, IEEE*, Zhixing Yan, *Graduate Student Member, IEEE*, Morten Rahr Nielsen, *Graduate Student Member, IEEE*, Thore Stig Aunsborg, Bjørn Rannestad, Hongbo Zhao, *Member, IEEE*, Michael Møller Bech, and Stig Munk-Nielsen, *Member, IEEE*

***Abstract*—Gate oscillations exist in paralleled SiC MOSFETs, which can cause false switching behavior and device damage. This article investigates gate oscillations in paralleled 10 kV SiC MOSFETs as it is currently one of the bottlenecks for paralleling. During the switching transient, the paralleled SiC MOSFETs operate in their saturation region, where a closed-loop feedback system is formed between the MOSFET transconductance and the parasitic distributions in the circuit. The instability of the closed-loop feedback system is key in describing the gate oscillation mechanism. Therefore, a small signal circuit model of two parallel 10 kV SiC MOSFETs is used to analyze this mechanism, which takes into account both the parasitic inductances and capacitances of the MOSFET, power module, and external connections to predict the impact of different parasitic parameters. From the circuit model, four methods are proposed to mitigate the gate oscillations. Finally, experiments are conducted in a double pulse test platform at 6 kV/20 A, showing a good prediction of the gate oscillations and significant damping by the proposed methods.**

***Index Terms*—10 kV SiC MOSFETs, double pulse testing, gate oscillation, medium voltage (MV), paralleling power module.**

I. Introduction

THE 10 kV silicon-carbide (SiC) MOSFETs have matured significantly in recent years due to technological advancements in the wide-band-gap (WBG) technology led by industry and academia [1], [2], [3]. A distinct advantage of the 10 kV SiC MOSFETs is their ability to enable simple two-level converter topology in medium voltage (MV) applications [4], which gains the benefits of less power loss [5] and lower system volume [6], [7]. To meet the demand of increasing the current/power rating of power converters, there exist three typical design options for paralleling on the converter level [8], power-module level [9], and chip level [10]. Paralleling on each of these hierarchical levels presents individual challenges and opportunities. Paralleling on the converter level introduces additional balance control among converters, while the chip level requires customized power module design and manufacturing processes [11]. Therefore, paralleling on the power-module level attracts significant attention from engineers due to simple implementation.

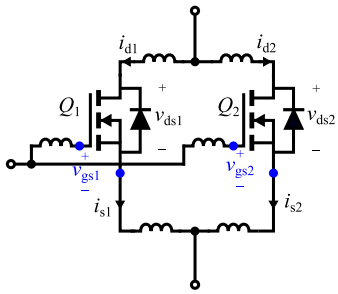

Fig. 1. Schematic of two MOSFETs connected in parallel.

A conceptual diagram of a parallel connection of two MOSFETs is depicted in Fig. 1, where the drain, gate, and source are connected, respectively. Parasitic inductances from the drain, source, and gate connections are unavoidable and intrinsic, but their values depend on the design. Switching oscillations can occur in both silicon (Si) and WBG devices. These oscillations fall into two main types. The first type results from a resonance between the circuit's parasitic inductance and the device's intrinsic capacitance [12], leading to voltage and current overshoots or undershoots [13], [14], namely *LC* oscillation [15]. The second type is caused by parasitic resonance, where a feedback loop forms between the device and the circuit's parasitic components, namely self-sustain oscillation [16]. Even more severely is the fact that MOSFETs are subject to immediate failure if the maximum gate oxide layer voltage capability is exceeded. Given the fact that there is only a small margin in terms of gate-source voltage between normal operating conditions and a fault scenario, the current study analyses voltage oscillations in the gate circuitry for the special case of parallel-connected SiC MOSFETs. Associated with the circuit elements described above, the fact that MOSFETs behave as linear amplifier when it is operating in the saturation region should be taken into account as well [17]. In particular, a feedback loop exists. The gate voltage affects the drain current which in turn couples back to the gate

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Gao Liu, Zhixing Yan, Morten Rahr Nielsen, Thore Stig Aunsborg, Hongbo Zhao, Michael Møller Bech, and Stig Munk-Nielsen are with the AAU Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: gaol@energy.aau.dk; zhya@energy.aau.dk; mrni@energy.aau.dk; tsu@energy.aau.dk; hzh@energy.aau.dk; mmb@energy.aau.dk; smn@energy.aau.dk).

Bjørn Rannestad is with the KK Wind Solutions, 7430 Ikast, Denmark (e-mail: bjran@kkwindsolutions.com).

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voltage depending on the parasitic parameters in the loop. In contrary to the *LC*-type oscillations, the self-sustain oscillation rooted in the nonzero gain due to SiC MOSFETs transconductance during the saturation region can grow rapidly without bounds if this feedback loop is unstable [18]. Clearly, this is highly undesirable, as reported in [19] and [20]. Therefore, it is essential to understand how the oscillation develops in parallel devices to mitigate these risks.

So far, several analytical models, which include the parasitic parameters of the circuit, have been proposed to investigate the oscillations in paralleling different power devices. A full model is built using Technology Computer Aided Design (TCAD) tools to analyze the oscillation phenomena in the s domain [21]. However, the computation load is heavy [22], which makes it difficult to investigate how the parameters correlate to the oscillation [23]. A full model of a multiport network is built for analysis of the forced oscillation in multichip IGBT power modules [24], which lacks the flexibility for investigating the impacts of parasitic parameters on the system stability. The gate oscillation among paralleled SiC MOSFETs contains two different modes, one being the common-mode (CM) gate oscillation, caused by the coupling between the gate signal and the drain signal, and the other type being the differential-mode (DM) gate oscillation [22], [25]. In addition, the DM gate oscillation is more pronounced compared with the CM gate oscillation [26]. The most severe oscillation is DM oscillation on the gate-source signal, of which the phase between two devices is 180° shifted [27]. This oscillation appears in gate-source, drain-source voltage and drain current. Its amplitude increases during the Miller plateau commuting between two paralleled SiC MOSFETs, results in extra voltage stress and overheating of the switching device [20]. Thus, it is essential to investigate and mitigate the DM gate oscillation in paralleled SiC MOSFETs.

A simplified model is proposed for the DM circuit assuming all dies placed closely on a direct bonded copper (DBC) in a power module can be simplified as a single switch with full parasitic inductance circuit model, which studies the low-voltage SiC MOSFETs [28]. In comparison to low-voltage applications, it has been reported that the parasitic capacitance, rather than parasitic inductance, is the primary cause due to capacitive current of $C\mathrm{d}v/\mathrm{d}t$ and extra switching loss of $\frac{1}{2}CV^2$ per switching cycle [29]. In addition, there are higher insulation requirements in MV applications with larger clearance and creepage distances [30]. Thus, the significance of parasitic parameters is different among MV and low-voltage power modules. Until now, the parasitic parameters on gate oscillation in MV power modules have not been fully explored in the existing literature.

To fill the research gap, the major contributions of the article are as follows.

1) Based on the small signal model derived from the half-circuit assumption, the parasitic capacitance is first considered, along with parasitic inductance in the paralleled 10 kV SiC MOSFETs.
2) The DM oscillations in paralleled 10 kV SiC MOSFETs are analyzed in depth for the first time with experimental verification provided.

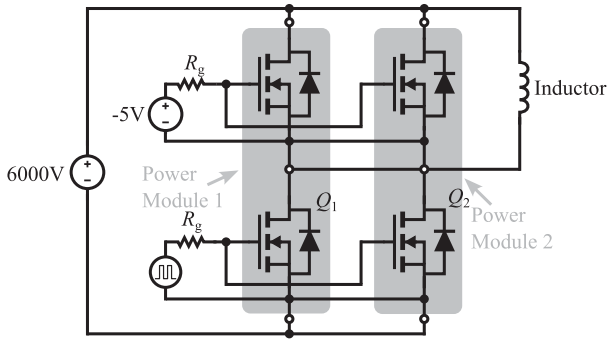


Fig. 2. Simplified schematic of low-side double pulse test for two parallel power modules.

3) Four methods are proposed to mitigate gate oscillations in paralleled 10 kV SiC MOSFETs. Additionally, the trade-offs among these mitigation methods are comprehensively analyzed and validated. Furthermore, the uniqueness of the proposed solutions for 10 kV SiC MOSFETs is highlighted.

The rest of this article is organized as follows. The problem formulation is presented in Section II. Section III presents a comprehensive overview of the parasitic elements in power modules, which is used to derive a simplified DM circuit and a small signal model. Section IV analyzes the influence of the parasitic elements in the circuit on the system stability. Therefore, different practical methods for mitigating the oscillation are proposed. In Section V, a double pulse test setup is built to test the MV power module based on 10 kV SiC MOSFETs and verify the theoretical analysis from Section III. Finally, Section VI concludes this article.

II. Problem Formulation

This article investigates gate oscillations in the paralleling of two single-chip power modules, which are populated with 300 mΩ 10 kV SiC MOSFET dies without antiparallel junction barrier Schottky diodes [31]. Hence, to investigate the gate oscillation mechanism and showcase the theoretical analysis in practice, the DPT is conducted according to the simplified schematic in Fig. 2. The implementation is different from paralleling modules using individual gate drivers [32] as the gate-source connections of the low-side and high-side switches are directly connected, such that only a single gate driver is required to drive both 10 kV SiC MOSFETs.

The turn-ON switching waveforms during a low-side DPT are shown in Fig. 3. The presence of gate oscillations during the Miller plateau is apparent. The amplitude of the gate oscillation is increasing. The oscillation also exists in drain-source voltage and is increasing in sync with the gate oscillation. This indicates that the oscillation is amplified in the Miller plateau, where SiC MOSFETs function as an amplifier. After the Miller plateau, the gate oscillations disappear as the 10 kV SiC MOSFETs do not operate in their saturation region.

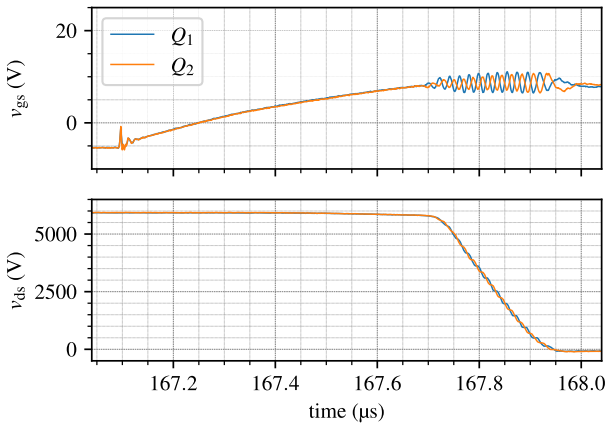


Fig. 3. Experimental waveforms of oscillations during a turn-ON switching event at 6000 V DC-link voltage and 20 A load current (detailed description will be conducted in Section V).

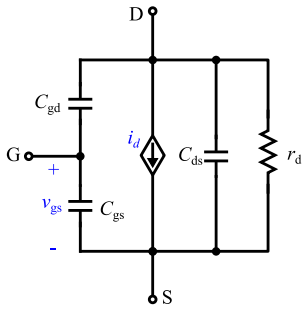


Fig. 4. Small signal model of MOSFET [17].

During the saturation region, the small signal model of the MOSFET is shown in Fig. 4. The intrinsic parameters of the MOSFET are the gate-source capacitance $C_{\rm gs}$, gate-drain capacitance $C_{\rm gd}$, and drain-source capacitance $C_{\rm ds}$. In addition, the output resistor $r_{\rm d}$ is included. The drain current $i_{\rm d}$ is a gate-source voltage $v_{\rm gs}$ controlled current source following:

$$i_{\rm d} = g_{\rm m} v_{\rm gs} \tag{1}$$

where $g_{\rm m}$ is the MOSFET small-signal transconductance. The gate oscillation is caused by the MOSFET intrinsic parameters in combination with the parasitic parameters of the circuit [28]. To reveal the gate oscillation mechanism, an analytical model of the gate oscillation will be conducted in the subsequent section.

III. Circuit Model of Paralleled Medium Voltage Power Modules

According to Fig. 2, two single-chip power modules based on 10 kV SiC MOSFETs are paralleled in practice.

A. Circuit Modeling of Parasitic Parameters

Different from the capacitance modeling for power modules in [33], the parasitic inductance needs to be included in the analytical model for the paralleled two low-side SiC MOSFETs. Fig. 5(a) illustrates the parasitic inductance and capacitance in a physical power module layout. The terminal "DC+", "OUT," and "DC-", the connection trace, and bonding wires belong to the power loop. The gate loop is formed by the "Gate" and "Source" terminals and the connection trace to the MOSFET. Parasitic inductance on the drain inside the power module is considered from the bottom plane of the 10 kV SiC MOSFET along with the trace on DBC to the "OUT" terminal. The power loop source inductance is regarded from the bonding wire, trace on DBC, and "DC-" terminal. Similarly, in the gate loop, as the Kelvin-source connection is utilized, the parasitic inductance on the gate and source in the power module both consist of the bonding wire, trace on DBC, and terminal. The parasitic capacitance is introduced by the layout plane and the base plate. Therefore, the physical power module in Fig. 5(a) can be modeled into Fig. 5(b).

The parasitic capacitance $C_{\sigma \rm d}$ in Fig. 5(b) is the lumped parasitic capacitance between the DBC copper layout connected with the low-side MOSFET drain and the baseplate as Fig. 5(a) depicts. Similarly, $C_{\sigma \rm dHS}$ exists between the DBC copper layout connected with the high-side MOSFET drain and the baseplate. $C_{\sigma \rm s}$ is the lumped parasitic capacitance between the DBC copper layout connected with the low-side source and the baseplate. $C_{\sigma \rm g}$ is the coupling between the low-side MOSFET gate DBC trace and baseplate. The parasitic parameters can be obtained from ANSYS Q3D [34]. Then, the circuit of low-side SiC MOSFET of the paralleled power modules with parasitic capacitance and inductance is derived in Fig. 5(c). The inductance of the "OUT cable," "dc- connection," and "gate-source connection" between two power modules are modeled. To simplify the analysis of the circuit and reduce the mathematical calculation of the circuit model in the following section, the high-side MOSFET and parasitic parameter can be simplified into the output capacitance of the 10 kV SiC MOSFET $C_{\sigma \rm ossi}$ series connected with parasitic capacitance on drain $C_{\sigma \rm dHSi}$ (i=1, 2).

B. Half-Circuit Assumption

To clarify how the gate oscillation occurs in Fig. 5(c), it is necessary to figure out the circuit basics first. As depicted in Fig. 6, the parasitic inductances in Fig. 5(c) are summed into one variable in each branch as expressed

$$\begin{cases} L_{\sigma \rm dx} = L_{\sigma \rm dpx} + L_{\sigma \rm outpx}, ({\rm x} = 1, 2) \\ L_{\sigma \rm gx} = L_{\sigma \rm gpx} + L_{\sigma \rm gcx} \\ L_{\sigma \rm ksx} = L_{\sigma \rm kspx} + L_{\sigma \rm scx} \\ L_{\sigma \rm sx} = L_{\sigma \rm spx} + L_{\sigma \rm DC-x}. \end{cases} \tag{2}$$

$R_{\rm g1}$ and $R_{\rm g2}$ are the kelvin gate resistors in the gate loop, and $R_{\rm g1}$=$R_{\rm g2}$. As the circuit is symmetrical about the center-line with the gate driving circuit, the circuit model for one MOSFET in the switch in Fig. 6 can be further simplified into a half circuit in Fig. 7(a) with the assumption:

1. The structure of the circuit is symmetrical.
2. The 10 kV SiC MOSFETs are identical in terms of intrinsic capacitance $C_{\rm ds}$, $C_{\rm gd}$, $C_{\rm gs}$, and transconductance $g_{\rm m}$.

Based on the assumption, the relation of parasitic inductance and capacitance in Fig. 6 are equal from the left half plane to the right half plane: $L_{\sigma \rm d1} = L_{\sigma \rm d2}$, $C_{\rm oss1} = C_{\rm oss2}$, $R_{\rm g1}$=$R_{\rm g2}$ $C_{\sigma \rm dHS1} = C_{\sigma \rm dHS2}$, $C_{\sigma \rm d1} = C_{\sigma \rm d2}$, $C_{\sigma \rm g1} =$

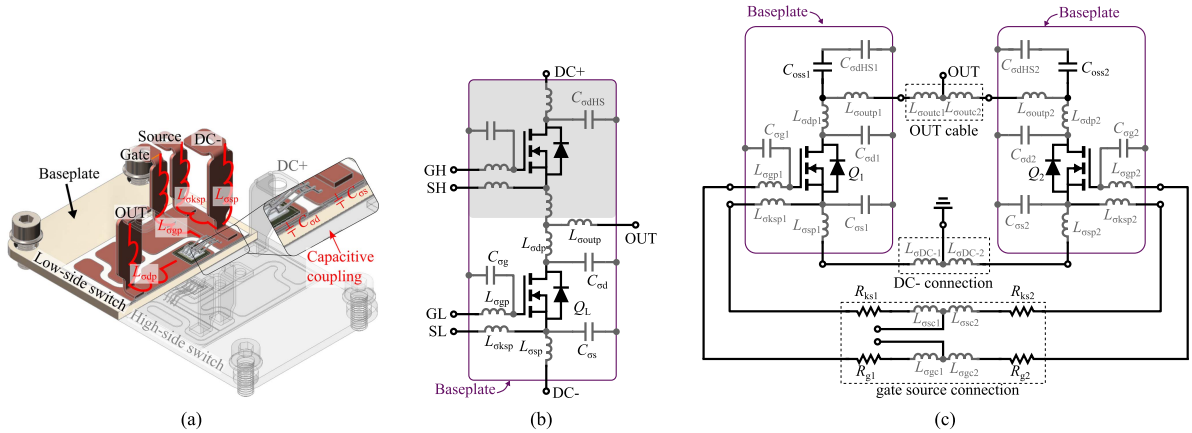


Fig. 5. (a) Half-bridge power module layout with sketches of the parasitic inductance and capacitance. (b) Equivalent circuit of parasitic inductance and capacitance. (c) Paralleled two low-side switch of the power module.

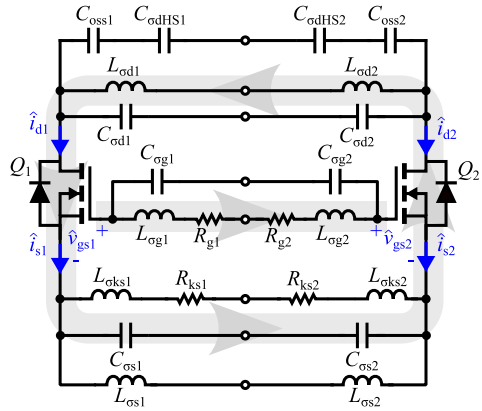


Fig. 6. Simplified circuit of two SiC MOSFETs paralleled in Fig. 5(c).

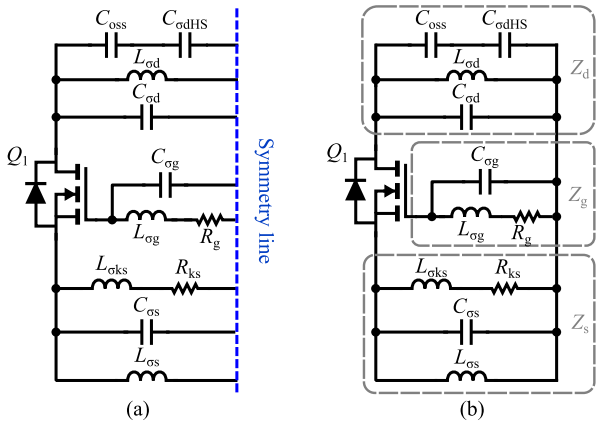


Fig. 7. Simplified active switch with (a) one side of the circuit in Fig. 6 and (b) after half-circuit assumption.

$C_{\sigma g2}$, $L_{\sigma g1} = L_{\sigma g2}$, $L_{\sigma ks1} = L_{\sigma ks2}$, $C_{\sigma s1} = C_{\sigma s2}$, and $L_{\sigma s1} = L_{\sigma s2}$.

During turn-ON transient in practical, when the gate driver steps from -5 to 20 V, the gate-source voltage starts to ramp up correspondingly from -5 to 20 V in 10 kV SiC MOSFETs. Since it excites the resonance between the parasitic inductance and capacitance in the circuit along with the MOSFET intrinsic capacitances, the gate-source voltage oscillation occurs. As Fig. 3 shows in Section II, the phase shift of the ac signal part in two MOSFETs is about 180°. It indicates that the ac signal circulates in the circuit between two MOSFETs, as depicted by the gray arrows in Fig. 6, with most of the circulating signal being DM. To analyze the DM oscillation mechanism, the transfer function of the small signal model of the circuit in Fig. 6 needs to be figured out based on the ac small signal [16].

The variables $\hat{v}_{\rm gs1}$, $\hat{v}_{\rm gs2}$, $\hat{i}_{\rm d1}$, $\hat{i}_{\rm d2}$, $\hat{i}_{\rm s1}$, and $\hat{i}_{\rm s2}$ are the ac small signals in the circuit. Since Q_1 and Q_2 have identical characterization, the relation among the ac small signal voltage and current can be obtained as

$$\begin{cases} \hat{v}_{\rm gs1} = -\hat{v}_{\rm gs2} \\ \hat{i}_{\rm d1} = -\hat{i}_{\rm d2} \\ \hat{i}_{\rm s1} = -\hat{i}_{\rm s2}. \end{cases} \tag{3}$$

According to Kirchhoff's Current Law, the symmetry line can be regarded as one circuit node. Besides that, the relation among $\hat{v}_{\rm gs1}$, $\hat{i}_{\rm d1}$, and $\hat{i}_{\rm s1}$ on one side of the switch in Fig. 7(a) satisfies (3) as well. Therefore, the half circuit in Fig. 7(a) can be derived by shorting the neutral point on the symmetry line in Fig. 7(b). The instability of one SiC MOSFET reflects the DM oscillation, where the parasitic parameters are half the total value of each parameter between two paralleled SiC MOSFETs.

Thus, the circuit in Fig. 7(b) can be transformed into the circuit in Fig. 8 including the MOSFET small signal model. The variables $Z_{\rm s}$, $Z_{\rm g}$, and $Z_{\rm d}$ are the impedance on the source, gate, and drain side, respectively, which can be obtained as follows:

$$Z_{\rm d} = \frac{1}{sC_{\sigma \rm d} + s\dfrac{C_{\rm oss}C_{\sigma \rm dHS}}{C_{\rm oss} + C_{\sigma \rm dHS}} + \dfrac{1}{sL_{\sigma \rm d}}} \tag{4}$$

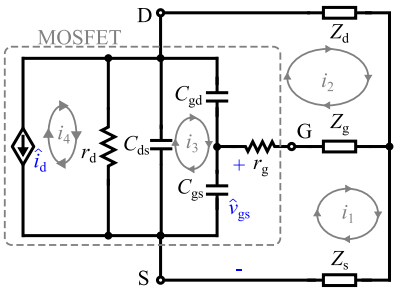


Fig. 8. Small signal model of the circuit in Fig. 7(b).

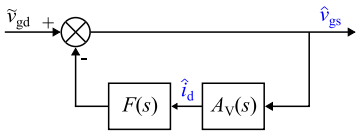


Fig. 9. Closed-loop block diagram derived from circuit in Fig. 8.

The relation between $\hat{i}_d$ and $\hat{v}_{gs}$ outside the MOSFET circuit can be obtained using the mesh current method in the following:

$$\begin{cases} i_1 Z_s + \frac{(i_1-i_3)}{sC_{gs}} + (i_1-i_2)(Z_g+r_g) = 0 \\ (i_2-i_1)(Z_g+r_g) + \frac{(i_2-i_3)}{sC_{gd}} + i_2 Z_d = 0 \\ (i_3-i_4)\frac{r_d}{1+sC_{ds}r_d} + \frac{(i_3-i_2)}{sC_{gd}} + \frac{(i_3-i_1)}{sC_{gs}} = 0 \\ i_4 = -\hat{i}_d. \end{cases} \tag{5}$$

By solving (5), a virtual impedance $Z(s)$ from i_d to v_{gs} can be established as

$$\hat{v}_{gs} = (i_3 - i_1)\frac{1}{sC_{gs}} = \hat{i}_d Z(s). \tag{6}$$

Inside the MOSFET, the small signal relation between v_{gs} and i_d follows (1). The relationship among the perturbation signal $\tilde{v}_{gd}$ injected in the system, v_{gs} and i_d can be expressed as shown in (7). Here, $\tilde{v}_{gd}$ represents the perturbation generated by the gate driver with asymmetrical input nodes connected to the gate-source terminals of the parallel power modules. This article focuses on methods to stabilize the system, while the elimination of the perturbation signal from the system could be a direction for future research. The MOSFET circuit can be transformed into the closed-loop feedback system in Fig. 9.

$$\hat{v}_{gs} = \tilde{v}_{gd} + \hat{i}_d Z(s) = \tilde{v}_{gd} - \hat{i}_d F(s). \tag{7}$$

$A_v(s)$ and $F(s)$ can be obtained

$$\begin{cases} A_v(s) = g_m \\ F(s) = -Z(s). \end{cases} \tag{8}$$

Therefore, by solving (5), (6), and (8), the closed-loop transfer function $T(s)$ is expressed as (details in Appendix)

$$T(s) = \frac{1}{1 + A_v(s)F(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{9}$$

where $T(s)$ is a high-order system when they are complex impedances. In the frequency domain, complex poles determine a modulated oscillation, with the decaying or growing rate depending on whether the real part of the pole is negative or positive. In a stable system, the dominant pole p_d is positioned the closest to the imaginary axis. In an unstable system, p_d corresponds to the highest exponentially increasing rate of the oscillation, which is the furthest pole from the imaginary axis on the right half plane. It can be expressed as

$$p_d = \sigma \pm j\omega_d. \tag{10}$$

To illustrate how oscillations occur, the damping ratio ζ_d is adopted according to (11). When $\zeta_d > 0$, the system is stable and the oscillation will decay. Otherwise, the oscillation will grow when $\zeta_d < 0$ as the system becomes unstable

$$\zeta_d = -\frac{\sigma}{\sqrt{\sigma^2 + \omega_d^2}}. \tag{11}$$

IV. Stability Analysis of 10 kV Power Module

To analyze and mitigate the gate oscillation issue in a parallel connection of two 10 kV SiC MOSFET power modules, the stability criteria of $T(s)$ is evaluated using the mathematical tools Maple and Python. First, put (5) into Maple and solve the intermediate variables i_1 and i_3 in Fig. 8. Then, $Z(s)$ can be obtained according to (6). Hence, extract the denominator and numerator from (9) in Maple and input to Python. Finally, the stability criteria such as poles and damping ratio can be calculated with the functions in Python.

A. Impacts of Circuit Parameters on Stability

According to Fig. 7(b), with the parasitics inside the module described in [34], the circuit parameter obtained from ANSYS Q3D and device parameters are listed in Table I.

To assess the stability of the system, the closed-loop transfer function *T*(s) can be solved using the extracted parasitic parameters. One pair of complex poles is located in the right half plane of the zero-pole map, with $\zeta_d = -0.005$. This indicates that the system is unstable and gate oscillations will occur.

The stability is related to the working condition. As the transconductance changes with the current i_d, the system stability can be influenced by the current. In Fig. 10(a), the system will go into an unstable region when the transconductance increases.

Besides that, the parasitic inductance and the gate resistance impact on the system stability. By sweeping the parasitic parameter $L_{\sigma d}$, $L_{\sigma g}$, R_g, $L_{\sigma ks}$, and $L_{\sigma s}$, the damping ratio ζ_d behaves differently. As shown in Fig. 10(b), (c), and (d), $L_{\sigma d}$, $L_{\sigma g}$, and R_g are positively related to the damping ratio, they can significantly stabilize the system. In Fig. 10(e) and (f), the larger $L_{\sigma ks}$ and $L_{\sigma s}$ are, the smaller ζ_d is. $L_{\sigma ks}$, $L_{\sigma s}$ have similar quantitative effect on ζ_d.

B. Oscillation Mitigation Guideline

By sweeping $L_{\sigma s}$ with another parameters the damping ratio distribution map can be obtained as in Fig. 11(a)–(d). In practice, the inductance $L_{\sigma d}$, $L_{\sigma g}$, $L_{\sigma ks}$, and $L_{\sigma s}$ is highly dependent on how the paralleled power modules are implemented. It illustrates that when $L_{\sigma s}$ is small, the larger $L_{\sigma d}$ is, the more stable

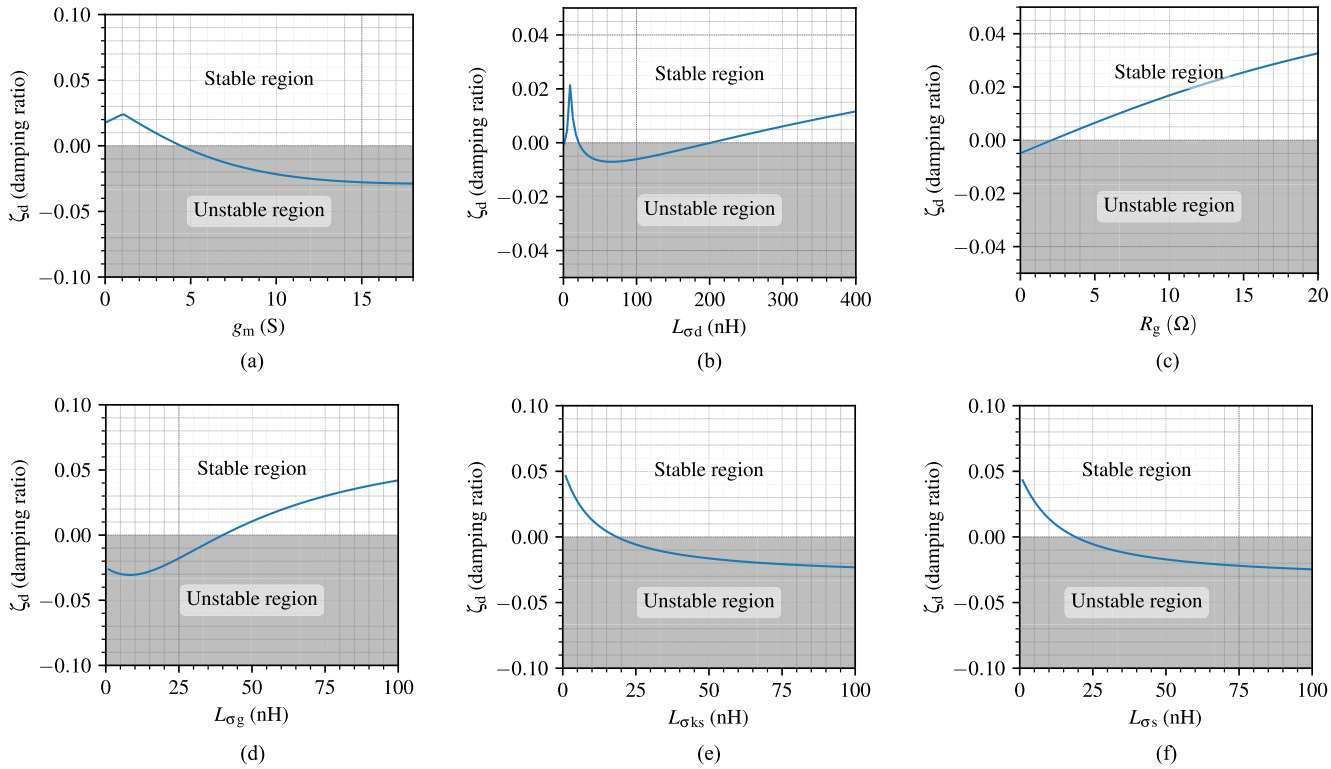


Fig. 10. Damping ratio ζ_d changes with the change of (a) transconductance g_m, (b) parasitic inductance $L_{\sigma d}$, (c) R_g on each gate, (d) parasitic inductance $L_{\sigma g}$, (e) parasitic inductance $L_{\sigma ks}$, and (f) parasitic inductance $L_{\sigma s}$.

it will be. Both $L_{\sigma d}$ and $L_{\sigma g}$ can mitigate the oscillation no matter how much $L_{\sigma s}$ is within the sweeping range. Adding extra resistance R_g on each MOSFET gate in parallel can help to stabilize the system as depicted in Fig. 11(c). Beside that, the small inductance in gate loop $L_{\sigma ks}$ can stabilize the system, ignoring how large $L_{\sigma s}$ is according to Fig. 11(d).

Based on the relation between the damping ratio and the parasitic parameters, the methods for mitigating the gate oscillation can be summarized for paralleled MV power modules.

1) Reduce the following parasitic inductances: $L_{\sigma s}$ or $L_{\sigma ks}$. In practice, the connection between two power modules needs to be as short as possible to reduce the parasitic inductance on the source side.

2) Increase the inductance or resistance on each gate of the paralleled MOSFETs. The larger the parasitic inductance and resistance on the gate side, the more stable the switching operation during the Miller plateau will be.

3) Increase the parasitic inductance on the drain side, $L_{\sigma d}$, to obtain stable switching operation during the Miller plateau.

V. Experimental Verification

To verify the theoretical analysis above, a prototype with paralleling of two power modules is built as shown in Fig. 12. The half-bridge power module is built with a single 10 kV SiC MOSFET per switch. The 10 kV SiC MOSFETs die is the third-generation die from Wolfspeed. Two power modules are connected using the copper bar and PCB. The parasitic parameter in the circuit has been given in Table I.

A. Differential-Mode Oscillation in Paralleled 10 kV SiC MOSFETs

To have access to the source current of Q_1 and Q_2 with the LeCroy CP030 current probe, a cable is used to connect the paralleled power modules. The gate-source voltages and source currents in the circuit—denoted as v_{gs1}, v_{gs2}, i_{s1}, i_{s2}, i_s are marked in Fig. 13(a). The DM current in the circuit can be obtained as

$$i_{dm} = \frac{i_{s1} - i_{s2}}{2}. \tag{12}$$

In Fig. 13(b), it is evident that the frequency of the DM source current aligns with the gate-source voltage. The total source current i_s is equal to the sum of i_{s1} and i_{s2}, and it does not contain a component with the same frequency as the DM source current. This confirms that DM oscillation is more pronounced in parallel 10 kV SiC MOSFETs.

B. Experimental Results on Instability

In the following experiment, the turn-ON dv/dt speed in the following experiment is around 28.8 V/ns.

1) Benchmark: Influence of drain-source voltage v_{ds} on the stability. As Fig. 14(a), the oscillation happens during the Miller plateau. The frequency is around 55 MHz. With the voltage

TABLE I
VALUES OF 10 KV SICMOSFET AND PARASITIC PARAMETERS

Symbol	Description	Value
g_{m}	MOSFET transconductance	5.3 S
r_{g}	MOSFET internal gate resistor	2.8 Ω
r_{d}	MOSFET output resistance	256 Ω
C_{gd} C_{ds} C_{gs}	MOSFET intrinsic gate-drain, drain-source, and gate-source parasitic capacitances at v_{ds}= 5000 V	3.4 pF 40 pF 6.545 nF
C_{oss}	High-side MOSFET output capacitance at v_{ds}= 1000 V	91.6 pF
$C_{\sigma\mathrm{dHS}}$	Parasitic capacitance between high-side drain and baseplate	68.3 pF
$C_{\sigma\mathrm{d}}$	Parasitic capacitance between low-side drain and baseplate	83.1 pF
$C_{\sigma\mathrm{g}}$	Parasitic capacitance between low-side gate and baseplate	35.6 pF
$C_{\sigma\mathrm{s}}$	Parasitic capacitance between low-side source and baseplate	33.9 pF
$L_{\sigma\mathrm{d}}$	Parasitic low-side drain inductance $L_{\sigma\mathrm{d}}$ = $L_{\sigma\mathrm{dpi}}$ + $L_{\sigma\mathrm{outpi}}$ + $L_{\sigma\mathrm{outci}}$ (i=1, 2) as shown in Fig. 5(c)	34.3 nH
$L_{\sigma\mathrm{g}}$	Parasitic low-side gate inductance $L_{\sigma\mathrm{g}}$ = $L_{\sigma\mathrm{gpi}}$ + $L_{\sigma\mathrm{gci}}$ (i=1, 2) as shown in Fig. 5(c)	35.8 nH
$L_{\sigma\mathrm{ks}}$	Parasitic low-side Kelvin inductance $L_{\sigma\mathrm{ks}}$ = $L_{\sigma\mathrm{ksi}}$ + $L_{\sigma\mathrm{sci}}$ (i=1, 2) as shown in Fig. 5(c)	23.8 nH
$L_{\sigma\mathrm{s}}$	Parasitic low-side source inductance $L_{\sigma\mathrm{s}}$ = $L_{\sigma\mathrm{spi}}$ + $L_{\sigma\mathrm{DC-i}}$ (i=1, 2) as shown in Fig. 5(c)	24.2 nH
R_{ks}	Kelvin connection resistor on source in gate loop	1 Ω
R_{g}	Kelvin connection resistor on gate in gate loop	0 Ω

dropping down to 0 V, the system is unstable according to the theoretical analysis. Therefore, the oscillation increases until the end of the Miller plateau.

2) Benchmark: the influence of load current. From Fig. 15, the oscillation amplitude increases with the i_{s} becoming larger. As the transconductance g_{m} increases with the current and the damping ratio is smaller when g_{m} is larger, the result in Fig. 15 matches with the analysis in Fig. 10(b).

C. Impacts of Parasitic Parameters on Paralleling 10 kV SiC MOSFETs

To verify the impacts of $L_{\sigma\mathrm{s}}$, $L_{\sigma\mathrm{ks}}$, $L_{\sigma\mathrm{g}}$, and $L_{\sigma\mathrm{d}}$ on gate-source oscillation in Section IV (B), four groups of case studies are conducted.

1) Increase the length and narrow the width of the copper trace between the two "DC-" terminals. Thus, the parasitic inductance $L_{\sigma\mathrm{s}}$ is increased by 9.1 nH. The amplitude of gate oscillation is increased in Fig. 16, which meets the damping ratio becomes smaller as the $L_{\sigma\mathrm{s}}$ is larger in Fig. 10(f).

2) Add a ferrite bead with 12 nH on $L_{\sigma\mathrm{ks}}$ on the source trace in the gate loop. The tested waveform in Fig. 17 shows that the oscillation is enlarged and meets the analysis in Fig. 10(e).

3) Insert a ferrite bead that has 21 nH on the "Gate" terminal of each power module to increase the $L_{\sigma\mathrm{g}}$. The experimental result in Fig. 18 shows that the oscillation is decaying even though the oscillation starts with a little high amplitude. It indicates that the system is a stable system with a positive damping ratio, which meets the theoretical analysis in Figs. 10(d) and 11(b).

4) The oscillation is mitigated via adding a 5.1 Ω resistor on each gate of the MOSFET in parallel as shown in Fig. 19. Compared with the benchmark, the increased resistance on the gate side can mitigate the oscillation in accordance with the theoretical plotting in Figs. 10(c) and 11(c).

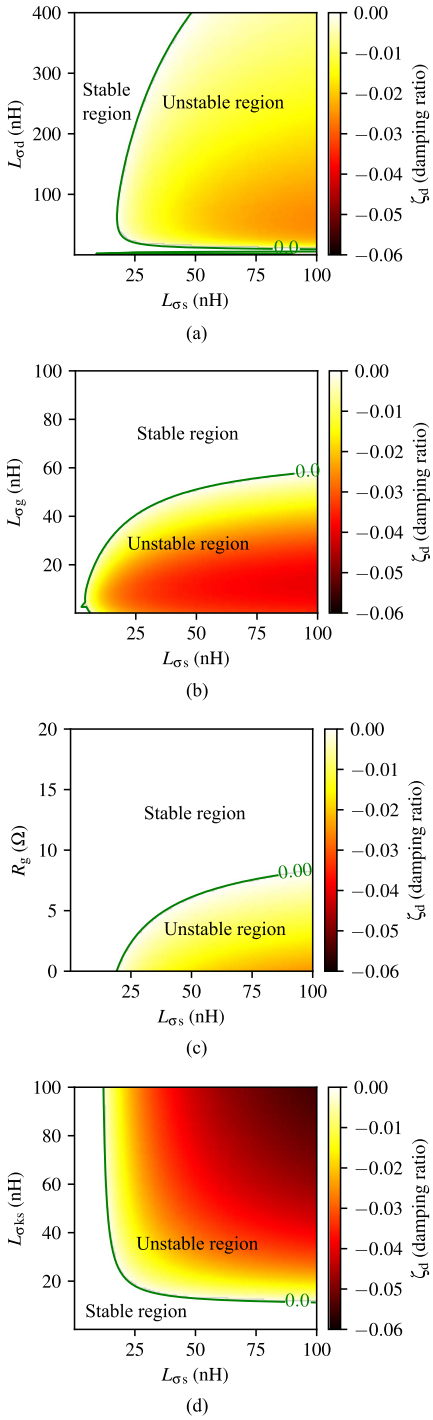


Fig. 11. Damping ratio ζ_{d} while sweeping (a) $L_{\sigma\mathrm{d}}$ and $L_{\sigma\mathrm{s}}$, (b) $L_{\sigma\mathrm{g}}$ versus $L_{\sigma\mathrm{s}}$, (c) R_{g} versus $L_{\sigma\mathrm{s}}$, and (d) $L_{\sigma\mathrm{ks}}$ versus $L_{\sigma\mathrm{s}}$.

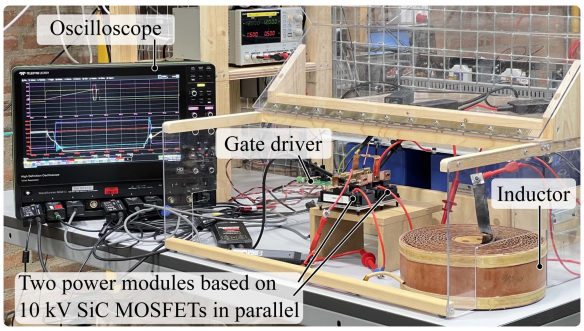


Fig. 12. Paralleled two power module double pulse platform (schematic in Fig. 2).

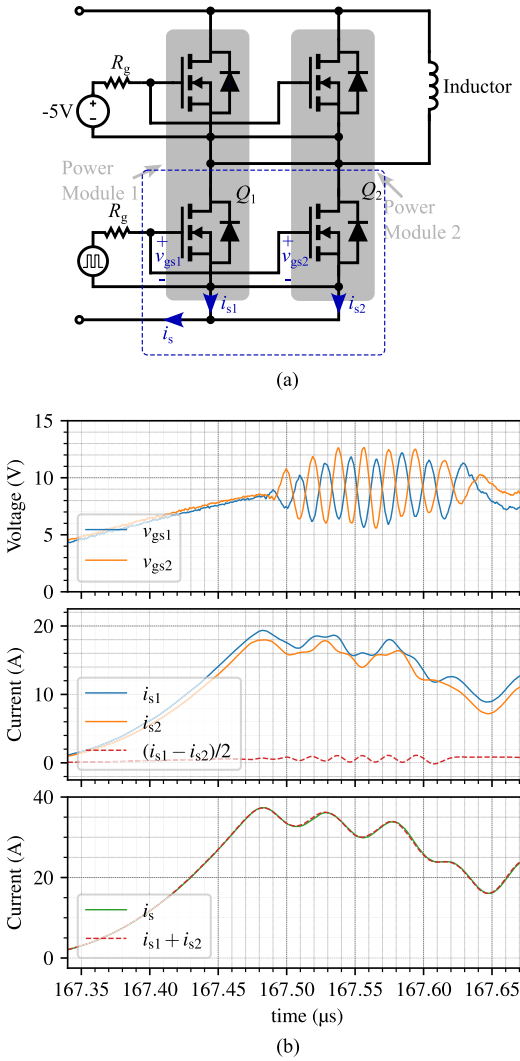


Fig. 13. (a) Simplified schematic of test platform for source current and (b) experimental waveform of turn-ON waveform at 6000 V DC-link voltage and 20 A load current.

5) By adding a 240 nH inductor on $L_{\sigma d}$ in each "OUT" terminal of the power module, the oscillation is completely suppressed. Compared with the benchmark, the increased $L_{\sigma d}$ has the capability to mitigate the oscillation in Fig. 20 as depicted in Figs. 10(c) and 11(a).

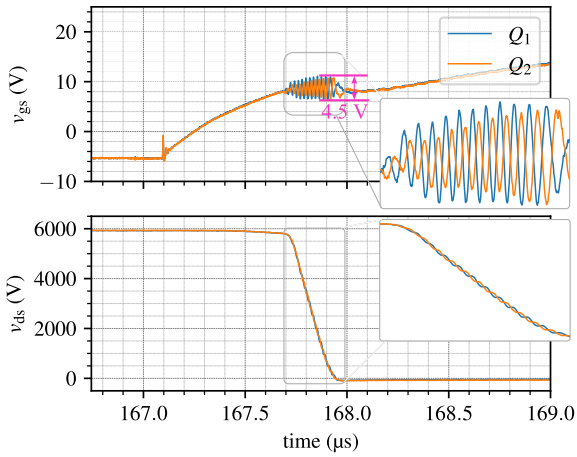


Fig. 14. Experimental benchmark turn-ON waveform at 6000 V DC-link voltage and 20 A load current.

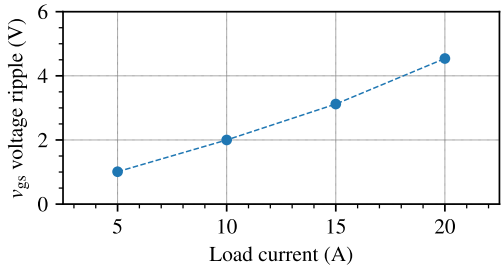


Fig. 15. Measured v_{gs} oscillation voltage amplitude during the Miller plateau under different load current and 6000 V DC-link voltage from experimental double pulse tests.

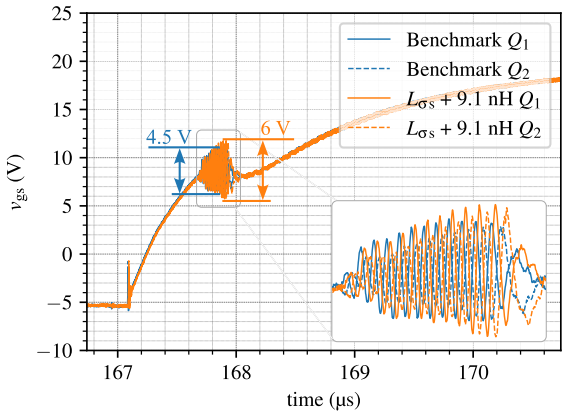


Fig. 16. Experimental turn-ON waveform with increased $L_{\sigma s}$ at 6000 V DC-link voltage and 20 A load current.

D. Discussion of the Methods

With these experimental results, the design guidelines presented in Section IV-B are verified. These solutions have their pros and cons in practical applications. A comparison of the different oscillation mitigation methods is illustrated in Table II.

1) Reducing the $L_{\sigma s}$ and $L_{\sigma ks}$ helps to mitigate the gate oscillation amplitude, as indicated by the theoretical analysis in

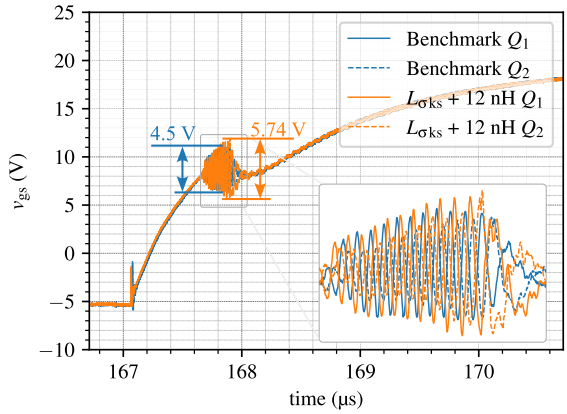


Fig. 17. Experimental turn-ON waveform with increasing $L_{\sigma ks}$ at 6000 V DC-link voltage and 20 A load current.

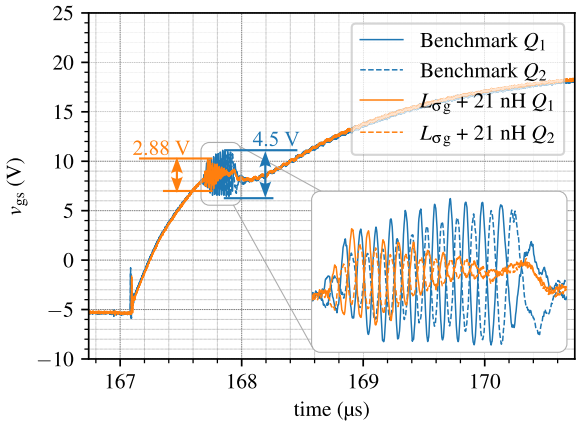


Fig. 18. Experimental turn-ON waveform after inserting a ferrite bead to increase $L_{\sigma g}$ at 6000 V DC-link voltage and 20 A load current.

TABLE II
COMPARISON OF DIFFERENT MITIGATION METHOD FOR PARALLELING 10 KV SIC MOSFETS

Method	Negative impact	Implementation
Reduce $L_{\sigma s}$ or $L_{\sigma ks}$	Constrained by the system structure	Difficult
Increase $L_{\sigma g}$	Enlarged crosstalk issue on the inactive switch	Easy
Increase resistor R_g on each gate	Enlarged crosstalk issue on the inactive switch	Easy
Increase $L_{\sigma d}$	Increased overshoot drain-source voltage during turn-OFF	Easy

Fig. 11(c) indicates. However, the parasitic inductance cannot be designed sufficiently small in MV applications. In practice, it is essential to maintain adequate clearance and creepage between parallel MV power modules based on 10 kV SiC MOSFETs, which limits the minimum values for parasitic inductance $L_{\sigma s}$ and $L_{\sigma ks}$.

2) Putting a ferrite bead on each gate terminal to increase $L_{\sigma g}$ can dampen the oscillation, whereas the ferrite bead should be within a limited value considering the crosstalk issue. As analyzed in [35], crosstalk occurs in the inactive switch of the half-bridge circuit. When the active switch turns ON or OFF, the dv/dt of the drain-source voltage on the inactive switch generates additional current flow from gate to drain, resulting in dips or bumps in the gate-source voltage. This crosstalk can lead to false turn-ON/OFF events or even damage to the gate and source of the inactive switch. As shown in Figs. 21 and 22, the voltage spike of the crosstalk issue worsens with an increase of 21 nH on $L_{\sigma g}$

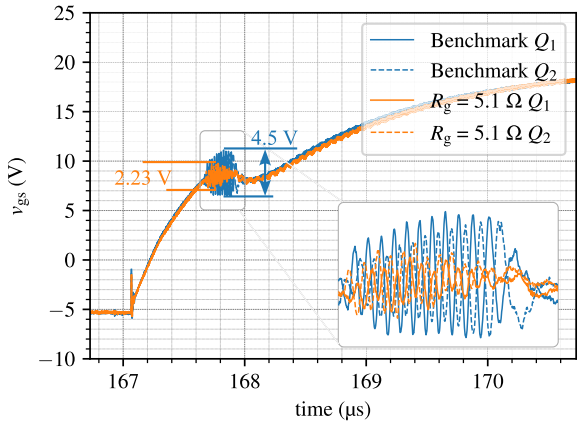


Fig. 19. Experimental turn-ON waveform with $R_g = 5.1\,\Omega$ on each gate under 6000 V DC-link voltage and 20 A load current.

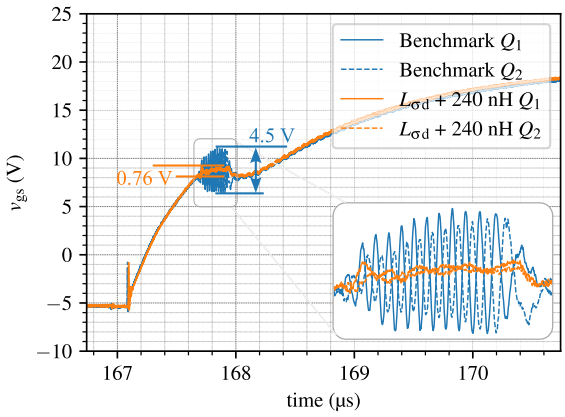


Fig. 20. Experimental turn-ON waveform with increased $L_{\sigma d}$ at 6000 V DC-link voltage and 20 A load current.

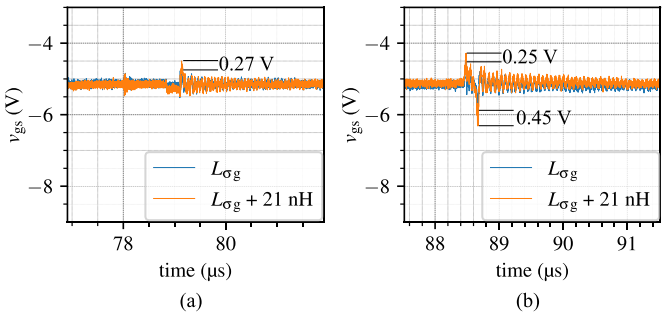


Fig. 21. Experimental waveform of crosstalk on the inactive switch when the active switch is turning ON with dv/dt (a) 27 V/ns at turning OFF and (b) 44 V/ns at turning ON.

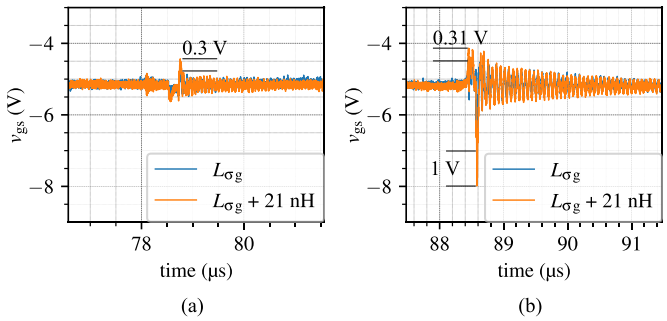


Fig. 22. Experimental waveform of crosstalk on the inactive switch when the active switch is turning ON with dv/dt (a) 35 V/ns at turning OFF and (b) 61 V/ns at turning ON.

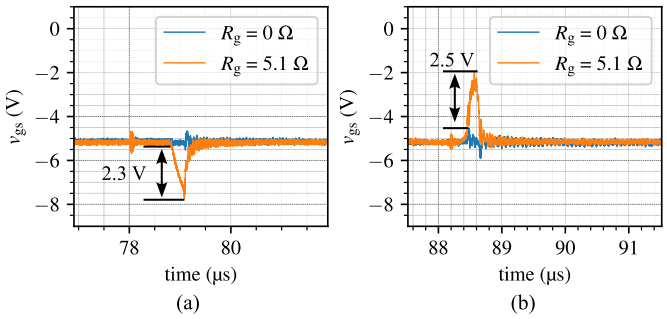


Fig. 23. Experimental waveform of crosstalk on the inactive switch when the active switch is turning ON with dv/dt (a) 27 V/ns at turning OFF and (b) 44 V/ns at turning ON.

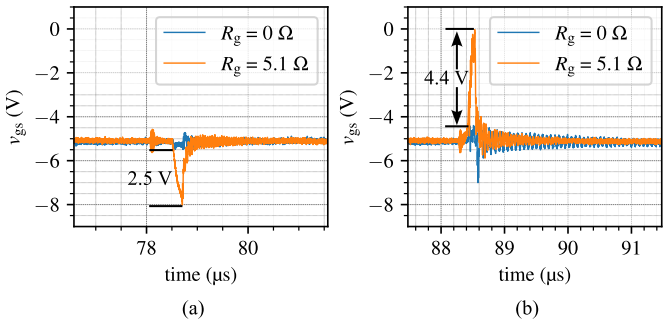


Fig. 24. Experimental waveform of crosstalk on the inactive switch when the active switch is turning ON with dv/dt (a) 35 V/ns at turning OFF and (b) 61 V/ns at turning ON.

during turn-ON and turn-OFF switching transient. In addition, the crosstalk will become worse with the increased dv/dt speed.

3) Similar to the solution with putting the ferrite bead on each gate, the increased gate resistors will cause a crosstalk issue as shown in Figs. 23 and 24. Besides that, it will slow down the di/dt and dv/dt during the switching transient since extra gate resistor on each gate are added [36].

4) By increasing $L_{\sigma d}$, the oscillation is completely suppressed. The increased $L_{\sigma d}$ causes a higher overshoot voltage due to $L_{\sigma d}\frac{di}{dt}$ when the switch is turning OFF. In Fig. 25, when dv/dt is 32.3 V/ns, the the di/dt of 10 kV SiC MOSFET is only 0.103 A/ns. Besides that, the dv/dt and di/dt between $L_{\sigma d}$ on

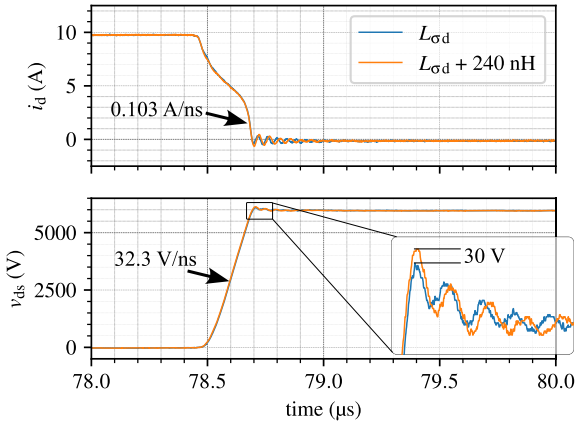


Fig. 25. Experimental waveform of overshoot voltage on the active switch caused by the increased $L_{\sigma d}$.

drain and $L_{\sigma d}$ + 240 nH on drain are almost the same. Only 30 V of increased overshoot voltage was caused by added $L_{\sigma d}$ with 240 nH. Compared with the low-voltage SiC MOSFET, the di/dt is about 1.25 A/ns when the dv/dt is around 40 V/ns [36], which is 10 times larger than that in 10 kV SiC with a similar dv/dt speed, which results in 10 times larger overshoot voltage for low-voltage SiC MOSFET. Since 10 kV SiC MOSFETs have a high absolute drain-source voltage, the overshoot voltage caused by the inductance $L_{\sigma d}$ is not a major concern. On one hand, it is better to select the inductance to mitigate the oscillation with minimized overshoot voltage. On the other hand, this approach is more advisable for 10 kV SiC MOSFETs compared to low-voltage SiC MOSFETs.

VI. Conclusion

To analyze gate oscillation in paralleled 10 kV SiC MOSFETs, this article employs the small signal model based on the half-circuit assumption. The circuit model accounts for parasitic capacitance within the customized MV power module, as well as internal and external inductance associated with the MV power module. Two customized MV power modules utilizing 10 kV SiC MOSFETs serve as the experimental platform, where the effectiveness of the analytical model is verified. Additionally, four mitigation methods for gate oscillation are introduced and validated through experiments, along with a discussion of their tradeoffs and negative impacts.

Appendix

$$
\begin{aligned}
a_2 &= (C_{ds}r_dC_{gd} + C_{ds}r_dC_{gs} + C_{gd}r_dC_{gs}) \\
&\quad \cdot [Z_d(Z_g + r_g) + Z_dZ_s + (Z_g + r_g)Z_s] \\
a_1 &= C_{ds}r_d(Z_d + Z_s) + C_{gd}Z_d(Z_g + r_g + Z_s + r_d) \\
&\quad + C_{gd}(Z_g + r_g)(Z_s + r_d) + C_{gs}r_d(Z_g + r_g) \\
&\quad + C_{gs}Z_s(Z_g + r_g + r_d) + C_{gs}Z_d(Z_g + r_g + Z_s) \\
a_0 &= Z_d + Z_s + r_d
\end{aligned}
$$

$$b_2 = a_2$$
$$b_1 = C_{\mathrm{gd}} g_{\mathrm{m}} r_{\mathrm{d}} (Z_{\mathrm{d}}(Z_{\mathrm{g}} + r_{\mathrm{g}} + Z_{\mathrm{s}}) + (Z_{\mathrm{g}} + r_{\mathrm{g}})Z_{\mathrm{s}}) + a_1$$
$$b_0 = Z_{\mathrm{s}} g_{\mathrm{m}} r_{\mathrm{d}} + a_0.$$

REFERENCES

[1] S. Madhusoodhanan et al., "Solid-state transformer and MV grid tie applications enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs based multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3343–3360, Jul./Aug. 2015.

[2] J. B. Casady et al., "New generation 10kV SiC power MOSFET and diodes for industrial applications," in *Proc. Int. Exhib. Conf. Power Electron. Intell. Motion Renewable Energy Energy Manage.*, 2015, pp. 1–8.

[3] D. Johannesson, M. Nawaz, and K. Ilves, "Assessment of 10 kV, 100 a silicon carbide MOSFET power modules," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5215–5225, Jun. 2018.

[4] A. Marzoughi, R. Burgos, and D. Boroyevich, "Investigating impact of emerging medium-voltage SiC MOSFETs on medium-voltage high-power industrial motor drives," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1371–1387, Jun. 2019.

[5] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kV SiC-based 7 kV/400 V DC transformer for future data centers," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 753–767, Jun. 2019.

[6] D.-M. Valcan, P. C. Kjær, L. Helle, S. Sahukari, M. Haj-Maharsi, and S. Singh, "Cost of energy assessment methodology for offshore AC and DC wind power plants," in *Proc. 13th Int. Conf. Optim. Elect. Electron. Equip.*, 2012, pp. 919–928.

[7] C. Dincan, P. Kjær, and L. Helle, "Cost of energy assessment of wind turbine configurations," in *Proc. 22nd Eur. Conf. Power Electron. Appl.*, 2020, pp. P.1–P.8.

[8] M. Schuck and R. C. N. Pilawa-Podgurski, "Ripple minimization through harmonic elimination in asymmetric interleaved multiphase DC–DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7202–7214, Dec. 2015.

[9] J. Fabre and P. Ladoux, "Parallel connection of 1200-V/100-A SiC-MOSFET half-bridge modules," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1669–1676, Mar./Apr. 2016.

[10] M.-K. Kim, Y.-D. Yoon, and S. W. Yoon, "Actual maximum junction temperature estimation process of multichip SiC MOSFET power modules with new calibration method and deep learning," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 6, pp. 5602–5612, Dec. 2023.

[11] J. Gersh, C. DiMarino, D. DeVoto, P. P. Paret, and J. Major, "Reliability analysis of large-area, low-pressure-assisted silver sintering for medium-voltage power modules," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5252–5259, Oct. 2022.

[12] Z. Zhang, B. Guo, and F. Wang, "Evaluation of switching loss contributed by parasitic ringing for fast switching wide band-gap devices," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9082–9094, Sep. 2019.

[13] Z. Chen, Y. Yao, D. Boroyevich, K. Ngo, and P. Mattavelli, "Exploration of a switching loop snubber for parasitic ringing suppression," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 1605–1612.

[14] I. Josifović, J. Popović-Gerber, and J. A. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3843–3854, Aug. 2012.

[15] J. Chen, X. Du, Q. Luo, X. Zhang, P. Sun, and L. Zhou, "A review of switching oscillations of wide bandgap semiconductor devices," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13182–13199, Dec. 2020.

[16] K. Wang, X. Yang, L. Wang, and P. Jain, "Instability analysis and oscillation suppression of enhancement-mode GaN devices in half-bridge circuits," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1585–1596, Feb. 2018.

[17] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability considerations for silicon carbide field-effect transistors," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4453–4459, Oct. 2013.

[18] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in half-bridge circuits switched with wide band-gap transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2380–2392, May 2014.

[19] D. Qin et al., "Oscillation issue and solution for solid-state circuit breaker using high power IGBT module," *IEEE Trans. Ind. Appl.*, vol. 60, no. 1, pp. 765–772, Jan./Feb. 2024.

[20] Infineon, "Dos and don'ts of SiC power semiconductors - paralleling," 2024. Accessed: Feb. 10, 2025. [Online]. Available: https://community.infineon.com/t5/Training/Dos-and-Don-ts-of-SiC-Power-Semiconductors-Paralleling/ba-p/775913#

[21] H. Kono and I. Omura, "Study of parasitic oscillation of a multi-chip SiC MOSFET circuit based on a signal flow graph model by TCAD simulation," *Solid-State Electron.*, vol. 177, 2021, Art. no. 107884. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0038110120303518

[22] I. Kovacevic-Badstuebner, U. Grossner, D. Popescu, and B. Popescu, "Transient stability analysis of discrete and multi-chip power semiconductor packages," in *Proc. 33rd Int. Symp. Power Semicond. Devices ICs*, 2021, pp. 391–394.

[23] H. Sakai, Y. Okawauchi, S. Yato, H. Araki, T. Atago, and K. Nakahara, "Simplified open-loop transfer functions to analyze influential parasitic parameters for oscillation caused by parallel connected transistors," in *Proc. 35th Int. Symp. Power Semicond. Devices ICs*, 2023, pp. 290–293.

[24] A. Zhu et al., "Accurate multiport network model for forced oscillations analysis and suppression of multichip IGBT power modules," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 552–569, Jan. 2024.

[25] M. Spang, S. Buetow, and G. Katzenberger, "Differential-mode oscillations between parallel IGBTs in power modules," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–10.

[26] Y. Shen, X. Dong, T. Schuetz, and R. Roesner, "Stability modeling for multichip SiC MOSFET power modules," in *Proc. 12th Int. Conf. Integr. Power Electron. Syst.*, 2022, pp. 1–6.

[27] F. Sawallich and H.-G. Eckel, "Inter-chip oscillation of paralleled SiC MOSFETs," in *Proc. Int. Exhib. Conf. Power Electron. Intell. Motion Renewable Energy Energy Manage.*, 2023, pp. 1–7.

[28] K. Saito, T. Miyoshi, D. Kawase, S. Hayakawa, T. Masuda, and Y. Sasajima, "Simplified model analysis of self-excited oscillation and its suppression in a high-voltage common package for Si-IGBT and SiC-MOS," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 1063–1071, Mar. 2018.

[29] B. F. Kjærsgaard et al., "Parasitic capacitive couplings in medium voltage power electronic systems: An overview," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9793–9817, Aug. 2023.

[30] X. Li, Y. Chen, H. Chen, R. Paul, X. Song, and H. A. Mantooth, "A 10 kV SiC MOSFET power module with optimized system interface and electric field distribution," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9540–9553, Aug. 2024.

[31] A. B. Jørgensen et al., "Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.8.

[32] L. Du et al., "Digital close-loop active gate driver for static and dynamic current sharing of paralleled SiC MOSFETs," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1372–1384, Apr. 2024.

[33] B. F. Kjærsgaard et al., "Discovery of loss imbalance in SiC half-bridge power modules–analysis and validations," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 5806–5819, May 2024.

[34] J. K. Jørgensen et al., "Loss prediction of medium voltage power modules: Trade-offs between accuracy and complexity," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 4102–4108.

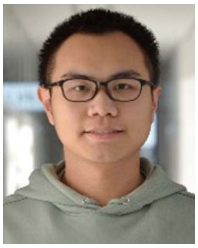
[35] H. Li et al., "Assist gate driver circuit on crosstalk suppression for SiC MOSFET bridge configuration," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1611–1621, Jun. 2020.

[36] S. K. Roy and K. Basu, "Analytical model to study hard turn-off switching dynamics of SiC MOSFET and schottky diode pair," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 861–875, Jan. 2021.

Gao Liu (Graduate Student Member, IEEE) received the B.Sc. degree in 2016 and the M.Sc. degree in electrical engineering in 2019 from Soutwest Jiaotong University, Chengdu, China.

He is currently a Research Assistant in Power Electronics with AAU Energy, Aalborg University, Aalborg, Denmark. His research interests include medium-voltage converters enabled by wide band-gap power devices.

Mr. Liu received the best paper award in the 11th IEEE Workshop on Wide Bandgap Power Devices and Applications–WiPDA 2024.



Zhixing Yan (Graduate Student Member, IEEE) received the B.Eng. degree in electrical engineering and automation from Southwest Jiaotong University, Chengdu, China, in 2018, and the M.Eng. degree in electrical engineering from the South China University of Technology, Guangzhou, China, in 2021. He is currently working toward the Ph.D. degree in power electronics with Aalborg University, Aalborg, Denmark.

His current research interests include medium-voltage converters and SiC gate driving.

Morten Rahr Nielsen (Graduate Student Member, IEEE) received the M.Sc. degree in energy engineering, with a specialization in power electronics and drives, from AAU Energy, Aalborg University, Aalborg, Denmark, in 2022.

He was a Visiting Researcher with the Electrical Engineering Division, Department of Engineering, University of Cambridge, Cambridge, U.K., in 2024. He is currently a Research Assistant with AAU Energy. His research interests include wide bandgap semiconductor devices and control of medium voltage converters.

Thore Stig Aunsborg (Graduate Student Member, IEEE) received the M.Sc. degree in nanophysics and material science from Aalborg University, Aalborg, Denmark, in 2016, and the Ph.D. degree in power electronic converter design from AAU Energy, Aalborg University, in 2023.

He was a Postdoc with AAU Energy until 2024. His research interests include high frequency resonant converters, wide band gap devices, medium voltage power converters, and power module packaging.

Bjørn Rannestad received the M.Sc. and Ph.D. degrees in electrical engineering from AAU Energy, Aalborg University, Aalborg, Denmark, in 1999 and 2019, respectively.

Since 2008 he has been with KK Wind Solutions, Ikast, Denmark, as a senior specialist in front end innovation with high-power converters for wind turbines and renewables. He has 23 years of experience in the power electronic industry. His research interests include the green energy transition, specifically electric energy conversion applications for wind and green hydrogen production.

Hongbo Zhao (Member, IEEE) received the Ph.D. degree in power electronics from AAU Energy, Aalborg University, Aalborg, Denmark, in 2021.

He was a Visiting Researcher with the University of Texas at Austin, and a Visiting Scholar with the University of Galway, Ireland. He is currently an Assistant Professor with AAU Energy. His research interests include the analysis and packaging of modern magnetic components, as well as the applications of wide bandgap semiconductor devices.

Dr. Zhao received the Villum Fellowship in 2022. He was awarded by Frenetic with the "Best Magnetic Design" in 2022. He was selected as a future entrepreneur by the Spin-outs Denmark program in 2023. He was the recipient of "The Bright Idea Award" by Otto Mønsteds Fond in 2023.

Michael Møller Bech received the M.Sc. and Ph.D. degrees in power electronics from Aalborg University, Aalborg, Denmark, in 1995 and 2000, respectively.

Since 2002, except for the period 2006–2009 where he was a Senior Engineer with Motorola Mobile Devices, he has been an Associate Professor with the AAU Energy Department, Aalborg University. His research interests include a broad range of disciplines such as power electronics and their applications to design optimization and control of mechatronic systems.

Stig Munk-Nielsen (Member, IEEE) received the M.Sc. and Ph.D. degrees in power electronics from Aalborg University, Aalborg, Denmark, in 1991 and 1997, respectively.

He is currently a Professor with AAU Energy, Aalborg University. His research interests include Si, SiC, and GaN components operating in soft and hard switching circuits, design challenges for low and medium voltage power modules, and converters with intended application in the industry.