An Efficient Location-Connection-Decoupling Layout Design Method for Multi-Chip SiC Modules With Low Electrical and Thermal Impedance

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***Abstract*—Design automation methods have recently garnered significant research interest in providing effective and advanced tools for generating optimal layout solutions for power modules. However, when addressing high-power silicon carbide (SiC) modules with numerous paralleled power dies, design efficiency, and effectiveness have become critical challenges. This article introduces a highly efficient location-connection-decoupling layout design automation method for multichip SiC power modules. The method focuses on the simultaneous minimization and equalization of electrothermal impedance. To minimize the calculation time, precise copper trace connection processes are decoupled, and an efficient copper expansion strategy is proposed for generating the base copper connections. The decoupling facilitates a reduction in the overall time required to achieve an advanced power module layout design. The proposed method is applied to the layout designs of three SiC power modules with varying numbers of power dies. The efficiency and effectiveness of the proposed method are demonstrated through a comparison of the modules' operational performances and the time required, as determined by the sequencing method. A prototype of the module has been showcased. Various electrical and thermal tests are conducted, and the results validate the feasibility of the proposed design method.**

***Index Terms*—Design automation, electrothermal coordination, layout design, multiple chips, silicon carbide (SiC) modules.**

I. INTRODUCTION

SILICON carbide (SiC) devices are nowadays popularly utilized in various industrial and transportation systems for their superior characteristics of high breakdown voltage, high reliable operating temperature, fast switching frequency, and low loss [1], [2], [3], [4]. However, when applied in high-power applications, such as wind power converters, electrified train traction systems, more- or all-electric aircraft, etc. [5], [6], due to the bare-die-size-caused current limitations, large quantities of SiC chips are often paralleled to provide sufficient current conducting capacities [7], [8], [9]. Therefore, layout design optimizations for multi-chip power modules have received extensive research attention.

The early works performed the optimal design of power modules' layouts with fixed relative positions of power dyes and terminals, subject to their detailed locations and connection structures [10], [11], [12], [13], [14], [15], [16], [17], [18]. In [13], Hingora et al. used a commercial tool, power-CAD, to obtain optimal designs considering electro-thermal and parasitic characteristics, starting from multiple preset layout choices. Hammadi et al. [14] used a framework iSIGHT (combining CATIA, Q3D, Orcad/Pspice, and ANSYS) to obtain the optimal distances and sizes of a power module. Alavi et al. [15] optimized the chip positions of a dual-pack IGBT module through the combination of a particle swarm optimization algorithm and a temperature field solver based on COMSOL. Chen et al. [16], [17], [18] used a genetic algorithm (GA) to quickly iterate to chip layout scheme by building a response surface model with temperature and chip position coordinates. However, the application of the above methods inevitably considers detailed copper trace structure and sizing design in subsequent work.

To eliminate experience-based constraints and to equitably expand the search space in the layout design, several layout design automation methods have been established and developed [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32]. In [19], [20], [21], [22], [23], [24], [25], Evans et al. at the University of Arkansas proposed PowerSynth, which uses normalized symbol maps to represent the layout structures and is capable of evaluating solutions on a second timescale given a layout template. In [26], Zhou et al. developed a graph-model-based approach, a very efficient method for generating layouts that can automatically generate templates for later optimizations and effectively extend the search space. In [27], [28], [29], [30], [31], Ning et al. proposed a sequence-method-based layout design automation approach to minimize parasitic and footprint, based on GA. As the search space of the sequence method can

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contain every possible solution, the design effect is guaranteed. To balance the optimization effect and efficiency, our group proposed dividing the sequencing method into two stages to realize the layout optimization of a phase-leg module by first arranging multiparallel chips in a single bridge arm and then setting the locations of two bridge arms [32]. The previous method can improve the design automation efficiency to some extent. However, as the bridge-arm-locating processes are tightly coupled with the copper-trace-connecting ones, when dealing with multichip paralleled modules, the iterations for an advanced result are still time-consuming.

In this article, an automated method for designing location-connection-decoupling (LCD) layouts is developed to meet the requirements for electro-thermal minimization and equalization. The bridge arm and terminal spatial locations as well as the copper trace connections are completely separated into two distinct stages in the proposed LCD automation method, which can reduce the overall computation time effectively. A very efficient copper expansion strategy is also proposed, that can generate basic but acceptable copper traces without any iteration, to achieve the decoupling. Then the copper trace architectures are further improved by iterations of the homogenization design method (HDM).

The rest of this article is organized as follows. Section II introduces the principles of the LCD design automation method. The electro-thermal extraction method is presented in Section III. The LCD design results and the consuming time are compared with others' methods in Section IV. Section V demonstrates the proposed layout design automation method for multiple-chip power modules, to validate its feasibility. Finally, Section VI concludes this article.

II. PROPOSED LCD DESIGN AUTOMATION METHOD

In order to achieve effective and efficient automatic layout designs for multichip paralleled SiC power modules, the optimization procedure comprises: parameter design and constraints of the modules, decoupling our previously proposed method [32] by the LCD method to assess the layout results, and evolutionary optimization of the layout. Fig. 1 illustrates the design process of the LCD, which generates an optimized layout design in three stages. During the GA optimizations in stages I to III, the objective function considers the junction temperature (T) and its mean square error (M_{T}), the inductance (L) and its mean square error (M_{L}), and the footprint area (S) to ensure synchronous minimization and equalization of electrothermal characteristics

$$\begin{cases} T < T_{\max} \quad M_T < M_{T\_\mathrm{limit}} \quad M_L < M_{L\_\mathrm{limit}} \\ \mathrm{obj} = \frac{1}{\mathrm{TLSM_L M_T}} \end{cases} \tag{1}$$

$$M_L = \sqrt{\frac{\sum_{i=1}^{N} \left(L_i - \bar{L}\right)^2}{N}} \tag{2}$$

$$M_T = \sqrt{\frac{\sum_{i=1}^{N} \left(T_i - \bar{T}\right)^2}{N}} \tag{3}$$

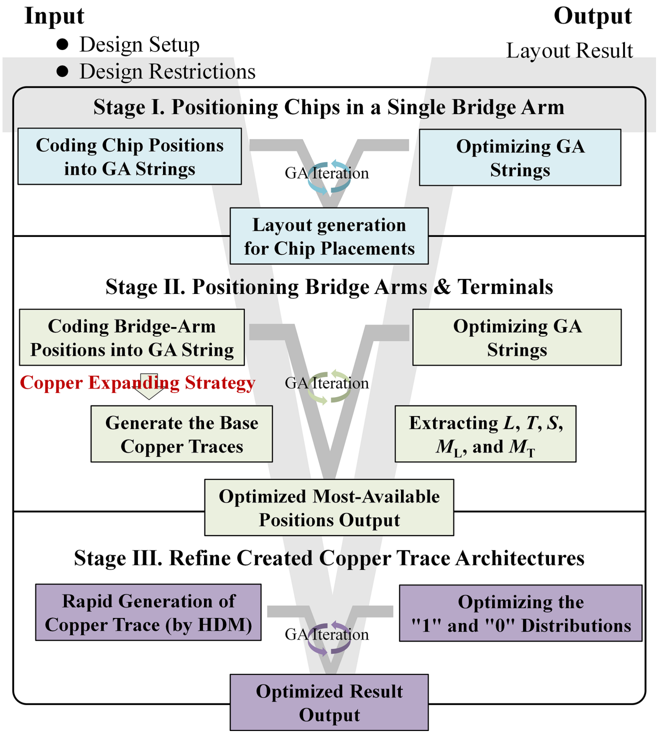


Fig. 1. Design processes of the proposed LCD method.

where L_i is the inductance of the ith-chip branch, $\bar{L}$ the averaged inductance of different chip-conducting branches, T_i the junction temperature of the ith-chip, and $\bar{T}$ the averaged junction temperature.

At input, the design setup (containing the device, substrate, and bond wire selections) and design restrictions (size and temperature constraints) are determined based on the design requirements (such as the rated voltage, rated current, and so on). As shown in Fig. 1, the detailed steps of the LCD design process are as follows.

A. Positioning Chips in a Single Bridge Arm in Stage I

In stage I, the multiparallel chips in a single bridge arm are optimally positioned using the sequence approach proposed as in Fig. 2. The chips in a single bridge arm are randomly positioned and coded into a GA string by relative positions and distances. For example, (13425, 54213) indicates that chip 2 is below chip 3 ($\times 3 \times 2 \times, \times \ \times 2 \times 3$), above Chip5 ($\times \ \times \ \times 25, 5 \times 2 \times \ \times$), and to the right of Chip4 ($\times \ \times 42 \times, \times 42 \times \ \times$); "11" indicates that chip 2 is oriented to the right, and "101011" denotes that a particular chip is horizontally distant from its left side by $5 \times d_{0\mathrm{I}}$ and vertically distant from the chip below by $3 \times d_{0\mathrm{I}}$. In the chip positioning process, the value of $d_{0\mathrm{I}}$ is determined to be the minimum required etching width to guarantee its feasibility of manufacturing. The position string is varied using GA based on the electrical and thermal parameters collected from the position. After the GA optimization has converged, the ideal chip placements in a single bridge arm are determined.

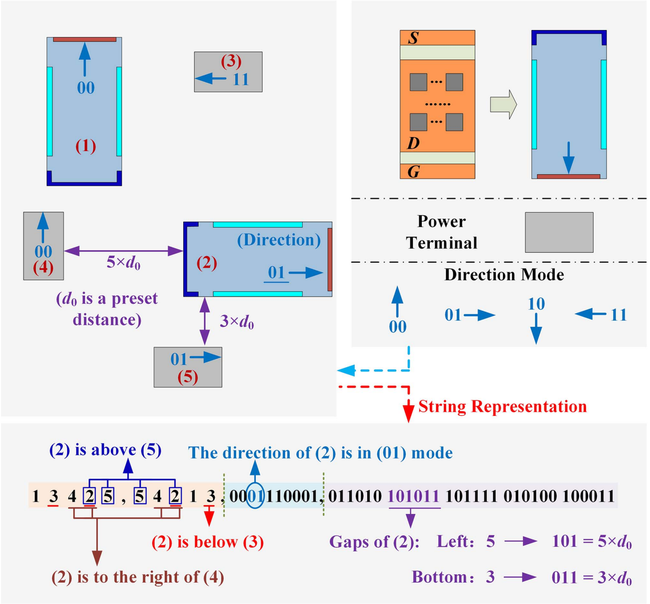
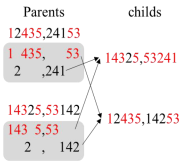
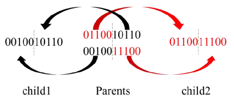


Fig. 2. GA string generation for bridge arm and terminal locations.

TABLE I
GENETIC ALGORITHM CROSSOVER MUTATION PROCESSES

GA String	Relative Positioning (First part)	Orientation/Distance (Second and third parts)
Crossover		
Mutation	12435,24153 ⇨ 12435,25143	0110010110 ⇨ 0110010100

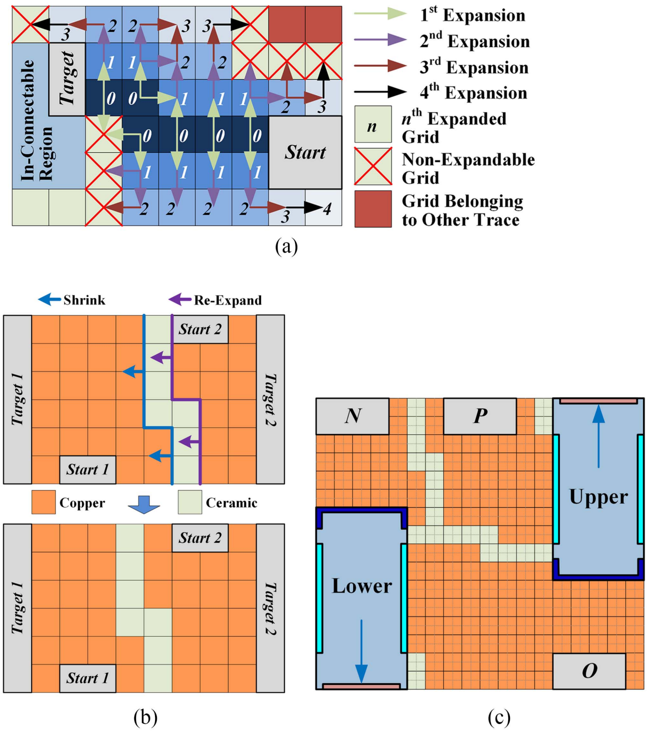


Fig. 3. Processes of a copper expanding method for basic copper trace generation used in stage II. (a) Expanding. (b) Shrinking and re-expanding. (c) Typical case.

B. Positioning of Bridge Arms & Terminals in Stage II

In stage II, instead of choosing the bridge arm and terminal positions alongside the copper trace structures, Fig. 1 shows that the locating methods in this article are completely decoupled from the copper trace generation processes. Consequently, just the bridge arm and terminal locations need to be determined separately using GA string illustrations, as illustrated in Fig. 2. The first portion of the GA string represents the relative positions of the bridge arms and terminals, the second part depicts the directions, and the third part represents the distances between them. The rules for coding the relative positions, directions, and distances are the same that have been used in stage I to locate the chips. It's worth noting that, in the bridge arm and terminal locating process, the smallest distance $d_{0\text{II}}$ is set to the etching width to guarantee its feasibility of manufacturing. Furthermore, in the GA string, the initial segment is encoded using decimal numbers, whereas the second and third segments employ binary numbers. The rationale behind this is that each number (refer to Fig. 2, numbers 1 to 5, for instance) in the first segment of the string is constrained to appear only once. Consequently, during the crossover and mutation processes of GA-based iterations, as depicted in Table I, it is advantageous to ensure these constraints by utilizing decimal coding for the first segment of the string. When addressing the second and third segments, since the encoded values lack such restrictions, binary coding is more suitable for the unrestricted crossover and mutation processes, as illustrated in Table I. Hence, a string that combines decimal and binary encoding is utilized.

It is important to highlight that in the original method [32], the generation of copper traces relies on iterative HDM. This process is then utilized in the subsequent stage of the proposed LCD method to refine the copper trace structure. Specifically, in each bridge arm locating step, this iterative refinement significantly increases the computational time due to the repeated processing required. By proposing the very efficient copper expansion methodology, as no iteration is required in obtaining an initial copper trace pattern for judging the fitness of the bridge arm location design, the overall time consumption can be effectively reduced. The rapidly generated copper traces meet electrical connection rules and can be utilized for estimating inductance for the current location design. The objective is to connect the bridge arms and terminals in the shortest path, and then extend the shortest connection paths to their in-connecting sides, as seen in Fig. 3(a). During expansions, newly extended grids should always be at least one grid away from in-connectable areas or grids from other traces, and the expansion operations should not be stopped until all available grids have been tried.

Furthermore, the resistances of the three copper traces (trace 1: P—upper bridge arm, trace 2: upper bridge arm, O—lower bridge arm, and trace 3: lower bridge arm—N) must be approximately equal. As illustrated in Fig. 3(b), the trace exhibiting reduced inductance must undergo a contraction to facilitate the expansion of the trace displaying augmented inductance. With respect to the design scheme pertaining to the bridge arm and terminal location, a fundamental copper trace structure is generated and depicted in Fig. 3(c).

In the case of the copper expansion process, a series of procedures are employed to facilitate the verification of connectivity as follows.

1) The entire area is tessellated into grids of predetermined grid sizes (d_{grid}). The d_{grid} is set twice the minimum required etching width $d_{0\text{II}}$ ($d_{\text{grid}} = 2 \times d_{0\text{II}}$) to rapidly achieve a copper trace expansion result. The $d_{0\text{II}}$ is illustrated by the dash lines in Fig. 3(c).
2) Starting from the edge closest to the sides of the upper bridge arm at the P terminal, a path-finding procedure is performed to find the shortest path that connects to the sides of the upper bridge arm. This is shown in detail in Fig. 3(a). The same procedure is then applied to the *O* and *N* terminals for the remaining connections. During the path-finding process, the marked path should always be at least one grid away from other symbols or areas to ensure isolation.
3) If the path does not reach the target, the design scheme is also marked as in-connectable. Otherwise, all paths could be effectively connected in a connectable design scheme.

C. Refine Created Copper Trace Architectures in Stage III

The optimized bridge arm and terminal positions from stage II are processed in stage III to refine rapidly created copper trace architectures using the HDM [30]. The substrate surface is then tessellated into grids with the grid size of the etch width $d_{0\text{II}}$, except for the bridge arm and terminal occupied regions. Copper traces are represented by the code “1” in the grids, while etching areas are denoted by “0.” GA optimizes the “1” and “0” distributions to produce an ideal copper connection design with minimal and balanced inductance. In addition, as the grid in this stage is finer than that in the copper expansion stage, the precision of the refined copper trace can be ensured in conjunction with the iterative HDM optimization.

III. Physical Property Models Used in LCD

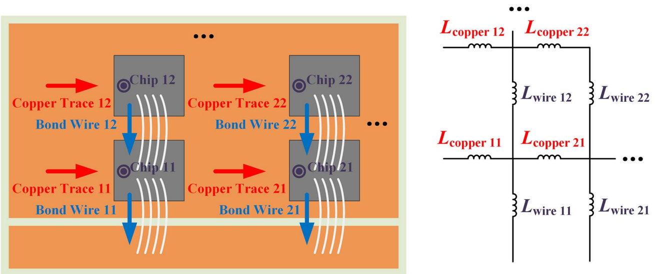
In the LCD automation method, an electro-thermal mathematical model is constructed to evaluate the results based on the objective function provided. The functions and characteristics of each setup are discussed in the following subsections.

A. Electrical Parameters Extraction

To simulate the parasitic inductance of the multichip parallel module, an electrical circuit is set up to represent the conduction conditions, as shown in Fig. 4(a) and (b). The self-inductance of the bond wires can be modeled as described in [33], [34]

$$L_{\text{wire}} = \frac{\mu l_1}{2\pi}\left(\ln\frac{2l_1}{d} - 1\right) \tag{4}$$

where μ is the magnetic conductivity, l_1 and d are the length and diameter of the wire.



(a) (b)

Fig. 4. Equivalent circuit for inductance extraction, where (a) conducting paths, and (b) inductance circuit.

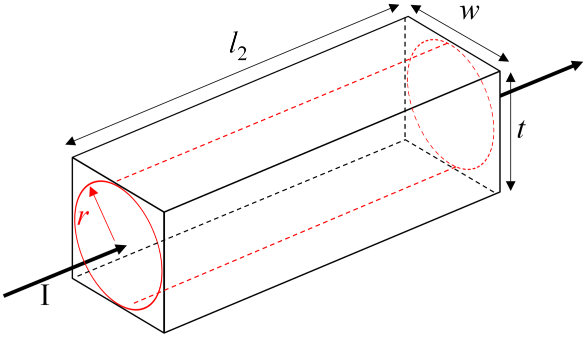


Fig. 5. Simplified scheme for thin rectangular conductors.

As illustrated in Fig. 5, thin rectangular conductors can be reduced to a simplified representation as circular wires with a radius (r) equal to half the thickness (t). Consequently, the self-inductance of copper traces can be expressed as [35]

$$L_{\text{trace}} = \frac{\mu l_2}{8\pi} + \frac{\mu}{2\pi}\left(l_2 \ln\frac{\sqrt{r^2 + l_2^2} + l_2}{r} - \sqrt{r^2 + l_2^2} + r\right) \tag{5}$$

where l_2 is the copper trace length.

B. Thermal Parameters Extraction

To accurately and efficiently estimate the junction temperature, a three-dimensional (3D) lumped-parameter thermal network (LPTN) is established. The transverse heat conduction phenomenon in the 3D LPTN generates a heat spreading angle, which results in the thermal resonance of adjacent chips [36], as illustrated in Fig. 6. Consequently, the transverse thermal resistances can be calculated based on the heat spreading angle covered area (S_i) in each conducting layer (the *i*th layer), and the S_{i} is simulated through an analytical model. In detail, the

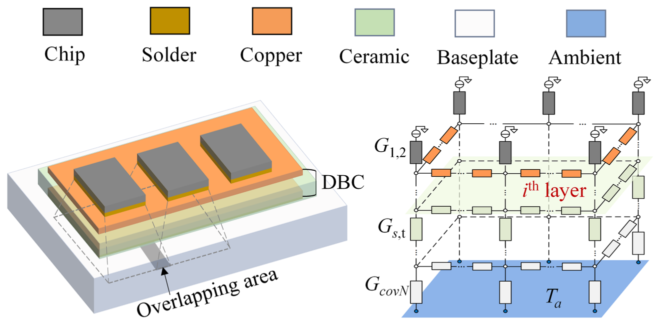


Fig. 6. Thermal network model of a multichip-paralleled module.

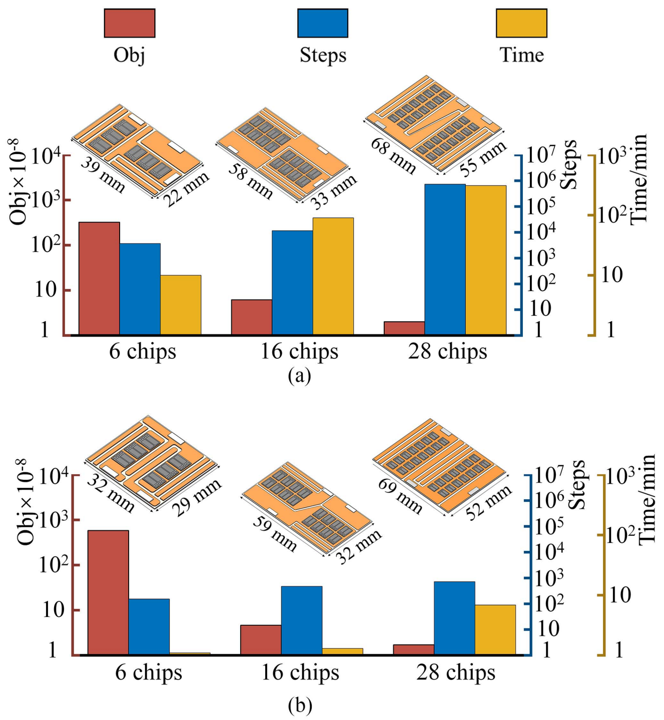


Fig. 7. Comparisons of objective values, iteration steps, and consumed time using (a) the reference method in [32] and (b) the proposed LCD method.

temperature rise in the ith layer can be modeled by [37]

$$T_i(x,y,z) = A_{i0} + B_{i0}z + \sum_{m=1}^{\infty} K_m(x) F_m(z) + \sum_{n=1}^{\infty} P_n(y) F_n(z) + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} K_m(x) P_n(y) F_{mn}(z) \quad (6)$$

where $K_m(x)$, $P_n(y)$, $F_m(z)$, $F_n(z)$, and $F_{mn}(z)$ are functions that can be expressed as [38]

$$\begin{cases} K_m(x) = \cos(\lambda_m x), \ P_n(y) = \cos(\delta_n y) \\ F_m(z) = A_{im}\cos h(\lambda_m z) + B_{im}\sinh(\lambda_m z) \\ F_n(z) = A_{in}\cos h(\delta_n z) + B_{in}\sinh(\delta_n z) \\ F_{mn}(z) = A_{imn}\cos h(\beta_{mn} z) + B_{imn}\sinh(\beta_{mn} z) \end{cases} \quad (7)$$

where A_{im} and B_{im} are the mth Fourier coefficients for temperature variation in the x-direction, A_{in} and B_{in} the nth Fourier coefficients for temperature variation in the y direction, A_{imn} and B_{imn} the Fourier cross-coefficients; and λ_m, δ_n, and β_{mn} the eigenvalues.

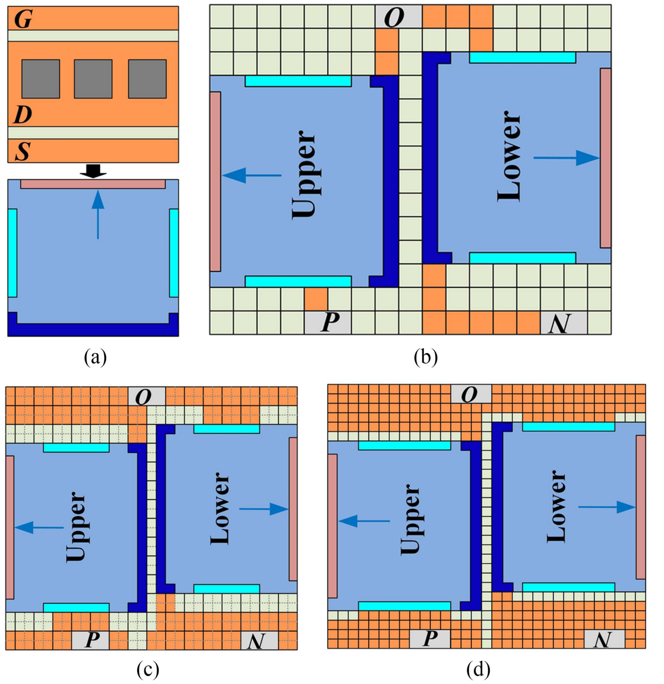


Fig. 8. Schema of three-chip parallel module LCD optimization process. (a) Bridge arm simplification. (b) Connectable design scheme. (c) Copper expansion architecture. (d) Refine created copper trace.

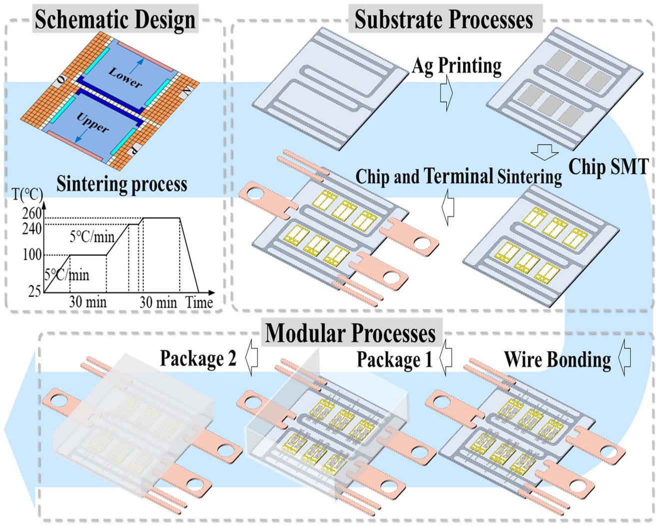
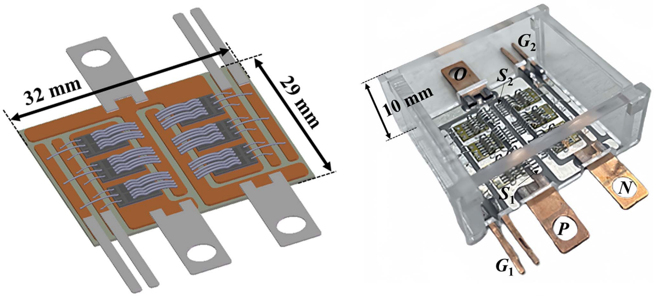


Fig. 9. Fabrication process of the prototype module.

Based on (7), the heat flux density in the ith layer can be formulated by [38]

$$\vec{q}_i(x,y,z) = \nabla T_i(x,y,z) = Q_{ix}(x,y,z)\vec{a}_x + Q_{iy}(x,y,z)\vec{a}_y + Q_{iz}(x,y,z)\vec{a}_z \quad (8)$$



(a) (b)

Fig. 10. (a) Schema of a half bridge 3-chip-paralleled 3D simulation model. (b) Module prototype.

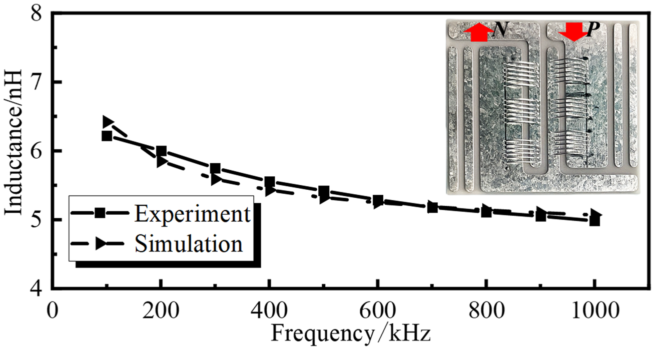


Fig. 11. Comparison between simulated and tested parasitic inductance.

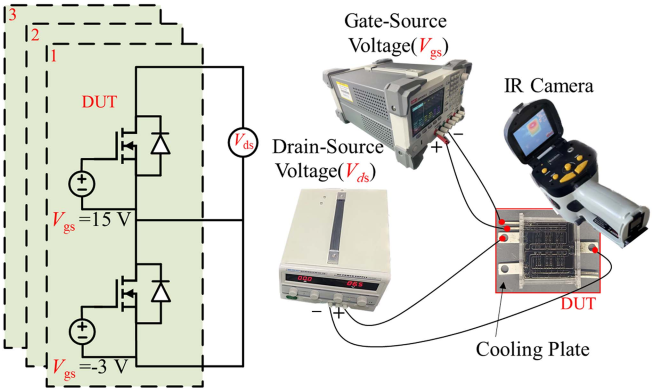
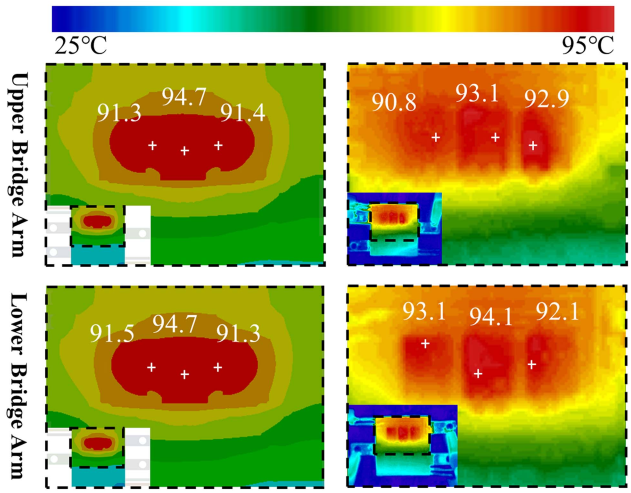


Fig. 12. Temperature measurement platform.

$$\begin{cases} Q_{ix}\left(x,y,z\right)=\sum_{m=1}^{\infty}K'_m(x)F_m(z) \\ +\sum_{n=1}^{\infty}\sum_{n=1}^{\infty}K'_m(x)P_n(y)F_{mn}(z) \\ Q_{iy}\left(x,y,z\right)=\sum_{m=1}^{\infty}P'_n(y)F_n(z) \\ +\sum_{n=1}^{\infty}\sum_{n=1}^{\infty}K_m(x)P'_n(y)F_{mn}(z) \\ Q_{iz}\left(x,y,z\right)=B_{i0}+\sum_{m=1}^{\infty}P_n(y)F'_n(z) \\ +\sum_{m=1}^{\infty}P_n(y)F'_n(z) \\ +\sum_{n=1}^{\infty}\sum_{n=1}^{\infty}K_m(x)P_n(y)F'_{mn}(z) \end{cases}. \tag{9}$$



(a) (b)

Fig. 13. Temperature distribution, where (a) simulated, and (b) tested.

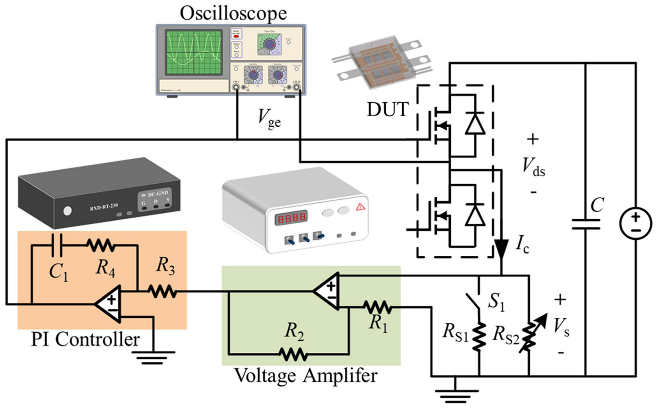


Fig. 14. Transient thermal impedance measurement circuit.

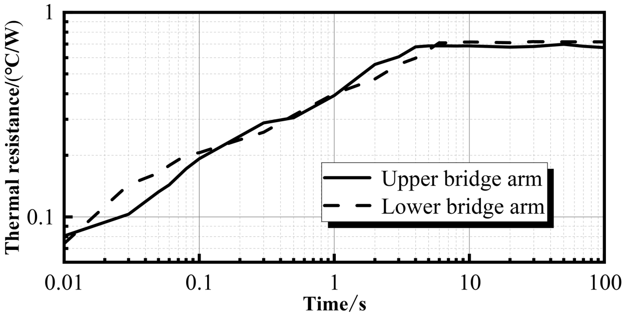


Fig. 15. Thermal impedance of both upper and lower bridge arms.

Since the heat spreading angle theory assumes that the heat flux is evenly distributed in the angle covered area (named the effective conduction area), the effective conduction area in the ith layer can therefore be modeled by [38]:

$$S_i=\frac{2p_{\text{chip}}}{Q_{iz}(x_C,\ y_C,\ z_{i\text{top}})+Q_{iz}(x_C,\ y_C,\ z_{i\text{bottom}})} \tag{10}$$

where p_{chip} is the power loss in each chip; x_C and y_C are the x-axis and y-axis values of the chip center, respectively; and $z_{i\text{top}}$

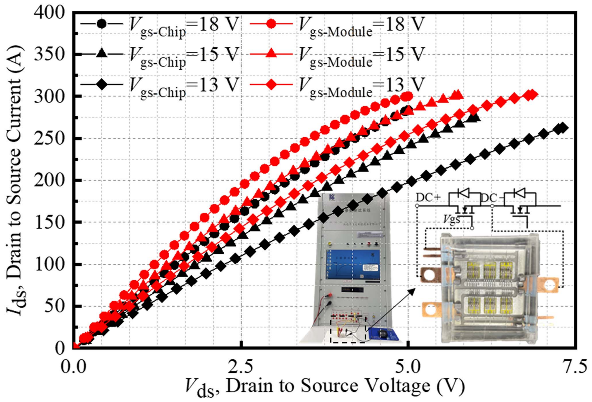
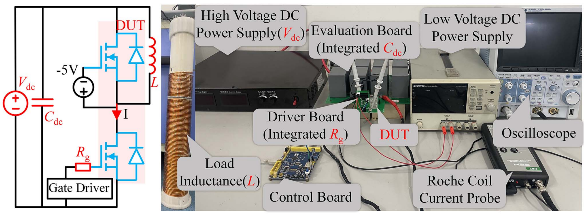
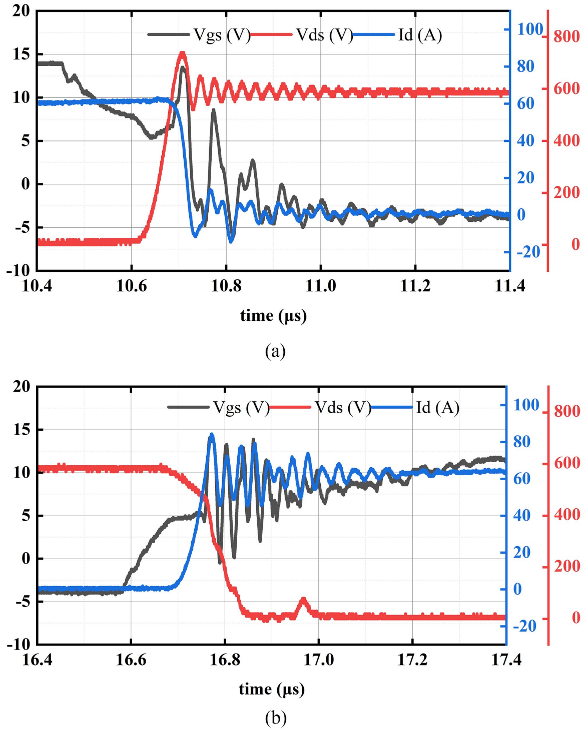


Fig. 16. Tested I_{ds} versus V_{ds} with different V_{gs}.



(a) (b)

Fig. 17. Double pulse platform, where (a) circuit, and (b) platform.



(a)

(b)

Fig. 18. Switching waveforms, where (a) turn-OFF transient, and (b) turn-ON transient.

TABLE II
MATERIAL LISTS

Element	Description
Power dies	WM1A045170B 1200 V, 6.3 mm × 4.8 mm × 0.2 mm
Substrate	Aluminum nitride (AlN) direct bond copper (DBC) 0.3 mm Cu - 0.32 mm AlN - 0.3 mm Cu
Bond wires	1 × 10 mils Al-wire for signal connections 6 × 15 mils Al-wire for power connections
Attachment	0.1 mm nano-silver paste [37]

and $z_{i\text{bottom}}$ the z-axis values of the top and bottom locations of the ith layer, respectively.

Once the effective conduction area of each layer has been established, the overlapping regions between the various chips in each conducting layer are acquired. The thermal coupling effects are a consequence of the overlapping regions, as illustrated in Fig. 6. Consequently, the thermal correlation between two power dies can be disregarded in instances where their effective conduction areas do not overlap. Consequently, when establishing the 3D LPTN, the overlapping regions are considered to contribute to both vertical (z-direction) and transverse thermal coupling (x-y plane) heat transfer. The 3D LPTN is illustrated in Fig. 6. The temperatures can be obtained by solving the following governing equations: (11), shown at the bottom of the next page, where $G_{s,t}$ is the heat conductance between node s and t, T_s is the temperature of node s, G_{covs} is the heat conductance between the convectional boundary node s and the coolant, q_s is the heat generation in node s, and T_a is the coolant (or ambient) temperature.

IV. LCD-BASED MULTICHIP MODULE LAYOUT DESIGNS

To verify the design efficiency and effectiveness of the proposed LCD approach, half-bridge power modules with three, eight, and fourteen parallel chips in a single bridge arm (6, 16, and 28 chips in total) are designed respectively. The SiC MOSFETs manufactured by China Electronics Technology Group Corporation (CETC) with the brand WM1A045170B, the AlN substrate (0.3 mm Cu—0.32 mm AlN—0.3 mm Cu), Al bonding wires (1 × 10 mils for signal connections and 6 × 15 mils for power connections), and nano-silver attachments (LT paste [39]) are used in the module design, as given in Table II.

In the designs, the packaging temperature tolerance is set to 175 °C; inductance and temperature mean square error are determined by the number of chips, thermal balance, and user requirements. The design objective and the constraints are as follows:

$$\begin{cases} T < 175^{\circ}\text{C} M_T < M_{T\_\text{limit}} M_L < M_{L\_\text{limit}} \\ \text{obj} = \frac{1}{TLSM_L M_T} \end{cases} . \tag{12}$$

The LCD design results for the three designs and the number of iterations required are compared with those obtained using a conventional sequence method described in [32], as shown in Fig. 7. As illustrated in the figure, the proposed LCD method is capable of generating module designs with objective values that are nearly identical to those produced by the sequence method in [32], while requiring significantly fewer iteration steps and times. In the case of the three-chip-paralleled module design, the number of iterations is reduced from 3689 to 152, representing a reduction of 95.88%. The time required is also reduced, from 10.00 min to 1.10 min, representing a reduction of 89.00%.

As the number of paralleled chips reaches 8 and 14, the reduction in iteration time (step) becomes more pronounced while maintaining the desired design outcome. The time reduction can reach 98.55% (from 89.77 min to 1.30 min) for eight-chip-paralleled designs and 97.79% (from 309.60 min to 6.84 min) for 14-chip-paralleled ones. It is noteworthy that even when working on a high-performance workstation, the design of a module with a relatively large chip quantity (14 chips in a single bridge arm and 28 chips in total) is time-consuming (exceeding five hours), whereas the design time of the proposed LCD method is more acceptable (approximately 0.11 h). In the range of power modules using a large number power chips in parallels, the LCD method is superior in terms of time compared to the benchmark method, while output results with almost the same fitness. Therefore, it is believed that the proposed approach can be advantageously used to design modules with even more chips.

V. PROTOTYPE AND EXPERIMENTAL VALIDATIONS

The three-chip parallel half-bridge SiC power module, as illustrated in Fig. 8, is structured by the LCD design. As shown in Fig. 8(a), stage I focuses on the generation of chip positions within the single bridge arm, optimization of their placement, and subsequent simplification of the bridge arm to accommodate the layout. In stage II, after generating a structure that satisfies the electrical interconnect requirements as shown in Fig. 8(b), the basic copper structure that satisfies the requirements is created through the copper expansion strategy as shown in Fig. 8(c) and the best available location is determined. Finally, in stage III, HDM is used to generate a more refined copper structure by iterative calculation and layout optimization, as shown in Fig. 8(d). The fabrication process of the optimized prototype module is shown in Fig. 9, where the three main steps are described as a design solution, substrate process, and modular process respectively. For validating the methodologies, the 3D simulation model and module prototype are produced as shown in Fig. 10(a) and (b), respectively. The following details the electrical and thermal tests on the prototype module.

A. Parasitic Inductance

To verify the design feasibility, the parasitic inductance of the module is numerically and experimentally investigated at various switching frequencies using an impedance analyzer. Fig. 11 shows that the measured parasitic inductance is consistent well with the simulated one, especially in the frequency range of 100 kHz to 1 MHz. The variation is limited to less than 3%. The module's parasitic inductance can reach as low as 4.99 nH@1 MHz.

B. Temperature Imbalance

To fully verify the temperature imbalance of the prototype power module, a comprehensive test platform is established, as shown in Fig. 12. A constant dc current is controlled by a dc power supplier (UDP3305S-E). The module is mounted with a cooling plate to guarantee a constant case temperature (25 ± 1 °C, monitored by a thermocouple on-site). An infrared thermal camera is used to measure the temperature distributions of the prototype module.

The temperature distribution of the prototype module is also simulated by finite-element analysis and subsequently tested by the abovementioned platform. The results are presented in Fig. 13 for further comparisons. The maximum temperature reaches 94.1 °C, which agrees with the simulated value. The mean square differences of the maximum chip temperature between the upper and lower bridge arms are 1.04 and 0.82, respectively, indicating that the temperature imbalance is significantly reduced.

C. Thermal Impedance

The transient thermal impedance is also measured using a commercial testing system BXD-RT-230. The system uses the forward voltage of the body diode of a MOSFET (V_{sd}) as a temperature-sensitive electrical parameter, because the variations of the V_{sd} are in linear relationship with temperature.

The testing circuit of the system is shown in Fig. 14. The load current I_c, which flows through the device, keeps sampling by sampling resistors (R_{s1} and R_{s2}). The switch S_1 of the current-sensing circuit is open during heating when the heating power of the device remains constant. Then the transient thermal impedance can be calculated as

$$Z_{th}(t_h) = \frac{V_{gs\_i} - V_{gs\_f}(t_h)}{K \cdot P} \tag{13}$$

$$P = I_{ch} \cdot V_{ds} = \frac{V_s \cdot V_{ds}}{R_{s1}} \tag{14}$$

where $I_{\text{ch}} = V_s/R_{s1}$, K is the relationship between the module gate-source voltage and the temperature, $V_{\text{gs\_}i}$ the gate-source

$$\begin{bmatrix} G_{1,1} & -G_{1,2} & \cdots & -G_{1,t} & \cdots & -G_{1,N} \\ -G_{2,1} & G_{2,2} & \cdots & -G_{2,t} & \cdots & -G_{2,N} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ -G_{s,1} & -G_{s,2} & \cdots & -G_{s,t} & \cdots & -G_{s,N} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ -G_{N,1} & -G_{N,2} & \cdots & -G_{N,t} & \cdots & G_{N,N} \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_s \\ \vdots \\ T_N \end{bmatrix} - \begin{bmatrix} G_{\text{cov}1} T_a \\ G_{\text{cov}2} T_a \\ \vdots \\ G_{\text{cov}s} T_a \\ \vdots \\ G_{\text{cov}N} T_a \end{bmatrix} = \begin{bmatrix} q_1 \\ q_2 \\ \vdots \\ q_s \\ \vdots \\ q_N \end{bmatrix} \tag{11}$$

TABLE III
STATIC ELECTRICAL PARAMETERS

Parameter	Test Conditions	Upper Arm	Lower Arm
$V_{\text{gs(th)}}$	$V_{\text{ds}} = \text{V}_{\text{gs}}$, $I_{\text{d}} = 28$ mA	2.34 V	2.38 V
I_{dss}	$V_{\text{ds}} = 1200$ V, $V_{\text{gs}} = 0$	< 1 nA	< 1 nA
$\text{V}_{\text{(br)dss}}$	$V_{\text{gs}} = 0$, $I_{\text{d}} = 100$ µA	1656 V	1662 V
I_{gssf}	$V_{\text{gs}} = 18$ V, $V_{\text{ds}} = 0$	67 nA	86 nA
R_{ds}(on)	$V_{\text{gs}} = 15$ V, $I_{\text{d}} = 100$ A	14.20 mΩ	14.60 mΩ
V_{fsd}	$V_{\text{gs}} = -4$ V, $I_{\text{sd}} = 50$ A	3.90 V	3.92 V

voltage before heating, V_{gs_f} the gate-source voltage after heating, t_{h} the corresponding heating time, I_{ch} drain current, and V_{ds} the drain-source voltage. The tested thermal resistances are shown in Fig. 15, with stabilized value of 0.69 °C/W and 0.72 °C/W for upper and lower bridge arms, respectively.

D. Static Characteristic and Switching Performance Tests

Additionally, the static and dynamic electrical performances of the prototype module are evaluated. A KEW3500 commercial instrument is used in obtaining the static characteristics. The data and test conditions are given in Table III, where V_{ds} is the drain-source voltage, I_{ds} the drain-source current, $V_{\text{gs(th)}}$ the gate threshold voltage, $I_{\text{ds}s}$ the zero gate-drain current, $V_{(\text{br})\text{ds}s}$ the drain-source breakdown voltage, $I_{\text{gss}f}$ the gate leakage current, R_{ds}(on) the drain-source ON-state current, $V_{\text{fs}d}$ the source-drain forward voltage, V_{gs} the gate-source voltage, I_{d} the continuous drain current, and I_{sd} the source-drain current. It can be found that the module can withstand a V_{ds} at 1200 V with a gate voltage of $V_{\text{gs}} = 0$ V ($I_{\text{dss}} < 1$ nA). Fig. 16 shows the output characteristic curves tested at $V_{\text{ds}} = 13$, 15, and 18 V.

Moreover, a double pulse platform has been constructed, as illustrated in Fig. 17. During the testing, the upper bridge arm chips are subjected to a negative gate-source voltage, thereby ensuring that they are turned OFF [40], [41]. Conversely, the lower bridge arm chips are controlled via an STM32 board. Fig. 18 illustrates the tested switching waveforms with gate resistance (R_g) of 20 Ω, bus voltage (V_{dc}) of 600 V, bus capacitance (C_{dc}) of 320 μF, load inductance (L) of 125 μH, and load current (I) of 60 A. The waveforms indicate a voltage overshoot of 140 V and a current overshoot of 24.40 A. The turn-ON and turn-OFF times are 115 and 267 ns, respectively. The static and dynamic characteristics of the designed module confirm the effectiveness and feasibility of the methodology.

VI. CONCLUSION

This article proposes a highly efficient LCD layout design automation method for multi-chip-paralleled half-bridge SiC power modules, which considers the minimization and equalization of electrothermal parameters in a synchronous manner. The proposed LCD method decouples the bridge-arm and terminal location process and the copper connection processes into two separate stages. An efficient method for expanding copper traces without the need for iterations is proposed and employed in the location stage to assist in the evaluation of locating designs. Subsequently, the HDM iterations are employed in the connection stage for the purpose of refining the copper trace structures. The LCD method is employed in the design of three modules, each with a different number of paralleled chips: 3; 8; and 14, separately. The decoupling of the iterations in the location and connection stages allows for a significant reduction in the overall time required to obtain an advanced layout design, i.e., 89.00%, 98.55%, and 97.79%, respectively.

Finally, a three-chip-paralleled module with specialized design criteria based on the LCD method is demonstrated and fabricated. Several electrical and thermal tests are performed and the results confirm the feasibility of the proposed method.

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