A T-Shaped High Isolation Gate Driver Power Supply for Medium-Voltage SiC Half-Bridges

Fengjuan Zhang, Hao Feng, *Member, IEEE*, Li Ran, *Fellow, IEEE*, and Jianyu Pan, *Member, IEEE*

***Abstract*—For medium-voltage wide bandgap devices, the interdependence between isolation capability and coupling capacitance is the major barrier to compact and insulation-reliable gate driver power supplies (GDPS). This article proposes a loosely coupled transformer with a customized T-shaped core and printed circuit board (PCB) coils, achieving high isolation and low capacitance within a limited footprint. Dual-output PCBs are oriented to reinforce the isolation between multiple coils, while orthogonal placement minimizes parasitic coupling. Bulk field grading is applied with an internal layer to reduce the electric field (E-field) stress, as well as alleviate the triple point. Finally, circuit decoupling is used to address the cross-coupling between multiple outputs, so that a quasi-constant voltage is available in each output channel against varying load while unregulated. The solution is tailored for a typical SiC half-bridge, which achieves a partial discharge inception voltage of 30 kV RMS with a minimal primary-to-secondary distance of 9.5 mm, a coupling capacitance of 2.65 pF, and an output power of 20 W per channel. The GDPS also supports self-regulated power delivery under slew rates of up to 180 kV/μs, indicating its high common-mode transient immunity level.**

***Index Terms*—Coupling capacitance, cross coupling, dual-output isolated gate driver power supply, isolation capability, medium-voltage (MV) silicon carbide (SiC) devices.**

I. Introduction

SILICON carbide (SiC) devices can achieve a tenfold blocking voltage compared to their Si counterparts with the same drift region thickness owing to higher dielectric breakdown electric field strength [1]. Currently, 10 kV SiC MOSFETs have been validated in many applications [2], [3], and the feasibility of 15 kV SiC MOSFETs for MV applications has also been widely discussed [4], [5].

However, the introduction of SiC MOSFETs in MV systems imposes significant challenges on the design of isolated gate driver power supplies (GDPS). On the one hand, GDPS needs to provide a sufficiently high isolation capability. On the other hand, to ensure the reliable operation of SiC MOSFETs under the high *dv/dt* conditions generated by fast switching in MV applications. A GDPS will require high common-mode transient immunity (CMTI). Minimizing the common-mode (CM) current can prevent failures in the control circuit [6].

Various methods have been explored to improve the insulation barrier and CM interference suppression of GDPS. Early studies, such as in [7], used optical fiber for power transfer to achieve high insulation levels and eliminate the coupling capacitance C_{ps}. However, the power output is limited to 0.5 W, which is not sufficient considering that the auxiliary power also supplies the sensing circuit and even cooling fans. Wireless power transfer (WPT) has been shown to meet the power requirement [8], [9]. Sun et al. [8] used circular litz wire coils to achieve an output power of 120 W and a high isolation voltage with a PDIV of 27 kV RMS in air only, along with a C_{ps} of 2.78 pF. Voltage transformer with a closed magnetic core is also commonly used in GDPS [10], [11]. Li et al.[10] proposed an isolated converter using silicone potting to reduce C_{ps}. A winding arrangement that significantly reduced the effective area between the coils and magnetic core, as well as between the primary and secondary coils, was suggested. This achieved a PDIV exceeding 15 kV RMS and a low C_{ps} of 1.03 pF, along with a compact structure. Additionally, a loosely coupled transformer (LCT) solution was presented in [12]. This solution used an isolation transformer with a magnetic core containing an air gap, employing insulated wires and layered insulation tape combined with silicone potting to improve the isolation capability. The PDIV test result was 20.6 kV RMS, with a low C_{ps} of 2.1 pF and a power output of 20 W. These studies have successfully balanced the isolation capability and parasitic capacitance of GDPS.

In addition to isolation capability and coupling capacitance as the primary design goals, recent years have seen increasing attention to multichannel GDPS, which are designed to supply multiple cells under different voltage potential or high voltage power semiconductor modules. Compared to single output, the high isolation and low CM current are harder to acquire in a small footprint, due to higher number of power channels. In [13] and [14], current transformers (CTs) are used, achieving high isolation performance and low capacitance. However, the E-field is highly sensitive to the transformer's geometry, and even slight misalignment of the primary conductor can reduce the PDIV. Additionally, this solution often requires a significant number of magnetic cores [15]. To maintain low capacitance

Received 10 December 2024; revised 25 February 2025; accepted 20 March 2025. Date of publication 25 March 2025; date of current version 26 May 2025. This work was supported in part by the National Key R&D Program of China under Grant 2024YFB4007504 and in part by the National Natural Science Foundation of China under Grant 52107179. Recommended for publication by Associate Editor S. Mekhilef. *(Corresponding author: Hao Feng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3554718.

Digital Object Identifier 10.1109/TPEL.2025.3554718

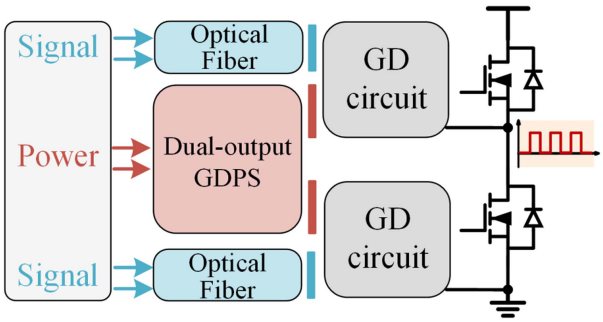

Fig. 1. Half-bridge circuit structure with proposed GDPS.

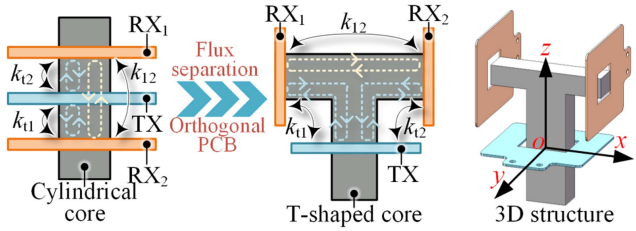

Fig. 2. Evolution process from cylindrical core to T-shaped core and the 3D structure of the proposed transformer.

while achieving a compact size and high voltage isolation, Nguyen and Gohil [16] proposes a coreless WPT method that enables a dual-channel output. However, due to the low coupling factor, it requires an ultra-high operating frequency of 4 MHz, which results in substantial converter loss and makes it difficult to increase the output power. Anurag and. Barbosa [17] propose an improved scheme by incorporating a cylindrical magnetic core. The core of such a structure is easy to fabricate, with PDIV test showing a maximum value of 15 kV. Due to the large overlapping area and the use of high dielectric constant materials, the coupling capacitance is comparatively high. Additionally, the presence of the cylindrical magnetic core results in a strong cross-coupling between the two secondary coils, causing mutual interference and preventing independent outputs. Li et al. [18] discusses decoupling methods for crosstalk. This issue requires thorough consideration in scenarios where coupling cannot be ignored. So far, research on multichannel GDPS remains relatively limited, particularly regarding alternative solutions beyond the CT, which are worth further exploration. In addition, for the system connected to 10 kV utility or above, the PDIV of isolation unit should be at least 18.75 kV, not to mention the PWM waveform imposed by power electronics [19]. However, the isolation capability of current multichannel GDPS systems is mostly insufficient to fulfill this standard.

A typical half-bridge circuit with high-isolation GDPS is shown in Fig. 1. In summary, the design of multichannel GDPS needs to consider the following requirements.

1) *High Isolation Capability*: This capability should encompass not only the isolation between the primary and secondary coils but also between different secondary coils.
2) *Low Coupling Capacitance*: To improve CMTI, the coupling capacitance between primary and secondary side should be as low as possible.
3) *Symmetric Magnetic Path*: To ensure that the output characteristics of different secondary sides are consistent, the coupling paths between primary and each secondary side should be symmetric.
4) *Minimal Cross-Coupling*: The cross-coupling between multiple secondary coils can be significant given certain core and winding arrangement. This results in the outputs of different channels affecting each other.

To meet the above requirements, this article proposes a customized T-shaped transformer to enhance isolation performance. Its tunable flux path and orthogonal printed circuit board (PCB) arrangement enables a major coupling capacitance reduction, while the compact geometry and inherent limited space between coils leads to a high E-field. To address the isolation issue, E-field grading and containment are made by adjusting the winding arrangement. Additionally, this article optimizes the geometry of magnetic core to achieve a tradeoff among multiple objectives. Experimental results show a PDIV of 30 kV RMS, and a coupling capacitance of 2.65 pF derived from CM current measurement. Finally, the proposed isolation unit is substituted into the dual-output 40 Watts GDPS to feed a SiC half bridge. Each channel independently achieves a quasi-constant voltage owing to the proposed circuit decoupling scheme, and operate stably at switching speeds of up to 180 kV/μs.

II. Design of Isolation Transformer

A. Magnetic Core Structure

In this article, an LCT structure with a magnetic core is adopted. Fig. 2 illustrates the cylindrical core isolation transformer [17], and the proposed T-shaped isolated transformer is motivated by two key principles. First, to minimize cross-coupling, the flux path between two receiver RX_1 and RX_2 should be separated from the main flux path. Second, direct overlapping between *TX* and *RX* increases the coupling capacitance. Orthogonal placement of the coils can significantly reduce the overlapping area, which is advantageous for reducing capacitance.

Meanwhile, the T-shaped core also retains the fully symmetrical magnetic circuit. The coupling factors can be represented by

$$k_{ij} = \frac{M_{ij}}{\sqrt{L_i L_j}} i, j = \mathrm{t}, 1\mathrm{or}2. \tag{1}$$

where the major coupling factors between *TX* and *RX* are defined as k_{t1} and k_{t2}, and the cross-coupling factor between RX_1 and RX_2 are defined as k_{12}.

The coil positions significantly influence both the major and cross-coupling factors. As shown in Fig. 3(a) and (b), when the *TX* coil moves upward along the z-axis, k_{t1} increases, and a same trend is observed for k_{t2}. Conversely, when the RX_2 coil moves outward along the x-axis, k_{12} decreases, while RX_1 and RX_2 remain symmetrically positioned about the x-axis. To minimize the cross-coupling factor without significantly reducing the major coupling factor, the *TX* coil is placed at the origin

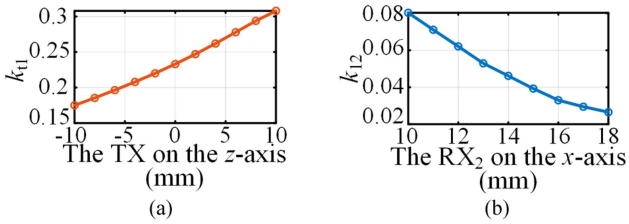

Fig. 3. (a) Variation of the coupling factor with the *TX* position along the *z*-axis. (b) Variation of the cross-coupling factor with the *RX* position along the *x*-axis.

TABLE I
KEY PARAMETERS IN E-FIELD FEM SIMULATION

Parameters	Value
FR4 dielectric strength[20]	45 kV/mm
FR4 relative dielectric constant[20]	4.6
Silicone dielectric strength[21]	25 kV/mm
Silicone relative dielectric constant[21]	2.8
T core potential in the FEM simulation	floating
TX potential in the FEM simulation	0 V
RX potential in the FEM simulation	20 kV

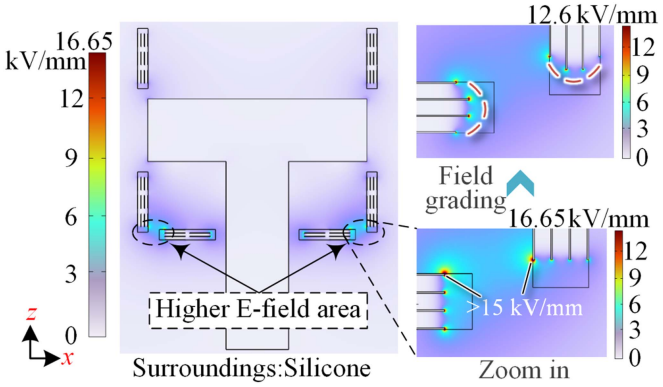

Fig. 4. E-field distribution of local high-field regions before and after applying field grading along the coil boundary (*xz* cross-section).

in the center of the core's lower section, and RX_1 and RX_2 are positioned symmetrically at the ends of the core's upper section.

B. Boundary Electric Field Grading

To ensure compactness and a sufficient coupling factor, the small clearance between *TX* and *RX* results in a high E-field. The E-field simulation settings are detailed in Table I.

To mitigate the E-field stress on the PCB, field grading is employed. Fig. 4 shows the E-field distribution of the *xz* cross-section in the T-shaped transformer, where the E-field stress is concentrated at the junction between *TX* and *RX*. By applying curvature to the copper's edges, the E-field becomes more uniform. The copper layer boundary settings are detailed in Fig. 5. Through parameter optimization, $E_{\max}$ is reduced from 16.65 kV/mm to 12.6 kV/mm, with optimal boundary offsets of 0.4 mm for *TX* (Δd_{TX}) and 0.5 mm for *RX* (Δd_{RX}).

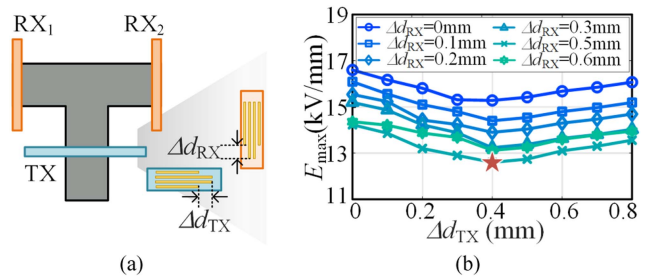

Fig. 5. (a) Coil boundary distance for *TX* (Δd_{TX}) and *RX* (Δd_{RX}). (b) Scanning results of E-field strength at PCB boundaries with different Δd_{TX} and Δd_{RX}.

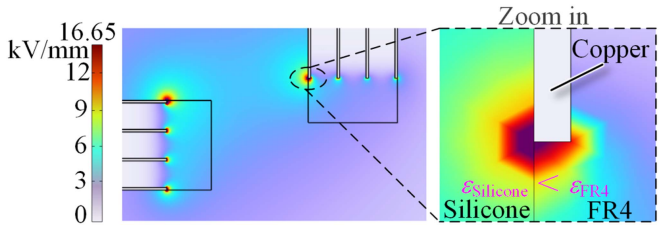

Fig. 6. E-field distribution near the triple point.

C. Solution of Triple Point Issue

There have been documented cases of surface insulation breakdown on PCBs [22]. As shown in Fig. 6, severe E-field distortion at the triple point is the cause of surface insulation failure. The E-field strength in these areas is several times higher than in unaffected areas. Due to the lower dielectric constant of silicone compared to FR4, the E-field in the silicone at the interface is higher. Additionally, the sharp geometry of the copper layer further exacerbates the E-field distortion.

Conventional methods for mitigating triple-point effects are the use of a semiconductive shielding layer [23]. However, the shielding layer poses challenges related to eddy current losses. To effectively address the triple point issue, this article proposes to transfer the high E-field from silicone to FR4.

As given in Table I, FR4 has better insulation performance and is more suitable for withstanding higher voltage stress than silicone. Moving the copper from PCB's outer layer to inner layer reduces $E_{\max}$ within the silicone, as shown in Fig. 7(a) and (b). The E-field in the silicone is notably decreased accompanied with the removal of the triple point. Although the tip of the copper still experiences high E-field, this can be tolerated for FR4.

Therefore, the position of the highest E-field is transferred from the silicone (lower dielectric strength) to the FR4 (higher dielectric strength). To better compare the isolation capability of two structures, partial discharge (PD) test will be conducted subsequently.

III. MULTIOBJECTIVE TRADE-OFFS ON GEOMETRY

A. Design Considerations

According to Section I, the GDPS for MV SiC MOSFET half-bridge should meet the following design requirements: high isolation capability; low coupling capacitance; a sufficient

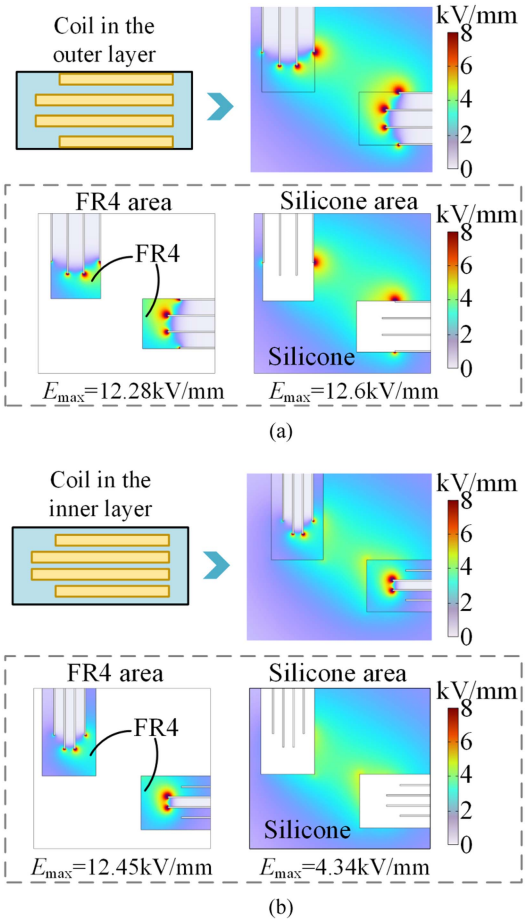

Fig. 7. Comparison of coil placement in the outer and inner the layers. (a) E-field distribution in FR4 and silicone areas when coil placement in the outer layer of PCB. (b) E-field distribution in FR4 and silicone areas when coil placement in the inner layers of PCB.

major coupling factor; and a compact footprint. Additionally, in single-core multichannel GDPS designs, the cross-coupling factor should be minimized. Since conflicts may exist between objectives, a multiobjective optimization process that accounts for all requirements is necessary.

B. Multiobjective Optimization

Several assumptions are made prior to optimization. The operating frequency is set to 1 MHz. When both *TX* and *RX* coils consist of four copper layers, the optimal copper thickness is 35 μm. The relationship between ac resistance and copper thickness can be evaluated using the Dowell formula [24].

Before simultaneously optimizing these parameters, the core geometry is defined, as shown in Fig. 8(a). Detailed parameters are given in Table II.

Among the four parameters of the core, l_u and l_l have the most significant on GDPS, as they directly determine the relative position of coils. Therefore, they are selected as variables for multiobjective optimization, providing the magnetic core with a high degree of tunability.

In contrast, w_u and w_l have a comparatively smaller effect on the E-field and are predefined to limit the number of optimization

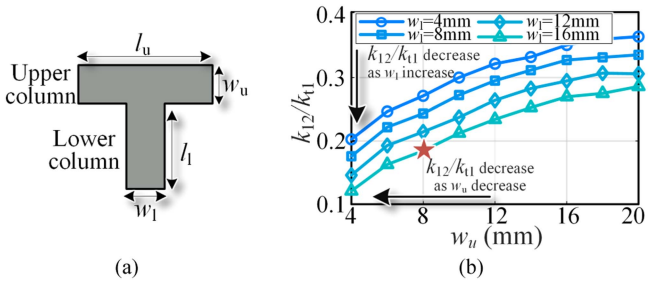

Fig. 8. (a) Diagram of magnetic core structural parameters. (b) Impact of w_u and w_l on k_{12}/k_{t1}.

TABLE II
SCAN PARAMETER SETTINGS

Parameters	Value
Copper thickness t_{copper}	35 μm
Upper column width w_u	8 mm
Lower column width w_l	16 mm
Column thickness t	10 mm
Upper column length l	30 mm – 80 mm
Lower column length l_l	20 mm – 70 mm

variables. Combined with the flux path distribution shown in Fig. 2, it can be concluded that increasing w_u will result in a larger M_{12} between RX_1 and RX_2, and increasing w_l will increase M_{t1} between TX and RX_1. This suggests that selecting a smaller w_u and a larger w_l can improve the primary coupling factor while reducing the cross-coupling factor. To quantify this effect, a parameter sweep is performed on w_u and w_l, using k_{12}/k_{t1} as the dependent variable in COMSOL simulations. The results are shown in Fig. 8(b), and we choose to set w_u to 8 mm and w_l to 16 mm. Further reduction in w_u is excluded due to excessively low coupling factor and increased manufacturing difficult.

As shown in Fig. 9, the optimization process consists of the following steps.

1) Perform magnetic and electric field simulations by sweeping all variables while keeping fixed parameters unchanged.
2) Extract key optimization metrics, including the maximum E-field strength $E_{\max}$ and coupling capacitance $C_{\rm ps}$ from the E-field simulation, as well as the coupling factor k_{t1} and cross coupling factor k_{12} from the magnetic field simulation.
3) Define the constraint range based on the parameter sweep results, ensuring the core volume V remains below 25 cm^3 and the ratio k_{12}/k_{t1} stays under 0.26. This constraint is crucial, as excessive cross-coupling can introduce significant mutual inductance between secondary coils, potentially reducing efficiency and causing voltage instability in constant-voltage output systems.
4) Identify feasible design points that satisfy $k_{t1} > 0.15$ while minimizing both $E_{\max}$ and $C_{\rm ps}$. The selected parameter set defines the final magnetic core structure.

The parameter scanning result is shown in Fig. 10 against the maximum E-field $E_{\max}$, coupling capacitance C_{ps} and k_{t1}/k_{12}, where the core lengths are converted into the core volume V.

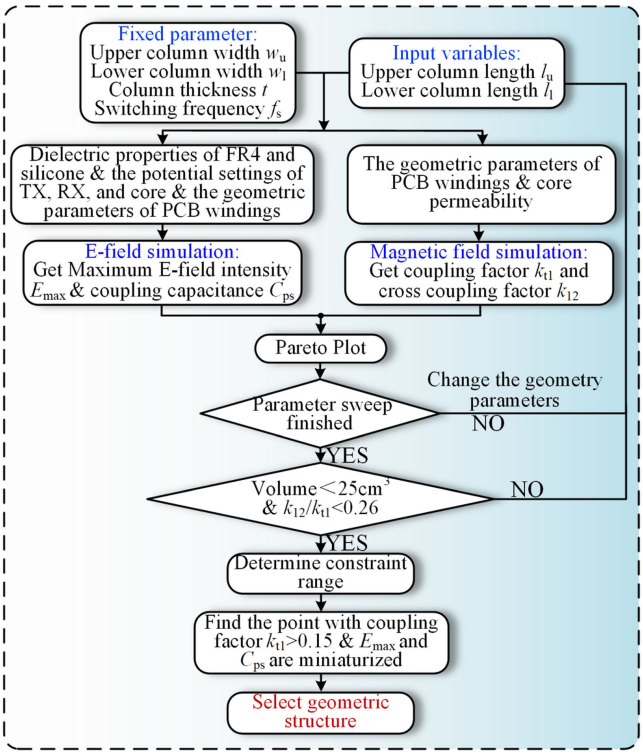

Fig. 9. Flowchart of multiobjective optimization.

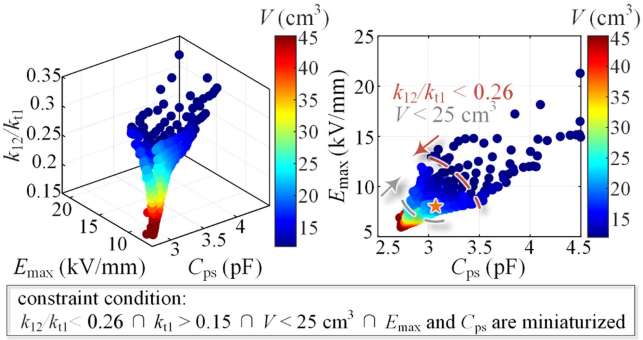

Fig. 10. Multiobjective optimization results.

Ultimately, after balancing multiple objectives, a core structure is chosen with an upper column length l_u of 45 mm and a lower column length l_l of 45 mm.

IV. Decoupling Method

A. Topology Selection

In a multichannel GDPS with a single magnetic core, cross-coupling between multiple receiving coils noticeably affects their output independence. Previous sections have proposed using a centralized core and coils to realize multioutputs. As a result, the cross-coupling is reduced, though a small portion remains. It is expected that the impact of cross-coupling is eliminated so that output voltage and power of each channel are self-governed. Moreover, the output voltage is preferred constant to further generate gate voltage. Hence, this section proposes

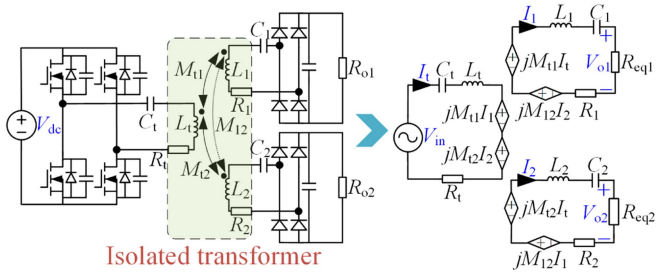

Fig. 11. Proposed dual-output GDPS topology and its equivalent circuit.

a dedicatedly tuned network to achieve nearly decoupled and constant output voltage under open-loop condition.

B. Decoupling Parameter Calculation

The proposed dual-output GDPS topology and its equivalent circuit is shown in Fig. 11. The input voltage V_{in} and the equivalent load R_{eq} are represented as

$$V_{in} = \frac{2\sqrt{2}}{\pi} V_{dc} \tag{2}$$

$$R_{eqi} = \frac{8}{\pi^2} R_{oi} i = 1, 2. \tag{3}$$

According to KCL and KVL, loop equations can be given as

$$\begin{bmatrix} V_{in} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Z_t & j\omega M_{t1} & j\omega M_{t2} \\ j\omega M_{t1} & Z_1 + R_{eq1} & j\omega M_{12} \\ j\omega M_{t2} & j\omega M_{12} & Z_2 + R_{eq2} \end{bmatrix} \begin{bmatrix} I_t \\ I_1 \\ I_2 \end{bmatrix} \tag{4}$$

where Z_t, Z_1, and Z_2 represent the equivalent impedances of the *TX* and each *RX*

$$Z_i = j\omega L_i + \frac{1}{j\omega C_i} + R_i i = t, 1 \text{or} 2. \tag{5}$$

The expressions for the output voltage gain are as follows:

$$G_{vi} = \left| \frac{V_o}{V_{in}} \right| = \left| \frac{I_i R_{eqi}}{V_{in}} \right|, i = 1, 2. \tag{6}$$

Substituting (4) into (6) yields the gain expression for the two channels

$$\begin{cases} G_{v1} = \left| \frac{\omega R_{eq1} (\omega M_{12} M_{t2} + j M_{t1} R_{eq2} + j M_{t1} Z_2)}{\omega^2 A + B} \right| \\ G_{v2} = \left| \frac{\omega R_{eq2} (\omega M_{12} M_{t1} + j M_{t2} R_{eq1} + j M_{t2} Z_1)}{\omega^2 A + B} \right| \end{cases} \tag{7}$$

where

$$\begin{cases} A = R_{eq2} + M_{t2}^2 R_{eq1} + M_{t1}^2 Z_2 + M_{t2}^2 Z_1 + M_{12}^2 Z_t \\ \quad -2j\omega M_{12} M_{t1} M_{t2} \\ B = R_{eq1} R_{eq2} Z_t + R_{eq2} Z_1 Z_t + R_{eq1} Z_2 Z_t + Z_1 Z_2 Z_t \end{cases}.$$

According to (7), it can be observed that G_{v1} and G_{v2} are related to the impedances (Z_1 Z_2 Z_t) and equivalent load resistance (R_{eq1} R_{eq2}). The interaction between voltage gains against load conditions can be attenuated by tuning resonant capacitors.

The parameter selection is described by Fig. 12. First, the load range and key parameters are defined. Then, a variety of capacitance is substituted into the gain expression in (7) and

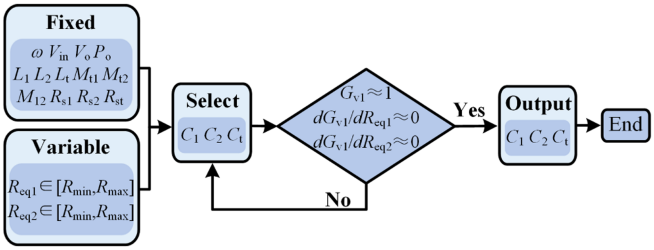

Fig. 12. Decoupling parameters scanning block diagram.

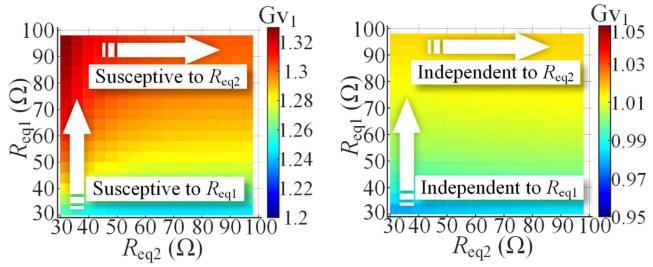

Fig. 13. Gain-Load relationship. (a) Before decoupling. (b) After decoupling.

the partial derivative expression with respect to the load. The decoupling parameters C_t, C_1 and C_2 can be concluded by repeating following process until the criteria are met.

Fig. 13(a) and (b) illustrates the impact of R_{eq1} and R_{eq2} on G_{v1}. The decoupling scheme renders G_{v1} almost immune from the load variation. G_{v2} demonstrates analogous trend due to symmetric receivers, and thus will not be discussed further.

V. Coupling Capacitance Estimation

A. Improved Coupling Capacitance Evaluation Method

The CM current across the isolation barrier causes malfunction on signal side and affect power operation in turn [25]. In Section III, the coupling capacitance has already been included in the multiobjective optimization. This section will focus on the modeling of CM current paths and proposes a method to estimate the coupling capacitance.

Direct measurement of CM current in gate driver designs poses significant challenges. To address this, the Z_M detection impedance method is employed [26]. As illustrated in Fig. 14(a) and (b), path 1 represents a traditional half-bridge, while path 2 corresponds to the half-bridge powered by the proposed GDPS. The Z_M detection impedance, consisting of a 1 nF capacitor in parallel with a 10 MΩ resistor, is placed between SGND and PGND. This configuration ensures Z_M has significantly lower impedance than lower-arm impedance Z_L. The 1 nF capacitance is much larger than the coupling capacitance of the isolated gate driver power supply (typically less than 10 pF), and the resistor simulates the impedance between the two grounds.

Conventional methods estimate the coupling capacitance C_{ps} using the peak values of i_{CM} and an approximated dv/dt. However, this approach is prone to inaccuracies due to sensitivity to experimental noise and transient anomalies. Additionally,

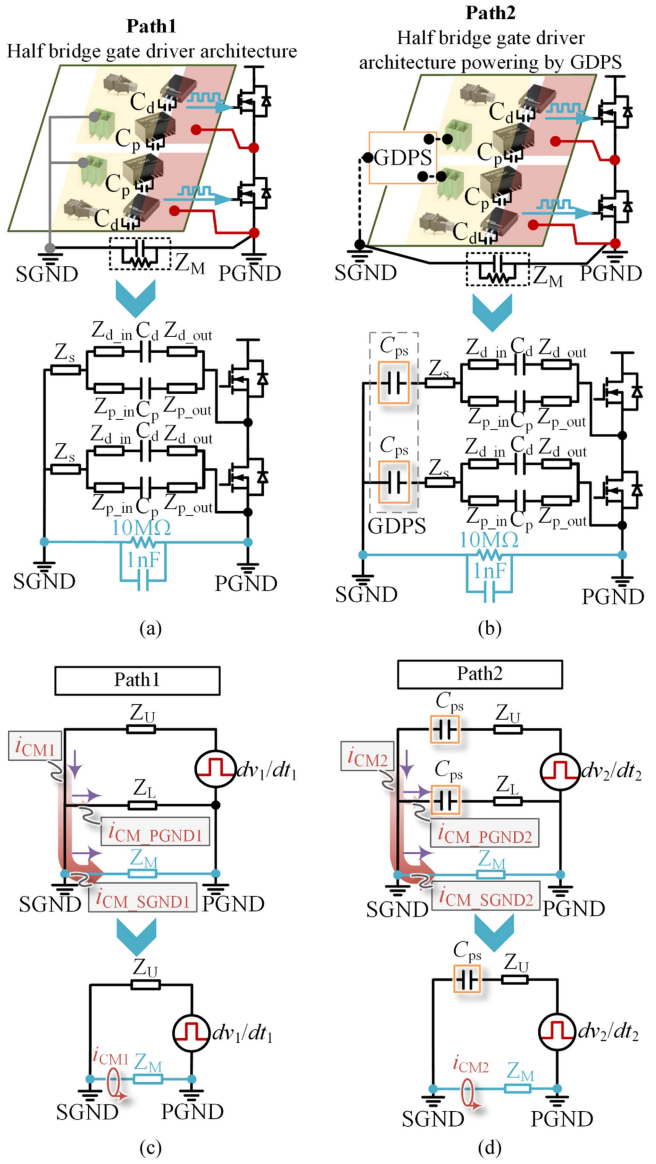

Fig. 14. Gate driver power architecture, illustrating different grounds, the PWM signal and the isolation barrier, along with their equivalent CM paths. (a) Path 1: A typical half-bridge. (b) Path 2: A half-bridge powered by the proposed GDPS. (c) Equivalent circuit corresponding for path 1. (d) Equivalent circuit corresponding for path 2.

isolated DC/DC regulators and PCB parasitic parameters can distort C_{ps} evaluation, as observed in prior studies [13], [17], [27].

To mitigate these limitations, this work adopts a time-domain integration-based approach. First, dv_1/dt_1 is measured using a standard SiC half-bridge [path 1, Fig. 14(a)], and the CM current i_{CM1} is measured by the Z_M impedance method. Next, the proposed GDPS is integrated into the gate driver side of the SiC half-bridge [path 2, Fig. 14(b)], and both dv_2/dt_2 and i_{CM2} are measured under identical conditions. Since most of the CM current flows through Z_M, the equivalent circuits for both paths can be simplified as shown in Fig. 14(c) and (d). The primary distinction between path 1 and path 2 is the introduction of the coupling capacitor C_{ps} by the GDPS. By defining the

TABLE III
PARASITIC PARAMETERS OF HF EQUIVALENT CIRCUIT IN FIG. 14

Symbol	Description	Value
Z_{d_in}	Input impedance of the gate driver IC	43.12 nH
C_d	Isolation capacitance of the gate driver IC	1.2 pF
Z_{d_out}	Output impedance of the gate driver IC	2.1 nH
Z_{p_in}	Input impedance of the DC/DC regulator	46.56 nH
C_p	Isolation capacitance of the DC/DC regulator	3.5 pF
Z_{p_out}	Output impedance of the DC/DC regulator	5.45 nH
Z_s	Parasitic impedance from SGND to devices	120 nH
Z_M	Impedance is added to measure the CM current	1nF//10 MΩ
i_{CM}	The total CM current	-
i_{CM_SGND}	CM current flowing into the signal ground	-
i_{CM_PGND}	CM current flowing into the power ground	-

equivalent capacitances for path 1 and path 2 as C_{Path1} and C_{Path2}, respectively, they can be expressed as.

$$C_{\text{Path1}} = \frac{i_{\text{CM1}}}{dv_1/dt_1} \tag{8}$$

$$C_{\text{Path2}} = \frac{i_{\text{CM2}}}{dv_2/dt_2}. \tag{9}$$

Time domain integration of i_{CM1} and i_{CM2} yields

$$C_{\text{Path1}} = \frac{\int i_{\text{CM1}}dt}{\Delta v_1} \tag{10}$$

$$C_{\text{Path2}} = \frac{\int i_{\text{CM2}}dt}{\Delta v_2}. \tag{11}$$

Given that C_{Path2} is equivalent to C_{Path1} in series with C_{ps}, the coupling capacitance C_{ps} can be derived as

$$C_{\text{ps}} = \frac{\frac{\int i_{\text{CM1}}dt}{\Delta v_1} \cdot \frac{\int i_{\text{CM2}}dt}{\Delta v_2}}{\frac{\int i_{\text{CM1}}dt}{\Delta v_1} - \frac{\int i_{\text{CM2}}dt}{\Delta v_2}}. \tag{12}$$

This approach differs from the conventional peak-based method by using the time-domain integral of i_{CM} and Δv_{ds}, removing reliance on error-prone peak values or approximated *dv/dt*. By integrating over the transient period, it reduces noise and transient effects. Additionally, it mitigates the impact of PCB parasitics and isolation units, leading to a more accurate and reliable estimation of C_{ps}.

B. Verification of Z_M Detection Method

Parasitic parameters and corresponding simulation results are given in Table III. Circuit impedance is extracted using ANSYS Q3D, while isolation capacitances for the driver IC and dc/dc regulator are obtained from datasheets. Ground connections and isolation components in a typical half-bridge configuration are depicted in Fig. 14(a).

Incorporating these parameters into LTspice allows simulations to evaluate whether the Z_M detection impedance method accurately captures total CM current. As illustrated in Fig. 15, the $i_{\text{CM\_SGND1}}$ waveform closely aligns with that of i_{CM1}, confirming the efficacy of the Z_M impedance approach.

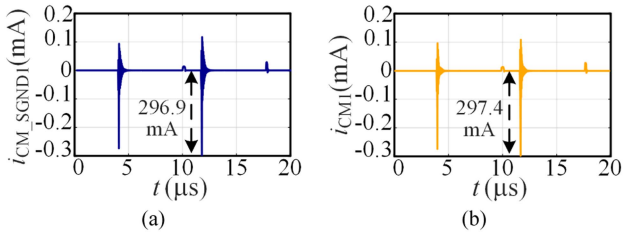

Fig. 15. (a) Simulated $i_{\text{CM\_SGND1}}$ in Fig. 14(c). (b) Simulated i_{CM1} in Fig. 14(c). The simulation is performed in LTspice with a voltage excitation of 1500 V and a switching slew rate of up to 57 kV/μs.

TABLE IV
CIRCUIT AND ISOLATED TRANSFORMER PARAMETERS OF GDPS

Coils	Parameters	Value
*T*x coil	Number of copper layers	4
	Number of turns	6
	Inductance L_t	3.93 μH
	Compensation capacitance C_t	7.9 nF
*R*x coil	Number of copper layers	4
	Number of turns	12
	Inductance L_1 L_2	6.38 μH
	Compensation capacitance C_1 C_2	4.9 nF
-	Mutual inductance M_{t1} M_{t2}	1.2 μH
-	Mutual inductance M_{12}	0.375 μH
-	Coupling factor k_{t1} k_{t2}	0.24
-	Cross coupling factor k_{12}	0.059
-	Core material	DMR51W
-	Switching device	EPC2218A
-	Switching frequency f_s	1 MHz
-	Output power P_{out}	>20 W
-	Output voltage V_{out}	(0.9−1.1)24
-	PDIV (T=25 °C, P= 101.3 kPa)	30 kV RMS
-	Coupling capacitance C_{ps}	2.65 pF

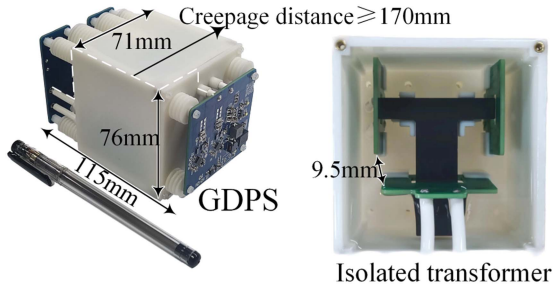

Fig. 16. Proposed GDPS and critical dimensions.

VI. EXPERIMENTAL VERIFICATION

A. Circuit Design and Output Function Verification

The circuit and isolated transformer parameters of the proposed GDPS are given in Table IV and the prototype is shown in Fig. 16. In accordance with IEC 61800-5-1: 2007, which requires a creepage distance of 125 mm for 25 kV RMS considering material group I and pollution degree 2, the prototype has achieved at least 170 mm. The GDPS dimensions are 115 mm × 71 mm × 76 mm (including the power unit and isolation unit).

Fig. 17(a) presents the efficiency curves as a function of output power, achieving a peak efficiency of 82% at 43.8 W. Fig. 17(b) illustrates the output voltage and power characteristics of the

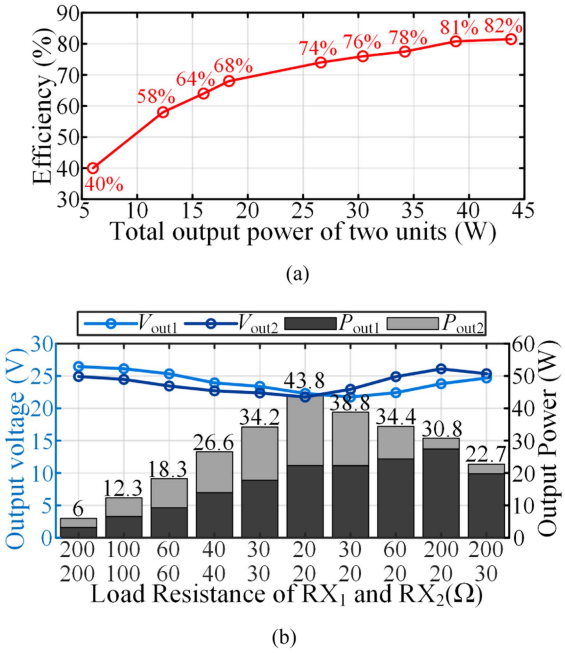

Fig. 17. (a) GDPS efficiency versus output power. (b) Output voltage and power versus load for both channels.

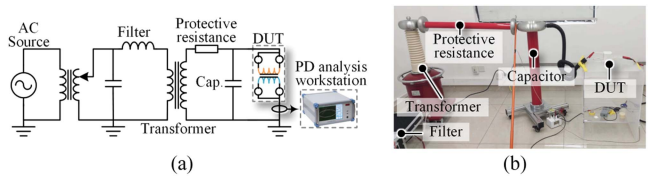

Fig. 18. (a) Schematic diagram of PD test. (b) PD test setup.

dual output channels under varying load conditions. The results demonstrate that the output voltage remains stable within 24V $\pm$ 10% regardless of load variations, satisfying the narrow input range requirements of the dc/dc regulator. Additionally, when operating across the full load range, the output power of each channel is primarily determined by its respective load, with a single channel capable of delivering over 20 W. These findings indicate that the proposed GDPS achieves mutual decoupling between the two channels and provides a nearly constant voltage output.

B. Isolation Capability Tests

To verify the isolation capability of the GDPS, PD tests are conducted, as illustrated in Fig. 18. The first set of experiments aims to demonstrate how placing the copper on the inner layers reduces the electric field strength. The experimental results in Fig. 19(a) and (b) align with the design in Fig. 7(a), while Fig. 19(c) and (d) corresponds to Fig. 7(b).

In Fig. 19(a), no obvious PD is detected at an applied voltage of 24 kV RMS, but PD initiation occurs when the voltage increases to 24.6 kV RMS, as shown in Fig. 19(b). However, when the copper layer is placed on the inner layer, PD effects only become apparent at a higher voltage of 31 kV RMS, as illustrated in Fig. 19(c) and (d). These results demonstrate that

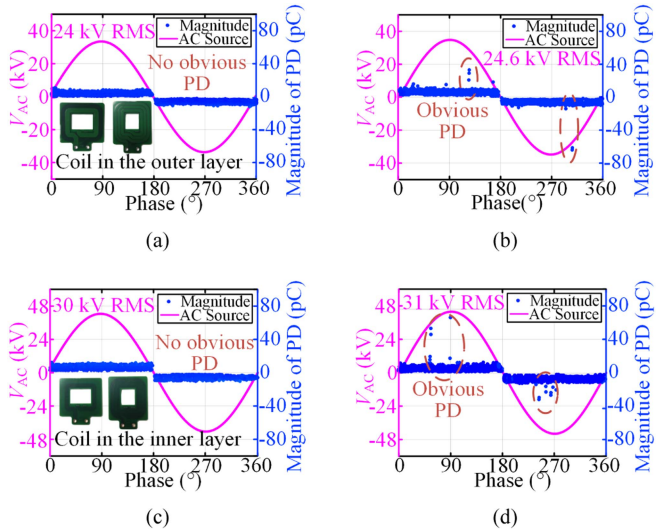

Fig. 19. PD test results between *TX* and *RX* coils. (a) Applied voltage is 24 kV RMS (coil in the outer layer). (b) Applied voltage is 24.6 kV RMS (coil in the outer layer). (c) Applied voltage is 30 kV RMS (coil in the inner layer). (d) Applied voltage is 31 kV RMS (coil in the inner layer).

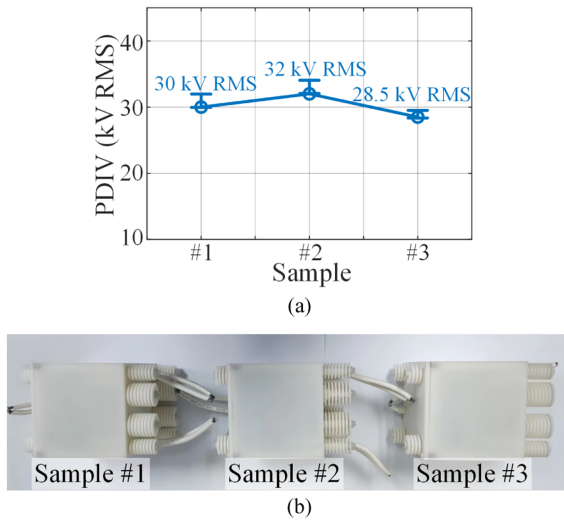

Fig. 20. (a) PD test results for the three samples. (b) Prototypes of the three samples.

the inner-layer copper configuration enhances isolation capability. Notably, a PDIV of 30 kV RMS is achieved between *TX* and *RX* with a separation distance of only 9.5 mm, highlighting the effectiveness of the proposed design. Additionally, repetitive PD tests further verify the robust high isolation capability of the proposed GDPS. As shown in Fig. 20, representative PD test results indicate that the PDIV of three samples exceeds 28.5 kV RMS.

Previous literature has primarily focused on the PDIV between *TX* and *RX*, while the isolation between the two *RX*s in a dual-output GDPS has been largely overlooked. By placing the copper layers on the inner layer of the PCB, the experimental results demonstrate a PDIV of 35 kV RMS, as shown in Fig. 21. This improved isolation voltage is attributed to the increased distance between RX_1 and RX_2.

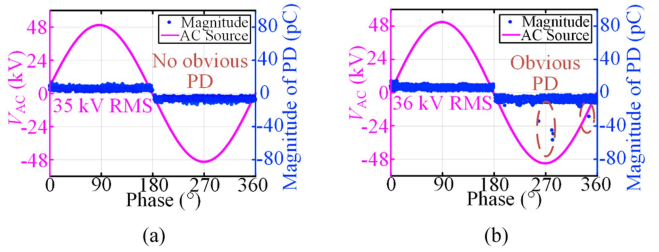

Fig. 21. PD test results between RX_1 and RX_2 coils. (a) Applied voltage is 30 kV RMS (coil in the inner layer). (b) Applied voltage is 31 kV RMS (coil in the inner layer).

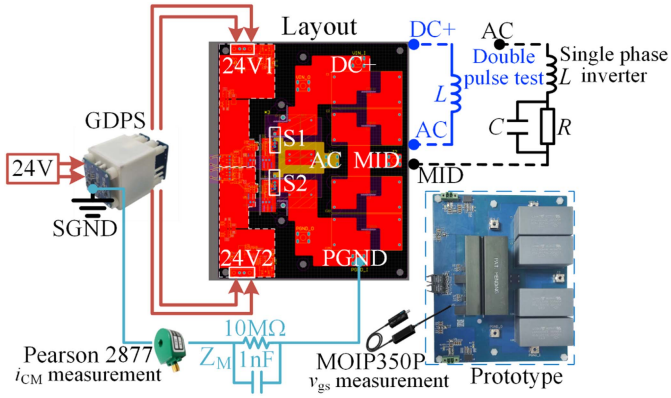

Fig. 22. Setup for multipulse test and single-phase inverter test.

C. Multipulse Test and Continuous Operation Test

The coupling capacitance of GDPS and its continuous operation capability are verified on a half-bridge prototype, as shown in Fig. 22. Utilizing the 3.3 kV SiC MOSFET MSC080SMA330B4 from Microchip [28], the setup can be configured as a multipulse test platform or a single-phase inverter. Optical isolated probes are employed for v_{gs} measurement to avoid introducing additional CM interference, while an high-frequency current transformer (HFCT) is selected for i_{CM} measurement due to its high-frequency, noninvasive, and sensitive characteristics.

The coupling capacitance of the proposed GDPS is evaluated through a multipulse test. The experiments show that when the external gate resistance $R_{g,ext}$ is set to 12 Ω, the amplitude of i_{CM1} reaches 426 mA at a dv_1/dt_1 rate of 65.4 kV/μs, while i_{CM2} peaks at 135 mA with a dv_2/dt_2 rate of 68.8 kV/μs, as shown in Fig. 23(a) and (b). By integrating i_{CM} over time and substituting Δv_{ds} into (12), the calculated C_{ps} is found to be 2.65 pF, as illustrated in Fig. 23(c) and (d). Furthermore, by reducing the external gate resistance $R_{g,ext}$ to improve the switching speed, the results show that the proposed GDPS does not fail until $R_{g,ext}$ drops below 2 Ω, at which point the switching speed exceeds 180 kV/μs. It indicates that the proposed GDPS has a high CMTI. The multipulse waveforms at $R_{g,ext} = 2\,\Omega$ are shown in Fig. 24.

Moreover, during continuous operation, the proposed GDPS exhibits consistent and stable output performance, as illustrated in Fig. 25. Additionally, the 5V power supply on the signal

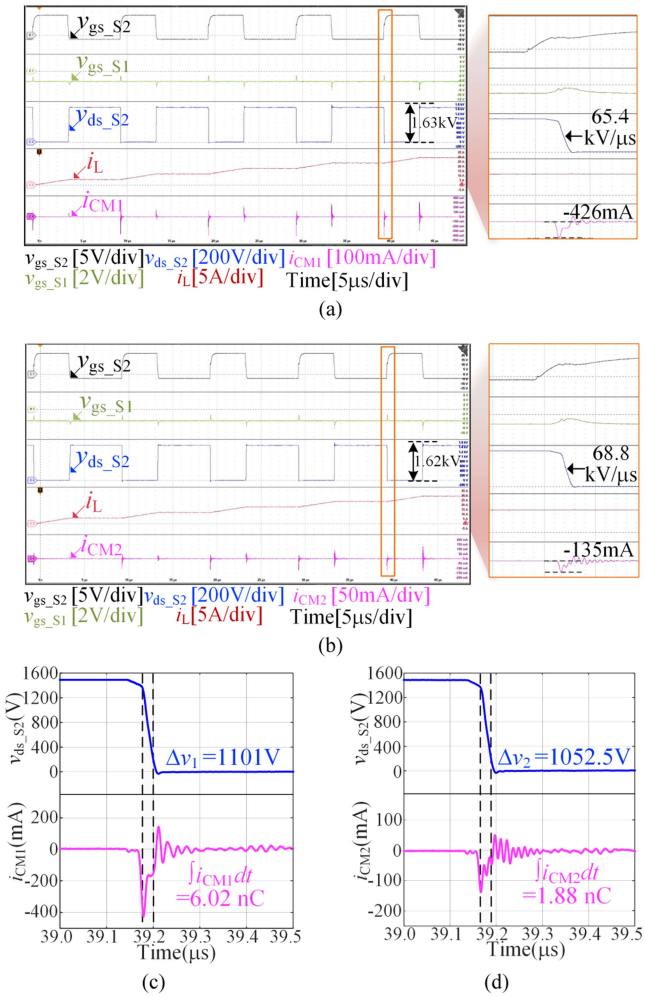

Fig. 23. Multipulse test waveforms at $R_{g,ext} = 12\,\Omega$. (a) CM current and slew rate measurements for path 1, showing $i_{CM1} = 426$ mA and $dv_1/dt_1 = 65.4$ kV/μs. (b) CM current and slew rate measurements for path 2, showing $i_{CM2} = 135$ mA and $dv_2/dt_2 = 68.8$ kV/μs. (c) Δv_1 and the time-domain integration of i_{CM1} in path 1. (d) Δv_2 and the time-domain integration of i_{CM2} in Path 2.

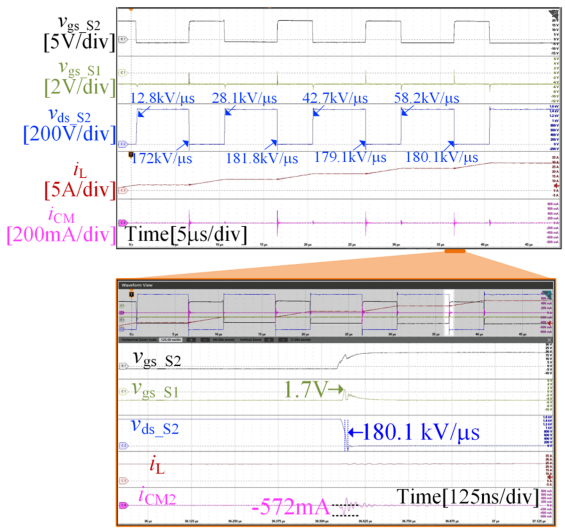

Fig. 24. Multipulse test waveforms at $R_{g,ext} = 2\,\Omega$, demonstrating a turn-OFF transient dv/dt of 180 kV/μs under 1500 V/25 A.

TABLE V
COMPARISON BETWEEN MULTICHANNEL GDPS

Institution	Scheme	PDIV (RMS)	Coupling capacitance	P_{out}	η_{max}	Channel numbers	Dimension of Isolation Barrier
CPES[14]	CT	11.6 kV	3.6 pF	4 × 20 W	NA	4	4π × 25 mm × 25 mm × 28 mm
UT Austin[15]	CT	4.6 kV	3 pF	4 × 10 W	72%	4	NA
UT Dallas[16]	WPT	NA	1.56 pF	2 × 4.25 W	47%	2	NA
MPEL Delta[17]	LCT	10.6 kV	5 pF	2 × 10 W	NA	2	40 mm × 35 mm × 35 mm
This article*	LCT	30 kV	2.65 pF	2 × 20 W	82%	2	70 mm × 71mm × 76 mm

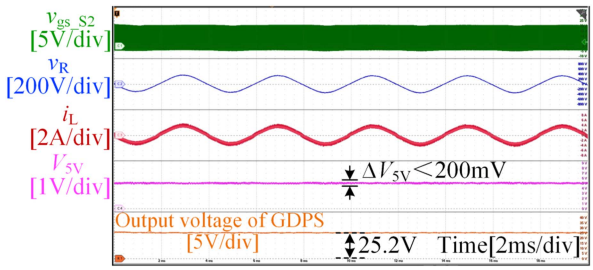

Fig. 25. Single phase inverter test waveform.

side consistently maintains a ripple below 200 mV during both turn-ON and turn-OFF events. This indicates that the CM current has negligible impact on the signal side.

D. Comparison With Existing Work

Existing multioutput GDPS solutions, including those designed for MV half-bridge applications, are summarized in Table V. The proposed GDPS in this article achieves superior isolation performance compared to CT-based solutions, higher power transfer capability than WPT-based designs, and significantly reduced coupling capacitance relative to other LCT solutions. Moreover, the achieved PDIV exceeds 18.75 kV (PD standard in 10 kV utility or above) with sufficient margin, representing an isolation level unmatched by existing multichannel GDPS. This article also ensures robust isolation capability between the two secondary coils, a critical yet often overlooked consideration in MV SiC MOSFET half-bridge applications.

VII. CONCLUSION

In this article, an isolation scheme and design method are proposed to fulfill the high isolation, low parasitics and multioutput capability for MV SiC MOSFET's gate driver power supply. To meet these demands, a T-shaped isolation unit is proposed for a SiC-based half-bridge. It integrates two output channels compactly without jeopardizing the isolation capacity. To achieve independent outputs for the two *RX* channels, a decoupling scheme is performed by properly tuning the resonant capacitor. The proposed solution reserves the potential for scaling up to higher number of outputs. Experiments show that the prototype achieves a PDIV of up to 30 kV RMS, a coupling capacitance of 2.65 pF, and an output power of 20 W per channel, while enabling independent constant voltage output on each *RX* channel under a limited footprint. Additionally, its CMTI is at least 180 kV/μs.

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