A Self-Regulating Active Gate Driver of Voltage Overshoot Suppression for SiC MOSFETs Under Variable Load Current Conditions

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***Abstract*—Compared to silicon-based devices, silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) can present faster switching speed and operate at higher switching frequency. However, the fast switching speed of SiC MOSFETs and the inevitable parasitic inductance in the power loop will cause the severe voltage overshoot during the device turn-OFF transient. And the peak value of the voltage overshoot increases with the load current, which will further aggravate the electromagnetic interference problem and considerably undermine the device reliability. In response to the above problems, this article proposes an active gate driver (AGD) with self-regulating functionality. The proposed AGD can not only quantitatively suppress the voltage overshoot under the variable load current conditions over time, but also has less effect on switching speed and switching loss. Through feedback and detection of the drain–source voltage $v_{\rm ds}$ and its rate of change $dv_{\rm ds}/dt$, the proposed method also achieves accurate identification of turn-OFF transient stage for the device. Furthermore, the proposed method can dynamically regulate the gate current of the device to control the $v_{\rm ds}$ overshoot with the set value. Finally, an experimental platform is designed to verify the proposed AGD scheme. Experimental results have shown that this method can achieve an optimal tradeoff between voltage overshoot and turn-OFF loss, and suppress the $v_{\rm ds}$ overshoot peak when the load current changes.**

***Index Terms*—Active gate driver (AGD), overshoot, SiC MOSFETs, switching loss.**

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I. Introduction

WIDE bandgap semiconductor power devices represented by silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFET) devices possess outstanding performance. Compared with silicon-based devices, SiC MOSFETs offer faster switching speeds, lower ON-resistance, and higher operating temperatures, and have found extensive application fields such as electric vehicles, new energy generation, and aerospace [1], [2], [3]. Nevertheless, the fast switching speed of SiC MOSFETs also brings about certain adverse effects. Due to the inevitable introduction of parasitic inductance during the layout of the power loop, the severe voltage overshoot occurs when SiC MOSFETs are turned OFF, and the peak value of the voltage overshoot is positively correlated with the load current magnitude [4]. Under high load current conditions, the voltage overshoot is extremely severe, which will significantly reduce the operating efficiency and reliability of SiC MOSFETs [5], [6].

At present, various approaches have been put forward to suppress the voltage overshoot during device turn-OFF transient, including increasing the gate resistance [7], optimizing the printed circuit board (PCB) layout [8], [9], adding snubber or damping circuits [10], [11], [12], and employing active gate driver. Increasing the gate resistance is one of the most common methods to suppress switching voltage overshoot. However, it will considerably reduce the device's switching speed and increase the switching losses. Optimizing the PCB layout to reduce parasitic inductance is an effective method to reduce switching voltage overshoot. However, this method is constrained by the device package, structure, and circuit board size, that has limited suppression effect. In practical applications, adding snubber circuit is also a frequently employed approach for suppressing voltage overshoot. Unfortunately, this method requires redesign of the snubber circuit parameters under various operating conditions such as different inputs or parameter changes, making it challenging to adapt to the changing operating conditions. By contrast, the active gate driver technology can dynamically adjust the driving parameters of devices to achieve flexible control of dv/dt, di/dt, current overshoot, and voltage overshoot during the device's switching process, which constitutes an effective means to enhance the performance of SiC MOSFETs [13].

Currently, numerous active gate drivers (AGDs) have been proposed to optimize the switching performance of power

TABLE I
COMPARISON TABLE OF THE PROPOSED AGD AND EXISTING AGD METHODS

Control method	References	Accurate modeling	*di/dt* independent regulation	Applicability of load variation conditions	Digital closed-loop control	Communication and computing delay	Target power device
Switching stage detection: open-loop Optimized target control: closed-loop	[14][16]	Yes	√	√	√	High	SiC MOSFET
	[19]	Yes	√	√	√	High	GaN FET
	[15]	Yes	√	√	√	High	SiC MOSFET
Switching stage detection: closed-loop Optimized target control: open-loop	[4]	Yes	√	×	×	\	SiC MOSFET
	[1][20][26]	No	√	×	×	\	SiC MOSFET
	[21]	No	√	√	×	\	IGBT
	[24][25][27]	No	√	√	×	\	SiC MOSFET
Switching stage detection: closed-loop Optimized target control: closed-loop	[28]	No	×	√	×	\	SiC MOSFET
	[22]	No	√	√	×	\	IGBT
	[23]	No	√	√	×	\	SiC MOSFET
	[31]	No	√	√	√	High	IGBT
	This paper	No	√	√	√	Low	SiC MOSFET

devices [1], [4], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31]. As shown in Table I, these methods can be categorized into three types based on the switching stage detection and optimization target control approaches: open-loop switching stage detection with closed-loop optimization target control, closed-loop switching stage detection with open-loop optimization target control, and closed-loop switching stage detection with closed-loop optimization target control. Among them, the open-loop switching stage detection methods are relatively straightforward in circuit design. First, an accurate model of the switching process is established, or a lookup table is created, and then fixed gate drive parameters are designed to optimize the device switching performance [14], [15], [16], [18], [19]. However, the precise modeling of the device poses significant difficulties, and the duration of the device switching transient varies with the load conditions, parasitic parameters, and device selection. The fixed gate drive parameters are difficult to meet the real-time changing conditions, that will result in the AGD not performing optimally.

Based on these, closed-loop switching stage detection methods that establish feedback loops for each stage of the device switching transient are proposed. For example, Camacho et al. [1] and Li et al. [20] directly detect the Miller plateau voltage of v_{gs} and indirectly identify the device switching transient stage through its transconductance. However, this method is prone to malfunction when the gate–source voltage oscillates, and its fixed parameters make it challenging to apply under varying operating conditions. For IGBT or SiC MOSFET modules, a method for identifying the switching transient stage by detecting the voltage at the Kelvin-packaged source (or emitter) and the *dv*/*dt* of the device is presented in papers [21], [22], [23]. However, discrete SiC MOSFETs have faster switching speeds, and the gate parameters may act at the wrong time due to the inherent delay of the AGD circuit. In [24], the integration of AGD circuits using the BCD (Bipolar-CMOS-DMOS) process is proposed, reducing the delay of the AGD effectively. However, this method incurs a high cost. In [4], [25], [26], and [27], by detecting v_{ds} or i_{d} and carefully designing the trigger threshold to activate the circuit in advance, the detection circuit delay of the AGD can be compensated, allowing for more accurate identification of the switching transient stage. Nevertheless, the trigger threshold design in [4] and [26] depends on the device's load current, making it difficult to identify the switching stage when the load current varies, accurately. In [22], [23], [28], and [31], closed-loop detection of the switching stage and closed-loop control of the optimization target are achieved. Among them, papers [22], [23], and [28] can adaptive adjustment of the driver parameters to control the *di*/*dt* and *dv*/*dt* of the device through an analog closed-loop control system implemented with high-bandwidth operational amplifiers. However, this method is inflexible in control, requires frequent hardware replacements during debugging, and is susceptible to interference. Furthermore, the method proposed in [28] regulates the turn-OFF speed during both the *dv*/*dt* and *di*/*dt* stages of the device, resulting in additional turn-OFF losses during the *dv*/*dt* stage. In [31], an AGD with self-regulating function for IGBTs is implemented, achieving digital closed-loop control with high reliability and flexibility. Nevertheless, this method requires costly FPGAs and DAC chips with high-speed communication capabilities. Due to communication delays, the optimal control effect may not be achieved under high-frequency operating conditions.

Based on the above analysis, it can be concluded that existing AGDs for voltage overshoot suppression are difficult to identify the transient stage of switching process under variable load current conditions, and there are challenges in dynamically regulating the degree of voltage overshoot suppression according to the load current. Therefore, this article proposes a self-regulating AGD of v_{ds} overshoot suppression for SiC MOSFETs, and the proposed method has the following advantages.

1) The detection circuit of the proposed AGD is independent of the load current magnitude and can accurately detect the current falling stage of the device even under varying load current conditions. Therefore, compared to conventional self-regulating drive methods, the proposed AGD can regulate the turn-OFF speed only during the current falling stage of the device turn-OFF process, thereby further reducing turn-OFF losses.

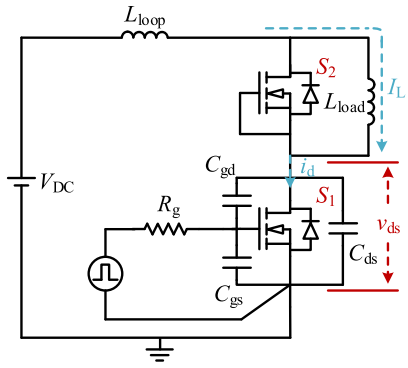

Fig. 1. Schematic diagram of the double pulse circuit.

TABLE II
PARAMETERS DESCRIPTION OF DOUBLE PULSE CIRCUIT

Parameters	Description
C_{gs}	Gate-source capacitance of S_1
C_{gd}	Gate-drain capacitance of S_1
C_{ds}	Drain-source capacitance of S_1
R_g	Gate resistance of S_1
L_{load}	Load inductance
L_{loop}	Loop parasitic inductance
V_{DC}	DC power supply
I_L	Load current of S_1
i_d	Drain current of S_1
v_{ds}	Drain-source voltage of S_1

2) The proposed AGD can dynamically regulate the gate drive current based on the magnitude of the device load current to keep the overshoot peak of v_{ds} within a set value.
3) Digital closed-loop control is achieved. Compared to traditional CPLD or FPGA solutions, the proposed AGD uses a low-cost microcontroller to implement closed-loop control. It integrates DAC and ADC peripherals and eliminates the communication delay between chips, which improves system integration and reduces costs. Additionally, the proposed method also offers stronger anti-interference capability and simplifies system debugging.

The rest of this article is structured as follows: in Section II, the turn-OFF characteristics of SiC MOSFETs are analyzed. Section III presents the principle of the proposed AGD and its hardware implementation. In Section IV, an experimental platform is established to validate the performance of the proposed AGD. Finally, Section V concludes this article.

II. TURN-OFF CHARACTERISTICS OF SIC MOSFETS

This section analyzes the turn-OFF characteristics of SiC MOSFETs using a double pulse circuit taking into account the parasitic parameters, as shown in Fig. 1. The parameters of the circuit are provided in Table II.

A. Analysis of the Turn-Off Characteristics of SiC MOSFETs

Fig. 2 illustrates the waveforms of the drain–source voltage (v_{ds}), drain current (i_d), and gate–source voltage (v_{gs}) during the

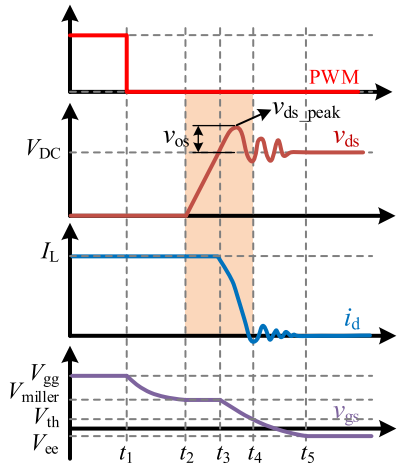

Fig. 2. Turn-OFF waveforms of SiC MOSFETs.

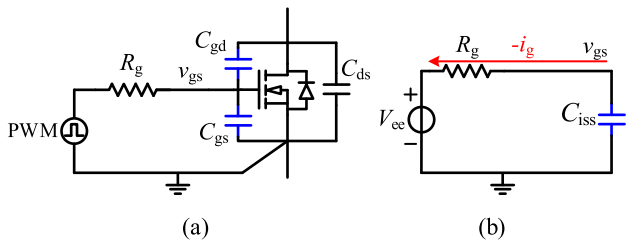

Fig. 3. Simplified circuit of the device driving loop during the i_d falling stage. (a) Driving circuit of the SiC MOSFET. (b) Simplified driving circuit during the i_d falling stage.

turn-OFF process of SiC MOSFETs. Typically, the device turn-OFF process is divided into four stages: the delay stage (t_1–t_2), the v_{ds} rising stage (t_2–t_3), the i_d falling stage (t_3–t_4), and the complete turn-OFF stage (t_4–t_5).

Stage 1: At t_1, the input signal pulsewidth modulation changes from high level to low level, causing the driving voltage of the driving chip to shift from positive driving voltage V_{gg} to negative driving voltage V_{ee}. Subsequently, the input capacitance C_{iss} ($C_{iss} = C_{gs}+C_{gd}$) discharges through the gate resistor R_g, resulting in a fall in v_{gs} until it reaches the Miller plateau voltage V_{miller}. During this stage, v_{ds} and i_d remain unchanged.

Stage 2: At t_2, v_{gs} drops to the Miller plateau voltage, at which time v_{ds} begins to rise. The rising rate of v_{ds} (dv_{ds}/dt) increases with the load current. The rate dv_{ds}/dt can be equated using (1), expressed as follows:

$$\frac{dv_{ds}}{dt}\,(\text{off}) = \frac{V_{th} + \frac{I_L}{g_m} - V_{ee}}{C_{gd}R_g} \tag{1}$$

where V_{th} represents the threshold voltage of SiC MOSFETs, I_L is the load current of the device, g_m is the transconductance of the device, and V_{ee} refers to the negative gate drive voltage of the device.

Stage 3: At t_3, v_{ds} rises to the bus voltage V_{DC}, i_d begins to fall, and the load current transfers to the freewheeling diode, and the device enters the saturation region. The driving circuit can be simplified to the circuit shown in Fig. 3, where v_{gs} falls

exponentially from the Miller plateau voltage V_{miller} until v_{gs} falls to threshold voltage V_{th}, at which point the device is fully turned OFF and i_{d} falls to 0 A. At this stage, the device can be modeled as a voltage controlled current source, and the falling rate of i_{d} is directly governed by v_{gs}. i_{d} can be calculated as follows:

$$i_{\mathrm{d}} = g_{\mathrm{m}}(v_{\mathrm{gs}} - V_{\mathrm{th}}). \tag{2}$$

Additionally, based on the circuit shown in Fig. 3, (3) and (4) can be derived as follows:

$$i_{\mathrm{g}} = C_{\mathrm{iss}}\frac{dv_{\mathrm{gs}}}{dt} \tag{3}$$

$$v_{\mathrm{gs}} = V_{\mathrm{ee}} - R_{\mathrm{g}}i_{\mathrm{g}}. \tag{4}$$

Based on (2), (3), and (4), the approximate expression for v_{gs} can be derived by the following:

$$v_{\mathrm{gs}} = V_{\mathrm{ee}} + (V_{\mathrm{miller}} - V_{\mathrm{ee}})e^{-\frac{t-t_3}{R_{\mathrm{g}}C_{\mathrm{iss}}}}. \tag{5}$$

The V_{miller}, is related to the load current I_{L}, as shown in (6). The larger the load current I_{L}, the greater the V_{miller}

$$V_{\mathrm{miller}} = \frac{I_{\mathrm{L}}}{g_{\mathrm{m}}} + V_{\mathrm{th}}. \tag{6}$$

Based on the relationship between i_{d} and v_{gs} from (2), i_{d} can be calculated as follows:

$$i_{\mathrm{d}} = g_{\mathrm{m}}\left[(V_{\mathrm{ee}} - V_{\mathrm{th}}) + (V_{\mathrm{miller}} - V_{\mathrm{ee}})e^{-\frac{t-t_3}{R_{\mathrm{g}}C_{\mathrm{iss}}}}\right]. \tag{7}$$

By differentiating (7), the maximum value of di_{d}/dt can be calculated as follows:

$$\frac{di_{\mathrm{d}}}{dt} = \frac{g_{\mathrm{m}}V_{\mathrm{ee}} - g_{\mathrm{m}}(I_{\mathrm{L}} + V_{\mathrm{th}})}{R_{\mathrm{g}}C_{iss}}. \tag{8}$$

It can be observed that di_{d}/dt is influenced by I_{L}, a large I_{L} will result in a high di_{d}/dt. Additionally, at this stage, the rapid fall in i_{d} induces a significant voltage drop across the parasitic inductance L_{loop} of the power loop. This voltage drop, combined with V_{DC}, generates a large voltage overshoot peak $v_{\mathrm{ds\_peak}}$ across the drain-source terminals of the device. The expression of $v_{\mathrm{ds\_peak}}$ can be given as follows:

$$v_{\mathrm{ds\_peak}} = V_{\mathrm{DC}} + L_{\mathrm{loop}}\left|\frac{di_{\mathrm{d}}}{dt}\right|. \tag{9}$$

Therefore, according to (9), the peak value of voltage overshoot $v_{\mathrm{ds\_peak}}$ increases with the increase of load current I_{L}.

Stage 4: At t_4, i_{d} reaches 0 A, and the input capacitor C_{iss} continues to discharge until t_5 when v_{gs} drops to the negative driving voltage and the device turn-OFF process ends.

In addition, as shown in Fig. 4, when the device is turned OFF, a turn-OFF loss E_{off} will occur in the overlap region between v_{ds} and i_{d}. For the same V_{DC} and I_{L}, the larger the absolute values of dv_{ds}/dt and di_{d}/dt, the smaller the E_{off}. E_{off} can be approximately calculated as follows [7]:

$$E_{\mathrm{off}} = \frac{1}{2}I_{\mathrm{L}}V_{\mathrm{DC}}\left(\frac{V_{\mathrm{DC}}}{|dv_{\mathrm{ds}}/dt|} + \frac{I_{\mathrm{L}}}{|di_{\mathrm{d}}/dt|}\right). \tag{10}$$

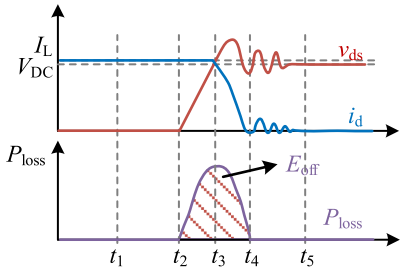

Fig. 4. Waveforms of device turn-OFF.

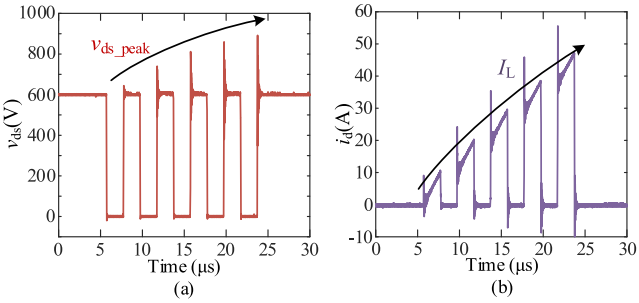

Fig. 5. $v_{\mathrm{ds\_peak}}$ increases with the increase of I_{L}. (a) v_{ds} waveform. (b) i_{d} waveform.

Based on the previous analysis, to mitigate the v_{ds} overshoot during the device turn-OFF process, as shown in (9), the v_{ds} overshoot can be controlled by regulating di_{d}/dt. As shown in Fig. 5, $v_{\mathrm{ds\_peak}}$ increases significantly with the rise of I_{L}. Hence, the di_{d}/dt needs to be dynamically adjusted in accordance with the variation of I_{L} to effectively suppress v_{ds}. The traditional methods slow down the entire turn-OFF process to achieve the same v_{ds} overshoot suppression, the proposed strategy has a much smaller impact on E_{off} according to (10). In addition, compared to the traditional AGDs with a fixed overshoot suppression effect, the proposed AGD can reduce losses under low-load current conditions, and decrease $v_{\mathrm{ds\_peak}}$ to ensure the safe operation of the device under high load current conditions.

III. Proposed AGD Topology Along With Its Hardware Implementation

Based on the analysis of the v_{ds} overshoot mechanism and the loss during device turn-OFF transient, as shown in Fig. 6, the proposed AGD identifies the descending stage of the i_{d} during the device turn-OFF process and adaptively regulates the v_{ds} overshoot peak by adjusting the device driving current. This method controls the v_{ds} overshoot peak value within the system-set limit under different load current conditions.

This section provides a detailed description of the proposed AGD topology and its hardware implementation. As shown in Fig. 7, the proposed AGD topology consists of the following main components:

1) *RC* voltage divider network;
2) stage detection circuit;
3) peak detection circuit;

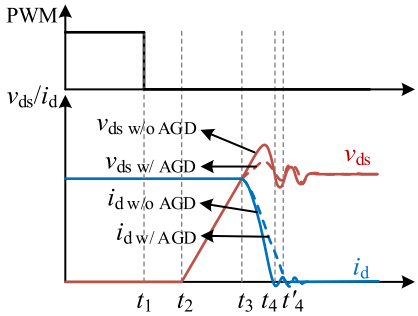

Fig. 6. Turn-OFF waveforms of SiC MOSFETs with and without AGD (dashed line represents the turn-OFF waveforms of SiC MOSFETs with AGD; solid line represents the turn-OFF waveforms of SiC MOSFETs without AGD).

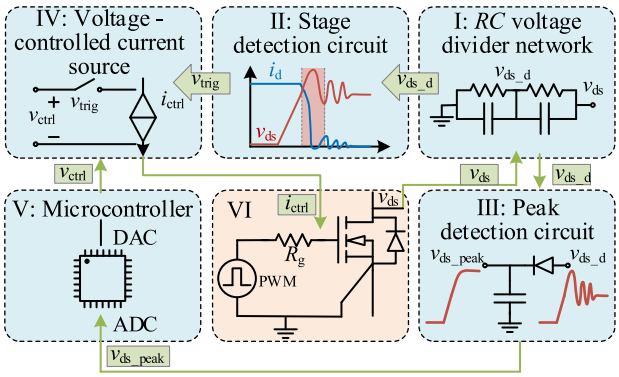

Fig. 7. Functional block diagram of the proposed AGD.

4) voltage-controlled current source;
5) microcontroller unit;
6) SiC MOSFETs.

Due to the extremely fast switching speed of SiC MOSFETs, the proposed AGD regulates the peak value of v_{ds} overshoot to the set value through the regulation of several switching cycles. As shown in Fig. 7, the proposed AGD collects the v_{ds} overshoot peak value by the peak detection circuit in the current switching cycle through the ADC peripheral of the microcontroller. And it can calculate the value of i_{ctrl} for the next switching cycle through the PI controller and output the voltage v_{ctrl} through the DAC peripheral of the microcontroller to control the output current i_{ctrl} of the voltage-controlled current source. The stage detection circuit triggers the operation of the voltage-controlled current source during the i_d falling stage and injects additional current into the device gate to regulate the driving current and control the di_d/dt, ultimately controlling the peak value of v_{ds} overshoot.

A. Proposed AGD Operating Principle

The proposed AGD circuit is simplified as shown in Fig. 8 when the current i_{ctrl} is injected into the gate during the i_d falling stage. The v_{gs} of the device can be calculated by (12). According to (2) and (12), the i_d during this stage can be approximately calculated by (13). The expression of di_d/dt can be further

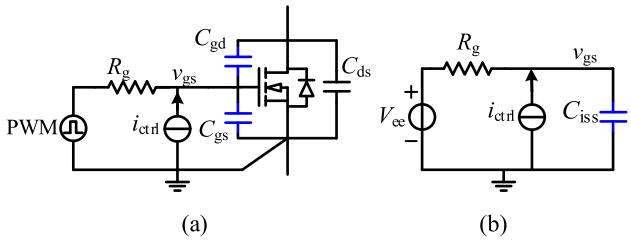

Fig. 8. Simplified circuit of the proposed AGD for the i_d falling stage (t_3–t_4). (a) Simplified circuit when the voltage-controlled current source model is adopted. (b) Further simplified circuit.

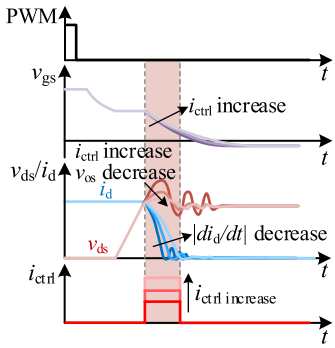

Fig. 9. Waveforms of v_{gs}, v_{ds}, and i_d when different i_{ctrl} are injected into the device gate.

derived from (13) and (14) as (15)

$$\tau = R_g C_{iss} \tag{11}$$

$$v_{gs} = (i_{ctrl}R_g + V_{ee}) + (V_{miller} - V_{ee} - i_{ctrl}R_g)e^{-\frac{t}{\tau}} \tag{12}$$

$$i_d = g_m\left[(i_{ctrl}R_g + V_{ee} - V_{th}) + (V_{miller} - V_{ee} - i_{ctrl}R_g)e^{-\frac{t}{\tau}}\right] \tag{13}$$

$$I_L = g_m(V_{miller} - V_{th}) \tag{14}$$

$$\frac{di_d}{dt} = \frac{V_{ee} - (I_L/g_m + V_{th}) + i_{ctrl}R_g}{(R_g C_{iss})/g_m}. \tag{15}$$

The overshoot voltage v_{os} is expressed as follows:

$$v_{os} = L_{loop}\left|\frac{di_d}{dt}\right| \tag{16}$$

$$v_{os} = L_{loop}\frac{I_L/g_m + V_{th} - i_{ctrl}R_g - V_{ee}}{(R_g C_{iss})/g_m}. \tag{17}$$

It is known from (17) that v_{os} can be regulated by adjusting the i_{ctrl}. Fig. 9 shows the waveforms of v_{gs}, v_{ds}, and i_d when different levels of i_{ctrl} are injected into the gate of the device.

It should be noted that i_{ctrl} is the output of the voltage-controlled current source in Part IV of Fig. 7. The input to this current source is v_{ctrl}, and the current source has a gain of 1, thus $i_{ctrl} = v_{ctrl}$. Fig. 10 shows the relationship between v_{os} and i_{ctrl} in (17). As i_{ctrl} increases, v_{os} decreases. However, when i_{ctrl} is constant, v_{os} increases with the load current I_L. Hence, in order

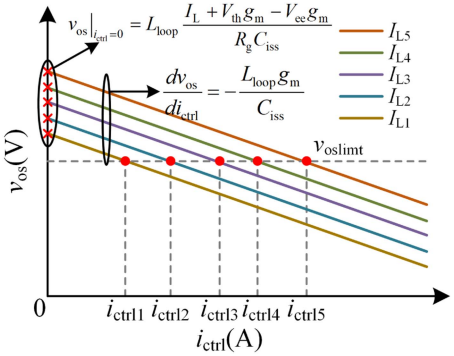

Fig. 10. Relationship between v_{os} and i_{ctrl} under diverse i_Ls.

to limit the voltage overshoot within the system-set limit, i_{ctrl} needs to be adjusted adaptively under different I_L conditions.

B. Proposed AGD Hardware Implementation.

The hardware implementation of each component of the proposed AGD is shown in Fig. 11.The key signals of SiC MOSFETs and the control signal timing of the proposed AGD are shown in Fig. 12.

1) RC Voltage Divider Network (Part I): Since the bus voltage at which the device operates is as high as several hundred volts, it is challenging for the stage detection circuit and the peak detection circuit to directly measure it. Therefore, an *RC* voltage divider network is employed to reduce v_{ds} to the voltage range that can be detected by the subsequent circuits. Furthermore, to minimize the impact of the parasitic capacitance of the circuit, compensation capacitors C_1 and C_2 are utilized to improve the dynamic performance of the voltage divider network. The voltage division ratio is determined by $R_2/(R_1+R_2)$, and the values of C_1 and C_2 satisfy as follows:

$$\frac{R_1}{R_2} = \frac{C_2}{C_1}. \tag{18}$$

2) Stage Detection Circuit (Part II): The proposed stage detection circuit does not rely on the signals associated with i_d and achieves the detection of the i_d falling stage only through v_{ds}.The current and voltage waveforms during the device turn-OFF process, along with the key signal of the proposed AGD, are shown in Fig. 12. The comparator CMP1 is used to identify the moment t_3 when i_d starts to fall. The theoretical value of the reference voltage V_{ref1} of CMP1 is $V_{DC}(R_2/(R_1+R_2))$. When the output voltage of the divider network v_{ds_d} rises to V_{ref1}, CMP1 outputs a high level.

To prevent the oscillation of v_{ds_d} from causing repeated level transitions of CMP1, a D flip-flop is used to synchronize the first rising edge of the CMP1 output, ultimately yielding a stable trigger signal. Meanwhile, a differential circuit composed of R_3 and C_3 is employed to differentiate v_{ds}. When the v_{ds} rises to its peak, v_{ds_dif} falls to zero. At this point, the falling speed of the i_d is no longer controlled. V_{ref2} is set at 0.1 V to configure CMP2 as a zero-crossing comparator, which outputs a negative edge signal when v_{ds_dif} drops to zero and is then inverted by INV1.

To prevent v_{ds_dif} oscillation from causing repeated transitions of INV1 output, likewise, a D flip-flop is utilized to synchronize the first rising edge of INV1. It is noted that v_{ds_dif} can be calculated by the following:

$$v_{ds\_dif} = R_3 C_3 \frac{dv_{ds}}{dt}. \tag{19}$$

Finally, an XOR gate is used to take the exclusive OR of the output signals from the two D flip-flops. Since there is a delay time t_{delay} in the actual circuit, as shown in Fig. 13, when positioning the moment t_3, it is necessary to appropriately lower the reference voltage V_{ref1} of CMP1 for triggering at t'_3. The value of V_{ref1} can be calculated as follows:

$$V_{ref1} = \left(V_{DC} - t_{delay}\frac{dv_{ds}}{dt}\right)\frac{R_2}{R_1+R_2}. \tag{20}$$

Additionally, when the v_{ds} rises to its peak, there is a delay from CMP2 to the current mirror output, the action interval of i_{ctrl} precisely lasts until the end of the i_d falling stage or even longer. After the end of the i_d falling stage, i_d is 0 A. Thus, the continuous output of i_{ctrl} after the end of the i_d falling stage does not increase the device loss, and V_{ref2} does not require special design.

3) Peak Detection Circuit (Part III): According to (5) and (6), it can be concluded that the absolute value of di_d/dt increases with the increase of I_L. Thus, the peak value of the v_{ds} overshoot also increases with the increase of I_L.

To suppress the v_{ds} overshoot under variable load conditions, it is essential to measure its peak value. However, since v_{ds} changes at an extremely high rate, directly detecting its peak value would require an ADC with a very fast sampling speed, and the collected data will need to be processed, leading to increased complexity and lower precision. The peak detection circuit can capture and hold the peak value of the v_{ds} overshoot, allowing a conventional ADC converter to be used.

As depicted in Fig. 11 III, the peak-hold circuit consists of a transconductance amplifier OP1, a voltage buffer OP2, a holding capacitor C_p, a MOS transistor Q_1, and diodes D_1 and D_2. When v_{ds_d} exceeds v_{ds_peak}, OP1 outputs current to charge C_p. After v_{ds_d} reaches its maximum and begins to decrease, D_1 becomes reverse-biased and the voltage across C_p remains unchanged. The high input impedance of OP2 slows down the voltage drop across C_p. When v_{ds_d} is lower than v_{ds_peak}, D_2 provides a current path for OP1, clamping the output of OP1 to 0 V. Furthermore, to prevent a substantial voltage drop of C_p due to excessive reverse recovery current of D_1, a Schottky diode is employed for D_1. After the ADC sampling is complete, C_p is discharged through Q_1, allowing C_p to normally maintain the peak of v_{ds_d} in the next cycle.

The transfer function of the peak-holding circuit is expressed as follows:

$$\frac{v_{ds\_peak}(s)}{v_{ds\_d}(s)} = \frac{2\pi g_{op1} f_{op2}}{C_p s^2 + 2\pi C_p f_{op2} s + 2\pi g_{op1} f_{op2}}. \tag{21}$$

In this study, g_{op1} is the transconductance of OP1, and f_{op2} is the bandwidth of OP2. The OP1 is OPA861, and the OP2 is OPA690. D_1 and D_2 are of BAT17, and the capacitance C_p is 68

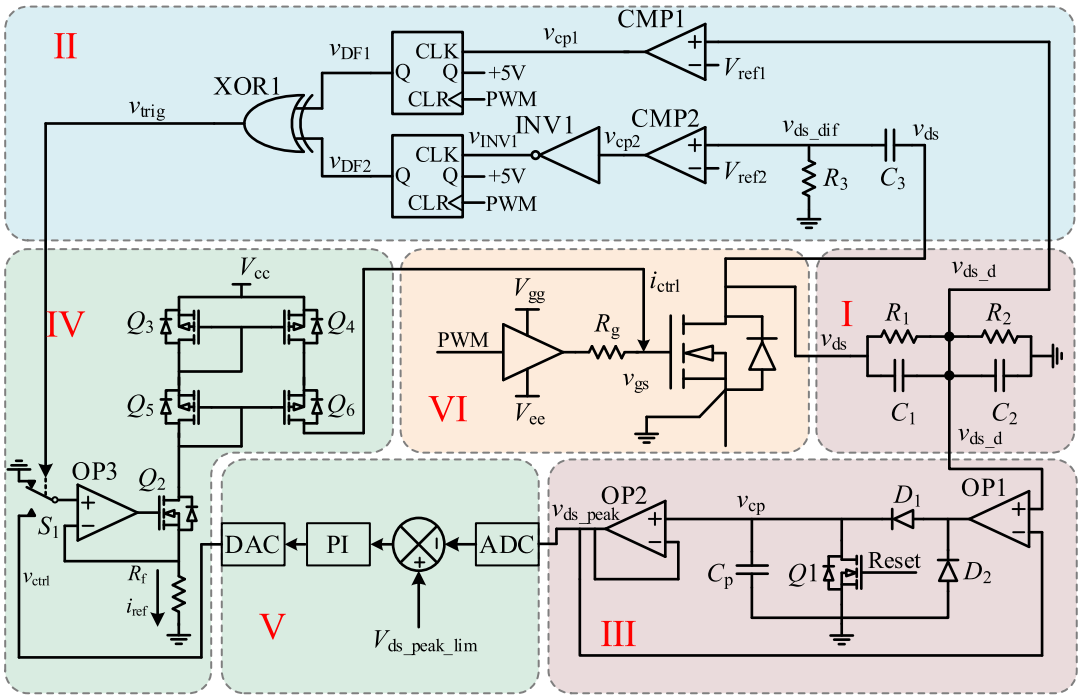

Fig. 11. Proposed AGD topological structure and its hardware implementation.

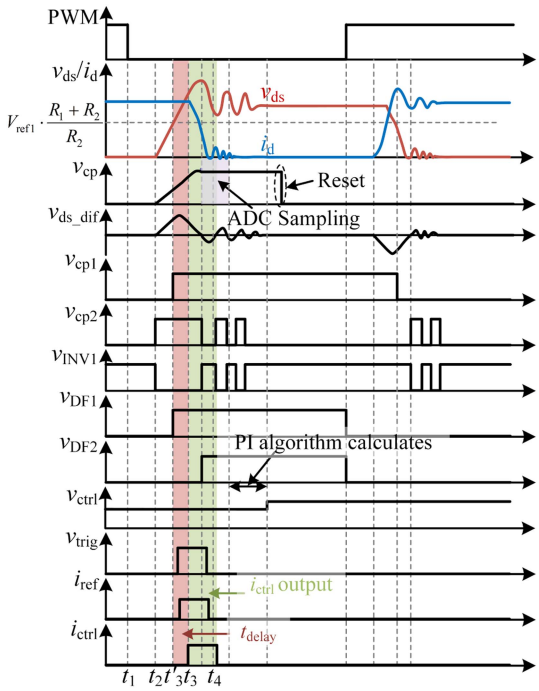

Fig. 12. Signal timing of the proposed AGD.

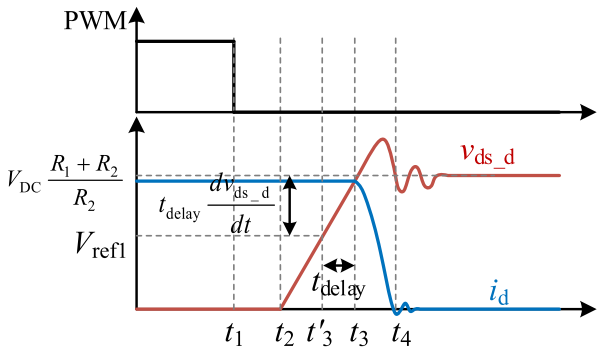

Fig. 13. Diagram of t_{delay} delay compensation.

pF. Based on the actual circuit parameters, the bandwidth of the peak-hold circuit is calculated as approximately 220 MHz. The rise time of v_{ds_d} is approximately 15 ns, and the bandwidth of v_{ds_d} can be estimated to be approximately 23.3 MHz from (22) [32], where T_r represents the signal rising time. Consequently, the peak-hold circuit can effectively extract the peak value of v_{ds_d}

$$f = \frac{0.35}{T_r}. \tag{22}$$

4) Voltage-Controlled Current Source (Part IV): As depicted in Fig. 11 IV, the voltage-controlled current source is composed of operational amplifier OP3, feedback resistor R_f, N-type MOSFET Q_2, and P-type MOSFETs Q_3 to Q_6. OP3, Q_2, and R_f constitute a reference current source, and the reference current i_{ref} is calculated by (23). Q_3 to Q_6 constitute a current mirror circuit, employing a cascode structure to augment the output impedance of the current mirror and furnish a stable i_{ctrl} when v_{gs} varies rapidly. Under these conditions, i_{ctrl} is approximately

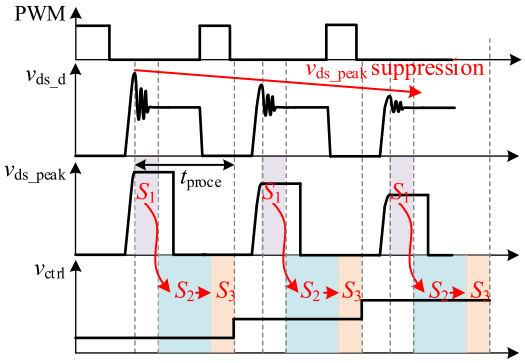

Fig. 14. Operational timing sequence of the control algorithm on the MCU.

TABLE III
CIRCUIT PARAMETERS

Symbol	Values
Input voltage V_{DC}	600 V/800 V
Load inductance L_{Load}	139 uH
Load resistor R_{L1}	5.7 Ω
Load resistor R_{L2}	0~33 Ω
Driver resistor R_g	15 Ω
Driver voltage V_G	+15 V/-5 V

equivalent to i_{ref}

$$i_{ref} = \frac{v_{ctrl}}{R_f} \tag{23}$$

$$i_{ctrl} \approx i_{ref} = \frac{v_{ctrl}}{R_f}. \tag{24}$$

5) Microcontroller Unit (MCU) (Part V): The MCU (STM32G474CET6 from ST) integrates a 12-bit ADC peripheral. The timing of the control algorithm operation on the MCU is shown in Fig. 14. During the S_1 stage, once the peak detection circuit acquires the peak value $v_{ds\_peak}(i)$ of this switching cycle during device turn-OFF transient, the ADC peripheral of the MCU samples it. After the S_1 stage ends, Q_1 is turned ON to reset C_p, and the algorithm transitions from the S_1 stage to the S_2 stage. In the S_2 stage, the MCU executes the PI control to calculate the control voltage $v_{ctrl}(i+1)$ for the next switching cycle of the current source. At this point, the algorithm transitions from S_2 to S_3. In the S_3 stage, the MCU's DAC peripheral updates the value of $v_{ctrl}(i+1)$, which controls the current mirror circuit's output current i_{ctrl}, ultimately regulating overshoot peak of $v_{ds\_peak}(i+1)$.

IV. EXPERIMENTAL VALIDATION

To validate the effectiveness of the proposed AGD, a continuous pulse experimental platform with load-switching functionality as depicted in Fig. 15 is established. The main parameters of the experimental platform are provided in Table III. The devices S_1 and S_2 are SiC MOSFETs (model C3M0040120K, 1200 V/66 A) from CREE, with S_1 being the device under test and S_2 acting as a freewheeling diode. L_{load} is the load inductance, while R_{L1} and R_{L2} are the load resistances. Load switching is achieved by

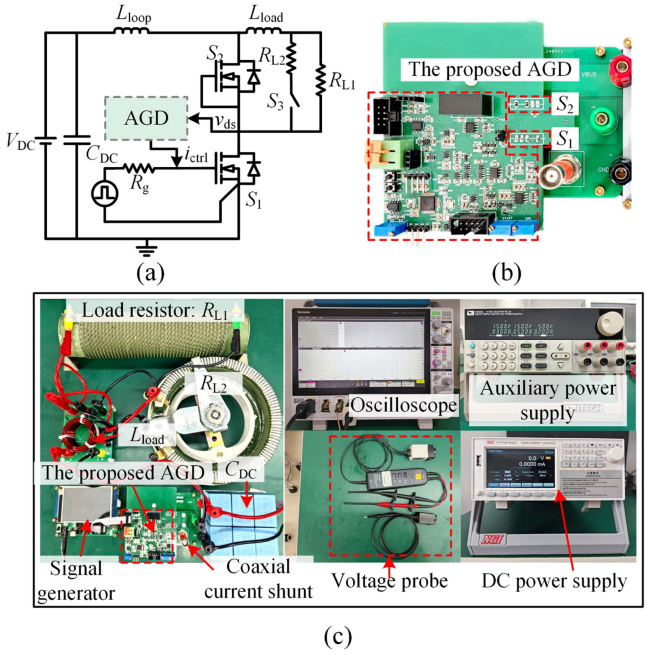

Fig. 15. Continuous pulse experimental platform with load switching functionality. (a) Schematic diagram. (b) Proposed AGD. (c) All experimental testing apparatus.

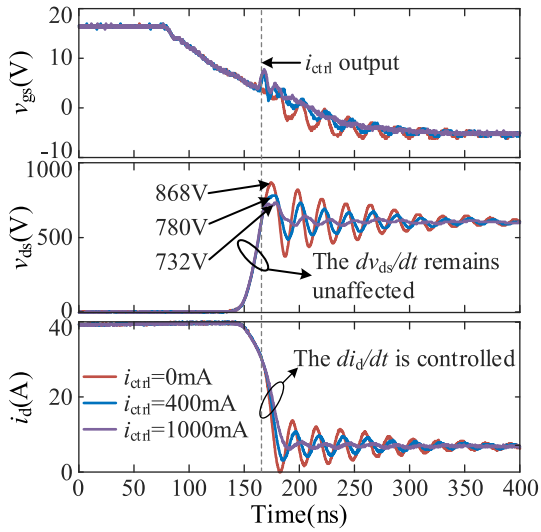

Fig. 16. Suppression effect of the proposed AGD on v_{ds} overshoot under different i_{ctrl} controls (V_{DC} = 600 V/I_L = 40 A).

operating switch S_3. Additionally, waveform measurements are conducted using an oscilloscope of MSO54B from Tektronix, and the signals of v_{ds}, i_d, and AGD of the device are measured using differential probes THDP0200 (200 MHz), coaxial shunts SSDN-10 (2 GHz), and passive probes (700 MHz), respectively.

A. Suppression Effect of the Proposed AGD on V_{ds} Overshoot and Its Loss Analysis

Fig. 16 shows the waveforms of v_{gs}, v_{ds}, and i_d of the proposed AGD when different i_{ctrl} values are injected into the device

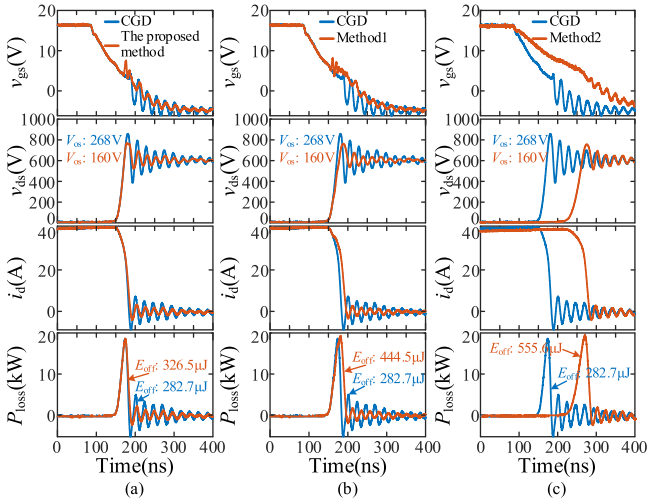

Fig. 17. Waveforms of v_{gs}, v_{ds}, i_d, and losses when the proposed AGD, the method of controlling *dv*/*dt* and *di*/*dt* simultaneously (Method 1), and the traditional method of increasing the gate resistance (Method 2) are applied respectively (test conditions: 600 V/40 A). (a) Proposed method. (b) Method 1 [28]. (c) Method 2.

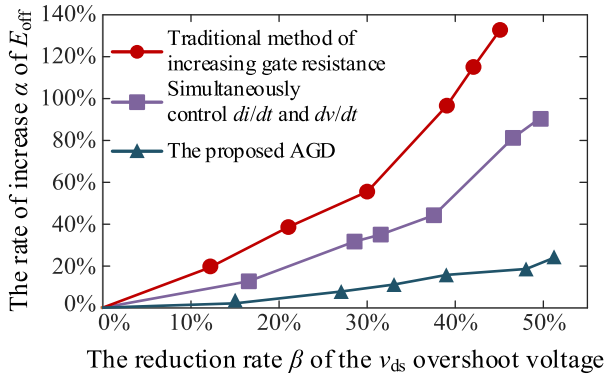

Fig. 18. Comparison of the increase rate α of E_{off} when the proposed AGD, the simultaneous control method of *dv*/*dt* and *di*/*dt*, and the traditional method of increasing the gate resistance achieve different v_{ds} overshoot suppression ratios β. (Test conditions: 600 V/40 A).

gate. Evidently, the proposed AGD effectively suppresses the v_{ds} overshoot by regulating i_{ctrl}. Since i_{ctrl} is only at the milliampere level and difficult to measure directly, the output time of i_{ctrl} is inferred by observing the variation of v_{gs}.

Under the operating condition with 600 V/40 A, the performances of the conventional gate driver (CGD), the proposed AGD, the method of simultaneously controlling *dv*/*dt* and *di*/*dt*, and the traditional method of increasing the gate resistance are compared, as shown in Fig. 17. When the v_{ds} overshoot voltage v_{os} is reduced from 268 to 160 V, the proposed AGD increases the turn-OFF loss by only 43.8 μJ. The method of concurrently controlling *dv*/*dt* and *di*/*dt* increases the turn-OFF loss by 161.8 μJ. The method of increasing the gate resistance raises the turn-OFF loss by 272.9 μJ, resulting in a 96.53% increase, and significantly prolongs the turn-OFF time of the device.

Nevertheless, the proposed AGD and the method of simultaneously controlling *dv*/*dt* and *di*/*dt* have almost no effect on the turn-OFF time of the device. To further validate that the proposed method achieves a better compromise between v_{ds} overshoot suppression and the increase in turn-OFF loss, Fig. 18 shows a comparison of the increments in loss among the proposed AGD, the method of simultaneously controlling *dv*/*dt* and *di*/*dt*, and the traditional method of increasing the gate resistance when different levels of v_{ds} overshoot suppression are achieved. α and β are expressed as follows:

$$\alpha = \frac{V_{os\_normal} - V_{os}}{V_{os\_normal}} \tag{25}$$

$$\beta = \frac{E_{off\_normal} - E_{off}}{E_{off\_normal}}. \tag{26}$$

Here, V_{os_normal} and E_{off_normal} are the overshoot voltage and turn-OFF loss when no voltage overshoot suppression methods are applied, and V_{os} and E_{off} represent the overshoot voltage and turn-OFF loss after the application of overshoot voltage suppression methods.

B. Verification of the Self-Regulating Capability of the Proposed AGD

In this article, the proposed AGD is finely tuned in terms of timing. The primary adjustment is made to V_{ref1} in Fig. 11 to compensate for the circuit delay time t_{delay}. The final value of V_{ref1} is set to 685 mV, ensuring that i_{ctrl} is accurately output during the i_d falling stage. The output timing of i_{ctrl} is not influenced by the I_L. Consequently, after a single time-domain fine-tuning, it can accurately identify the i_d falling stage without requiring any further modification to the circuit parameters.

To verify the accuracy of the proposed AGD in identifying the i_d falling stage under various load current working conditions, Fig. 19 presents the action timings of i_{ctrl} when I_L is 25, 35, 45, and 55 A. Since i_{ctrl} is only at the milliampere level and is challenging to measure directly, its output timing can be identified by observing the variation stage of the v_{gs} fall slope. It is evident that i_{ctrl} operates during the i_d falling stage under different I_L and has no impact on the rising speed of v_{ds}.

Fig. 20 demonstrates the self-regulation capability of the proposed AGD. In the microprocessor, the overshoot peak of v_{ds} is limited to 730 V. After the proposed AGD begins operation, it automatically adjusts over five switching cycles, reducing the overshoot peak of v_{ds} from 812 V to the set value of 730 V.

The proposed AGD also possesses the self-regulating function under varying load current conditions. In this article, when the bus voltages are 600 and 800 V, respectively, and I_L suddenly changed from 20 to 40 A, the suppression effect of the proposed AGD on the overshoot peak of v_{ds} is evaluated. As shown in Fig. 21(a), under a bus voltage of 600 V and without the application of the proposed AGD, I_L increases from 20 to 40 A, causing the v_{ds} overshoot peak to rise sharply to 860 V. Nevertheless, as shown in Fig. 21(b), when the proposed AGD is applied and I_L changes from 20 to 40 A, the v_{ds} overshoot peak can be effectively suppressed to the set value of 750 V after several switching cycles of self-regulating. Similarly, in

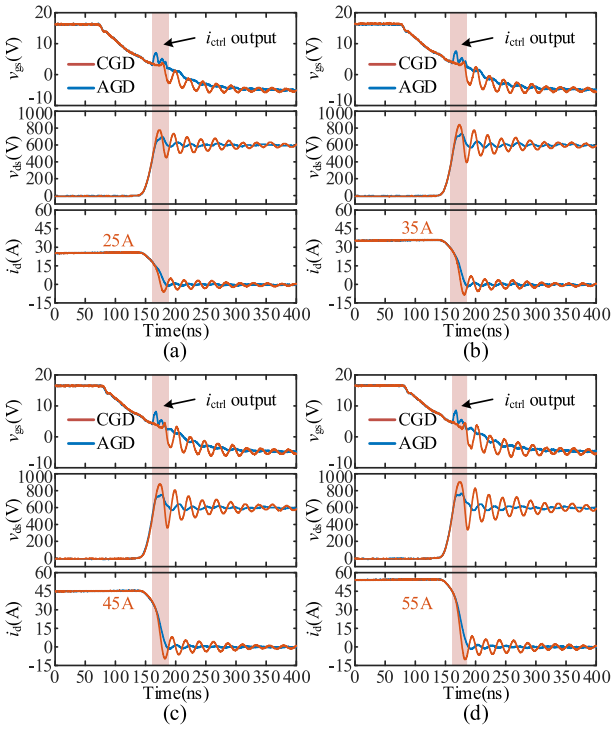

Fig. 19. Output timing of i_{ctrl} in the case of different I_{L}. (a) $I_{\mathrm{L}} = 25$ A. (b) $I_{\mathrm{L}} = 35$ A. (c) $I_{\mathrm{L}} = 45$ A. (d) $I_{\mathrm{L}} = 55$ A.

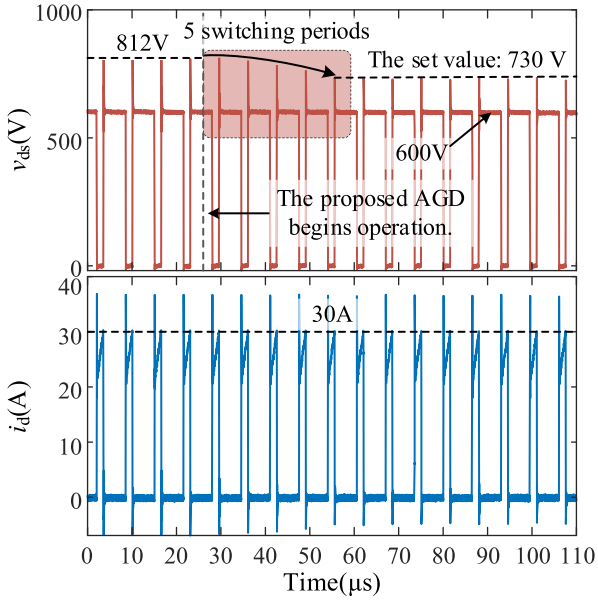

Fig. 20. v_{ds} overshoot control performance of the proposed AGD under the 600 V/30 A operating condition.

Fig. 22(a), when the bus voltage is 800 V and I_{L} changes from 20 to 40 A, the v_{ds} overshoot peak will rise to 1060 V when the proposed AGD is not applied. As shown in Fig. 22(b), the proposed AGD effectively suppresses the v_{ds} overshoot peak to the set value of 950 V after several switching cycles of regulation. It is important to note that at the moment of I_{L} change, the rise rate increases very rapidly. Due to the limited response speed

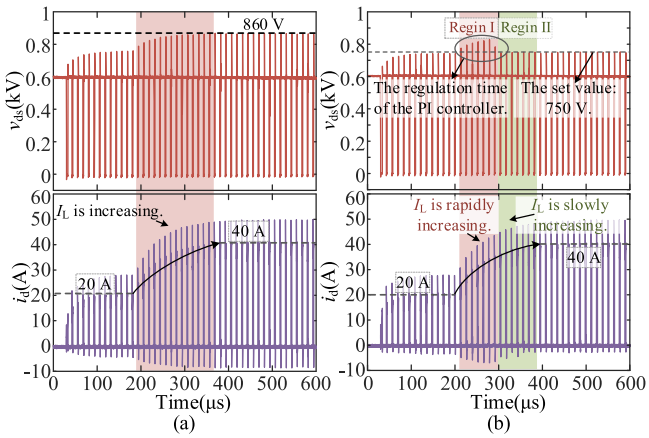

Fig. 21. Experimental waveforms of the proposed AGD and CGD under a bus voltage of 600 V when load current changes from 20 to 40 A. (a) CGD. (b) Proposed AGD.

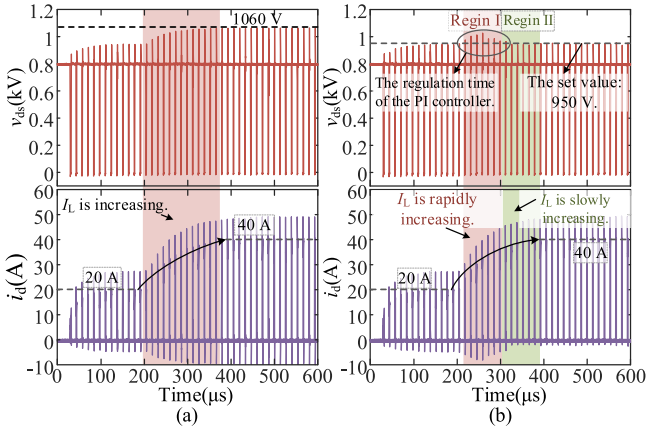

Fig. 22. Experimental waveforms of the proposed AGD and CGD under a bus voltage of 800 V when load current changes from 20 to 40 A. (a) CGD. (b) Proposed AGD.

of the PI controller, the v_{ds} overshoot peak will exceed the set value for several cycles. However, during the final stage of the I_{L} mutation period [Region II of Figs. 21(b) and 22(b)], when the decrease rate of I_{L} slows down, the v_{ds} overshoot peak has been controlled to the set value. Hence, in practical applications, under conditions where the I_{L} change is not significant, the v_{ds} overshoot peak during the I_{L} change period will not substantially exceed the set value.

V. Conclusion

This article presents an AGD with self-regulating functionality based on low-cost microcontrollers. The parameter design of its turn-OFF transient detection circuit is independent of the load current, and its closed-loop control can mitigate the impact of load current variations on the v_{ds} overshoot peak, effectively. Through several cycles of self-regulating during load current changes, the v_{ds} overshoot peak can be quantitatively suppressed. The proposed AGD is compared with the control method of *dv*/*dt* and *di*/*dt*, as well as the traditional method of

increasing gate resistance, in terms of achieving different levels of $v_{\rm ds}$ overshoot suppression. Additionally, the suppression effect on the voltage overshoot peak is evaluated when the load current changes from 20 to 40 A under dc-bus voltages of 600 and 800 V. The experimental results indicate that the proposed AGD can reduce the voltage overshoot peak by 38.8% under the test condition of 600 V/40 A. Furthermore, the proposed method has a 26.5% reduction in turn-OFF loss compared to the controlling *dv*/*dt* and *di*/*dt* method, and a 41.2% reduction compared to the increasing gate resistance method. Therefore, compared with conventional self-regulating drive methods, the proposed method can achieve an optimal tradeoff between voltage overshoot and turn-OFF loss. In addition, it can suppress the $v_{\rm ds}$ overshoot peak when the load current changes, effectively.

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