Thermal Balance Oriented Model Predictive Control for 100 kHz Large-Signal Parallel Inverters With Optimized Pulse Patterns

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***Abstract*—In sound navigation and ranging, the parallel inverters are required to drive electroacoustic transducers to emit 100 kHz acoustic waves. Optimized pulse patterns (OPPs) can achieve the wide bandwidth of the parallel inverters with high switching frequency utilization. However, the junction temperatures of parallel inverters by using OPPs are imbalanced at a low carrier ratio. The inductance mismatches exacerbate the reliability issue. Therefore, this article proposes a thermal balance oriented model predictive control (TBOMPC) for 100 kHz Large-Signal Parallel Inverters with OPPs. First, the principle and the reliability of OPPs are analyzed. Then, the mathematical model is constructed for the inductance parameters. The initial switching states of TBOMPC are designed to identify the inductance parameters. The proposed TBOMPC takes account of the inductance mismatches and redistributes the switching states of OPPs, which can effectively balance the junction temperatures of power devices at a low carrier ratio. Finally, the effectiveness of the proposed method is verified by the experimental results. The maximum junction temperature differences of TBOMPC are less than 1.5°C under inductance mismatches.**

***Index Terms*—Inductance mismatches, maximum junction temperature difference, parallel inverters, thermal balance oriented model predictive control (TBOMPC).**

I. Introduction

THE sound navigation and ranging (SONAR) can be used to explore the biological behaviors and variations of marine organisms, which is of great significance to the safety of marine ecosystems [1], [2], [3]. The parallel inverters are required to drive the electroacoustic transducers to emit acoustic waves [4], [5]. The bandwidth of the parallel inverter is from tens of kHz to hundreds of kHz in high-power scenarios [6], [7], [8]. However, the junction temperatures of power devices in parallel inverters are imbalanced. The inductance mismatches exacerbate the inconsistency of the bridge arm current [9], [10], further making junction temperatures of power devices more imbalanced. The series and parallel topologies of the converters are shown in Fig. 1, and the junction temperature imbalance of parallel topology is more serious.

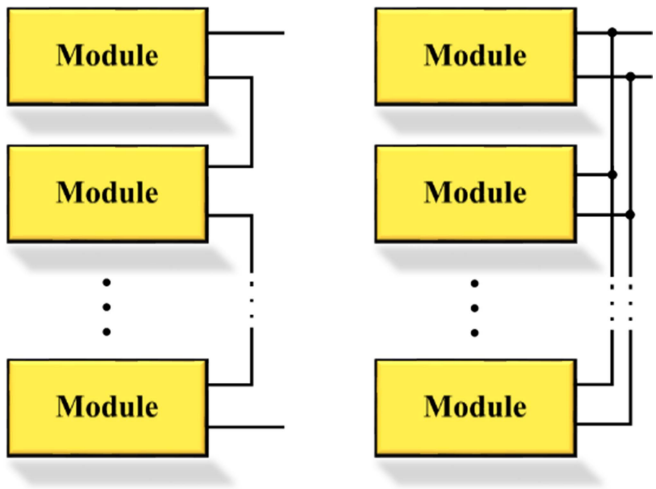

Fig. 1. Series and parallel topologies of the converters. (a) Series. (b) Parallel.

The existing thermal balance oriented controls (TBOCs) maintain consistent lifetimes across different modules by adjusting output power, redistributing switching states, and so on [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. The comprehensive comparison of TBOCs is listed in Table I. Liserre et al. [11], [12], [13] has conducted extensive research on high reliability, particularly on the issue of different remaining useful lifetimes. An advanced discontinuous modulation method has been proposed, which can manipulate thermal stress independently by adjusting output power. The decentralized power-sharing method is proposed to improve overall system performance and reliability by appropriately sharing active and reactive power between different modules [14]. A centralized thermal stress oriented strategy is proposed to reduce the thermal

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TABLE I
COMPREHENSIVE COMPARISON OF THERMAL BALANCE ORIENTED CONTROLS

TBOCs	Topology	Controlled Variable	Carrier Ratio	Parameter Mismatches	Affect Output	Universal Applicability
Ko et al. [11] and Ko et al. [12]	Series	Power Routing	High	Not Considered	Yes	Limited
Ko et al [13] and Jiang et al. [14]	Parallel	Power Routing	High	Not Considered	Yes	Limited
Wang et al. [15]	Parallel	Switching Frequency, Reactive Power	High	Not Considered	Yes	Limited
Sheng et al. [16], Hahn et al. [17], and Han et al. [19]	Series	Switching States	High	Not Considered	No	Not Limited
Wang et al. [18], Novak et al. [20], and Chowdhury et al. [21]	Single	Switching States	High	Not Considered	No	Not Limited
Geyer et al. [26] and Koukoula et al. [27]	Single	Switching States	Low	Not Considered	Yes	Not Limited
TBOMPC	Parallel	Switching States	Low	Considered	No	Not Limited

stress of multiple inverters by the reactive power injection [15]. The above methods balance the junction temperatures by adjusting active power and reactive power. However, the application scenarios of the above methods are limited.

The traditional modulation strategies can balance junction temperatures of power devices by redistributing switching states. The active bypass with thyristor for half-bridge submodules and symmetrical modulation for full-bridge submodules-based active thermal control strategies are employed to reduce the junction temperature [16]. An active thermal balancing algorithm in [17] takes into account the junction temperature of the most stressed power semiconductor in each SM for junction temperature balance. The pulse width modulation method is based on the periodic alternate use of power devices, which can balance junction temperatures of power devices and minimize temperature rise [18]. These improved modulation strategies can effectively balance the junction temperatures of power devices. However, when the parameters are mismatched, the effectiveness of balancing junction temperatures may be weakened.

The finite-control set model predictive control (FCS-MPC) with multiobjective optimization has been widely applied in thermal balance. FCS-MPC can effectively address the issue of imbalanced thermal stress, but weighting factors of electrical and thermal variables are hard to design. Active thermal control is realized by the state distribution algorithm for the superior dynamic performance and high reliability [19]. The advantages of the FCS-MPC in achieving junction temperature balance in hybrid neutral point clamped (NPC) and active NPC converters are studied in [20]. Two switching sequences with different zero vectors in each sector are alternately selected, which can balance the loss and thermal stress [21]. However, the carrier ratio of the existing FCS-MPC is high, which is not suitable in high-frequency scenario (such as 100 kHz).

Low-carrier-ratio methods, such as optimal pulse patterns (OPPs), have been widely used in the field of motor drive [22], [23], [24]. Meanwhile, low-carrier-ratio methods with high switching frequency utilization have gradually been applied in 100 kHz large-signal multiphase converters [25]. However, the junction temperature imbalance of low-carrier-ratio methods is more serious. Professor Tobias Geyer has focused on the reliability of OPPs and improved the reliability by constraining the switching loss and conduction loss. However, the output performance of OPPs may be affected [26], [27]. Meanwhile, low-carrier-ratio methods considering parameter mismatches need to be further studied in the junction temperature balance.

This article proposes the thermal balance oriented model predictive control (TBOMPC) for the 100 kHz large-signal parallel inverter. TBOMPC is based on the optimal switching angles and optimal states of OPPs, which has high switching frequency utilization and excellent output performance. The carrier ratio of TBOMPC is low, which is suitable in high-frequency scenario. The proposed TBOMPC can identify the inductance parameters and redistribute the switching states to balance the junction temperatures with mismatched parameters.

The rest of this article is organized as follows. In Section II, the principle of OPPs is described, and the reliability of OPPs is analyzed. TBOMPC is proposed in Section III. In Section IV, the effectiveness of the proposed method is verified by experiments. Finally, Section V concludes this article.

II. OPTIMAL PULSE PATTERNS

OPPs can minimize the harmonic content of multilevel voltage. The theoretical optimal states and optimal switching angles of OPPs ensure high switching frequency utilization and excellent output performance.

A. Basic Principle

The certain range of harmonic content is minimized by the OPPs with a low carrier ratio. The specific implementation steps of OPPs are as follows.

1) Reasonable states of multilevel voltage.
2) Expression of multilevel voltage.
3) Fourier coefficients of multilevel voltage.
4) Amplitude and phase expressed by Fourier coefficients.
5) Total harmonic distortion (THD) expressed by Fourier coefficients.

6) The optimal states and optimal switching angles of the multilevel voltage are calculated to minimize THD.

The three-full-bridge parallel inverter is used in this article, which is shown in Fig. 5. To ensure that each power device turns on and off at least once per output cycle, the carrier ratio is set to 6. There are four reasonable states in Fig. 2.

In Fig. 2, the green up arrow represents the increase of one level, and the red down arrow represents the decrease of one level. The switching transitions ΔV_j $(j = 0, 1, \ldots, 11)$ can be expressed by the level of the multilevel voltage V_j $(j = 0, 1, \ldots, 12)$

$$\Delta V_j = V_{j+1} - V_j, \quad j = 0, 1, \ldots, 11. \tag{1}$$

The switching transitions ΔV_j $(j = 0, 1, \ldots, 11)$ take the value of -1 or 1. The expression of multilevel voltage $u_m(\theta)$ is as follows:

$$u_m(\theta) = \begin{cases} V_0 \frac{U_{\mathrm{dc}}}{3}, & 0 \le \theta < \alpha_0 \\ V_{j+1} \frac{U_{\mathrm{dc}}}{3}, & \alpha_j \le \theta < \alpha_{j+1}, j = 0, 1, \ldots, 10 \\ V_{12} \frac{U_{\mathrm{dc}}}{3}, & \alpha_{11} \le \theta < 2\pi \end{cases} \tag{2}$$

where U_{dc} is the dc voltage, α_j ($j = 0, 1, \ldots, 11$) are the switching angles. Fourier coefficients a_n ($n = 0, 1, 2, \ldots$) and b_n ($n = 1, 2, \ldots$) are calculated over a period of 2π [22], [23], [24]

$$a_n = \begin{cases} \frac{2V_0 U_{\mathrm{dc}}}{3} - \frac{U_{\mathrm{dc}} \sum_{i=0}^{11} \Delta V_i \alpha_i}{3\pi}, & n = 0 \\ -\frac{U_{\mathrm{dc}} \sum_{i=0}^{11} \Delta V_i \sin(n\alpha_i)}{3n\pi}, & n = 1, 2, 3, \ldots \end{cases} \tag{3}$$

$$b_n = \frac{U_{\mathrm{dc}} \sum_{i=0}^{11} \Delta V_i \cos(n\alpha_i)}{3n\pi}, \quad n = 1, 2, 3, \ldots. \tag{4}$$

Considering the requirements of dc offset, fundamental RMS value, phase, and switching angles

$$\begin{cases} a_0 = 0, a_1 = 0, b_1 = \sqrt{2} U_1 \\ 0 \le \alpha_0 \le \alpha_1 \le \ldots \le \alpha_{11} \le 2\pi \end{cases}. \tag{5}$$

The multilevel voltage contains a large number of harmonics. THD of the voltage is used to evaluate the quality of the voltage waveform

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2} U_n^2}}{U_1} \times 100\% \tag{6}$$

where U_1 is the root mean square (RMS) value of the fundamental voltage, U_n ($n = 2, 3, \ldots$) is the RMS value of the nth harmonic voltage. The optimization object is the THD of multilevel voltage. When the operating condition (OC) is determined, the RMS value of the fundamental voltage U_1 is a fixed value. The high-order harmonics can be absorbed by the filter capacitor and filter inductor, and the low-order harmonics (second, third, …,ninth) are the main focus. Therefore, the optimization function $G(\Delta V_0, \ldots, \Delta V_{11}, \alpha_0, \ldots, \alpha_{11})$ can be simplified by Fourier coefficients as follows:

$$G(\Delta V_1, \ldots, \Delta V_{11}, \alpha_1, \ldots, \alpha_{11}) = \sum_{n=2}^{9} \left(a_n^2 + b_n^2\right). \tag{7}$$

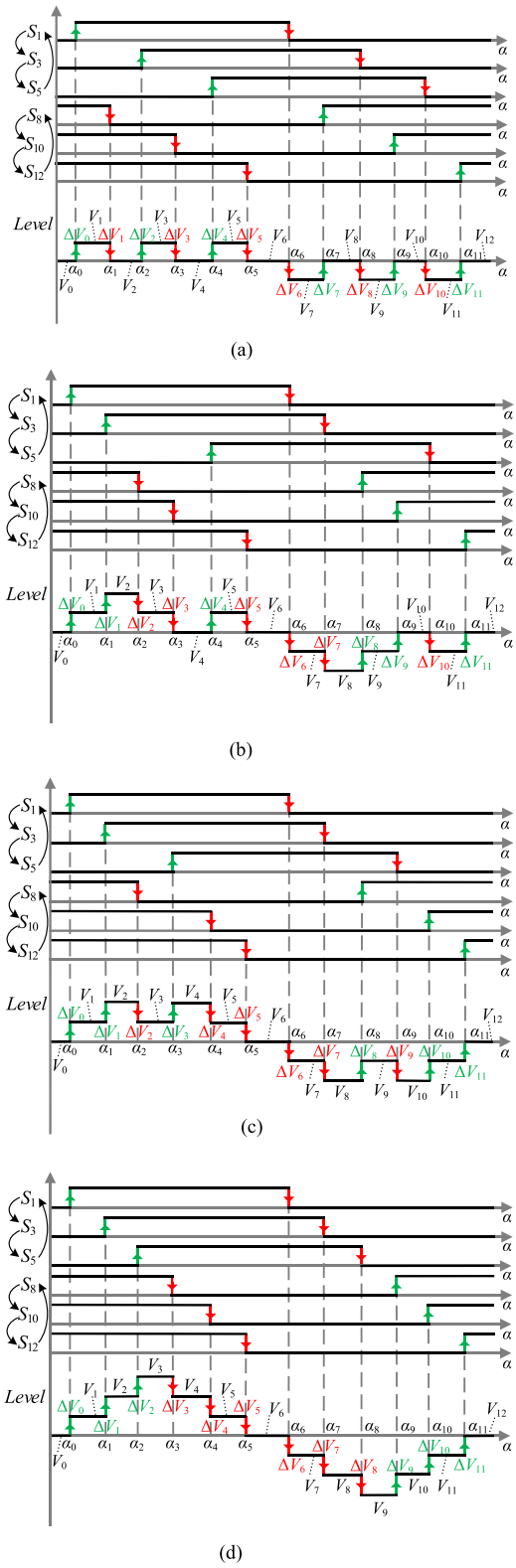

Fig. 2. Four reasonable states for the full modulation index range. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

The optimal switching angles at different modulation indexes M are shown in Fig. 3.

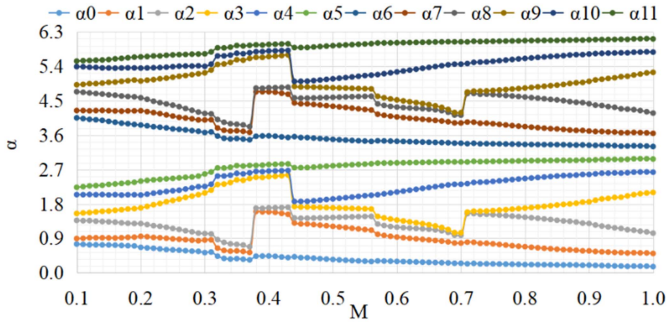

Fig. 3. Optimal switching angles at different modulation indexes.

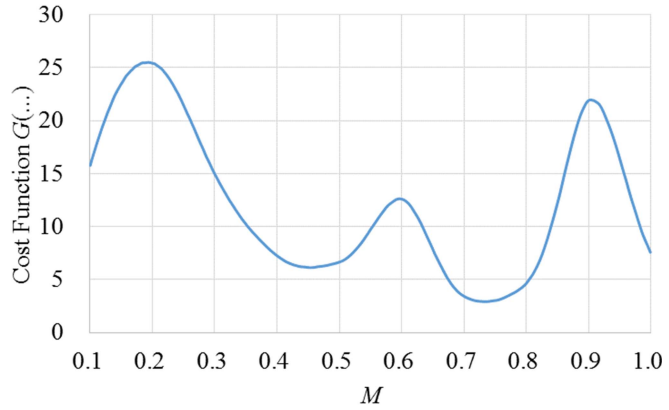

Fig. 4. Minimum values of the cost function at different modulation indexes.

The optimal states at different modulation indexes are selected by traversing all reasonable states

$$\text{Optimal State} = \begin{cases} \text{State1}, & M \le 0.37 \\ \text{State2}, & 0.38 \le M \le 0.43 \\ \text{State3}, & 0.44 \le M \le 0.70 \\ \text{State4}, & 0.71 \le M \le 1.00 \end{cases}. \quad (8)$$

The minimum values of the cost function at different modulation indexes are shown in Fig. 4. There are three peaks at the modulation indexes of 0.2, 0.6 and 0.9. Meanwhile, the minimum values of the cost function at the low modulation index and high modulation index are generally high. The fundamental voltage at low modulation index is low, so THD of low modulation index is higher than that of high modulation index.

B. Reliability Analysis

The four optimal states can be obtained by the phase-shifted square waves in Fig. 2. The detailed constructions are as follows.

1) *First Half of the Fundamental Waveform*: When the level increases, power devices (S_1, S_3, S_5) turn ON and power devices (S_2, S_4, S_6) turn OFF. When the level decreases, power devices (S_8, S_{10}, S_{12}) turn OFF and power devices (S_7, S_9, S_{11}) turn ON.
2) *Second Half of the Fundamental Waveform*: When the level decreases, power devices (S_1, S_3, S_5) turn OFF and power devices (S_2, S_4, S_6) turn ON. When the level increases, power devices (S_8, S_{10}, S_{12}) turn ON and power devices (S_7, S_9, S_{11}) turn OFF.

The detailed constructions make the junction temperatures of power devices as balanced as possible. To further balance the junction temperatures, each power device is rotated in turn. The above constructions are used in OPPs. However, there are two reliability issues in Fig. 3.

1) If the optimal switching angles satisfy the half-wave symmetry (M = 0.5, 0.7, 0.8, 0.9, 1.0), the control signals of power devices can be composed of 50% duty square waves. The different switching angles lead to imbalanced junction temperatures of power devices. The inductance mismatches exacerbate the reliability issue.
2) If the optimal switching angles do not satisfy the half-wave symmetry (M = 0.1, 0.2, 0.3, 0.4, 0.6), the control signals of power devices cannot be composed of 50% duty square waves. The imbalanced junction temperatures can be a more serious reliability issue.

III. Thermal Balance Oriented Model Predictive Control

The imbalanced junction temperatures of power devices can be caused by OPPs. Therefore, TBOMPC is proposed to identify the inductance parameters and redistribute the switching states of OPPs, which can balance junction temperatures of power devices. The control block diagram of the TBOMPC is shown in Fig. 5. The main steps of TBOMPC are predictive model, rolling optimization, and feedback.

A. Inductance Parameter Identification

The inductance parameter identification is based on the estimated output voltage at the switching transition moment. When the inductance parameters L_j (j = 1, 2,…,6) are inconsistent with the setting value L_p, there are discontinuous changes in the estimated output voltage (red curve) in Fig. 6.

In Fig. 5, the Kirchhoff's voltage law at the point *A/B*

$$\begin{cases} u_1(t) - L_1 \frac{di_1(t)}{dt} = u_A(t) \\ u_2(t) - L_2 \frac{di_2(t)}{dt} = u_A(t) \\ u_3(t) - L_3 \frac{di_3(t)}{dt} = u_A(t) \\ u_4(t) - L_4 \frac{di_4(t)}{dt} = u_B(t) \\ u_5(t) - L_5 \frac{di_5(t)}{dt} = u_B(t) \\ u_6(t) - L_6 \frac{di_6(t)}{dt} = u_B(t) \end{cases} \quad (9)$$

where $u_j(t)$ (j = 1, 2,…,6) is the output voltage of the bridge arm, $i_j(t)$ (j = 1, 2,…,6) is the inductor current of the bridge arm, $u_A(t)$ is the node voltage at point *A*, and $u_B(t)$ is the node voltage at point *B*. The Kirchhoff's current law at the point *A/B*

$$i_L(t) = \sum_{j=1}^{3} i_j(t) = -\sum_{j=4}^{6} i_j(t) \quad (10)$$

where $i_L(t)$ is the total inductor current. The output voltage $u_o(t)$ is the difference between the node voltage $u_A(t)$ and $u_B(t)$

$$u_o(t) = \frac{L_2L_3u_1(t) + L_1L_3u_2(t) + L_1L_2u_3(t) - L_1L_2L_3\frac{di_L(t)}{dt}}{L_1L_2 + L_1L_3 + L_2L_3}$$

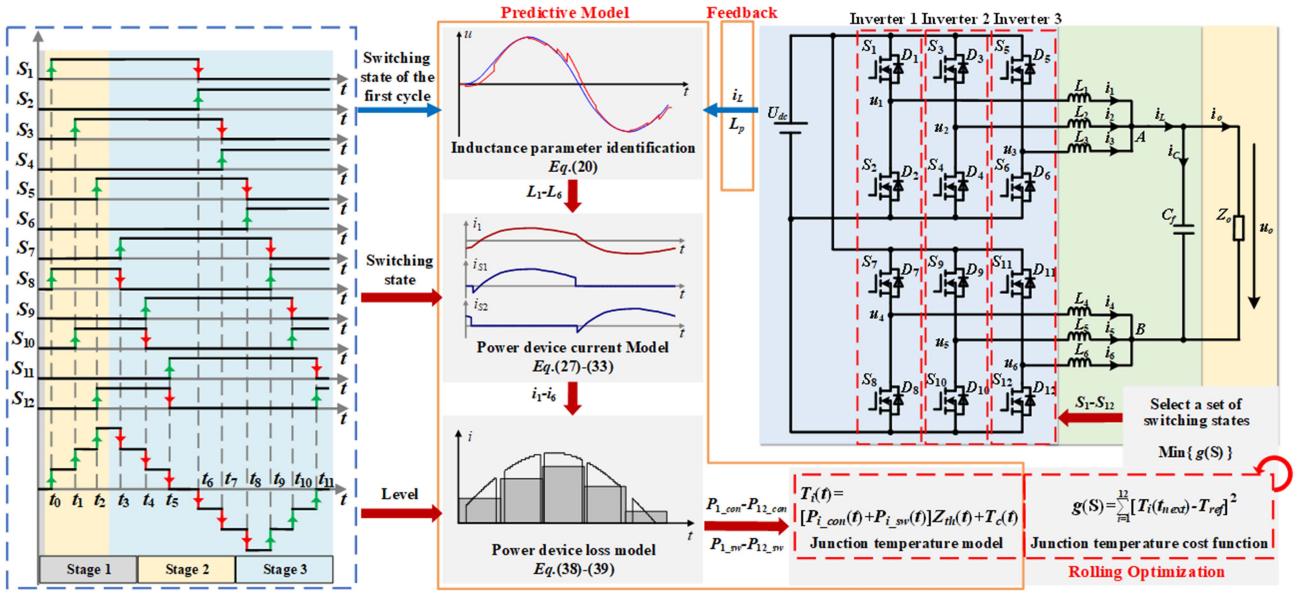

Fig. 5. Block diagram of the thermal balance oriented model predictive control.

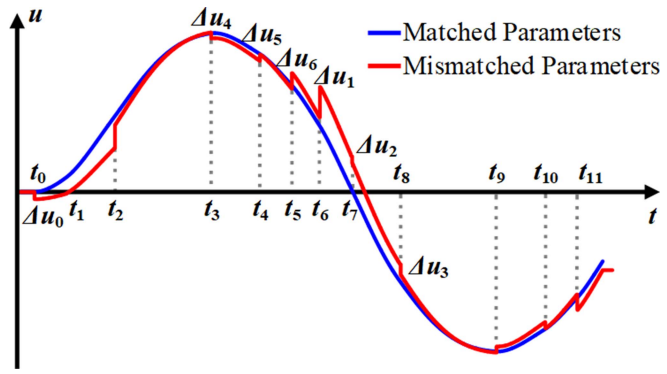

Fig. 6. Estimated output voltage at matched/mismatched parameters.

$$-\frac{L_5L_6u_4(t)+L_4L_6u_5(t)+L_4L_5u_6(t)+L_4L_5L_6\frac{di_L(t)}{dt}}{L_4L_5+L_4L_6+L_5L_6}. \tag{11}$$

In Fig. 5, the three-full-bridge parallel inverter is divided into inverters 1–3. The switching states of the first cycle are designed to identify the inductance parameters, which is divided into three main stages as follows.

Stage 1: Inverters 1–3 are locked, meaning that the control signals of all power devices are OFF.

Stage 2: Inverters 1–3 are operated one by one, meaning that the power devices turn ON in turn.

Stage 3: Inverters 1–3 are fully operational, meaning that at least one power device turns ON in each bridge arm.

In Fig. 5, t_i ($i=0,1,\ldots,11$) represent the switching transition moments in the first cycle. Taking state 4 as an example, the partial expression of the ideal estimated output voltage $u*\ e(t)$ in the first cycle is as follows:

$$u_e^*(t)=\begin{cases} u_1(t)-u_4(t)-2L_p\frac{di_L(t)}{dt}, & t=t_0 \\ \frac{\sum_{j=1}^{3}u_j(t)-\sum_{j=4}^{6}u_j(t)-2L_p\frac{di_L(t)}{dt}}{3}, & t=t_3-t_8 \end{cases}. \tag{12}$$

The change values caused by mismatched inductance parameters at the switching transition moments, which are defined as the output voltage model error $\Delta u^*(t)$

$$\Delta u^*(t)=[u_o(t)-u_o(t-T_e)]-[u_e^*(t)-u_e^*(t-T_e)] \tag{13}$$

where T_e is the estimation period. In Fig. 6, the discretization of the output voltage model error $\Delta u^*(k)$ is as follows:

$$\Delta u^*(k)=\begin{cases} \Delta u_0, & kT_e=t_0 \\ \Delta u_4, & kT_e=t_3 \\ \Delta u_5, & kT_e=t_4 \\ \Delta u_6, & kT_e=t_5 \\ \Delta u_1, & kT_e=t_6 \\ \Delta u_2, & kT_e=t_7 \\ \Delta u_3, & kT_e=t_8 \end{cases} \tag{14}$$

where $\Delta u_j (j=0,1,\ldots,6)$ are the change values of the estimated output voltage at the switching transition moments. The difference values in the change rate of the total inductor current between the adjacent moments are defined as k_j ($j=0,1,\ldots,6$). k_j ($j=0,1,\ldots,6$) at the switching transition moments (the second stage t_0 and the third stage t_3-t_8) in the first cycle are as follows:

$$\frac{i_L(k)+i_L(k-2)-2i_L(k-1)}{T_e}=\begin{cases} k_0, & kT_e=t_0 \\ k_4, & kT_e=t_3 \\ k_5, & kT_e=t_4 \\ k_6, & kT_e=t_5 \\ k_1, & kT_e=t_6 \\ k_2, & kT_e=t_7 \\ k_3, & kT_e=t_8 \end{cases}. \tag{15}$$

TABLE II
SIX FALLING TIME OF EACH STATE

State 1	State 2	State 3	State 4	L_j	Δu^*	k_j
t_1	t_2	t_2	t_3	L_4	Δu_4	k_4
t_3	t_3	t_4	t_4	L_5	Δu_5	k_5
t_5	t_5	t_5	t_5	L_6	Δu_6	k_6
t_6	t_6	t_6	t_6	L_1	Δu_1	k_1
t_8	t_7	t_7	t_7	L_2	Δu_2	k_2
t_{10}	t_{10}	t_9	t_8	L_3	Δu_3	k_3

The first rising time t_0 and the six falling time of each power device are used by inductance parameter identification. The six falling time of each state is given in Table II.

The inductance parameters L_j ($j = 1, 2, \ldots, 6$) are as follows:

$$\begin{cases} -k_0\left(L_1+L_4-2L_p\right)=\Delta u_0 \\ \left(\frac{1}{3}-X_{56}\right)U_{\mathrm{dc}}-k_4\left(L_1X_{23}+L_4X_{56}-\frac{2}{3}L_p\right)=\Delta u_4 \\ \left(\frac{1}{3}-X_{46}\right)U_{\mathrm{dc}}-k_5\left(L_1X_{23}+L_4X_{56}-\frac{2}{3}L_p\right)=\Delta u_5 \\ \left(\frac{1}{3}-X_{45}\right)U_{\mathrm{dc}}-k_6\left(L_1X_{23}+L_4X_{56}-\frac{2}{3}L_p\right)=\Delta u_6 \\ \left(\frac{1}{3}-X_{23}\right)U_{\mathrm{dc}}-k_1\left(L_1X_{23}+L_4X_{56}-\frac{2}{3}L_p\right)=\Delta u_1 \\ \left(\frac{1}{3}-X_{13}\right)U_{\mathrm{dc}}-k_2\left(L_1X_{23}+L_4X_{56}-\frac{2}{3}L_p\right)=\Delta u_2 \\ \left(\frac{1}{3}-X_{12}\right)U_{\mathrm{dc}}-k_3\left(L_1X_{23}+L_4X_{56}-\frac{2}{3}L_p\right)=\Delta u_3 \end{cases} \tag{16}$$

where X_{12}, X_{13}, X_{23}, X_{45}, X_{46}, and X_{56} are the contributions of each bridge arm inductor current to the total inductor current

$$X_{12}=\frac{L_1L_2}{L_1L_2+L_1L_3+L_2L_3}=\frac{1}{3}+\frac{k_3\left(\Delta u_1+\Delta u_2\right)-\left(k_1+k_2\right)\Delta u_3}{U_{\mathrm{dc}}\left(k_1+k_2+k_3\right)} \tag{17}$$

$$X_{13}=\frac{L_1L_3}{L_1L_2+L_1L_3+L_2L_3}=\frac{1}{3}+\frac{k_2\left(\Delta u_1+\Delta u_3\right)-\left(k_1+k_3\right)\Delta u_2}{U_{\mathrm{dc}}\left(k_1+k_2+k_3\right)} \tag{18}$$

$$X_{23}=\frac{L_2L_3}{L_1L_2+L_1L_3+L_2L_3}=\frac{1}{3}+\frac{k_1\left(\Delta u_2+\Delta u_3\right)-\left(k_2+k_3\right)\Delta u_1}{U_{\mathrm{dc}}\left(k_1+k_2+k_3\right)} \tag{19}$$

$$X_{45}=\frac{L_4L_5}{L_4L_5+L_4L_6+L_5L_6}=\frac{1}{3}+\frac{k_6\left(\Delta u_4+\Delta u_5\right)-\left(k_4+k_5\right)\Delta u_6}{U_{\mathrm{dc}}\left(k_4+k_5+k_6\right)} \tag{20}$$

$$X_{46}=\frac{L_4L_6}{L_4L_5+L_4L_6+L_5L_6}=\frac{1}{3}+\frac{k_5\left(\Delta u_4+\Delta u_6\right)-\left(k_4+k_6\right)\Delta u_5}{U_{\mathrm{dc}}\left(k_4+k_5+k_6\right)} \tag{21}$$

$$X_{56}=\frac{L_5L_6}{L_4L_5+L_4L_6+L_5L_6}=\frac{1}{3}+\frac{k_4\left(\Delta u_5+\Delta u_6\right)-\left(k_5+k_6\right)\Delta u_4}{U_{\mathrm{dc}}\left(k_4+k_5+k_6\right)}. \tag{22}$$

B. Power Device Current Model

SiC MOSFETs are selected as the power devices, which can achieve channel conduction in the first quadrant and the third quadrant. Therefore, the current of the power devices depends on the control signals. The diode only conducts during the dead time, which can be neglected. The relationship between the current of power devices and the inductor current is as follows:

$$i_{S(2j-1)}\left(t\right)-i_{S(2j)}\left(t\right)=i_j\left(t\right),\qquad j=1,2,\ldots,6 \tag{23}$$

where $i_{S(2j-1)}(t)$ and $i_{S(2j)}(t)$ ($j = 1, 2, \ldots, 6$) are the current of the upper and the current of lower power devices, respectively. The inductor current of each bridge arm is as follows:

$$i_1\left(t_{\mathrm{now}}\right)=X_{23}i_L\left(t_{\mathrm{now}}\right)+\frac{\int_0^{t_{\mathrm{now}}}\left[\left(L_2+L_3\right)u_1\left(t\right)-L_3u_2\left(t\right)-L_2u_3\left(t\right)\right]dt}{L_1L_2+L_1L_3+L_2L_3} \tag{24}$$

$$i_2\left(t_{\mathrm{now}}\right)=X_{13}i_L\left(t_{\mathrm{now}}\right)+\frac{\int_0^{t_{\mathrm{now}}}\left[\left(L_1+L_3\right)u_2\left(t\right)-L_3u_1\left(t\right)-L_1u_3\left(t\right)\right]dt}{L_1L_2+L_1L_3+L_2L_3} \tag{25}$$

$$i_3\left(t_{now}\right)=X_{12}i_L\left(t_{now}\right)+\frac{\int_0^{t_{now}}\left[\left(L_1+L_2\right)u_3\left(t\right)-L_2u_1\left(t\right)-L_1u_2\left(t\right)\right]dt}{L_1L_2+L_1L_3+L_2L_3} \tag{26}$$

$$i_4\left(t_{\mathrm{now}}\right)=-X_{56}i_L\left(t_{\mathrm{now}}\right)+\frac{\int_0^{t_{\mathrm{now}}}\left[\left(L_5+L_6\right)u_4\left(t\right)-L_6u_5\left(t\right)-L_5u_6\left(t\right)\right]dt}{L_4L_5+L_4L_6+L_5L_6} \tag{27}$$

$$i_5\left(t_{\mathrm{now}}\right)=-X_{46}i_L\left(t_{\mathrm{now}}\right)+\frac{\int_0^{t_{\mathrm{now}}}\left[\left(L_4+L_6\right)u_5\left(t\right)-L_6u_4\left(t\right)-L_4u_6\left(t\right)\right]dt}{L_4L_5+L_4L_6+L_5L_6} \tag{28}$$

$$i_6\left(t_{\mathrm{now}}\right)=-X_{45}i_L\left(t_{\mathrm{now}}\right)+\frac{\int_0^{t_{\mathrm{now}}}\left[\left(L_4+L_5\right)u_6\left(t\right)-L_5u_4\left(t\right)-L_4u_5\left(t\right)\right]dt}{L_4L_5+L_4L_6+L_5L_6} \tag{29}$$

where t_{now} is the current moment. The bridge arm inductor current can be obtained by piecewise constant integration of the output voltage, and only the total inductor current needs to be sampled, which reduces the number of current sensors.

C. Junction Temperature Model

The average junction temperature and the junction temperature swing are two important indicators for the thermal reliability of power devices. The junction temperatures of power devices $T_i(t)$ ($i = 1, 2, \ldots, 12$) are expressed as follows:

$$T_i\left(t\right)=\left[P_{i\_\mathrm{con}}\left(t\right)+P_{i\_\mathrm{sw}}\left(t\right)\right]Z_{th}\left(t\right)+T_c\left(t\right) \tag{30}$$

where $P_{i\_\mathrm{con}}(t)$ and $P_{i\_\mathrm{sw}}(t)$ $(i=1,2,\ldots,12)$ are the conduction losses and switching losses of power devices, respectively, $T_c(t)$ is the case temperature, $Z_{th}(t)$ is the thermal impedance between the power device and the case. The thermal impedance $Z_{th}(t)$ is as follows:

$$Z_{th}(t) = R_{th}\left(1 - e^{-\frac{t}{\tau_{th}}}\right) \tag{31}$$

where τ_{th} is the time constant depending on the thermal resistance R_{th} and the thermal capacity C_{th}

$$\tau_{th}=R_{th}C_{th}. \tag{32}$$

The junction temperature can be discretized to calculate the junction temperature swing

$$\Delta T_i(k) = \Delta T_c(k)$$
$$\sum_{q=1}^{k}\left[P_{i\_\mathrm{con}}(q) + P_{i\_\mathrm{sw}}(q)\right]R_{th}\left(1 - e^{-\frac{\Delta t}{\tau_{th}}}\right)e^{-\frac{(k-q)\Delta t}{\tau_{th}}} \tag{33}$$

where $\Delta T_i(k)$ is the junction temperature swing of the power device at moment k, $\Delta T_c(k)$ is the temperature change of the case at moment k, and Δt is the discretized time interval. The periodic junction temperature swing is significantly affected by the output frequency. When the output frequency reaches kHz, the periodic junction temperature swing can be ignored. The conduction loss predictive values $P_{i\_\mathrm{con}}(t_{\mathrm{next}})$ are as follows:

$$P_{i\_\mathrm{con}}(t_{\mathrm{next}}) = \begin{cases} P_{i\_\mathrm{con}}(t_{\mathrm{now}}) + \frac{t_{\mathrm{next}}-t_{\mathrm{now}}}{T_o}R_{ds}i_{Si}^2(t_{\mathrm{now}}), & S_i \text{ is ON} \\ P_{i\_\mathrm{con}}(t_{\mathrm{now}}), & S_i \text{ is OFF} \end{cases} \tag{34}$$

where t_{next} is the next switching time, R_{ds} is the ON-resistance of SiC MOSFET. When the power device current is positive, turn-on and turn-off losses will occur at the moments of turning ON and OFF, respectively. When the power device current is negative, there is no switching loss at the switching moments. The switching loss predictive values $P_{i\_\mathrm{sw}}(t_{\mathrm{next}})$ are as follows:

$$P_{i\_\mathrm{sw}}(t_{\mathrm{next}}) = \begin{cases} P_{i\_\mathrm{sw}}(t_{\mathrm{now}}) + \frac{E_{\mathrm{on}}[i_{Si}(t_{\mathrm{now}})]}{T_o}, & S_i \text{ turns on} \\ & i_{Si}(t) > 0 \\ P_{i\_\mathrm{sw}}(t_{\mathrm{now}}) + \frac{E_{\mathrm{off}}[i_{Si}(t_{\mathrm{now}})]}{T_o}, & S_i \text{ turns off} \\ & i_{Si}(t) > 0 \\ P_{i\_\mathrm{sw}}(t_{\mathrm{now}}), & \text{else} \end{cases} \tag{35}$$

where $E_{\mathrm{on}}[i_{Si}(t_{\mathrm{now}})]$ and $E_{\mathrm{off}}[i_{Si}(t_{\mathrm{now}})]$ are the turn-ON and turn-OFF energy of the power device current $i_{Si}(t_{\mathrm{now}})$ at the current moment t_{now}, respectively.

D. Cost Function

There are several key steps of cost function.

1) The cost function is calculated only at the optimal switching angles, and the cost function is calculated at most 6 times at each optimal switching angle.
2) Based on the optimal states and the optimal switching angles calculated by OPPs, the switching states of power devices are redistributed at a specific level.

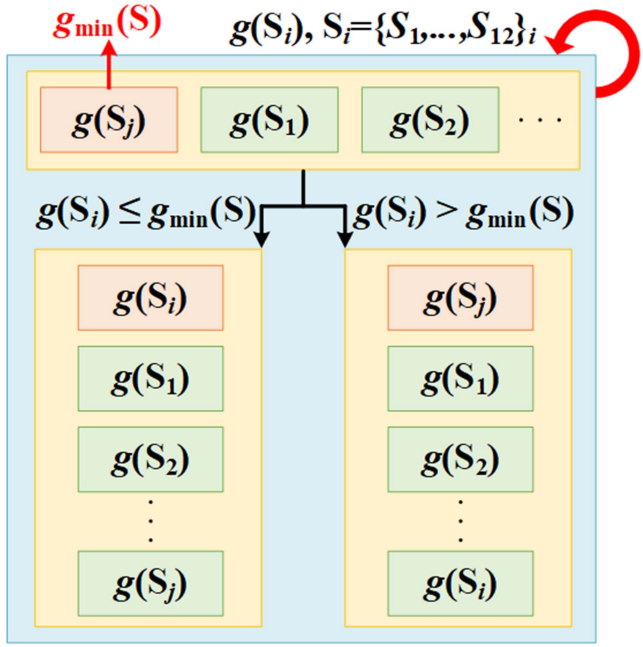

Fig. 7. Implementation steps of rolling optimization.

3) The thermal coupling between the devices has little effect on the switching sequences with the limited calculation times.

The junction temperature cost function should ensure that the junction temperatures of the power devices are balanced. The junction temperature cost function $g(S)$ is expressed as follows:

$$g(S) = \sum_{i=1}^{12}\left[T_i(t_{\mathrm{next}}) - T_{\mathrm{ref}}\right]^2 \tag{36}$$

where T_{ref} is the reference of the average junction temperature. The expression of the reference of the average junction temperature T_{ref} is as follows:

$$T_{\mathrm{ref}} = (1-\eta)P_oR_{th} + T_c \tag{37}$$

where η is the efficiency, P_o is the output power. The efficiency η takes the value of 95%.

The optimization process is a rolling optimization. There are some sets of switching states in the finite set, and the switching states are substituted into the cost function. A set of switching states is selected to minimize the cost function. The implementation steps are shown in Fig. 7.

When the level is determined, the switching state of each power device is the switching distribution, and the number of switching distribution directly determines the calculation number of the cost function. When the level is 3/-3, the number of switching distribution is 1. When the level is 2/-2, the number of switching distribution is 6. When the level is 1/-1, the number of switching distribution is 15. When the level is 0, the number of switching distribution is 20. Taking level of 0 as an example, when the power device with the largest loss is OFF, and the power device with the smallest loss is ON, the maximum number of switching distribution is 6. The cost function is

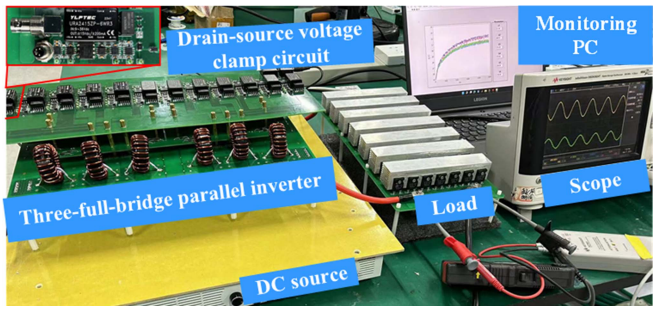

Fig. 8. Three-full-bridge parallel inverter experimental platform.

TABLE III
EXPERIMENTAL PARAMETERS AND HARDWARE COMPONENTS

Parameter	Value
DC voltage U_{DC}/V	400
Inductor L_p/μH	40
Filter capacitor C_f/nF	16
Resistance R_o/Ω	30
Modulation index M	0.1-1.0
Output frequency f_o/kHz	100
SiC Mosfet	CCS050M12CM2
Isolated Gate Driver	CGD15FB45P
Field Programmable Gate Array (Controller)	EP4CE10E22C8
Flash Memory	M25P64VMF

calculated at most six times at each optimal switching angle. Altera EP4CE10E22C8 with 10320 logic elements available and Quartus II software v13.0 are used, and the clock of field programmable gate array is set to 200 MHz by using phase locked loop. The calculation time of the cost function takes up a maximum of 6 clock cycles at each optimal switching angle.

IV. EXPERIMENTAL VERIFICATION

To verify the effectiveness of TBOMPC, the three-full-bridge parallel inverter experimental platform is built in Fig. 8. The junction temperatures of power devices are measured by drain-source voltage clamp circuit in Fig. 8. The experimental parameters and hardware components are given in Table III.

A. Matched Parameters

TBOMPC is based on the states and the switching angles calculated by OPPs, so TBOMPC maintains consistent THD with OPPs as shown in Fig. 9.

The measurement error causes the difference in the THD between the OPPs and TBOMPC. The difference is within the acceptable range. The fundamental voltage at low modulation index is low, so the difference of low modulation index is higher than that of high modulation index. When the modulation index is more than 0.4, the THD of TBOMPC is less than 3%. Therefore, the output performance of TBOMPC can meet the application requirements.

When the inductance parameters L_j ($j = 1, 2, \ldots, 6$) are the setting value L_p, the maximum junction temperature differences of OPPs and TBOMPC are shown in Fig. 10. The maximum

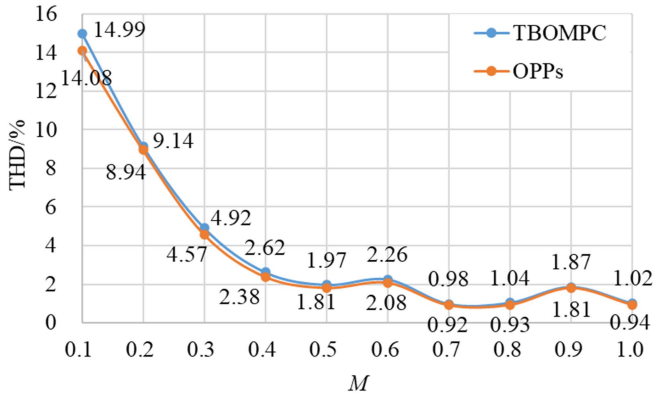

Fig. 9. THD of OPPs and TBOMPC.

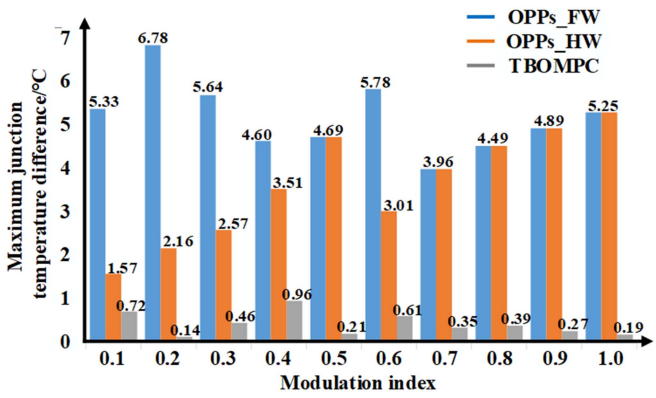

Fig. 10. Maximum junction temperature differences of OPPs and TBOMPC.

junction temperature differences of OPPs are basically between 4°C and 6°C. The maximum junction temperature difference of OPPs even reaches 6.78°C at the modulation index of 0.2. TBOMPC can keep the maximum junction temperature differences during the full modulation index range within 1.0°C.

When the modulation index is 1.0, the junction temperature waveforms of OPPs and TBOMPC with matched parameters are shown in Fig. 11. TBOMPC can balance the junction temperatures with matched parameters. The switching states of TBOMPC is adjusted with the junction temperature, and the switching frequency of TBOMPC is more than that of OPPs. Meanwhile, the maximum carrier ratio of TBOMPC is still low.

B. Mismatched Parameters

Considering the consistency and the cost, the inductance parameter mismatches are allowed. The manufacturing process of magnetic core is the main reason for the inductance parameter mismatches. The parameter mismatches can reach up to 25%.

The theoretical inductance parameters L^* are set to 30–50 uH. The OCs of parameter mismatches are given in Table IV. The inductance parameters in the three-full-bridge parallel inverter experimental platform are the actual inductance parameters L_a. The actual inductance parameters L_a are measured by an

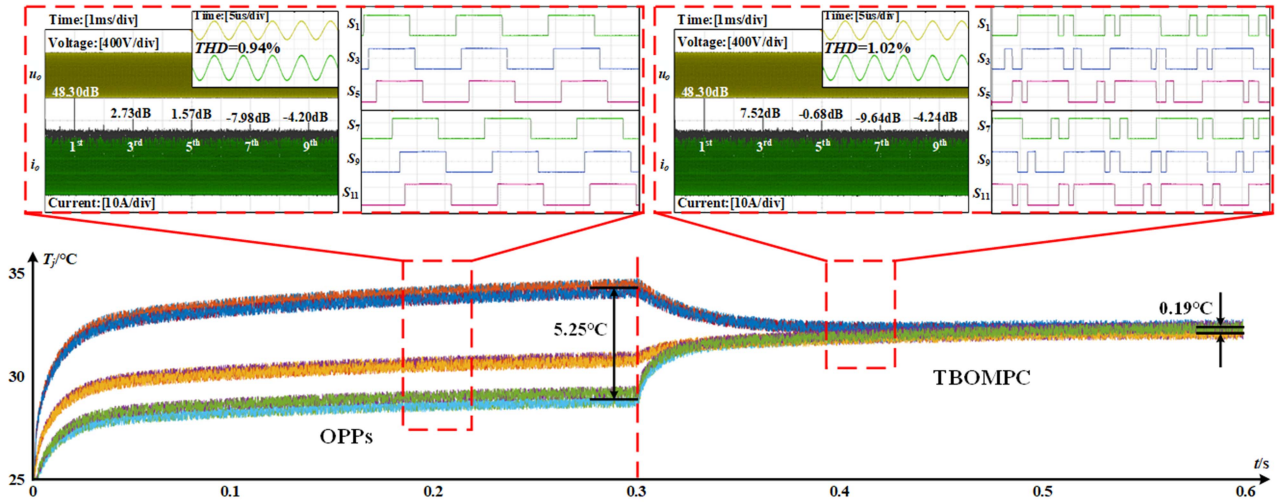

Fig. 11. Output voltage, output current, switching sequences and junction temperature waveforms of TBOMPC and OPPs with matched parameters: 40 uH/40 uH/40 uH/40 uH/40 uH/40 uH.

TABLE IV
OPERATING CONDITIONS OF PARAMETER MISMATCHES

OCs	Parameters	1	2	3	4	5	6
1	L^*/uH	30	40	40	40	40	40
	L_a/uH	30.23	40.55	39.64	40.20	41.1	41.8
	L_e/uH	31.04	40.53	39.28	39.86	40.28	40.68
	L_{Dev}/%	2.68	0.06	0.91	0.84	1.99	2.68
2	L^*/uH	30	40	50	50	40	30
	L_a/uH	30.23	40.55	49.03	52.08	39.64	29.88
	L_e/uH	29.76	39.66	49.69	50.24	40.61	30.53
	L_{Dev}/%	1.57	2.19	1.35	3.53	2.44	2.17

impedance meter in advance, and the actual inductance parameters L_a are as close to the theoretical inductance parameters L^* as possible. The inductance parameters L_e are estimated by TBOMPC. The deviation L_{Dev} between the actual inductance parameters L_a and the estimated inductance parameters L_e is as follows:

$$L_{\text{Dev}} = \frac{|L_a - L_e|}{L_a} \times 100\%. \tag{38}$$

It can be seen from Table IV that there are multiple inductance parameter mismatches. The deviation between the actual inductance parameters L_a and the estimated inductance parameters L_e is within an acceptable range with a maximum of 3.53%. TBOMPC can effectively identify the inductance parameters.

Under the typical OCs, the output voltage, output current and junction temperature waveforms of TBOMPC and OPPs are shown in Figs. 12 and 13. The output voltage and output current waveforms of TBOMPC are the same as those of OPPs. The modulation index changes from 0.6 to 1.0 in Fig. 12, and the modulation index changes from 1.0 to 0.8 in Fig. 13. The junction temperatures of power devices $T_i(t)$ ($i = 1, 2, \ldots, 12$) are defined as T_j in Figs. 12 and 13. The junction temperature data can be obtained once per switching period (a small amount of unreasonable data is eliminated).

In Fig. 12, the third, fifth, and seventh output voltage harmonics are the main harmonic content at the modulation index of 0.6, and the third and fifth output voltage harmonics are the main harmonic content at the modulation index of 1.0. In Fig. 13, the third and fifth output voltage harmonics are the main harmonic content at the modulation index of 1.0, and the third output voltage harmonic is the main harmonic content at the modulation index of 0.8. Under the two OCs, the output voltage harmonics are greatly affected by inductance parameters. The higher the parameter mismatches, the worse the THD. THD is still less than 3% with mismatched parameters, which ensures the application effect of TBOMPC.

Under OC 1, only inductance parameter L_1 is reduced by 25%. When the modulation index changes from 0.6 to 1.0, the maximum junction temperature differences of OPPs are 8.24°C, and 7.40°C, respectively, in Fig. 12. Under OC 2, the inductance parameters L_1 and L_6 are reduced by 25%, and the inductance parameters L_3 and L_4 are increased by 25%. When the modulation index changes from 1.0 to 0.8, the maximum junction temperature differences of OPPs are 6.23°C, and 7.28°C, respectively, in Fig. 13. The maximum junction temperature differences of OPPs with mismatched parameters are larger than those of OPPs with matched parameters. The mismatched parameters make the temperature differences of OPPs more imbalanced.

The inductance difference is the main influencing factor of the maximum junction temperature difference, but the maximum junction temperature difference does not necessarily increase with the increase of inductance difference. When the modulation index is 1.0, the maximum junction temperature difference of OC 1 is larger than that of OC 2. Inverters 1–3 are operated one by one, meaning that the power devices turn ON in turn. The junction temperatures of power devices (S_1, S_7) are the largest, and the junction temperatures of power devices (S_5, S_{11}) are the smallest. In OC 1, L_1 (Inverter 1, S_1) decreases and the maximum

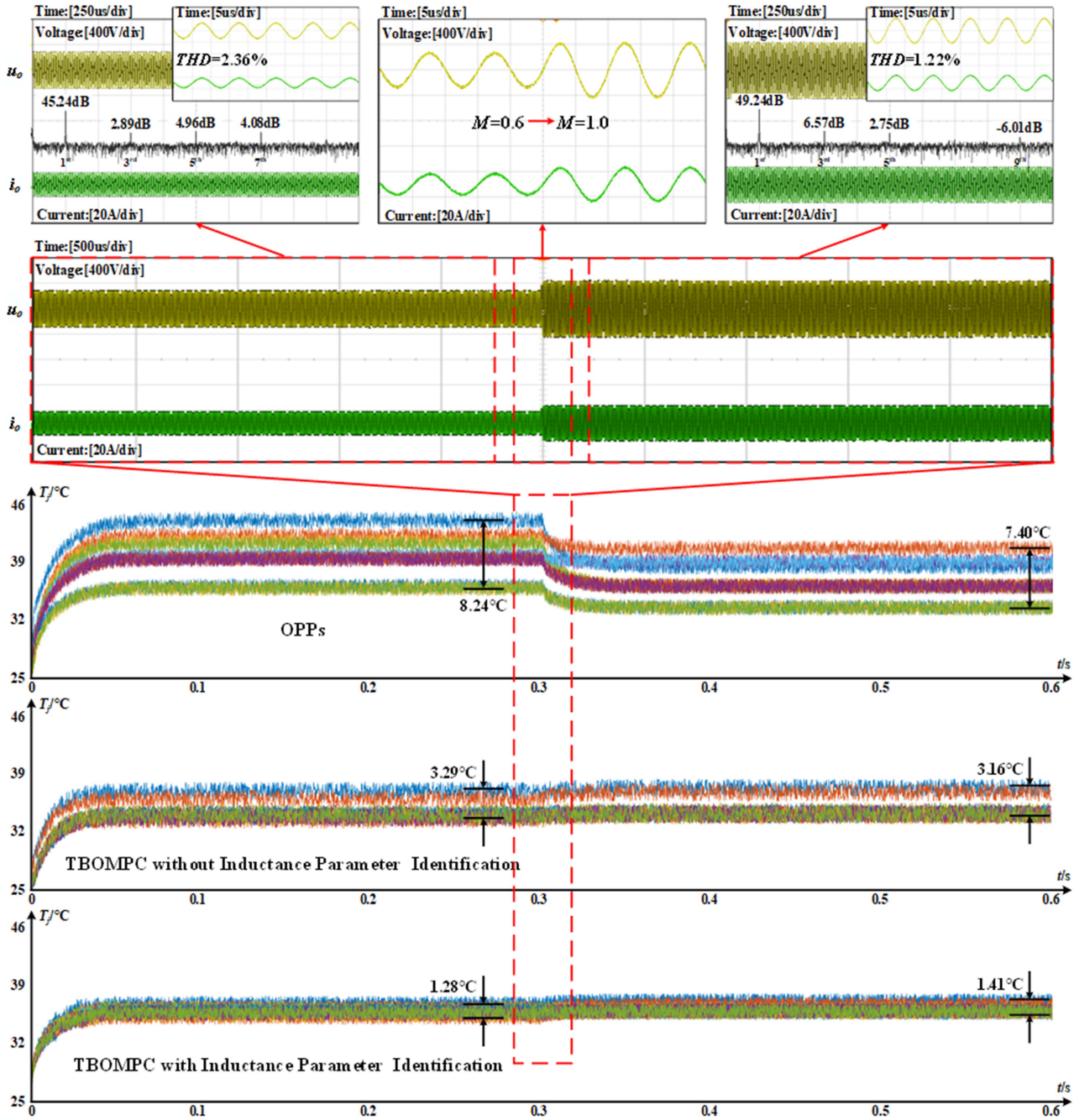

Fig. 12. Output voltage, output current and junction temperature waveforms of TBOMPC and OPPs under operating condition 1: 30 uH/40 uH/40 uH/40 uH/40 uH/40 uH.

junction temperature difference increases. Although L_1 (inverter 1, S_1) decreases in OC 2, L_4 (inverter 1, S_7) increases and L_6 (inverter 3, S_{11}) decreases. The maximum junction temperature difference of OC 2 can be smaller than that of OC 1.

Low carrier ratio causes the junction temperature in low modulation index higher than that in high modulation index. The output current of the three-full-bridge parallel inverter is high in high modulation index, but the power device current is not high in high modulation index. The state of modulation index 0.6 is state 3, and the state of modulation index 0.8 and 1.0 is state 4. In Fig. 2, the turn-ON interval between S_3 and S_5 in state 3 is larger than that in state 4, so the current of power devices (S_1, S_3) in state 3 is larger than that in State 4, and the current of power devices (S_5) in state 3 is smaller than that in state 4. In state 4, the larger the modulation index, the shorter the turn-on interval of each power device. RMS values of each power device current are listed in Table V under different OCs and different modulation indexes.

When the inductance parameters are mismatched and modulation indexes are changed, the maximum junction temperature

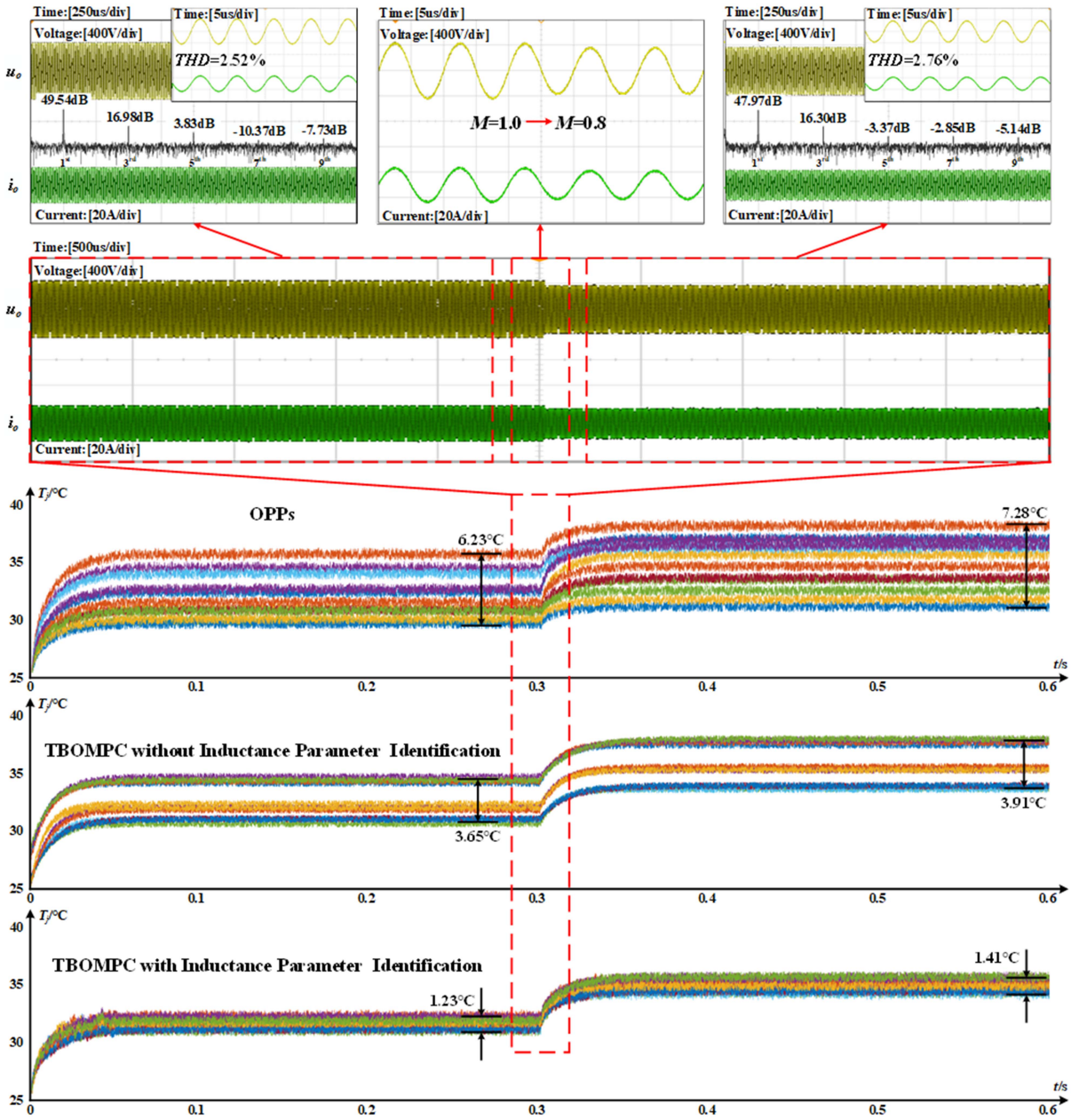

Fig. 13. Output voltage, output current and junction temperature waveforms of TBOMPC and OPPs under operating condition 2: 30 uH/40 uH/50 uH/50 uH/4 0uH/30 uH.

TABLE V
RMS VALUES OF EACH POWER DEVICE CURRENT

OCs	M	S_1	S_3	S_5	S_8	S_{10}	S_{12}
1	0.6	8.44 A	7.73 A	5.47 A	6.80 A	6.37 A	5.61 A
	1.0	5.13 A	4.68 A	2.24 A	2.99 A	4.23 A	4.24 A
2	0.8	6.78 A	5.75 A	2.03 A	2.82 A	5.20 A	5.51 A
	1.0	5.56 A	4.32 A	1.89 A	2.44 A	4.06 A	4.88 A

differences of TBOMPC with inductance parameter identification are 1.28°C, 1.41°C, 1.23°C, and 1.41°C, respectively. The maximum junction temperature differences are less than 1.5°C, which are within an acceptable range. Compared with OPPs, TBOMPC with inductance parameter identification effectively reduces the maximum junction temperature differences.

To highlight the usefulness of the inductance parameter identification, the results of TBOMPC without inductance parameter identification are also shown in Figs. 12 and 13. TBOMPC without inductance parameter identification is affected by the inductance parameters, and the maximum junction temperature differences of TBOMPC without inductance parameter identification are more than 3.0°C. When the degree of mismatched parameter is different, the difference between the maximum junction temperature difference of TBOMPC without inductance parameter identification is large. Compared with TBOMPC without inductance parameter identification, TBOMPC with

inductance parameter identification provides better ability to handle parameter mismatches. Therefore, TBOMPC with inductance parameter identification can maintain a good temperature balance with different inductance parameters and modulation indexes.

V. Conclusion

TBOMPC in this article balanced the junction temperatures of the power devices. The maximum junction temperature difference of OPPs was 6.78°C with matched parameters. The maximum temperature differences of OPPs were greatly affected by inductance parameters. The maximum junction temperature difference of OPPs was even more than 8°C with mismatched parameters. TBOMPC improved the thermal balance issue of OPPs in the following ways.

1) TBOMPC could identify the inductance parameters by the designed first cycle. The maximum deviation between the actual inductance parameter and the estimated inductance parameter was only 3.53%.
2) TBOMPC could redistribute switching states based on OPPs by cost function. The maximum junction temperature differences of TBOMPC were within 1.5°C with matched/mismatched parameters.

Therefore, TBOMPC could accurately identify inductance parameters and reasonably balance the junction temperatures of power devices.

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