Reliability Improved Discontinuous Pulse Width Modulation for NPC Inverters Operated at High Modulation Index

Dong-Jin Lee, *Student Member, IEEE*, Jae-Heon Choi, *Student Member, IEEE*, and Ui-Min Choi, *Senior Member, IEEE*

***Abstract*—In a three-level neutral point clamped (NPC) inverter, the power devices and dc-link capacitors are considered the most reliability-critical components, and their wear-out failure is primarily caused by thermal loading resulting from power losses. It has been found in a previous study that a discontinuous pulse width modulation (DPWM) reduces the power loss and improves the reliability of power devices. However, it reduces the reliability of the dc-link capacitors, and thus the reliability of the NPC inverter. This article proposes a DPWM method called reliability improved DPWM (RI-DPWM) to improve the reliability of the NPC inverter by reducing the thermal loadings of both the power devices and dc-link capacitors while keeping the advantage of the conventional DPWM, reducing the power loss without additional deterioration in output current total harmonic distortion compared with conventional DPWM. The proposed RI-DPWM method is a good alternative to the conventional DPWM to improve the efficiency and reliability of the NPC inverter operated at high modulation index which is greater than or equal to 0.898 with a power factor of 1 or close to 1. The effectiveness of the proposed method is verified through simulations and experiments.**

***Index Terms*—Capacitor, discontinuous pulse width modulation (DPWM), neutral point clamped (NPC) inverter, power device, photovoltaic (PV) inverter, PV system, pulse width modulation (PWM), reliability.**

I. Introduction

GLOBAL warming is mainly caused by greenhouse gas (GHG) emissions, with 20 gigatons of carbon dioxide equivalent ($GtCO_2$-eq) originating from the global energy system, constituting 34% of total GHG emissions [1]. The most effective alternative to reducing GHG emissions is renewable energy generation, with photovoltaic (PV) energy generation being the most promising among GHG emission mitigation options. PV energy generation has the most potential among GHG emission mitigation options, and PV energy generation capacity has grown by more than 20% over the past decade [1], [2]. To substitute conventional fossil fuel generation, PV energy generation needs to achieve a more competitive levelized cost of energy (LCOE). Improving the reliability of PV energy systems leads to lower LCOE because it reduces operation and maintenance costs and increases annual energy production [3].

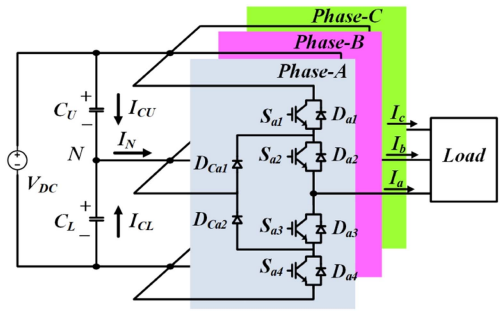

Fig. 1. Structure of a three-level NPC inverter.

According to the previous research in [4] and [5], PV inverters are considered one of the reliability-critical parts of PV systems. Furthermore, the wear-out failures of power devices and capacitors caused by thermal stress are generally regarded as one of the main causes of failure of inverters. Thus, much research has been performed to improve the reliability of the PV inverter by increasing the lifetime of the power devices and capacitors.

Fig. 1 shows the configuration of a three-level neutral point clamped (NPC) inverter. The NPC inverter is widely utilized in power electronic applications, including renewable generation systems, due to its advantages. These advantages include high efficiency, low total harmonic distortion (THD), and use of power devices with lower rated voltage compared with the conventional two-level inverter [6], [7]. However, the NPC inverter has an imbalanced power loss distribution among power devices. Furthermore, it has a low-frequency ripple current in the dc-link capacitors due to its structure, which contributes to the power loss of the dc-link capacitors.

Since the pulse width modulation (PWM) affects the performance of the inverter, much research has been performed on reducing the thermal stress of the power device and capacitor

Received 4 October 2024; revised 17 December 2024 and 26 January 2025; accepted 25 February 2025. Date of publication 4 March 2025; date of current version 14 April 2025. This work was supported in part by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) under Grant 2022R1A2C1091791 and in part by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) and the Ministry of Trade, Industry and Energy (MOTIE) of the Republic of Korea under Grant RS-2023-00266248. Recommended for publication by Associate Editor M. Novak. *(Corresponding author: Ui-Min Choi.)*

The authors are with the Department of Smart ICT Convergence Engineering, Seoul National University of Science and Technology, Seoul 01811, South Korea (e-mail: 23512113@seoultech.ac.kr; 21512098@seoultech.ac.kr; uch@seoultech.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3547374.

Digital Object Identifier 10.1109/TPEL.2025.3547374

by decreasing their power loss through the PWM methods. In [8] and [9], the discontinuous PWM (DPWM) methods are proposed to reduce not only the power loss but also the thermal stress of the power device. However, as analyzed in [10], the DPWM increases the thermal stress in the dc-link capacitors because the high ripple current occurs in the dc-link capacitors. Various PWM methods to reduce the thermal stress of dc-link capacitors are proposed in [11], [12], and [13]. The main idea of these PWM methods is to replace the voltage vectors causing a large dc-link capacitor current with other vectors. However, these PWM methods cannot decrease the power loss of the power devices and their junction temperature at the same time. The hybrid PWM method proposed in [13] even increases the switching loss of the power devices. Applying the above PWM methods also deteriorates the THD of the output current more than that of conventional DPWM.

This article proposes a discontinuous PWM method called reliability improved DPWM (RI-DPWM) for improving the reliability of both dc-link capacitors and power devices compared with a conventional space vector modulation (SVM) and the conventional DPWM so that both the reliability and efficiency of the three-level NPC inverter are improved. The initial study based on the simulation has been performed in [10]. Through the proposed RI-DPWM method, the reliability of the dc-link capacitor is significantly improved, but its negative effects on the reliability and efficiency of the power devices are negligible compared with conventional DPWM. Therefore, the advantages of DPWM in terms of efficiency and lifetime improvements of power devices are maintained. The proposed RI-DPWM method is a good alternative to the conventional DPWM to improve the efficiency and reliability of the NPC inverter operated at high modulation index, which is greater than or equal to 0.898 with a power factor of 1 or close to 1. The feasibility and effectiveness of the proposed RI-DPWM method are assessed through simulation and experiments, comparing it with conventional SVM and DPWM, and other PWM methods.

II. Thermal Loading Analysis of Power Devices and Capacitor

A. Power Losses of Power Device and Capacitor

The junction temperature (T_j) of the power device and the hot-spot temperature (T_{hot}) of the capacitor are determined by their power loss, and they can be modeled by the Foster thermal model [14]. The power loss of power device ($P_{\text{loss\_device}}$) is represented by a sum of the conduction loss (P_{cond}) and switching loss (P_{sw}) as

$$P_{\text{loss\_device}} = P_{\text{cond}} + P_{\text{sw}}. \tag{1}$$

The average conduction and switching losses for the switching period are expressed as (2) given in [15]

$$P_{\text{cond}} = \frac{1}{T_s}\int_0^{T_S} V_{\text{CE}(i_C,\,T_j)} \cdot i_c \, dt = V_{\text{CE}(i_C,\,T_j)} \cdot i_c \cdot D$$
$$P_{\text{sw}} = f_{\text{sw}} \cdot E_{\text{sw(ref)}} \left(\frac{i_c}{I_{c(\text{ref})}}\right)^{ki} \left(\frac{v_{cc}}{V_{cc(\text{ref})}}\right)^{kv} \tag{2}$$

where V_{CE} is ON-state collector-emitter voltage (V_{CE}), i_c is the collector current, T_s is the switching period, duty cycle (D) of the switching period, f_{sw} is the switching frequency, $E_{\text{sw(ref)}}$ is the reference value of the switching energy, $I_{c(\text{ref})}$ and $V_{cc(\text{ref})}$ are the reference collect current and the reference collector-emitter voltage at the measurement condition, v_{cc} is the actual collector-emitter voltage, and k_i and k_v are the constants that represent the current and voltage dependency of switching losses, respectively and can be found in [15].

The power loss of the capacitor ($P_{\text{loss\_cap}}$) is determined by the equivalent series resistance (ESR) of the capacitor and root-mean-square (RMS) value of the capacitor current (I_{cap}), and it is given as

$$P_{\text{loss\_cap}} = \sum_{i=1}^{m} \left[\text{ESR}\left(f_i, T_{\text{hot}}\right) \cdot I_{\text{cap}}^2\left(f_i\right)\right]. \tag{3}$$

Since ESR has different values depending on the frequency, $P_{\text{loss\_cap}}$ must be calculated as ESR and current value at specific frequency f_i. ESR is decreased as the frequency increases. Furthermore, it is T_{hot} dependent. Therefore, it needs to be considered. The dependency of ESR on f_i and T_{hot} is evaluated by the manufacturer and provided through the datasheet [16].

B. Thermal Loadings of Power Device and Capacitor

T_j of the power device is obtained as

$$T_j(t) = P_{\text{loss\_device}}(t) \cdot Z_{th(j-h)}(t) + P_{\text{loss\_}m}(t) \cdot Z_{th(h-a)}(t) + T_a(t) \tag{4}$$

where $P_{\text{loss\_}m}$ is the power loss of the power device module, T_a is the ambient temperature, $Z_{th(j-h)}$ and $Z_{th(h-a)}$ are the thermal impedances from the junction to heat sink, and the thermal impedance from the heat sink to ambient, respectively.

T_{hot} of the capacitor can be expressed as

$$T_{\text{hot}}(t) = T_a(t) + Z_{th(hs-a)}(t) \cdot P_{\text{loss\_cap}}(t) \tag{5}$$

where $Z_{th(hs-a)}$ is the thermal impedance from the hot-spot to the ambient.

The thermal impedance for both the power device and capacitor can be expressed as

$$Z_{th}(t) = \sum_{i=1}^{n} R_{th_i}\left(1 - e^{-\frac{t}{\tau_i}}\right), \ (\tau_i = R_{th_i} \cdot C_{th_i}) \tag{6}$$

where R_{th} and C_{th} are the thermal resistance and capacitance, respectively and i denotes the different layers of the Foster model.

III. Pulse Width Modulation Methods of Three-Level NPC Inverter

As shown in Fig. 1, the neutral point current (I_N) is a sum of the upper capacitor current (I_{CU}) and the lower capacitor current (I_{CL}). The magnitudes of I_{CU} and I_{CL} are identical when their capacitances are the same, and it is expressed as

$$I_N = I_{\text{CU}} + I_{\text{CL}}. \tag{7}$$

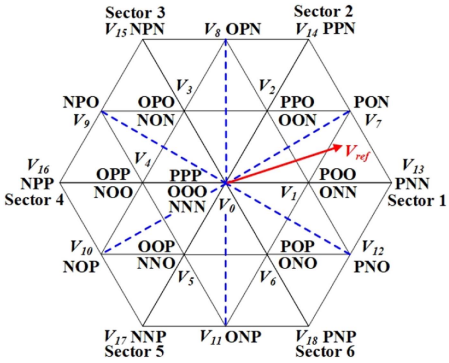

Fig. 2. Space vector diagram and a reference voltage vector.

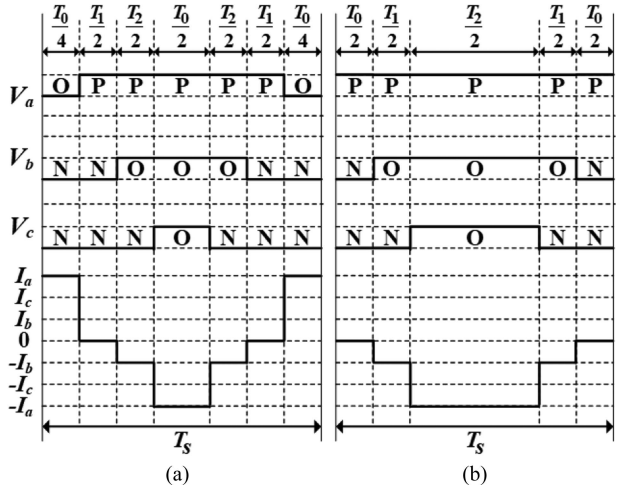

Fig. 3. The switching states and the neutral point current. (a) conventional SVM. (b) conventional DPWM.

However, it is worthwhile mentioning that I_{CU} and I_{CL} do not have the same value simultaneously.

According to the operation of power devices, each leg has the switching states called [P], [O], and [N], and the corresponding pole voltages of $+V_{\mathrm{DC}}/2$, 0, $-V_{\mathrm{DC}}/2$, respectively. The NPC inverter has a total of 27 switching state combinations, which are represented in a space vector diagram as shown in Fig. 2. The space vector diagram is divided into six sectors according to the phase with the highest reference voltage, where the phase current is also the highest if the power factor is 1. In this article, the power factor is considered as 1. According to magnitude, the space vectors are classified by zero, small, medium, and large voltage vectors. They determine I_N because the switching state corresponding to its voltage vector represents the phase connected to the neutral point.

A. Conventional SVM

The conventional SVM selects the voltage vectors that are the closest to the reference voltage vector V_{ref} on the space vector diagram. When V_{ref} is located in sector 1 as shown in Fig. 2, the SVM synthesizes the voltage vectors V_1, V_7, and V_{13} to generate V_{ref}, where the switching sequence is formed as shown in Fig. 3(a) so that the switching state of each phase is changed one time during a switching period T_s. When the switching state is [PNN], $|I_N|$ becomes zero, and when the switching state is [PON], $|I_N|$ is $|I_b|$. When the switching state is [ONN] or [POO], $|I_N|$ is equal to $|I_a|$, which is the highest current among the three-phase currents. Therefore, the small voltage vectors lead to a large capacitor current in any sector.

B. Conventional DPWM

The conventional DPWM also uses the same voltage vectors as the SVM. However, only one type of switching state of small voltage vectors is used to fix the switching state of one phase having the highest output current in the sector to [P] or [N], depending on its polarity. When V_{ref} is in Sector 1, under the DPWM, only the P-type switching state of the small voltage vector [POO] is used in the switching sequence to clamp the switching state of phase-A to [P] as shown in Fig. 3(b). Thus, the switching loss of power devices is reduced compared with the SVM. Especially, the power loss of the outer power devices of $S_{x1,4}$ is reduced, and thus their T_j is decreased. Since the applied voltage vectors and their dwell time are the same, the RMS value of I_N is the same as the SVM. However, compared with the SVM, $P_{\mathrm{loss\_cap}}$ is increased when conventional DPWM is applied as analyzed in [10]. In a switching cycle, the polarity of I_N is changed under the SVM since there are both P-type and N-type switching states of the small voltage vector as shown in Fig. 3(a). However, under the DPWM, the polarity of I_N is kept since there is only one type of switching state of a small voltage vector in a switching cycle during the clamping period. Therefore, the ripple current of the dc-link capacitor under the DPWM has lower frequency components than that under the SVM, which results in an increase in the power loss of the capacitor and thus T_{hot}.

IV. Proposed Discontinuous Pulse Width Modulation Method to Improve Reliability of NPC Inverter

A. Reliability Improved DPWM (RI-DPWM)

The conventional DPWM improves the power device reliability by reducing their T_j. However, it increases the T_{hot} of the dc-link capacitor due to the low-frequency ripple current.

As a result, the reliability of the NPC inverter could be decreased due to the decrease in reliability of the dc-link capacitor. This article proposes an RI-DPWM method, which not only increases the reliability of the capacitor by reducing its T_{hot} but also keeps the advantage of the DPWM in terms of the efficiency and reliability improvement of power devices. The main idea of RI-DPWM is to eliminate the small voltage vector in the switching sequence or to replace it with another small voltage vector so that $|I_N|$ does not become the highest phase current while clamping the switching state of one phase having the highest current. If the V_{ref} is in Sector 1, Sector 1 of the space vector diagram is divided into four regions as shown in Fig. 4. In region 1, V_{ref} is synthesized by V_6, V_{12}, and V_{13}, and therefore, the switching sequence is formed as [POP]-[PNO]-[PNN]-[PNO]-[POP] as shown in Fig. 5(a). In this switching sequence, the switching state of phase-A is clamped to [P], and

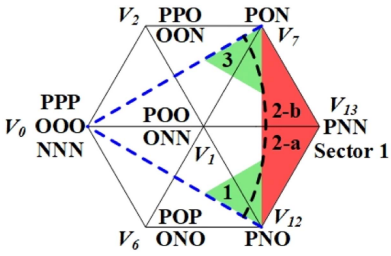

Fig. 4. RI-DPWM in Sector 1.

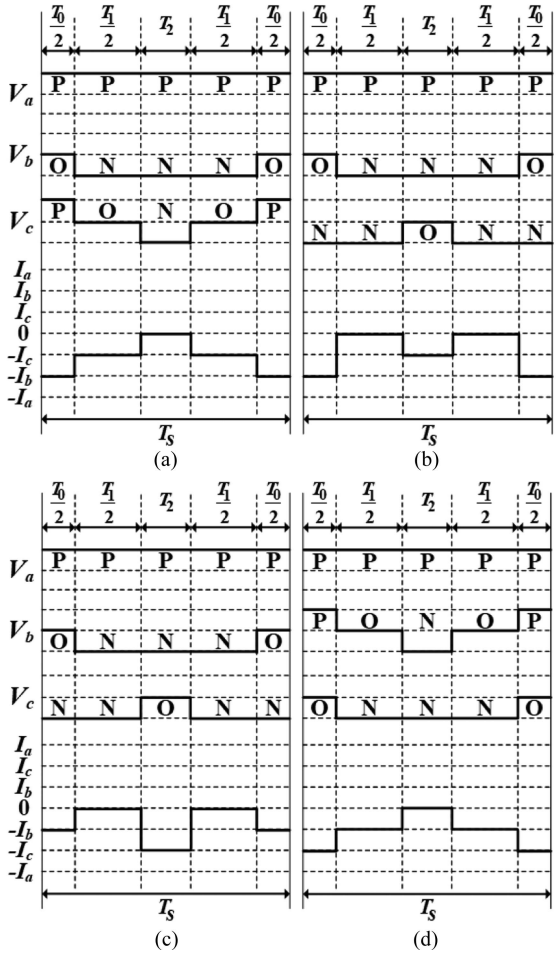

Fig. 5. Switching states and the neutral point current under RI-DPWM. (a) Region 1. (b) Region 2-a. (c) Region 2-b. (d) Region 3.

phase-B and phase-C have the switching state [O], but not at the same time.

It means that the highest current of phase-A does not flow to the neutral point and relatively lower currents of phase-B and phase-C flow to the neutral point. Thus, I_N is reduced as shown in Fig. 5(a). Consequently, the ripple current of the dc-link capacitor is reduced, and thus T_{hot} of the dc-link capacitor decreases. In terms of the power devices, maintaining the switching state of phase-A as [P] leads to a reduction in switching losses. This reduction contributes to improvements in efficiency and a decrease in power device junction temperature. In this switching

TABLE I
SWITCHING SEQUENCES OF RI-DPWM

Sector	Region	Switching sequence
1	1	[POP]-[PNO]-[PNN]-[PNO]-[POP]
	2	[PON]-[PNN]-[PNO]-[PNN]-[PON]
	3	[PPO]-[PON]-[PNN]-[PON]-[PPO]
2	1	[ONN]-[PON]-[PPN]-[PON]-[ONN]
	2	[OPN]-[PPN]-[PON]-[PPN]-[OPN]
	3	[NON]-[OPN]-[PPN]-[OPN]-[NON]
3	1	[PPO]-[OPN]-[NPN]-[OPN]-[PPO]
	2	[NPO]-[NPN]-[OPN]-[NPN]-[NPO]
	3	[OPP]-[NPO]-[NPN]-[NPO]-[OPP]
4	1	[NON]-[NPO]-[NPP]-[NPO]-[NON]
	2	[NOP]-[NPP]-[NPO]-[NPP]-[NOP]
	3	[NNO]-[NOP]-[NPP]-[NOP]-[NNO]
5	1	[OPP]-[NOP]-[NNP]-[NOP]-[OPP]
	2	[ONP]-[NNP]-[NOP]-[NNP]-[ONP]
	3	[POP]-[ONP]-[NNP]-[ONP]-[POP]
6	1	[NNO]-[ONP]-[PNP]-[ONP]-[NNO]
	2	[PNO]-[PNP]-[ONP]-[PNP]-[PNO]
	3	[ONN]-[PNO]-[PNP]-[PNO]-[ONN]

sequence, the switching state of phase-C is changed two times in a switching cycle. Therefore, its switching loss is increased. However, it is not significant because the current of phase-C is the smallest in this region. In other words, the amount of decreased switching loss of phase-A is greater than the amount of increased switching loss of phase-C. V_{ref} is composed of V_7, V_{12}, and V_{13} and V_2, V_7, and V_{13} in region 2 and region 3, respectively. The switching sequences in these regions are represented in Fig. 5(b), (c), and (d). In all switching sequences of Sector 1, phase-A is fixed to the switching state [P], and its phase current does not flow to the neutral point. Therefore, the power loss reductions in both the capacitor and power device are achieved.

The switching sequences of RI-DPWM in all sectors are given in Table I. In all switching sequences, the switching state of the phase having the highest current is clamped, and its current does not flow to the neutral point. The dwell times of the voltage vectors for the switching sequence of each region are obtained from Table II, where θ_r is the angle between V_{ref} and the large voltage vectors, and its range is from -30° to +30°. The equations given in Table II can be applied to all sectors.

It is worth mentioning that the proposed RI-DPWM can be applied when the modulation index is greater than or equal to 0.898, as indicated by the black dotted line in Fig. 4, where the modulation index is defined as $\sqrt{3}\ V_{\text{ref}} / V_{\text{DC}}$. However, it is important to note that applications, such as grid-connected inverters typically operate with a high modulation index.

B. Neutral Point Voltage Control Strategy

When the imbalance of the two capacitor voltages occurs, it is necessary to increase or decrease the capacitor current, and therefore, the small voltage vectors have to be employed to balance two capacitor voltages.

TABLE II
DWELL TIMES OF THE SPACE VECTOR ACCORDING TO THE REGIONS IN RI-DPWM

Region	Dwell times
1	$T_0 = T_s\left[\frac{2\sqrt{3}\lvert V_{ref}\rvert \cdot sin(\theta_r - \pi/3)}{V_{DC}} + 2\right]$ $T_1 = T_s\left[\frac{6\lvert V_{ref}\rvert \cdot sin(\pi/6 - \theta_r)}{V_{DC}} - 2\right]$ $T_2 = T_s\left[\frac{2\sqrt{3}\lvert V_{ref}\rvert \cdot sin(\theta_r)}{V_{DC}} + 1\right]$
2	$T_0 = T_s\left[\frac{2\sqrt{3}\lvert V_{ref}\rvert \cdot sin(\theta_r - \pi/3)}{V_{DC}} + 2\right]$ $T_1 = T_s\left[\frac{6\lvert V_{ref}\rvert \cdot \cos(\theta_r)}{V_{DC}} - 3\right]$ $T_2 = T_s\left[2 - \frac{2\sqrt{3}\lvert V_{ref}\rvert \cdot sin(\theta_r + \pi/3)}{V_{DC}}\right]$
3	$T_0 = T_s\left[2 - \frac{2\sqrt{3}\lvert V_{ref}\rvert \cdot sin(\theta_r + \pi/3)}{V_{DC}}\right]$ $T_1 = T_s\left[\frac{6\lvert V_{ref}\rvert \cdot sin(\pi/6 + \theta_r)}{V_{DC}} - 2\right]$ $T_2 = T_s\left[1 - \frac{2\sqrt{3}\lvert V_{ref}\rvert \cdot sin(\theta_r)}{V_{DC}}\right]$

If the upper capacitor voltage (V_{CU}) is higher than the lower capacitor voltage (V_{CL}), the P-type switching state of a small voltage vector is employed instead of one medium voltage vector in region 2 of all Sectors and the N-type switching state of small voltage vectors in regions 1 and 3 of sectors 2, 4 and 6. For example, in region 2a of sector 1, the switching state of the medium voltage vector [PON] is replaced with the P-type switching state of the small voltage vector [POO] so that the switching sequence is formed as [POO]-[PNO]-[PNN]- [PNO]-[POO] instead of the switching sequence of [PON]-[PNN]-[PNO]-[PNN]-[PON]. In this switching sequence, phase-A is fixed to [P] as the proposed RI-DPWM. Therefore, the advantage for reducing the switching loss, and thus, the junction temperature can be kept while balancing two capacitor voltages. The switching sequences in region 1 and region 3 of sector I can be maintained since they include the P-type switching states in their switching sequences. In region 1 of sector 4, [NON] has to be replaced with [OPO] to increase V_{CL} and therefore, the switching sequence is formed as [OPO]-[NPO]-[NPP]-[NPO]-[OPO]. In this switching sequence, phase-B is fixed to [P] in place of phase-A, fixed to [N]. Therefore, the advantage to reduce the switching loss somewhat can be maintained.

In the case that V_{CL} is higher than V_{CU}, one medium voltage vector in region 2 of all sectors and also the P-type switching state of small voltage vectors in regions 1 and 3 of sectors 1, 3, and 5 is substituted with the N-type switching state of a small voltage vector. In region 2a of sector 2, the N-type switching state [OON] is employed and thus the switching sequence becomes [OON]-[PON]-[PPN]-[PON]-[OON], where the clamping of phase-C to [N] can be kept. The switching sequences for balancing two capacitor voltages in all sectors are given in Table III.

It is worthwhile to mention that since this unusual situation does not continue during the entire operating period of the NPC inverter in various applications, the proposed strategy can be applied whenever the imbalance of the two capacitor voltages occurs. Furthermore, because the period that the neutral-point voltage control method is applied is negligible compared with the whole lifetime of the NPC inverter, it does not have any notable effect on the lifetime decrease in the power devices and dc-link capacitors and thus the NPC inverter. In situations where continuous neutral-point voltage deviation occurs due to various factors of the inverter, only a small adjustment of the neutral-point current is typically necessary since the neutral-point voltage deviation due to them is generally not significant. Consequently, the neutral-point voltage balancing method needs to be employed for a short duration in the fundamental period of the output voltage. During the remainder of the period, the proposed RI-DPWM can be applied.

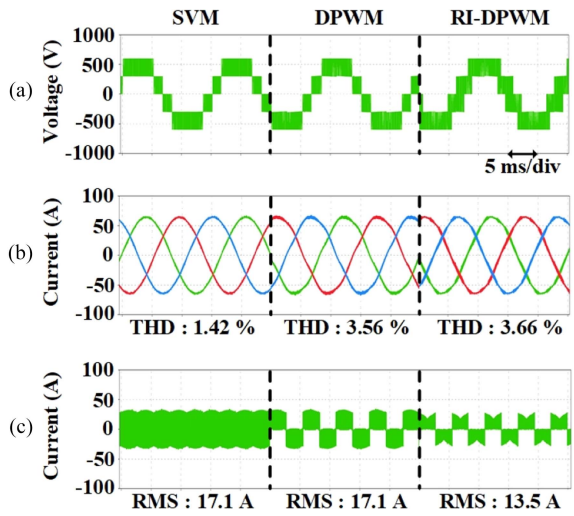

Fig. 6. Simulation results of the conventional SVM, DPWM, and RI-DPWM. (a) Line-to-line voltage (V_{AB}). (b) output currents. (c) Capacitor current (I_{CU}).

C. Performance Comparison Under Different PWM Methods

The performances of the NPC inverter under the conventional SVM, conventional DPWM, and proposed RI-DPWM are comparatively analyzed under the conditions given in Table IV. The IGBT module and dc-link capacitor considered for the thermal loadings analysis are F3L75R07W2E3_B11 from Infineon and DCMC112T500EE2B from Cornel Dubilier, respectively.

The dc-link is composed of the two capacitors connected in series.

Fig. 6 shows the line-to-line voltage, output currents, and I_{CU} under the SVM, conventional DPWM, and proposed RI-DPWM, respectively. The THD of the output current is 1.42% under the SVM, 3.56% under the DPWM, and 3.66% under the proposed RI-DPWM. As expected, DPWM methods increase the THD of the output current compared to SVM, with no significant additional increase when RI-DPWM is applied. It only increases by 0.1% compared to conventional DPWM. In terms of the RMS value of I_{CU}, it is 17.1 A under both SVM and conventional DPWM but reduces by 13.5 A under the RI-DPWM.

TABLE III
SWITCHING SEQUENCES FOR NEUTRAL POINT VOLTAGE CONTROL

Sector	Region	Switching sequence	
		$V_{CU} > V_{CL}$	$V_{CU} < V_{CL}$
1	1	[POP]-[PNO]-[PNN]-[PNO]-[POP]	[ONO]-[PNO]-[PNN]-[PNO]-[ONO]
	2a	[POO]-[PNO]-[PNN]-[PNO]-[POO]	[ONN]-[PNN]-[PNO]-[PNN]-[ONN]
	2b	[POO]-[PON]-[PNN]-[PON]-[POO]	[ONN]-[PNN]-[PON]-[PNN]-[ONN]
	3	[PPO]-[PON]-[PNN]-[PON]-[PPO]	[OON]-[PON]-[PNN]-[PON]-[OON]
2	1	[POO]-[PON]-[PPN]-[PON]-[POO]	[ONN]-[PON]-[PPN]-[PON]-[ONN]
	2a	[PPO]-[PPN]-[PON]-[PPN]-[PPO]	[OON]-[PON]-[PPN]-[PON]-[OON]
	2b	[PPO]-[PPN]-[OPN]-[PPN]-[PPO]	[OON]-[OPN]-[PPN]-[PPN]-[OPN]
	3	[OPO]-[OPN]-[PPN]-[OPN]-[OPO]	[NON]-[OPN]-[PPN]-[OPN]-[NON]
3	1	[PPO]-[OPN]-[NPN]-[OPN]-[PPO]	[OON]-[OPN]-[NPN]-[OPN]-[OON]
	2a	[OPO]-[OPN]-[NPN]-[OPN]-[OPO]	[NON]-[NPN]-[OPN]-[NPN]-[NON]
	2b	[OPO]-[NPO]-[NPN]-[NPO]-[OPO]	[NON]-[NPN]-[NPO]-[NPN]-[NON]
	3	[OPP]-[NPO]-[NPN]-[NPO]-[OPP]	[NOO]-[NPO]-[NPN]-[NPO]-[NOO]
4	1	[OPO]-[NPO]-[NPP]-[NPO]-[OPO]	[NON]-[NPO]-[NPP]-[NPO]-[NON]
	2a	[OPP]-[NPP]-[NPO]-[NPP]-[OPP]	[NOO]-[NPO]-[NPP]-[NPO]-[NOO]
	2b	[OPP]-[NPP]-[NOP]-[NPP]-[OPP]	[NOO]-[NOP]-[NPP]-[NOP]-[NOO]
	3	[OOP]-[NOP]-[NPP]-[NOP]-[OOP]	[NNO]-[NOP]-[NPP]-[NOP]-[NNO]
5	1	[OPP]-[NOP]-[NNP]-[NOP]-[OPP]	[NOO]-[NOP]-[NNP]-[NOP]-[NOO]
	2a	[OOP]-[NOP]-[NNP]-[NOP]-[OOP]	[NNO]-[NNP]-[NOP]-[NNP]-[NNO]
	2b	[OOP]-[ONP]-[NNP]-[ONP]-[OOP]	[NNO]-[NNP]-[ONP]-[NNP]-[NNO]
	3	[POP]-[ONP]-[NNP]-[ONP]-[POP]	[ONO]-[ONP]-[NNP]-[ONP]-[ONO]
6	1	[OOP]-[ONP]-[PNP]-[ONP]-[OOP]	[NNO]-[ONP]-[PNP]-[ONP]-[NNO]
	2a	[POP]-[PNP]-[ONP]-[PNP]-[POP]	[ONO]-[ONP]-[PNP]-[ONP]-[ONO]
	2b	[POP]-[PNP]-[PNO]-[PNP]-[POP]	[ONO]-[PNO]-[PNP]-[PNO]-[ONO]
	3	[POO]-[PNO]-[PNP]-[PNO]-[POO]	[ONN]-[PNO]-[PNP]-[PNO]-[ONN]

TABLE IV
SIMULATION PARAMETERS

Parameter	Value
Rated power (P_{rated})	30 [kW]
DC-link voltage (V_{DC})	600 [V]
Grid voltage (V_g)	220 [V_{rms}]
Grid frequency (f_g)	60 [Hz]
Switching frequency (f_{sw})	20 [kHz]
DC-link capacitance	1100 [μF]
Filter inductance	0.5 [mH]
Modulation index (MI)	0.898
Power factor (PF)	1

The FFT analysis of the I_{CU} and the corresponding $P_{\mathrm{loss\_cap}}$ and T_{hot} of the dc-link capacitor under the three PWM methods are shown in Figs. 7 and 8, respectively. The RMS value of I_{CU} is 17.1 A for both SVM and conventional DPWM. However, under conventional DPWM, the capacitor ripple current at 180 Hz significantly increases from 3.3 to 15.8 A. Although the ripple current at 60 kHz decreases from 10 to 2.5 A under conventional DPWM, the higher ESR values at low-frequency regions result in a higher power loss of 3.4 W compared to 3 W under SVM. When RI-DPWM is applied, the ripple currents generally decrease compared to those under the DPWM. Especially, at 20 kHz, the ripple current decreases from 12 to 4 A. Compared to the SVM, although the low-frequency ripple current at 180 Hz increases to 15 A, the ripple currents at other frequencies decrease overall. It decreases from 15.5 to 4.5 A at 20 kHz, and 10 A to 2 A at 60 kHz. Consequently, the $P_{\mathrm{loss\_cap}}$ is reduced to 2.6 W. The corresponding T_{hot} is shown in Fig. 8(b), assuming T_a

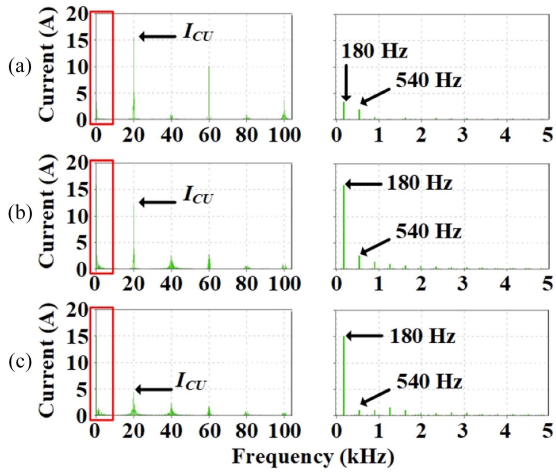

Fig. 7. DC-link capacitor current in the frequency domain. (a) conventional SVM. (b) conventional DPWM. (c) RI-DPWM.

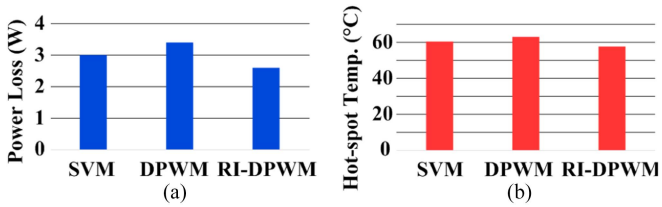

Fig. 8. Thermal loading of the DC-link capacitor. (a) Power loss. (b) Hot-spot temperature.

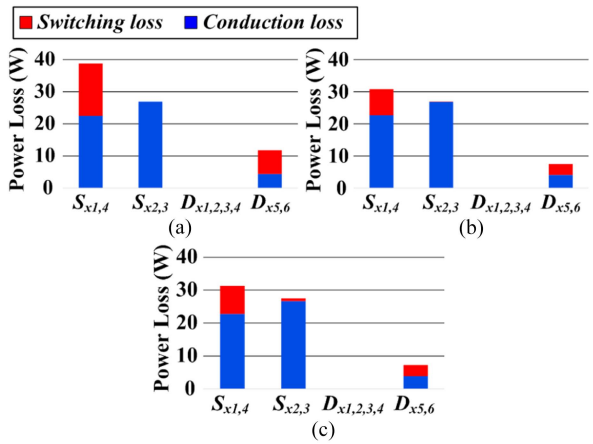

Fig. 9. Power losses distribution of the power devices when the modulation index is 0.898 and the power factor is 1. (a) conventional SVM. (b) conventional DPWM. (c) RI-DPWM.

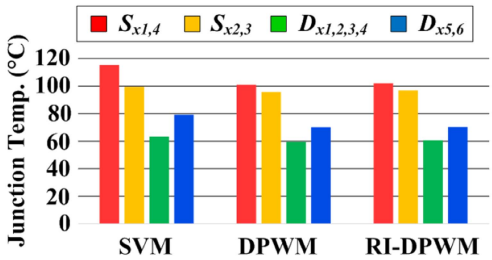

Fig. 10. Junction temperature of power devices under different PWM methods when the modulation index is 0.898 and the power factor is 1.

of 40 °C. T_{hot} is highest at 63 °C under the conventional DPWM, followed by T_{hot} of 60 °C under the SVM and T_{hot} of 57.7 °C under the RI-DPWM.

The power loss distribution, which is the average power loss for the fundamental period of the output, and the corresponding junction temperature of the power devices, which is the maximum junction temperature during the fundamental period of the output, are shown in Figs. 9 and 10, respectively. Compared to the case under the SVM, when the conventional DPWM is applied, the T_j of $S_{x1,4}$ decreases from 115.3 °C to 101 °C, and the switching loss of $S_{x1,4}$ is reduced from 38.8 to 30.8 W. Since $S_{x1,4}$ are considered the reliability-critical components due to having the highest T_j, and therefore, their T_j reduction plays a significant role in the reliability improvement of the NPC inverter. The total power loss caused by the power devices is significantly reduced from 465.6 to 391.2 W. Under the RI-DPWM, the power loss of $S_{x1,4}$ is similar to that under conventional DPWM at 31.3 W, and therefore the T_j is also similar to 102 °C. The total power loss due to power devices under RI-DPWM is 396.6 W, with a slight increase of about 3.6 W compared to conventional DPWM due to increased switching losses in $S_{x2,3}$. However, this increase is not significant, and there is still a considerable reduction in power loss compared with SVM.

More comparative analysis is performed under different modulation indices by considering one additional conventional PWM method called nearest three virtual space vector PWM (NTV-SVPWM) [17] and three additional PWM methods [11], [18], [19], [20] for improving the reliability of the NPC inverter called method-1 [11], method-2 [18], and method-3 [19], [20] in this article as given in Table V. It is seen that the performances of the NPC inverter under the NTV-SVPWM are almost similar to those under the SVM. No significant differences can be found. In the cases of method-1, method-2, and method-3, there are significant drops in T_{hot}. Method-3 shows the best performance to reduce T_{hot}. However, there are no reductions in T_j of outer power devices of $S_{x1,4}$ and also in the power loss compared with those under the conventional SVM since they are developed for mainly reducing T_{hot} of the dc-link capacitors. Similar results are obtained under the higher modulation index of 0.95. Therefore, it is difficult to directly compare them since the main purpose of the PWM methods is a bit different. Nevertheless, the comparison results clearly show the advantage of the proposed RI-DPWM to improve the reliability of both dc-link capacitors and power devices with reduced power loss. Consequently, the proposed RI-DPWM reduces the T_{hot} of the dc-link capacitors while maintaining the advantages of the DPWM in terms of junction temperature and power loss reductions. Furthermore, there is no significant additional increase in output current THD compared to conventional DPWM. Therefore, it could be a good alternative to the conventional DPWM.

It is worthwhile to mention that the advantages of the proposed RI-DPWM for improving the reliability of the power devices by reducing the maximum junction temperature of the outer power devices and reducing the power loss are effective when the power factor is close to 1. Under the lower power factor such as 0.8, since the fixed phase does not have the highest current, the reduced switching loss of the fixed phase is not higher than that of the increased switching loss of another phase. Therefore, the proposed RI-DPWM method is effective when the power factor is close to 1, and thus, it will be useful for applications that operate with a power factor close to 1.

V. Mission Profile Based Comparative Reliability Analysis of NPC Inverter

A. Lifetime Model of the Power Device

Thermal stress is the main cause of wear-out failure of the power device. The thermal stress factors such as junction temperature swing (ΔT_j), mean junction temperature (T_{jm}), and heating time (t_{on}) are typically considered to estimate the lifetime represented as the number of cycles to failure (N_f). They are obtained from the thermal loading profiles through the Rainflow counting method, where the thermal loading can be

TABLE V
COMPARATIVE ANALYSIS OF THE NPC INVERTER UNDER DIFFERENT PWM METHODS

Modulation Index	PWM Method	Hot-spot Temp. (°C)	Junction Temp. (°C)					Power Loss (W)	THD (%)
	Component	$C_{U,L}$,	$S_{x1,4}$	$S_{x2,3}$	$D_{x1,4}$	$D_{x2,3}$	$D_{x5,6}$		
0.898	*RI-DPWM*	57.7	102.0	96.7	60.3	60.3	70.4	396.6	3.66
	SVM	60.0	115.3	99.4	63.2	63.2	78.9	465.6	1.42
	NTV-SVPWM [17]	60.3	115.3	99.5	63.3	63.3	79.2	465.6	1.52
	DPWM	63.3	101.0	95.6	59.6	59.6	70.3	391.2	3.56
	Method-1 [11]	53.6	115.7	99.5	63.3	63.3	79.0	466.2	2.91
	Method-2 [18]	45.8	116.0	99.6	63.4	63.4	79.1	467.4	2.70
	Method-3 [19],[20]	42.7	115.6	99.5	63.3	63.3	76.0	465.6	2.70
0.95	*RI-DPWM*	53.2	102.5	95.7	59.5	59.5	68.3	390.0	3.22
	SVM	56.0	115.5	99.0	62.8	62.8	76.2	456.6	1.47
	NTV-SVPWM [17]	56.2	115.6	99.0	62.9	62.9	76.3	456.6	1.57
	DPWM	57.5	102.0	95.5	59.4	59.4	68.3	388.2	2.77
	Method-1 [11]	53.6	115.7	99.5	63.3	63.3	79.0	466.2	2.91
	Method-2 [18]	45.8	116.0	99.6	63.4	63.4	79.1	467.4	2.70
	Method-3 [19],[20]	42.7	115.6	99.5	63.3	63.3	76.0	465.6	2.70

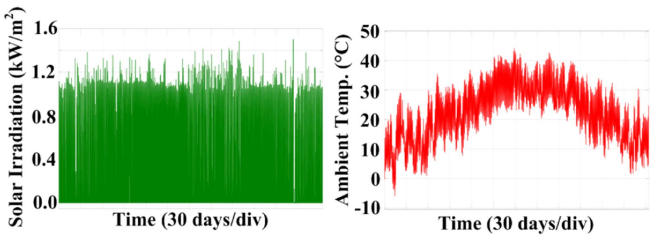

Fig. 11. Annual mission profile of PV system recorded in Iza, Spain.

obtained through the look-up table-based approach as explained in [21]. Then, N_f is determined by putting the thermalstress factors into a lifetime model.

In this article, the lifetime model presented in [22] is used as

$$N_f = A \cdot (\Delta T_j)^{-\beta 1} \cdot \exp\left(\frac{\beta 2}{T_{jm}+273}\right) \cdot (t_{\text{on}})^{\beta 3} \cdot I^{\beta 4} \cdot (V_c)^{\beta 5} \cdot D^{\beta 6}. \tag{8}$$

More detailed information for the lifetime model can be obtained from [22]. In this case study, the lifetime model presented in (8) is used because the lifetime model of the target IGBT module is not available, and this article is focused on bond-wire fatigue. Therefore, it is recommended that the lifetime results should be used to verify the feasibility and effectiveness of the proposed method through comparison, and the results are valid only for this case study.

As shown in Fig. 11, since the ambient temperature and the solar irradiation change in real conditions, the power device is subjected to varying thermal stress. Therefore, annual accumulated damage (AD) considering the annual mission profile of the PV system can be calculated based on the Palmgren–Miner rule as

$$\text{AD} = \sum_{i=1}^{k} \frac{N_i}{(N_f)_i} \tag{9}$$

where N_i is the number of cycles at a particular stress level i, and N_f is the number of cycles to failure at that same stress level i. When the AD reaches the value of 1, the device is considered to fail [23].

B. Lifetime Model of the Capacitor

The wear-out failure of the electrolytic capacitor is mainly caused by the thermal stress. Therefore, the lifetime model of the capacitor is generally expressed as

$$L_f = L_0 \cdot \left(\frac{V}{V_0}\right)^{-n} \cdot 2^{\frac{T_0 - T_{\text{hot}}}{10}} \tag{10}$$

where L_f is the time to failure of the capacitor, L_0, V_0, and T_0 are the lifetime, voltage, and T_{hot} at the reference condition, and V is the capacitor voltage at the using condition. The related parameters can be found in [24]. By applying a similar approach as with the power device, the AD of the capacitor can be calculated as (9).

C. Reliability Analysis of NPC Inverter in PV System

The lifetime models used in this article do not have the statistical analysis results. Therefore, the reliability function of each component is not available, which is essential for the system-level reliability evaluation. The Monte Carlo analysis is employed to perform the reliability analysis of the NPC inverter including all dc-link capacitors and power devices, where a population of 10 000 samples and a 5% variation with a normal distribution in the parameters of the lifetime model and equivalent thermal stress factors are considered as previous research in [25].

The lifetime distribution of individual components obtained by Monte Carlo simulation is fitted into Weibull distribution as

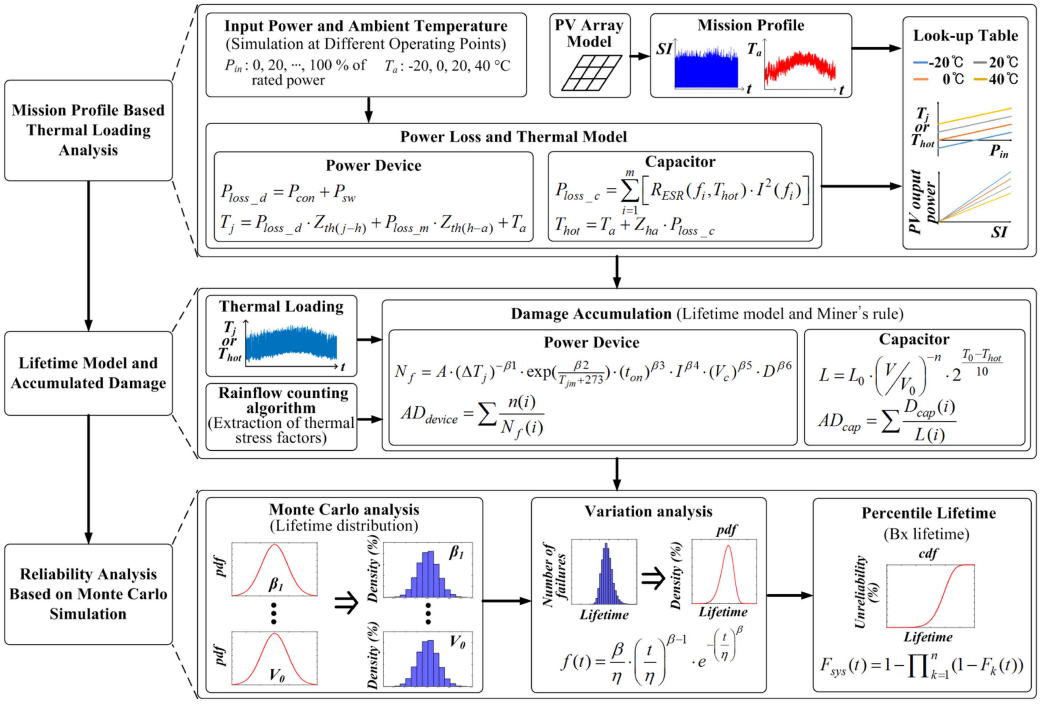

Fig. 12. Procedure for mission-profile-based reliability analysis of NPC inverter.

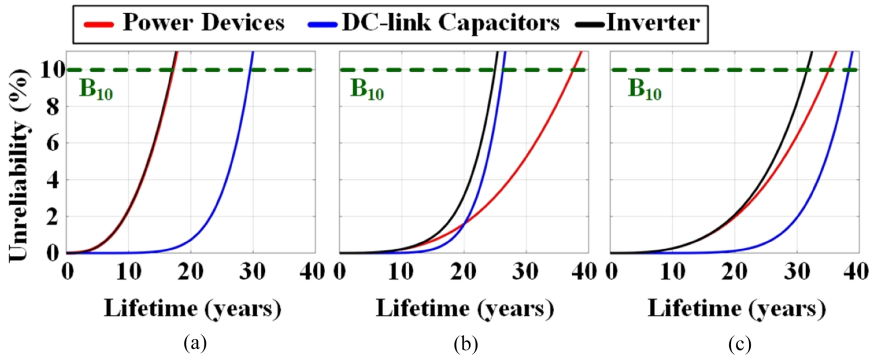

Fig. 13. Unreliability functions according to the PWM methods under (a) conventional SVM, (b) conventional DPWM, and (c) RI-DPWM.

follows:

$$f(t) = \frac{\beta}{\eta} \cdot \left(\frac{t}{\eta}\right)^{\beta-1} \cdot e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{11}$$

where *f(t)* is the probability density function, *t* is the operating time, β is the shape parameter, and η is the scale parameter. The cumulative distribution function of *f(t)* is called the unreliability function and is denoted *F(t)*. Then, the unreliability function of the inverter system $F_{sys}(t)$ including all components is obtained as

$$F_{sys}(t) = 1 - \prod_{k=1}^{n} (1 - F_k(t)) \tag{12}$$

where *n* is the number of components, and $F_k(t)$ is the unreliability function of the k_{th} component in the system. The unreliability function provides information on the percentile lifetime, called B_x lifetime, which indicates the lifetime of a population of the NPC inverter. This article assumes that the target B_{10} lifetime is 30 years.

The above explained procedure for mission-profile based reliability analysis of the NPC inverter is illustrated in Fig. 12.

Fig. 13 shows the unreliability functions of power devices, dc-link capacitors, and the NPC inverter under the SVM, DPWM, and RI-DPWM, respectively. As shown in Fig. 13(a), under the SVM, the B_{10} lifetimes of the power device and DC-link capacitor are 17.2 years and 29.8 years, respectively.

The B_{10} lifetime of the NPC inverter system considering all power devices and DC-link capacitors is 17.1 years. In this case, the reliability of the dc-link capacitor plays a key role in the reliability of the NPC inverter. In the case of conventional DPWM, as shown in Fig. 13(b), the B_{10} lifetime of the power devices is increased to 37.4 years owing to the T_j reduction in $S_{x1,4}$.

TABLE VI
COMPARATIVE ANALYSIS OF PERFORMANCE AND RELIABILITY OF THE NPC INVERTER UNDER DIFFERENT PWM METHODS

PWM Method	*Lifetime of DC-link Capacitors (B_{10} lifetime*)	*Lifetime of Power Devices (B_{10} lifetime)	*Lifetime of NPC Inverter (B_{10} lifetime)	**Power Loss (W)	**THD (%)	NP Voltage Balancing
SVM	Relatively moderate (29.8 years)	Relatively short (17.2 years)	Not satisfied (17.1 years)	465.6	1.42	Simple to implement Implementing without modification in the switching sequence
DPWM	Relatively short (26.1 years)	Relatively long (37.4 years)	Not satisfied (24.8 years)	391.2	3.56	Moderate to implement Requiring the modification in the switching sequence
RI-DPWM	Relatively long (38.3 years)	Relatively long (35.1 years)	Satisfied (31.6 years)	396.6	3.66	Moderate to implement Requiring the modification in the switching sequence

*B_{10} lifetimes are based on the mission profile of the case study. **Power loss and THD are at the rated power of 30 kW.

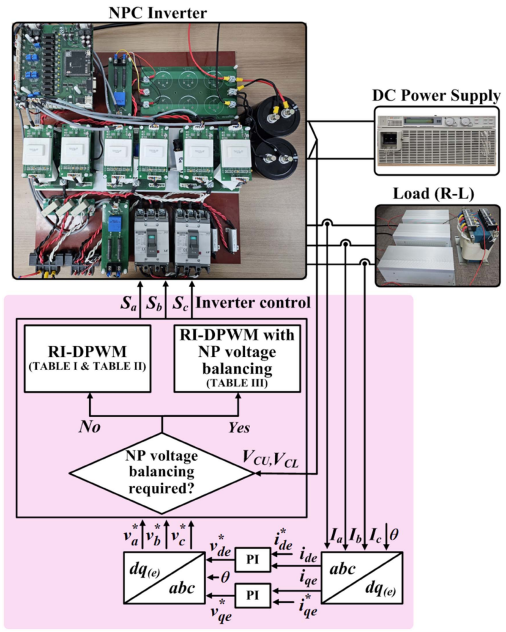

Fig. 14. Experimental setup and control structure (PI: proportional integral controller, PWM: pulse width modulation, and *S*: switching function).

However, the B_{10} lifetime of the dc-link capacitor is reduced to 26.1 years. Consequently, the B_{10} lifetime of the inverter system is 24.8 years, not reaching the target lifetime of 30 years. Under the proposed RI-DPWM as shown in Fig. 13(c), the B_{10} lifetime of power devices of 35.1 years is obtained. It is similar to that under the conventional DPWM, and almost twice as long as that under the SVM. In the case of the dc-link capacitor, it has the longest B_{10} lifetime of 38.3 years as expected. Thus, the B_{10} lifetime of the NPC inverter of 31.6 years is obtained. Consequently, thanks to the proposed RI-DPWM, the reliability of the power device and dc-link capacitor are improved, and thus the B_{10} lifetime of the NPC inverter of more than 30 years is achieved.

It is worthwhile mentioning that the B_{10} lifetime of 30 years is considered as the target lifetime of the inverter according to [26] and it could be different from case to case.

The comparative analysis results of the reliability and performance of the NPC inverter are given in Table VI. The results clearly show the effectiveness of the proposed RI-DPWM in terms of reliability while maintaining similar efficiency, THD, and NP voltage balancing ability compared with conventional DPWM. Therefore, the proposed RI-DPWM method is a good alternative to conventional DPWM when DPWM is required to be applied to the NPC inverter to reduce power loss, improve reliability, or achieve both of them.

TABLE VII
EXPERIMENTS PARAMETERS

Parameter	Value
DC-link voltage (V_{DC})	400 [V]
Output frequency (f_g)	60 [Hz]
Switching frequency (f_{sw})	20 [kHz]
DC-link capacitance	2200 [μF]
Load resistor	20 [Ω]
Load inductor	1.5 [mH]

VI. EXPERIMENTAL RESULTS

The experimental setup and its control structure are shown in Fig. 14. For the experiments, the typical proportional-integral controller-based current control is implemented by measuring the three-phase currents. Furthermore, the measured upper and lower capacitor voltage are used for the proposed RI-DPWM and neutral point voltage control method.

The parameters for the experimental validation of the RI-DPWM are given in Table VII.

Fig. 15 shows the results of the output currents in the time and frequency domains, as well as the line-to-line voltages and the pole voltages for the SVM, conventional DPWM, and RI-DPWM when the modulation index is 0.898. The pole voltages are clamped to [P] or [N] for 60°, respectively. As shown in Fig. 15(c), in contrast to the SVM and conventional DPWM, the magnitude of the *dv/dt* of the line-to-line voltage under RI-DPWM undergoes an increase from $V_{DC}/2$ to V_{DC} in a certain region. This indicates an increase in the THD of the output current, denoted by the harmonic current difference. While the SVM shows approximately 100 mA of harmonic current for phase-A at 20 kHz, RI-DPWM exhibited a higher value of 200 mA.

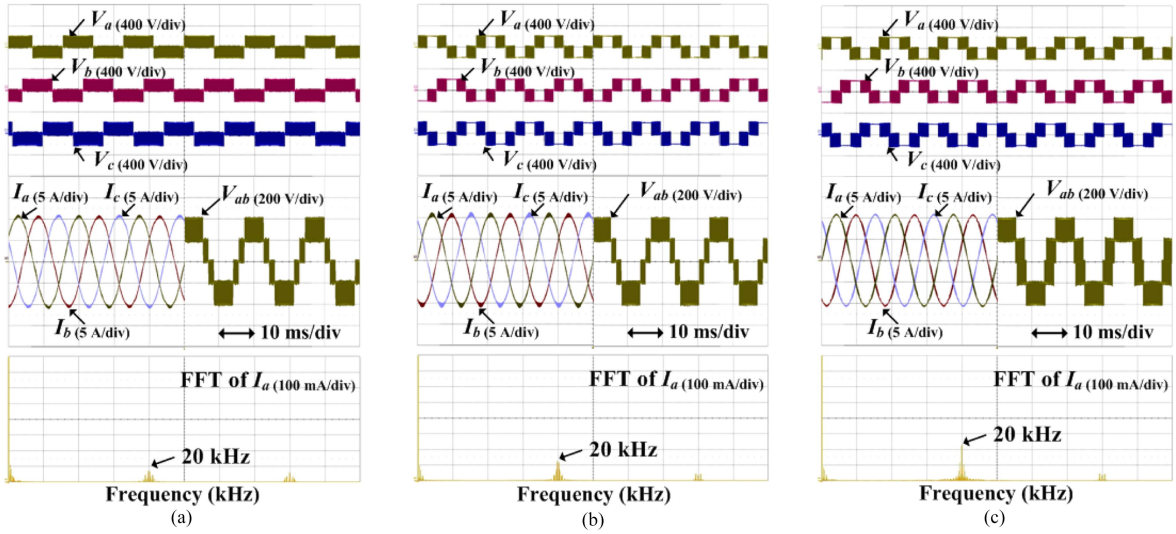

Fig. 15. Pole voltages, line-to-line voltages, and output currents in the time and frequency domains under (a) conventional SVM, (b) conventional DPWM, and (c) proposed RI-DPWM.

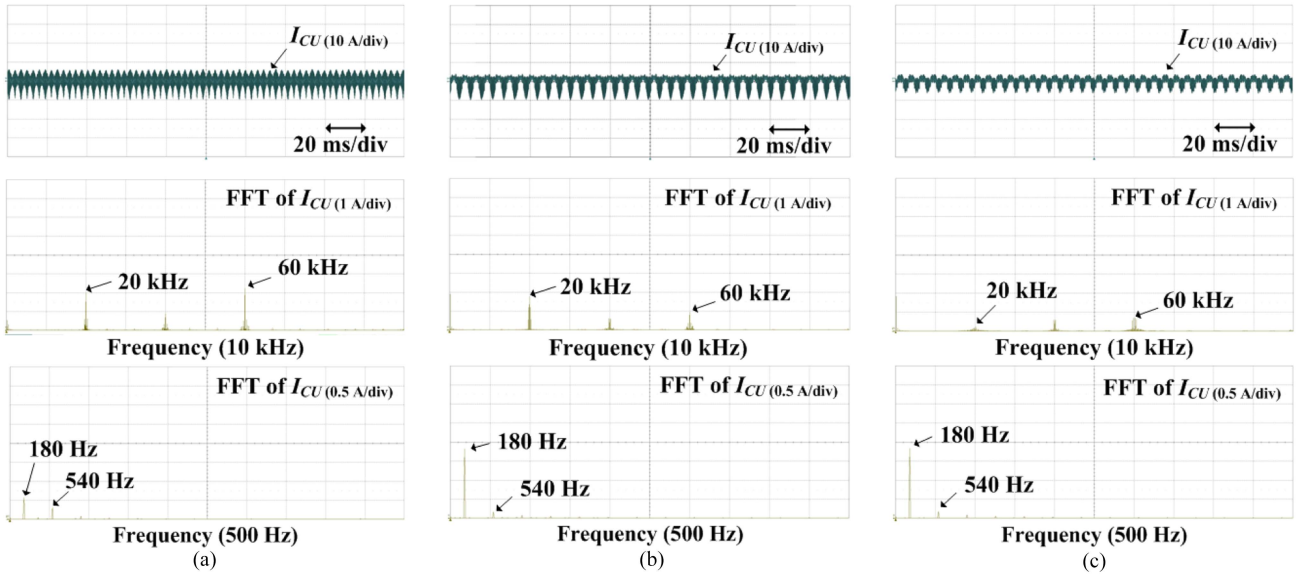

Fig. 16. Upper capacitor current (I_{CU}) in time and frequency domains under (a) conventional SVM, (b) conventional DPWM, and (c) proposed RI-DPWM.

The upper capacitor current (I_{CU}) under different PWM methods is shown in Fig. 16. In the frequency domain, the SVM has the upper capacitor current of 0.6, 2.0, and 2.2 A at 180, 20, and 60 kHz, respectively as shown in Fig. 16(a). As shown in Fig. 16(b), under the conventional DPWM, although the neutral point current reduces to 0.95 A from 2.2 A at 60 kHz, it increases from 0.6 to 1.8 A at 180 Hz. Since the current in the low-frequency band has a greater impact on the power loss of the DC-link capacitor compared to the high-frequency band, an increase in the power loss of the DC-link capacitor is expected under the conventional DPWM.

Under the proposed RI-DPWM as shown in Fig. 16(c), even though the upper capacitor current at 180 Hz increases similarly to conventional DPWM compared with the conventional SVM, there are significant reductions not only in the upper capacitor current at 60 kHz from 2.2 to 0.7 A compared with the conventional SVM, but also in the upper capacitor current at 20 kHz from 2.0 and 1.9 to 0.2 A compared with both conventional SVM and DPWM, respectively.

It contributes to that the dc-link capacitors have the lowest power loss under the proposed RI-DPWM. These experimental results show similar results to the simulations. Therefore, RI-DPWM can reduce the power losses of the power devices and dc-link capacitors, resulting in decreased thermal loadings and effectively enhancing the reliability of the PV inverter system.

The upper and lower capacitor voltages under the SVM, conventional DPWM, and proposed RI-DPWM are shown in Fig. 17. It is seen that under normal operating conditions, when

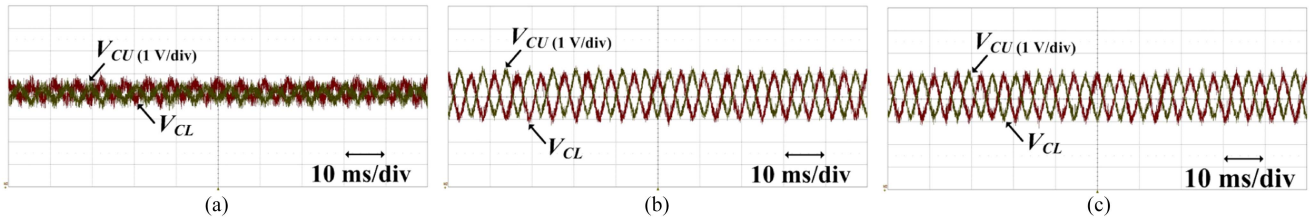

Fig. 17. Upper and lower capacitor voltages (V_{CU}, V_{CL}) under (a) conventional SVM, (b) conventional DPWM, and (c) proposed RI-DPWM.

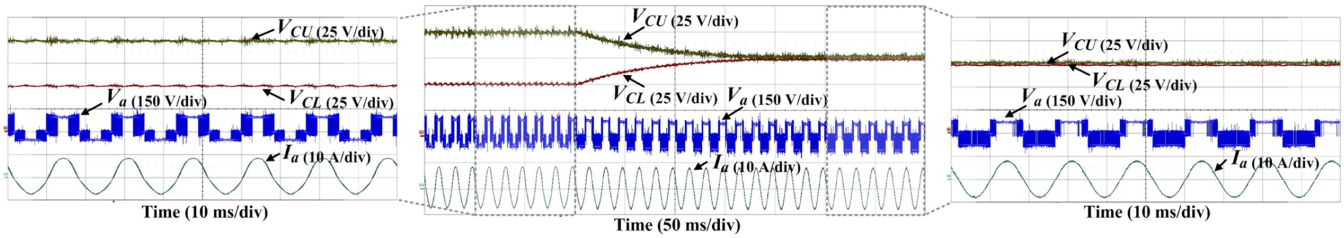

Fig. 18. Neutral point voltage control when the upper capacitor voltage (V_{CU}) is higher than the lower capacitor voltage (V_{CL}).

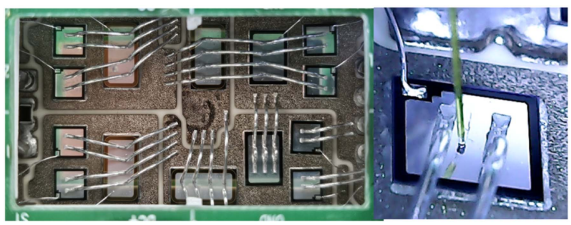

Fig. 19. Opened IGBT module with optic fiber sensor.

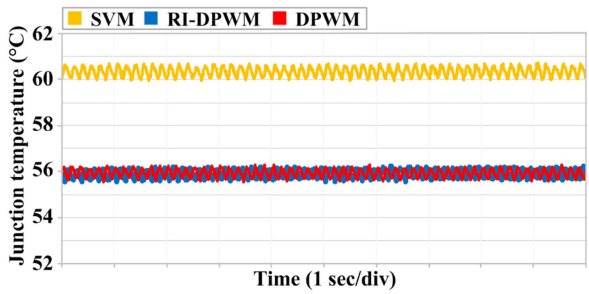

Fig. 20. Measured T_j of S_{a1} under the conventional SVM, DPWM, and proposed RI-DPWM, respectively.

the proposed RI-DPWM is applied, the two capacitor voltages are balanced to the same value of 200 V, and its oscillation is almost the same as that under the conventional DPWM.

Fig. 18 shows the experimental results of the neutral point voltage control strategy when the upper capacitor voltage ($V_{\rm CU}$) is higher than the lower capacitor voltage ($V_{\rm CL}$). The dc-link voltage is set to 150 V and the resistor of 90 Ω is connected in parallel to the lower capacitor to make the deviation between the upper capacitor and lower capacitor voltages. The distortion in the output current can be seen when the imbalance between the capacitor voltages occurs. After the neutral point voltage control method presented in Table III is applied, the two capacitor voltages are balanced to 75 V by decreasing $V_{\rm CU}$ and increasing $V_{\rm CL}$ and the distortion in output current is eliminated.

The junction temperature of S_{a1} is measured by the Coresens signal conditioner equipped with optic fiber sensors manufactured by Opsens through the opened IGBT module as shown in Fig. 19.

Fig. 20 shows the measured T_j of S_{a1} under the conventional SVM, DPWM, and proposed RI-DPWM. The T_j of S_{a1} is reduced from about 60.5 °C to about 56 °C under the DPWM methods. There is no notable difference between T_j of S_{a1} under conventional DPWM and T_j of S_{a1} under proposed RI-DPWM.

It clearly shows the effectiveness of the proposed RI-DPWM on the reliability improvement of the power devices by reducing their junction temperatures, and the ability to be almost similar to the conventional DPWM can be maintained.

VII. Conclusion

This article proposes the discontinuous PWM, called RI-DPWM for improving the reliability of the NPC inverter operated at high modulation index. The proposed RI-DPWM improves the reliability of the dc-link capacitors by reducing their $T_{\rm hot}$ compared with the conventional SVM and DPWM. Furthermore, the RI-DPWM maintains the advantages of the conventional DPWM, which are the reductions in power loss and the T_j compared with SVM. The reliability improvement of the NPC inverter with the RI-DPWM is validated through the case study of the system-level reliability evaluation of the NPC inverter by considering the mission profile of the PV system. The NPC inverter with the RI-DPWM has the longest B_{10} lifetime of 31.6 years, which is 85% and 27% increases compared with those under the SVM and conventional DPWM, respectively. In addition, the feasibility and effectiveness of the RI-DPWM method are also verified through experiments. The proposed RI-DPWM method is a good alternative to the conventional DPWM to improve the efficiency and reliability of the NPC inverter operated at a high modulation index with a power factor of 1 or close to 1.

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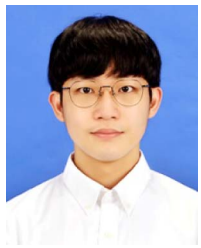
Dong-Jin Lee (Student Member, IEEE) received the B.S. degree in electronic and IT media engineering in 2023 from Seoul National University of Science and Technology, Seoul, Korea, where he is currently working toward the M.S. degree in electrical and electronic engineering.

His research interests include reliability of power electronic components and systems, power electronics in renewable energy generation and electric vehicles, and multilevel converter.



Jae-Heon Choi (Student Member, IEEE) received the B.S. and M.S. degrees in electronic and IT media engineering and ICT convergence engineering from Seoul National University of Science and Technology, Seoul, South Korea, in 2021 and 2023, respectively.

He is currently the Manager with the Power Electronics Research and Development Team, LS Electric Company Ltd., Anyang, South Korea. His research interests include the reliability of power electronic components and systems, power electronics in renewable energy generation and electric vehicles, and multilevel converters.

Ui-Min Choi (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical and electronic engineering from Ajou University, Suwon, Korea, in 2011 and 2013, respectively, and the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 2016.

From 2016 to 2018, he was a Post-doctoral Researcher with the Department of Energy Technology, Aalborg University. In 2018, he was with the Department of Smart ICT Convergence Engineering, Seoul National University of Science and Technology, Seoul, South Korea, where he is currently an Assistant Professor. He was a Partner Researcher with Grundfos Holding A/S, Bjerringbro, Denmark, from 2014 to 2016. His research interests include the reliability of power electronic components and systems, power electronics in renewable energy generation and electric vehicles, and multilevel converters.

Dr. Choi was the recipient of the IEEE Power Electronics Transactions Second Prize Paper Award in 2017. He is currently an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE OPEN JOURNAL OF POWER ELECTRONICS, and *Journal of Power Electronics*.