Low-Capacitance Three-Phase Series-Connected Modular Multilevel Converter With Second Harmonic Voltage Injection and High Capacitor Voltage Ripples for HVDC Application

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***Abstract*—To significantly reduce energy storage requirements, this article proposes a low-capacitance three-phase series-connected modular multilevel converter with second harmonic voltage injection and high capacitor voltage ripples (HR SC-MMC). The lower limit of the capacitor voltage is reduced by the second harmonic voltage injection. Based on this new limit, the SM capacitance can be redesigned, achieving a considerable reduction through high capacitor voltage ripple operation. The dc value of the capacitor voltage is slightly reduced to keep the peak capacitor voltage unchanged. The control and design methods are introduced to keep the SM capacitor voltage larger than the lower limit within the full operation range. The comparison results show that the HR SC-MMC effectively reduces the valve volume and cost, avoids a significant increase in the total power loss, and keeps the switch installation capacity and P-Q capability unchanged. Although the rms current and power loss of SM capacitors are increased, this may be acceptable, as the capacitor ripple current capability is underutilized and the increase in total power loss is small compared to existing methods. The correctness of the theoretical analysis and the feasibility of the HR SC-MMC are verified via 800-kV 733.3-MW simulations and 300-V 1.6-kW experiments.**

***Index Terms*—Capacitor voltage ripple, HVdc converters, low capacitance, modular multilevel converter (MMC), second harmonic voltage injection.**

I. Introduction

THE modular multilevel converter (MMC) has become a preferred converter topology in high-voltage direct-current (HVdc) transmission projects, owing to the features of the modular and scalable structure, low harmonics, and low switching losses [1], [2], [3]. Due to the physical separation of the three-phase arms in MMC, the submodule (SM) capacitors need to withstand the low-frequency energy variation, which is dominated by the fundamental and second-order ones [4]. Therefore, the SM capacitor with large capacitance is usually used in the MMC to limit the capacitor voltage ripple within an acceptable range. The large SM capacitance considerably increases the volume and cost of the system, which demands a proper solution [5].

Research on the energy storage requirement reduction method of the MMC for HVdc application has been conducted and reported in the literature [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. These methods can be classified into five categories: 1) circulating current injection methods, 2) third-order harmonic voltage injection methods, 3) active power filter (APF) methods, 4) full bridge SM (FBSM) methods, and 5) low-capacitance-based methods. The second-order circulating current can be used to reduce the capacitor voltage ripple and the SM capacitance. The injection of second-order circulating current is discussed in [6] and [7] for steady state and in [8] for SLG fault conditions. The third-order harmonic voltage can also be used to reduce the SM capacitance by shaping the arm voltage [9] or reducing the ac side current [10]. The combination of third-order harmonic and second-order circulating current is evaluated in [11]. The APF methods implement additional APF circuits in the SM to provide low-frequency energy variation, so the capacitance can be considerably reduced. The half-bridge SM (HBSM) with buck-type APF is investigated in [12]. The HBSM with symmetrical split-capacitor-type APF method is proposed in [13] and further investigated in [14]. In [15], the asymmetrical design is evaluated to further reduce the capacitance of HBSM with split-capacitor-type APF. In [16], the APF circuit for FBSM is discussed. Based on the negative voltage states of the FBSM, many methods are proposed to reduce the energy storage requirement. In [17] and [18], the modulation index is raised by the FBSM to achieve the energy storage reduction. In [19] the dc link voltage under reactive power operation conditions is reduced by the FBSM to achieve the energy storage reduction. The low-capacitance-based methods realize the SM capacitance reduction by accepting higher capacitor

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voltage ripples. This method was first proposed in [20] for the cascaded H-Bridge STATCOM and further improved by third harmonic voltage and third harmonic currents, respectively, in [21] and [22]. The low-capacitance MMC is proposed in [23], in which the SM number is increased to compensate for the operation range reduction caused by the high capacitor voltage ripple. In [24], the third-order harmonic voltage is used to limit the operation range reduction.

However, the injection of the second-order circulating current and the third-order harmonic voltage leads to a considerable increase in the converter current rating and output voltage, respectively. Therefore, the achievable energy storage reduction is limited. The APF methods and FBSM methods reduce the energy storage but increase the overall switch capacity and the power loss of the converter, which further influences the cost and volume of the system. Moreover, the existing low-capacitance methods achieve the SM capacitance reduction at the expense of the reduction in the inductive reactive power operation range of the converter. Although some new ideas have been proposed recently, such as the switching-cycle balancing control [25], the multilevel dc-link converter with single-device modules in series [26], the Arm Multiplexing MMC [27], and the shared capacitor MMC [28], they achieve a considerable reduction in energy storage but may suffer from control complexity, series of devices, or insulation problems.

Three-phase series-connected MMC (SC-MMC) is proposed in [29] and [30] as an alternative topology to the conventional MMC. Under the same power operation range and dc voltage conditions, the switch capacity, overall arm inductance, and energy storage requirement of these two converters are the same. Owing to the series structure, SC-MMC has the potential advantage in applications like power tapping from existing HVdc systems, city-infeed, ultra-HVdc transmission, and OFF-shore wind [31], [32]. With the help of high-current devices like IGCT [33], [34], the SC-MMC may become a promising solution for the HVdc application. However, it also requires large energy storage as the MMC.

Considering the situation above, this article proposes a low-capacitance SC-MMC with second harmonic voltage injection and high capacitor voltage ripples for HVdc applications, which is referred to as the SC-MMC with high-ripple (HR SC-MMC). Two steps are needed to realize the HR SC-MMC. Step one: the proposed second harmonic voltage is injected into the arm to shape the arm output voltage and further reduce the lower limit of the SM capacitor voltage. The proposed injection reduces the maximum and minimum values of the arm output voltage in all operation conditions, without affecting the original dc and fundamental components in the arm voltage. After the injection, the lower limit of the SM capacitor voltage is reduced and additional space for capacitor voltage appears. Step two: this additional space of capacitor voltage is further utilized to achieve the volume and cost reduction of the converter. To achieve a higher reduction, this article proposes to maintain the SM number and peak value of the capacitor voltage unchanged, but reduce the SM capacitance, i.e., the high capacitor voltage ripple operation. The SM capacitor voltage ripple increases as the capacitance decreases. Then, the dc value of the capacitor voltage is also reduced to keep the maximum value of the SM capacitor voltage unchanged.

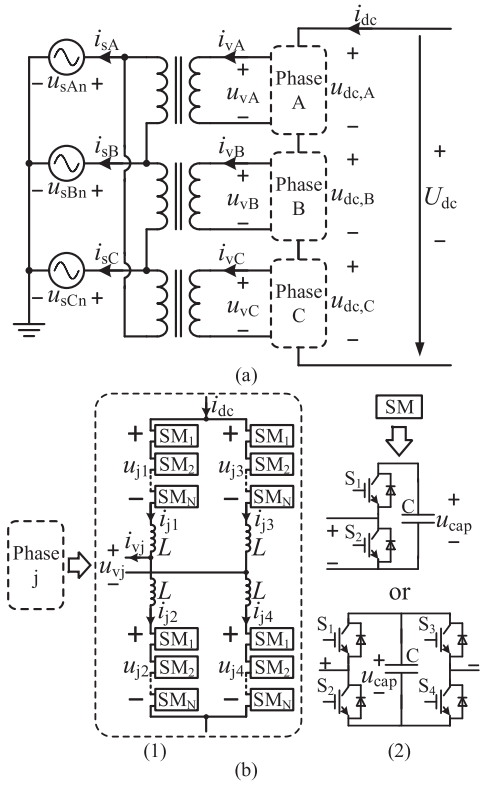

Fig. 1. Structure of the SC-MMC converter. (a) Circuit Architecture. (b) Structure of SC-MMC per phase and topologies of corresponding submodules, i.e., the half-bridge submodule and full-bridge submodule.

A detailed comparison between the existing and the proposed methods is conducted. Compared to existing methods, the proposed HR SC-MMC has at least one of the following advantages.

1) The energy storage requirement of the converter can be further reduced, which further reduces the volume and cost of the converter.
2) The switch installation capacity and SM number remain unchanged. The significant increase in the total power loss can be avoided.
3) Since the proposed second harmonic voltage injection reduces the lower limit of the capacitor voltage, the overmodulation or operation range reduction caused by the higher capacitor voltage ripple can be avoided.

The impacts of the proposed method on the rms current, power loss, and temperature rise of the SM capacitor are also analyzed. Although the rms current and power loss of SM capacitors are increased, this may be acceptable, as the capacitor ripple current capability is underutilized and the increase in total power loss is small compared to existing methods.

II. Principle of Proposed HR SC-MMC

A. Circuit Architecture

The circuit diagram of the SC-MMC is shown in Fig. 1. It is composed of three single-phase MMCs connected in series, and the ac side of each MMC is connected to the secondary winding

of one single-phase transformer. The primary windings of the three single-phase transformers are connected to the utility grid with a delta connection.

The structure of each single-phase MMC is shown in Fig. 1(b). It consists of four arms, each of which is built from N submodules and one arm inductor. The output voltages of four arms are referred to as u_{j1}, u_{j2}, u_{j3}, and u_{j4}, respectively, where j = A, B, and C represent phase A, B, and C. SC-MMC can be realized by various kinds of SMs [1]. For simplification, this article just takes HBSM and FBSM as examples.

Two steps are needed to realize the proposed HR SC-MMC, which are the proposed second harmonic voltage injection and high capacitor voltage ripple operation. The details are explained as follows.

B. Proposed Second Harmonic Voltage Injection

Step one: the proposed second harmonic voltage is injected into the arm to shape the arm output voltage. It aims to reduce the maximum and minimum values of the arm output voltage without affecting the original dc and fundamental components so that the lower limit of the SM capacitor voltage can be reduced. To achieve this goal, the phase angle of the injected second harmonic voltage is fixed to π. Then, the output voltages of the four arms in phase j can be written as follows:

$$\begin{cases} u_{j1} = u_{j4} = U_{dc}/6 - u_{vj}/2 + u_{2nd,j} \\ u_{j2} = u_{j3} = U_{dc}/6 + u_{vj}/2 + u_{2nd,j} \end{cases} \tag{1}$$

where j = A, B, C, u_{vj} is the ac output voltage and $u_{2nd,j}$ is the injected second harmonic voltage of phase j and they can be expressed as

$$u_{vj} = U_v \cos(\omega t + \theta_j) \qquad u_{2nd,j} = U_h \cos(2(\omega t + \theta_j) + \pi) \tag{2}$$

θ_j is the phase angle of output voltage. U_v and U_h are the amplitudes of the ac output voltage and injected second harmonic voltage, respectively. Then, the maximum value of (1) can be solved as

$$\begin{aligned} &\max(u_{j1}) = \max(u_{j2}) = \max(u_{j3}) = \max(u_{j4}) \\ &= \begin{cases} U_{dc}/6 + U_v/2 - U_h, & \text{when} U_h \in [0, U_v/8] \\ U_{dc}/6 + {U_v}^2/(32U_h) + U_h, & \text{when} U_h \in (U_v/8, \infty) \end{cases}. \end{aligned} \tag{3}$$

And the minimum value of (1) can be solved as

$$\begin{aligned} &\min(u_{j1}) = \min(u_{j2}) = \min(u_{j3}) = \min(u_{j4}) \\ &= U_{dc}/6 - U_v/2 - U_h. \end{aligned} \tag{4}$$

It can be observed that the maximum and minimum values of the four arms are the same and reduced with the increase of U_h. Thus, the arm output voltage can be shaped by the proposed second harmonic voltage injection, achieving maximum and minimum value reduction without influencing the original dc and fundamental components. The waveforms of the arm output voltage under different shaping conditions are shown in Fig. 2, where U_v is set as $0.85 \times U_{dc}/6$ as an example.

According to the symmetry of the three-phase ac output voltage and injected second harmonic voltage, the simplified circuit of HR SC-MMC can be obtained in Fig. 3. In each phase,

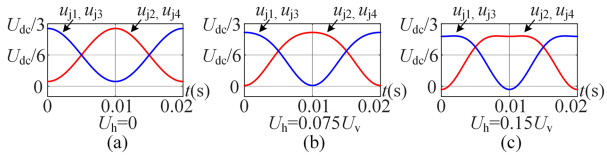

Fig. 2. Waveforms of the arm output voltage under different shaping conditions. (a) Without shaping. (a) Shaping by 7.5% second harmonic voltage. (a) Shaping by 15% second harmonic voltage.

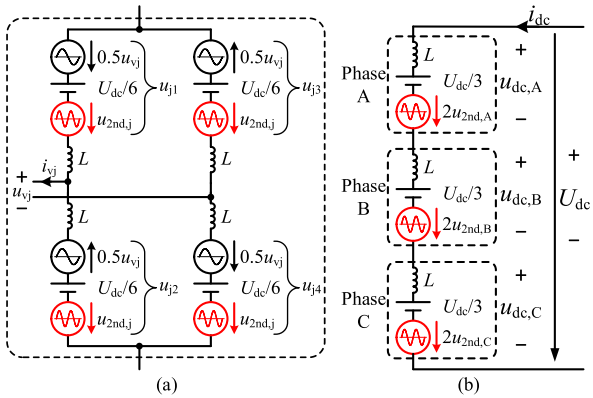

Fig. 3. Equivalent circuit of HR SC-MMC. (a) Equivalent circuit of HR SC-MMC per phase. (b) DC-side equivalent circuit of HR SC-MMC.

the second harmonic voltages in the four arms are arranged in the same direction, as shown in Fig. 3(a). Therefore, the second harmonic voltage is automatically cancelled out on the ac side. Although the second harmonic voltage will appear on the dc side of each phase with twice amplitude ($2u_{2nd,j}$), it can be further cancelled out on the dc side of the SC-MMC, as shown in Fig. 3(b).

Thus, the proposed second harmonic voltage injection can shape all arm output voltages of the SC-MMC similarly and avoid affecting the ac or dc sides of the SC-MMC.

Assuming the SM is well balanced, the SM output voltage and capacitor voltage after the proposed second harmonic voltage injection can be shown in Fig. 4(a). The maximum SM output voltage, which is proportional to the arm output voltage, is reduced after the proposed harmonic injection. Therefore, the lower limit of the SM capacitor voltage is reduced and additional space for capacitor voltage appears after the proposed harmonic component injection, as shown in Fig. 4(a). Although the injected voltage may cause the capacitor ripple power to increase under some operation conditions, the increase is minor because the amplitude of the injected second harmonic voltage is relatively lower.

C. High Capacitor Voltage Ripple Operation

Step two, this additional space of capacitor voltage provided by the proposed second harmonic voltage injection can be further utilized to reduce the energy storage of the converter and further achieve volume and cost reduction. The energy storage of converter E can be expressed as

$$E = 12N \times {}^1\!/_2 C U_{c,peak}^2 \tag{5}$$

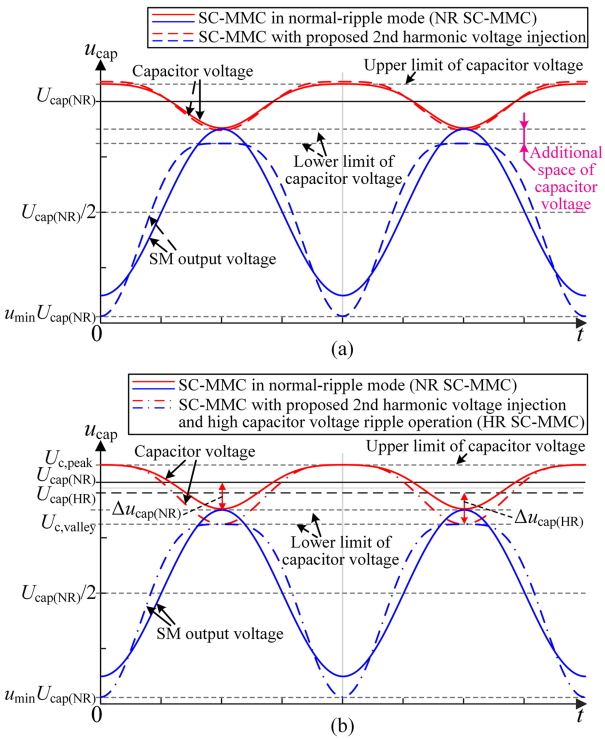

Fig. 4. SM output voltage and SM capacitor voltage of NR SC-MMC and HR SC-MMC. (a) Step one: SC-MMC only with proposed second harmonic voltage injection. (b) Step one and two: SC-MMC with proposed second harmonic voltage injection and high capacitor voltage ripple operation, i.e., HR SC-MMC.

where C is the capacitance, $U_{\mathrm{c,peak}}$ is the peak value of the capacitor voltage, and N is the SM number per arm.

It can be seen from (5) that there are various approaches to utilize this additional capacitor voltage space, such as reducing SM number N, reducing the peak capacitor voltage $U_{\mathrm{c,peak}}$, or increasing the capacitor voltage ripple by reducing the capacitance C. To achieve a higher reduction of the converter volume, this article proposes to maintain the SM number N and peak value of the capacitor voltage $U_{\mathrm{c,peak}}$ unchanged, but reduce the capacitance C, i.e., the high capacitor voltage ripple operation. As shown in Fig. 4(b), after the capacitance C reduction, the capacitor voltage ripple is increased from $\Delta u_{\mathrm{cap(NR)}}$ to $\Delta u_{\mathrm{cap(HR)}}$. To keep the peak value of the SMs capacitor voltage $U_{\mathrm{c,peak}}$ unchanged, the dc value of the SMs capacitor voltage should be reduced from $U_{\mathrm{cap(NR)}}$ to $U_{\mathrm{cap(HR)}}$.

As a result, the additional space for capacitor voltage provided by the proposed second harmonic injection is fully utilized to achieve the capacitor voltage ripple increase and capacitance reduction, comparing Fig. 4(a) and (b). Owing to the proposed second harmonic injection, the original dc and fundamental components of the arm voltage remain unchanged. Therefore, the converter can achieve normal operation with lower SM capacitance, avoiding overmodulation, SM number increase, or the operating range reduction in existing high-ripple methods.

For simplicity, the SC-MMC operating with an upper limit of 10% ripple rate hereafter is referred to as the SC-MMC with normal-ripple (NR SC-MMC).

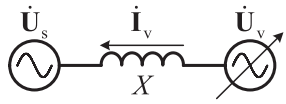

Fig. 5. Equivalent circuit of SC-MMC connected to a grid.

III. Analysis and Evaluation of HR SC-MMC

For an SC-MMC connected to a power grid, the amplitude of the fundamental component in the arm voltage changes with the power factor angle, thereby influencing the proposed harmonic injection. In this section, the amplitude of the injected second harmonic voltage U_{h} under different power factor angles and the SM capacitor voltage in HR SC-MMC is derived. Then, the capacitor voltage ripple rate is redesigned based on the new lower limit of the capacitor voltage. The energy storage, cost, and volume of the converter are further evaluated.

A. Analysis of the Arm Voltage and Current

For an SC-MMC connected to a power grid, the equivalent circuit is illustrated in Fig. 5. According to [23], by ignoring the vertical component of the voltage drop across the inductor X, the amplitude of the converter ac output voltage U_{v} can be expressed as

$$U_{\mathrm{v}} \approx \sqrt{2}U_{\mathrm{SN}}\left[1 + X_{\mathrm{pu}}I_{\mathrm{v\_pu}}\sin\left(-\varphi\right)\right] \tag{6}$$

where U_{SN} is the nominal grid rms voltage, φ is the power factor angle, X_{pu} and $I_{\mathrm{v\_pu}}$ are the per-unit values of the interface inductance and the output current, respectively, which can be expressed as

$$X_{\mathrm{pu}} = X/(U_{\mathrm{SN}}/I_{\mathrm{N}}) \qquad I_{\mathrm{v\_pu}} = I_{\mathrm{v}}/I_{\mathrm{N}} \tag{7}$$

where I_{N} is the nominal rms current. As shown in (6), U_{v} is changing with the power factor angle φ, thereby the amplitude of the second harmonic voltage U_{h} should change correspondingly. As shown in Fig. 4, the additional space for capacitor voltage is limited by the lower limit of the SM output voltage. The per-unit value of the SM output voltage's lower limit is defined as u_{min}, which is influenced by the operating margin and the FBSM number in the arm.

To fully utilize the voltage margin of the arms, the minimum value of the arm output voltage is controlled to be equal to the lower limit under all operation conditions, i.e., (4) equals $u_{\mathrm{min}} \times U_{\mathrm{dc}}/3$. Then, the amplitude of second harmonic voltage U_{h} under different power factor angles φ can be derived as

$$U_{\mathrm{h}} = \left(0.5 - 0.5U_{\mathrm{v}}/(U_{\mathrm{dc}}/3) - u_{\mathrm{min}}\right)(U_{\mathrm{dc}}/3)\,. \tag{8}$$

Defining the modulation index of fundamental component m_{a} and second harmonic voltage m_{h} as follows:

$$m_a = U_{\mathrm{v}}/(U_{\mathrm{dc}}/3) m_{\mathrm{h}} = U_{\mathrm{h}}/(U_{\mathrm{dc}}/3). \tag{9}$$

Then, (8) can be derived as

$$m_{\mathrm{h}} = 0.5 - 0.5m_a - u_{\mathrm{min}}. \tag{10}$$

The amplitude of the injected second harmonic voltage U_{h} is influenced by the power factor angle and the u_{min}. It reaches the minimum and maximum value under rated capacitive reactive power and rated inductive reactive power operation, respectively.

B. Analysis of the SM Capacitor Voltage

The SM capacitor voltage in the HR SC-MMC is analyzed below. The SM capacitor voltage consists of dc and ripple components. For the dc component, a factor k_{h} is defined to indicate the reduction of the dc value of capacitor voltage, which is expressed as follows:

$$k_{\mathrm{h}} = \frac{U_{\mathrm{cap(NR)}}}{U_{\mathrm{cap(HR)}}} = \frac{1+\varepsilon_{\mathrm{HR}}}{1+\varepsilon_{\mathrm{NR}}} \tag{11}$$

where $U_{\mathrm{cap(NR)}}$ and $U_{\mathrm{cap(HR)}}$ are the dc values of the capacitor voltage of the NR SC-MMC and HR SC-MMC, respectively. The $\varepsilon_{\mathrm{NR}}$ and $\varepsilon_{\mathrm{HR}}$ are the capacitor voltage ripple rates of the NR SC-MMC and HR SC-MMC, respectively, which are defined as

$$\varepsilon_{\mathrm{NR}} = \frac{\max\left|\Delta u_{\mathrm{cap(NR)}}\right|}{U_{\mathrm{cap(NR)}}} \quad \varepsilon_{\mathrm{HR}} = \frac{\max\left|\Delta u_{\mathrm{cap(HR)}}\right|}{U_{\mathrm{cap(HR)}}} \tag{12}$$

where $\Delta u_{\mathrm{cap(NR)}}$ and $\Delta u_{\mathrm{cap(HR)}}$ are the capacitor voltage ripples of the NR SC-MMC and HR SC-MMC, respectively. Then, the following relationship can be obtained:

$$U_{\mathrm{dc}}/3 = NU_{\mathrm{cap(NR)}} = k_{\mathrm{h}} NU_{\mathrm{cap(HR)}} \tag{13}$$

where N is the SM number per arm. Taking the SM of the A1 arm as an example, the output voltage and current of the A1 arm can be expressed as

$$i_{\mathrm{A1}} = 0.5I_{\mathrm{dc}} + 0.5i_{\mathrm{vA}} \tag{14}$$

$$u_{\mathrm{A1}} = U_{\mathrm{dc}}/6 - U_{\mathrm{v}}\cos(\omega t)/2 - U_{\mathrm{h}}\cos(2\omega t) \tag{15}$$

where the I_{dc} is the dc side current and the i_{vA} is the output current of phase A, they can be expressed as

$$I_{\mathrm{dc}} = 0.5m_a\sqrt{2}I_{\mathrm{vA}}\cos(\varphi)\, i_{\mathrm{vA}} = \sqrt{2}I_{\mathrm{vA}}\cos(\omega t+\varphi) \tag{16}$$

where the I_{vA} is the rms value of the output current. Combining (9), (13), and (15), the average switching function of A1 arm S_{A1} can be derived as

$$S_{\mathrm{A1\_av}} = \frac{u_{\mathrm{A1}}}{NU_{\mathrm{cap(HR)}}} = \frac{k_{\mathrm{h}}}{2}\left[1 - m_a\cos(\omega t) - 2m_{\mathrm{h}}\cos(2\omega t)\right]. \tag{17}$$

Then, the capacitor current $i_{\mathrm{cap,A1}}$ can be derived as

$$i_{\mathrm{cap,A1}} = i_{\mathrm{A1}}S_{\mathrm{A1\_av}} = \frac{\sqrt{2}k_{\mathrm{h}}I_{\mathrm{a}}}{8}\begin{pmatrix} 2\cos(\omega t+\varphi) - m_a^2\cos(\varphi)\cos(\omega t) \\ -2m_{\mathrm{h}}\cos(\omega t-\varphi) - m_a\cos(2\omega t+\varphi) \\ -2m_{\mathrm{h}}m_a\cos(\varphi)\cos(2\omega t) \\ -2m_{\mathrm{h}}\cos(3\omega t+\varphi) \end{pmatrix}. \tag{18}$$

The capacitor voltage ripple can be derived as

$$\tilde{u}_{\mathrm{cap,A1}} = \frac{\int i_{\mathrm{cap,A1}}dt}{C_{\mathrm{sm}}} = \frac{k_{\mathrm{h}}}{\omega}\frac{\sqrt{2}I_{\mathrm{N}}}{8C_{\mathrm{sm}}}I_{\mathrm{vA\_pu}}f_{\mathrm{r(HR)}}(\omega t) \tag{19}$$

$$f_{\mathrm{r(HR)}}(\omega t) = \begin{pmatrix} 2\sin(\omega t+\varphi) - m_a^2\cos(\varphi)\sin(\omega t) \\ -2m_{\mathrm{h}}\sin(\omega t-\varphi) - m_{\mathrm{h}}m_a\cos(\varphi)\sin(2\omega t) \\ -1/2 m_a\sin(2\omega t+\varphi) - 2/3 m_{\mathrm{h}}\sin(3\omega t+\varphi) \end{pmatrix} \tag{20}$$

where $f_{\mathrm{r(HR)}}$ is defined as the ripple waveform function of the HR SC-MMC. If the SM capacitor voltage ripple rate is limited to a given value of $\varepsilon_{\mathrm{HR}}$, the SM capacitance $C_{\mathrm{sm(HR)}}$ should be chosen to fulfill the following equation:

$$\varepsilon_{\mathrm{HR}} = \frac{\frac{k_{\mathrm{h}}}{\omega}\frac{\sqrt{2}I_{\mathrm{N}}}{8C_{\mathrm{sm(HR)}}}\max\left(f_{\mathrm{r(HR)}}(\omega t)\right)}{U_{\mathrm{cap(HR)}}}. \tag{21}$$

Then, substituting (21) into (19), the capacitor voltage ripple can be further expressed as

$$\tilde{u}_{\mathrm{cap,A1}} = \frac{\varepsilon_{\mathrm{HR}}U_{\mathrm{cap(HR)}}}{\max\left(f_{\mathrm{r(HR)}}(\omega t)\right)}I_{\mathrm{vA\_pu}}f_{\mathrm{r(HR)}}(\omega t). \tag{22}$$

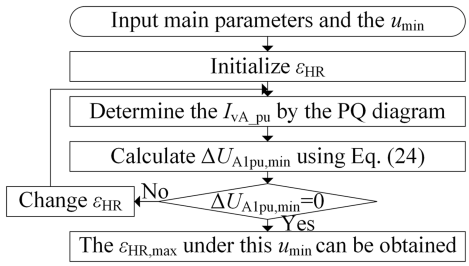

Fig. 6. Flowchart for obtain the maximum SM capacitor voltage ripple rate $\varepsilon_{\mathrm{HR,max}}$.

C. Redesign of the Capacitor Voltage Ripple Rate

The capacitor voltage ripple rate is increased to $\varepsilon_{\mathrm{HR}}$ in the HR SC-MMC to achieve energy storage reduction. However, the excessive increase in $\varepsilon_{\mathrm{HR}}$ will lead to overmodulation and reduce the operation range. Therefore, the maximum value of $\varepsilon_{\mathrm{HR}}$, i.e., the maximum capacitor voltage ripple rate $\varepsilon_{\mathrm{HR,max}}$, is evaluated considering the lower limit of the capacitor voltage.

In essence, the lower limit of the capacitor voltage is to ensure the full power range operation can be achieved without causing overmodulation. That is, the SM capacitor voltage must always be greater than the SM output voltage at any given instant. Thus, the voltage difference between the capacitor voltage and output voltage of the SM in the A1 arm is calculated and further pre-united to $U_{\mathrm{cap(HR)}}$. The result ΔU_{A1pu} can be shown as follows:

$$\Delta U_{\mathrm{A1pu}} = \begin{pmatrix} 1+\varepsilon_{\mathrm{HR}}I_{\mathrm{vA\_pu}}f_{\mathrm{r(HR)}}(\omega t)/\max\left(f_{\mathrm{r(HR)}}(\omega t)\right) \\ -k_{\mathrm{h}}/2\left(1-2m_{\mathrm{h}}\cos(2\omega t) - m_a\cos(\omega t)\right) \end{pmatrix}. \tag{23}$$

To meet the lower limit of the capacitor voltage, the $\Delta U_{\mathrm{A1pu}} \geq 0$ should be satisfied. The minimum value of ΔU_{A1pu} under different t and φ can be solved by the numerical method and labeled as $\Delta U_{\mathrm{A1pu,min}}$

$$\Delta U_{\mathrm{A1pu,min}} = \min_{\varphi\in[-\pi,\pi]}\left[\min_{t\in[0,0.02]}\left[\Delta U_{\mathrm{A1pu}}\right]\right]. \tag{24}$$

The $\Delta U_{\mathrm{A1pu,min}}$ is related to $I_{\mathrm{vA\_pu}}$, $\varepsilon_{\mathrm{HR}}$, and $u_{\min}$. The $I_{\mathrm{vA\_pu}}$ corresponds to φ on the boundary of the P-Q capability curve, which indicates the operation range of the converter. In this article, the full power operation range is chosen as an example. Thus, $I_{\mathrm{vA\_pu}}$ is set to 1 as a constant. Finally, the $\varepsilon_{\mathrm{HR,max}}$ under different $u_{\min}$ can be obtained by the flowchart shown in Fig. 6.

Fig. 7(a) displays the result of the $\varepsilon_{\mathrm{HR,max}}$ when the $u_{\min}$ changes, with $X_{\mathrm{pu}} = 0.1$ and $m_0 = \sqrt{2}U_{\mathrm{SN}}/(U_{\mathrm{dc}}/3) = 0.85$. It can be observed that when $u_{\min}$ declines, $\varepsilon_{\mathrm{HR,max}}$ rises and exceeds

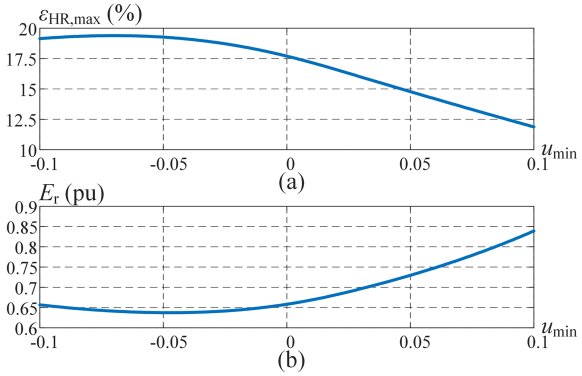

Fig. 7. Waveforms of the maximum SM capacitor voltage ripple rate $\varepsilon_{\mathrm{HR,max}}$ and the normalized energy storage E_{r} with the change of the $u_{\min}$ in HR SC-MMC. (a) Curve of $\varepsilon_{\mathrm{HR,max}}$. (b) Curve of E_{r}.

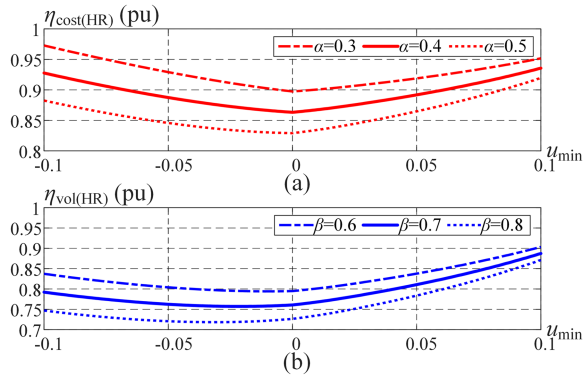

Fig. 8. Waveforms of the cost and the volume with the change of the $u_{\min}$ in HR SC-MMC. (a) Curves of cost. (b) Curves of volume.

10%. The $\varepsilon_{\mathrm{HR,max}}$ reaches 14.78% when $u_{\min}$ equals 0.05. The capacitor voltage ripple rate of HR SC-MMC $\varepsilon_{\mathrm{HR}}$ should not be higher than $\varepsilon_{\mathrm{HR,max}}$ and $\varepsilon_{\mathrm{HR}} = \varepsilon_{\mathrm{HR,max}}$ is chosen in the article as an example.

D. Evaluation of Energy Storage Reduction

After obtaining the $\varepsilon_{\mathrm{HR}}$, the normalized energy storage E_{r} of the HR SC-MMC per unit to the NR SC-MMC can be derived. According to (21), the SM capacitance of the proposed HR SC-MMC $C_{\mathrm{sm(HR)}}$ can be expressed as

$$C_{\mathrm{sm(HR)}} = \frac{k_{\mathrm{h}}}{\omega}\frac{\sqrt{2}I_{\mathrm{N}}}{8\varepsilon_{\mathrm{HR}}U_{\mathrm{cap(HR)}}}I_{\mathrm{vA\_pu}}\max\left(f_{\mathrm{r(HR)}}\left(\omega t\right)\right). \tag{25}$$

The SM capacitance of NR SC-MMC $C_{\mathrm{sm(NR)}}$ can be obtained similarly by changing $\varepsilon_{\mathrm{HR}}$ to $\varepsilon_{\mathrm{NR}}$ and m_{h} to zero. Then, the energy storage of two converters can be calculated by (5). Due to the SM number N and peak value of the capacitor voltage $U_{\mathrm{c,peak}}$ remains unchanged in the HR SC-MMC, the normalized energy storage E_{r} can be further derived as

$$E_{\mathrm{r}} = \frac{E_{\mathrm{HR}}}{E_{\mathrm{NR}}} = \frac{C_{\mathrm{sm(HR)}}}{C_{\mathrm{sm(NR)}}} = k_{\mathrm{h}}^2\frac{\varepsilon_{\mathrm{NR}}}{\varepsilon_{\mathrm{HR}}}\frac{\max\left(f_{\mathrm{r(HR)}}\left(\omega t\right)\right)}{\max\left(f_{\mathrm{r(NR)}}\left(\omega t\right)\right)} \tag{26}$$

where $f_{\mathrm{r(NR)}}$ is the ripple waveform function of the NR SC-MMC. It can be expressed as

$$f_{\mathrm{r(NR)}}\left(\omega t\right) = \begin{pmatrix} 2\sin\left(\omega t+\varphi\right) - m_a^2\cos\left(\varphi\right)\sin\left(\omega t\right) \\ -\left(m_a/2\right)\sin\left(2\omega t+\varphi\right) \end{pmatrix}. \tag{27}$$

The curve of E_{r} following the change of $u_{\min}$ is illustrated in Fig. 7(b). The E_{r} decreases with $u_{\min}$. When $u_{\min}$ equals 0.05, $\varepsilon_{\mathrm{HR,max}}$ reaches 14.78%, and the energy storage of HR SC-MMC reduces to 72.97% of that in NR SC-MMC.

E. Evaluation of the Cost and Volume Reduction

The cost and volume of the SM can be evaluated from the perspectives of the capacitor and semiconductor valve. In the NR SC-MMC, the proportion that the capacitor accounts for the total cost and volume of the SM is defined as α and β, respectively. Therefore, the semiconductor valve accounts for the total cost and volume of the SM are 1–α and 1–β, respectively. The values of α and β may vary within a certain range for different designs and applications [23]. In this article, the cases of $\alpha = 0.3$, 0.4, and 0.5 are considered for the cost evaluation, and $\beta = 0.6$, 0.7, and 0.8 are considered for the volume evaluation. The cost and volume of the NR SC-MMC are set to 1.0 p.u. and the values of the HR SC-MMC are normalized to the NR SC-MMC for better understanding. The cost and volume of the capacitor are assumed to be proportional to the nominal energy storage E_r of the converter. The cost and volume of the semiconductor valve are assumed to be proportional to the switch installation capacity S_{sw} of the converter, which can be calculated by multiplying the overall voltage stress and the current stress of the switches in the converter.

It should be noticed that when the $u_{\min}$ is lower than zero in the HR SC-MMC, the minimum value of the arm output voltage becomes negative. Then, some HBSM should be replaced by FBSM to provide the negative output voltage. The replacement ratio can be expressed as follows:

$$k_{\mathrm{FB}} = \frac{N_{\mathrm{FB}}}{N} = \begin{cases} 0, & u_{\min} \geq 0 \\ -u_{\min}U_{\mathrm{cap(NR)}}/U_{\mathrm{cap(HR)}} = -u_{\min}k_{\mathrm{h}}, & u_{\min} < 0 \end{cases} \tag{28}$$

where N_{FB} is the number of FBSMs. Therefore, the per-unit values of the cost and volume of the HR SC-MMC can be calculated as follows:

$$\eta_{\mathrm{cost(HR)}} = \alpha E_{\mathrm{r}} + \left(1-\alpha\right)S_{\mathrm{sw}} = \alpha E_{\mathrm{r}} + \left(1-\alpha\right)\left(1+k_{\mathrm{FB}}\right) \tag{29}$$

$$\eta_{\mathrm{vol(HR)}} = \beta E_{\mathrm{r}} + \left(1-\beta\right)S_{\mathrm{sw}} = \beta E_{\mathrm{r}} + \left(1-\beta\right)\left(1+k_{\mathrm{FB}}\right). \tag{30}$$

In HR SC-MMC, the normalized energy storage can be decreased to E_{r} and the normalized switch installation capacity increased to $(1 + k_{\mathrm{FB}})$. The curves of the cost and volume of the HR SC-MMC following the change of $u_{\min}$ are illustrated in Fig. 8. It can be seen that when $u_{\min}$ is lower than zero, the volume cannot be further reduced and the cost will be considerably increased. Therefore, the $u_{\min}$ is chosen as 0.05 in the rest of this paper. When $u_{\min} = 0.05$, $\alpha = 0.4$, and $\beta = 0.7$,

TABLE I
COMPARISON OF THE CAPACITANCE REDUCTION METHODS FOR SC-MMC

Parameter	Benchmark	Modulation index increase [10]	Circulating current control [6]	Existing high voltage ripple [23]	Variable DC voltage [19]	Proposal
Rated capacity (S / MVA)			733.3			
Rated dc link voltage (U_{dc} / kV)			800			
Rated ac rms voltage at valve side (U_v / kV)	160.12	184.14	160.12	160.12	160.12	160.12
Number of SMs in each arm (N)	133 HB	133 HB	133 HB	147 HB	67 HB+67 FB	133 HB
Rated capacitor voltage (U_{cap} / kV)	2.005	2.005	2.005	1.907	2.005	1.922
Capacitor voltage ripple rate (ε)	10%	10%	10%	15.65%	10%	14.78%
Energy storage (E_{c_total} / p.u.)	1	0.84	0.65	0.671	0.67	0.73
Switch Installation Capacity (S_{sw} / p.u.)	1	0.91	1.30	1.1	1.5	1
Valve volume (η_{vol} / p.u.)	1	0.86	0.84	0.80	0.92	0.81
Valve cost (η_{cost} / p.u.)	1	0.88	1.04	0.93	1.17	0.89
Number of series Cap. elements (N_S)	2	2	2	2	2	2
Number of parallel Cap. elements (N_P)	29	24	19	18	20	21
Rms current limit for SM Cap. ($I_{cap,limit}$ / A)	2349	1944	1539	1458	1620	1701
Rms value of SM Cap. current (I_{cap} / A)						
Rated active power	292.8	224.1	188.0	287.4	292.8	302.3
Rated capacitive reactive power	412.9	367.6	300.4	388.2	357.6	420.8
Rated inductive reactive power	416.9	378.3	345.6	402.8	292.9	466.1
Power loss of all SM Cap. ($P_{loss,cap}$ / %)						
Rated active power	0.0034%	0.0024%	0.0022%	0.0054%	0.0049%	0.0050%
Rated capacitive reactive power	0.0069%	0.0065%	0.0056%	0.0108%	0.0067%	0.0099%
Rated inductive reactive power	0.0070%	0.0069%	0.0074%	0.0116%	0.0045%	0.0121%
Temperature rise of SM Cap. (ΔT_{core} / °C)						
Rated active power	0.62	0.52	0.60	1.45	1.30	1.25
Rated capacitive reactive power	1.25	1.43	1.56	2.87	1.78	2.48
Rated inductive reactive power	1.28	1.52	2.07	3.09	1.19	3.04
Power loss of switching devices ($P_{loss,sw}$ / %)						
Rated active power	0.4922%	0.4476%	0.5393%	0.5290%	0.6484%	0.4883%
Rated capacitive reactive power	0.3737%	0.3320%	0.4183%	0.3953%	0.5469%	0.3658%
Rated inductive reactive power	0.4035%	0.3653%	0.4449%	0.4317%	0.5744%	0.4026%
Power loss of converter (P_{loss} / %)						
Rated active power	0.4956%	0.4500%	0.5415%	0.5344%	0.6533%	0.4933%
Rated capacitive reactive power	0.3806%	0.3385%	0.4239%	0.4061%	0.5536%	0.3757%
Rated inductive reactive power	0.4105%	0.3722%	0.4523%	0.4433%	0.5789%	0.4147%

Numbers are calculated under α=0.4, β=0.7, m_0=$\sqrt{2}U_{SN}/(U_{dc}/3)$=0.85, ε_{NR}=0.1. The per-unit values are normalized to the benchmark and the power losses are expressed as a percentage of rated capacity. Benchmark is an SC-MMC with pure dc circulating current and arm output voltage without a second harmonic voltages. The parallel resonant branch at the triple fundamental frequency is added in the modulation index increase method to block the third order current. In the circulating current control method, the amplitude of the injected second-order current is the same as the rated dc current in arms. For the existing high voltage ripple method, the parameters are designed for full active and reactive power operation.

the cost of HR SC-MMC can be reduced to 0.89 p.u. and the volume of HR SC-MMC can be reduced to 0.81 p.u.

IV. COMPARISON WITH OTHER CAPACITANCE REDUCTION METHODS

To justify the advantage of the proposed method over other capacitance reduction methods, a detailed comparison is performed based on a 733.3 MVA/800 kV condition. The entire power factor range is considered and all methods can output full active and reactive power. The comparison is performed in terms of energy storage, switch installation capacity, volume and cost of valve, SM capacitor design, and power loss. The rms value of SM capacitor current, power loss of all SM capacitors, and temperature rise of the SM capacitor are considered. The power losses of switching devices and the converter are also investigated. The detailed comparison results are summarized in Table I. All per-unit numbers are normalized to the benchmark. For the proposed method, the $u_{\min}$ is set to 0.05 as an example.

A. Comparison Processes

Based on different methods, the SC-MMC has different SM numbers, capacitances, and rated capacitor voltages. Therefore, the energy storage requirement defined in (5) is used to evaluate the total capacitor usage, and the per-unit results are shown in Table I. According to Fig. 7(b), the nominal energy storage requirement of the proposed method can be reduced to 0.73 when $u_{\min}$ is set to 0.05.

TABLE II
PARAMETERS OF THE CAPACITOR ELEMENT

Capacitance C (μF)	Rated Voltage V_R (V)	Can Dia D (mm)	Can Height H (mm)	Current T_A=55°C I_{rms} (A)	Typ. ESR R_{ESR}(10k) (mΩ)	Thermal Resistance R_{thcc} (°C/W)	Thermal Resistance R_{thca} (°C/W)	Max. Mass (kg)
770	1200	116	162	81	2.1	0.8	1.5	1.8

The switch investment is mainly determined by the switch installation capacity. By multiplying the overall voltage stress and current stress of the switches, the switch installation capacity of different methods can be obtained. When $u_{\min}$ is set to 0.05, the overall voltage stress and current stress remain unchanged in the proposed method.

The valve volume and cost of the different methods can be estimated by (29) and (30), which are directly influenced by the nominal energy storage and the nominal switch installation capacity. In this comparison, $\alpha = 0.4$ and $\beta = 0.7$ are considered. The valve volume and cost of the proposed method can be calculated as $(0.7 \times 0.73 + 0.3 = 0.81)$ and $(0.4 \times 0.73 + 0.6 = 0.89)$, respectively.

The SM capacitors for different methods are designed and compared as follows. The SM capacitor consists of N_S and N_P capacitor elements in series and parallel to meet the voltage and capacitance requirements. The Cornell Dubilier metallized film capacitor with part number 947D771K122DLRSN (Type 947D) is chosen as the capacitor element. Its parameters are shown in Table II according to [35]. As the maximum SM capacitor voltage is the same in all methods, all N_S equals 2. Whereas,

the N_{P} is proportional to the normalized SM capacitance. In the proposed method, the normalized SM capacitance equals normalized energy storage. Thus, N_{P} of the proposed method can be calculated as (round$(29 \times 0.73) = 21$). Then, the rms current limit of SM capacitor $I_{\mathrm{cap,limit}}$ under different methods can be further calculated as $N_{\mathrm{P}} \times I_{\mathrm{rms}}$, where I_{rms} is the ripple current limit of elements. The N_{P} and $I_{\mathrm{cap,limit}}$ for other methods are calculated and listed in Table I.

The rms values of SM capacitor current I_{cap} for different methods at typical operating conditions are obtained through the simulation, and the results are summarized in Table I. It can be seen that although the rms current limit of the SM capacitor is reduced due to the capacitance reduction, it still meets the operation requirements, i.e., $I_{\mathrm{cap,limit}} > I_{\mathrm{cap}}$.

Then, the power losses of all SM capacitors can be calculated as follow according to [36]:

$$P_{\mathrm{loss,cap}} = 12N \sum_{h=1}^{N_h} \left[\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}} R_{\mathrm{ESR}}(f_h) \times \left[I_{\mathrm{cap}}(f_h) \right]^2 \right] \quad (31)$$

where $I_{\mathrm{cap}}(f_{\mathrm{h}})$ is the rms value of the ripple current at frequency f_{h} and $R_{\mathrm{ESR}}(f_h)$ is the capacitor element's equivalent series resistance (ESR) at frequency f_h. The $I_{\mathrm{cap}}(f_{\mathrm{h}})$ is obtained by the simulation results and the $R_{\mathrm{ESR}}(f_h)$ can be calculated by

$$R_{\mathrm{ESR}}(f_h) = R_{\mathrm{ESR}}(10\mathrm{k}) - A/10\mathrm{k} + A/f_h \quad (32)$$

where A is 31.83 and $R_{\mathrm{ESR}}(10\mathrm{k})$ is 2.1 mΩ based on the data form [35]. After obtaining the power losses of all SM capacitor $P_{\mathrm{loss,cap}}$, the temperature rise of the SM capacitor ΔT_{core} can be calculated as

$$\Delta T_{\mathrm{core}} = P_{\mathrm{loss,cap}} (R_{\mathrm{thcc}} + R_{\mathrm{thca}}) / (12N \times N_{\mathrm{P}} \times N_{\mathrm{S}}) \quad (33)$$

where the R_{thcc} and R_{thca} are the thermal resistance from core-to-case and case-to-ambient, respectively. The results of $P_{\mathrm{loss,cap}}$ and ΔT_{core} are listed in Table I.

Finally, the power losses of the switches $P_{\mathrm{loss,sw}}$ for different methods at typical operating conditions are obtained through the simulation based on [37]. The Infineon 3300 V/2400 A FZ2400R33HE4 IGBT module is selected as the switch for all SMs in the comparison. The power losses of the converter P_{loss} can be calculated by adding $P_{\mathrm{loss,sw}}$ and $P_{\mathrm{loss,cap}}$. The results are summarized in Table I.

B. Discussions

Based on Table I, the switch installation capacity is reduced in the modulation index increase method. However, the values of the circulating current control, the existing high voltage ripple method, and the variable dc voltage method are increased due to the injected current, the additional HBSMs, and the required FBSMs, respectively. The value of proposed method is same as the benchmark.

The volume of the proposed method is reduced by 5.81%, 4.02%, and 11.75% compared to the modulation index increase, the circulating current control, and the variable dc voltage methods, respectively, and is comparable to that of the existing high voltage ripple method. Meanwhile, the cost of the proposed method is reduced by 14.23%, 3.92%, and 23.63% compared to circulating current control, the existing high voltage ripple, and variable dc voltage methods, respectively, and is similar to the cost of the modulation index increase method.

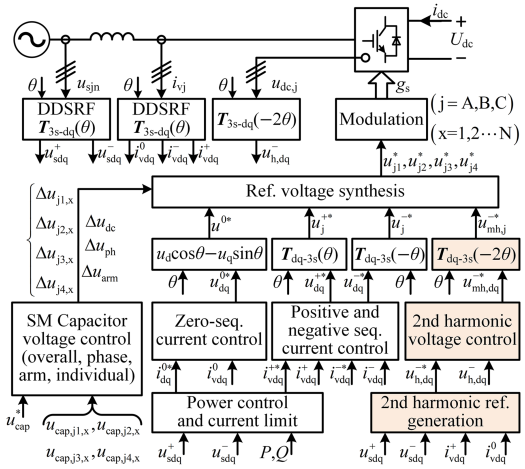

Fig. 9. Overall control diagram of HR SC-MMC.

The rms current, power loss, and temperature rise of SM capacitors are further increased in the proposed method. The overheating may influence the lifetime of the capacitor, which should be considered in practical applications. However, the SM capacitor usually needs to be large enough (capacitance) to constrain the voltage ripple, while having sufficient ripple current capability to avoid overheating [5]. Thus, increasing the rms current and the power loss of the capacitor to trade for the capacitance reduction may be acceptable [38].

As the rated capacitor voltage decreases, the power loss of the switching devices in the proposed method decreases slightly. The total power loss of the proposed method only increases in rated inductive reactive power operation, from 0.4105% to 0.4147%, compared to the benchmark due to the higher SM capacitor losses and lower switching device losses.

To summarize, although the circulating current control, existing high voltage ripple, and variable dc voltage methods can achieve higher energy storage reduction than the proposed method, the increasing switch installation capacity limits the volume and cost reduction and further causes higher power loss. The modulation index increase method can reduce both energy storage and power loss, but the energy storage reduction is limited, and an additional ac side filter is needed for SC-MMC. In contrast, the proposed method effectively reduces the valve volume and cost, avoids a significant increase in the total power loss, and keeps the switch installation capacity and P-Q capability unchanged. Although the rms current and power loss of SM capacitors are increased, this may be acceptable, as the capacitor ripple current capability is underutilized and the increase in total power loss is small compared to existing methods.

V. Control Algorithm

The operation of the proposed HR SC-MMC relies on an effective control algorithm. A general control scheme is developed in this article, as shown in Fig. 9, which consists

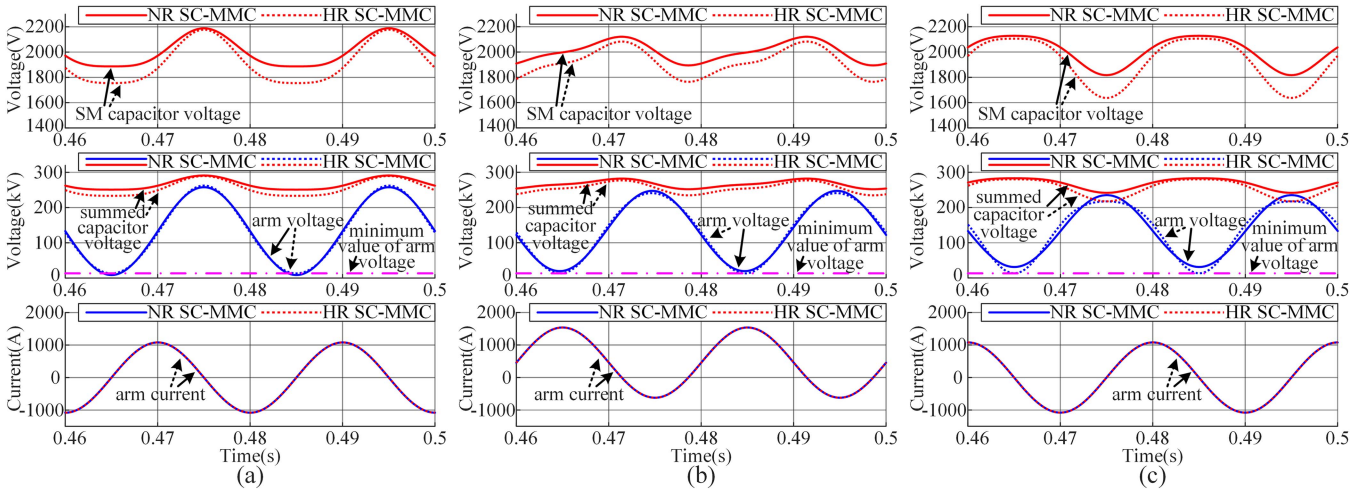

Fig. 10. Simulation results of NR SC-MMC and HR SC-MMC under different steady-state operation conditions. (a) Rated capacitive reactive power output condition. (b) Rated active power output condition. (c) Rated inductive reactive power output condition.

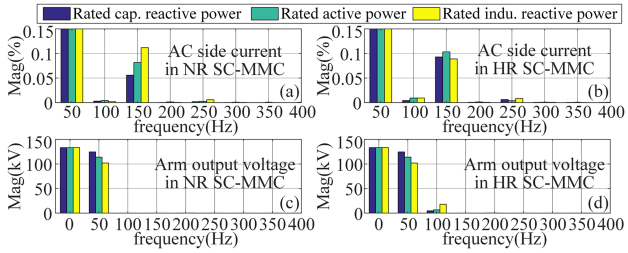

Fig. 11. FFT results of NR SC-MMC and HR SC-MMC under different steady-state operation conditions. (a) FFT results of AC side current in NR SC-MMC. (b) FFT results of AC side current in HR SC-MMC. (c) FFT results of arm output voltage in NR SC-MMC. (d) FFT results of arm output voltage in HR SC-MMC.

of power control, current control, SM capacitor voltage control, second harmonic voltage reference generation, and second harmonic voltage control.

To realize the operation of HR SC-MMC under normal and unbalanced ac grid conditions, the power control and current control methods based on positive, negative, and zero sequence control in [30] are used. In the *dq* synchronous reference frame, the positive-sequence current reference i^{+*}_{vdq} is generated according to the required ac-side active and reactive power. The negative-sequence current reference i^{-*}_{vdq} is set to zero to keep the grid current balanced. The zero-sequence current reference i^{0*}_{vdq} is set to balance the unbalanced power input from the ac grid.

The SM capacitor voltage control balances the voltage of each SM and further adjusts it to the target value, which can be further divided into overall capacitor voltage control, phase capacitor voltage control, arm capacitor voltage control, and individual capacitor voltage control. It is similar to the control in MMC [39].

The second harmonic voltage in the phase arm should be controlled to decrease the maximum value of the arm output voltage. In balance ac grid condition, based on (2), (8), and (9), the second harmonic voltage reference in *dq* synchronous

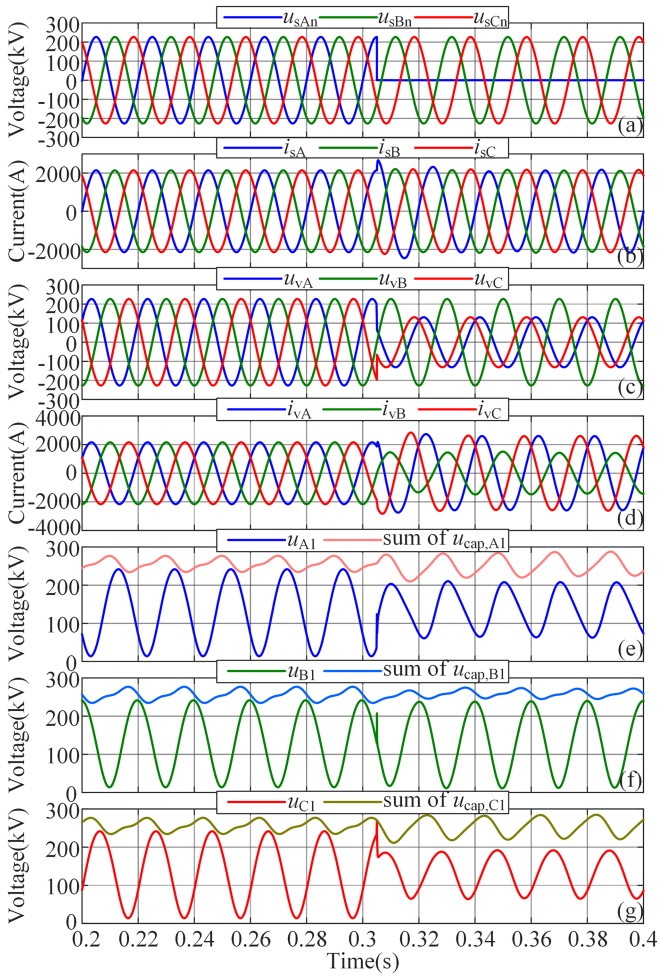

Fig. 12. Simulation results of HR SC-MMC under the single line-to-ground fault on the grid side. (a) Three-phase voltages at the grid side of transformers. (b) Three-phase currents at the grid side of transformers. (c) Three-phase voltages at the converter side of transformers. (d) Three-phase currents at the converter side of transformers. (e) Output voltage and summed capacitor voltage of A1 arm. (f) Output voltage and summed capacitor voltage of B1 arm. (g) Output voltage and summed capacitor voltage of C1 arm.

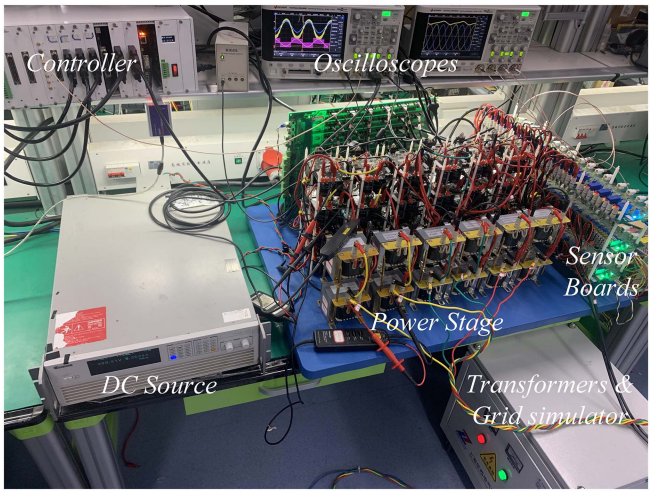

Fig. 13. Photograph of the experimental platform.

reference frame $u^{-*}_{\mathrm{h,dq}}$ can be generated as

$$\begin{bmatrix} u^{-*}_{\mathrm{h\_d}} \\ u^{-*}_{\mathrm{h\_q}} \end{bmatrix} = -\frac{U_{\mathrm{dc}}}{3}\left[0.5 - 0.5M_0\left(1 - X_{\mathrm{pu}} i^{+}_{\mathrm{vq}}\right) - u_{\mathrm{min}}\right]\begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{34}$$

where $i^{+}{}_{\mathrm{vq}}$ is equal to the $I_{\mathrm{vA\_pu}} \times \sin(\varphi)$. Under the unbalanced ac grid condition, the second harmonic voltage reference should be generated based on the maximum amplitude of the converter phase output voltage

$$\begin{bmatrix} u^{-*}_{\mathrm{h\_d}} \\ u^{-*}_{\mathrm{h\_q}} \end{bmatrix} = -\frac{U_{\mathrm{dc}}}{3}\left[0.5 - 0.5\,\frac{\max\left(U_{\mathrm{va}}, U_{\mathrm{vb}}, U_{\mathrm{vc}}\right)}{U_{\mathrm{dc}}/3} - u_{\mathrm{min}}\right]\begin{bmatrix} 1 \\ 0 \end{bmatrix} \tag{35}$$

where the U_{va}, U_{vb}, and U_{vc} are the estimated amplitudes of the converter's three-phase output voltage. They can be calculated by the positive and negative sequence voltage of the grid ($u^{+}{}_{\mathrm{sdq}}$, $u^{-}{}_{\mathrm{sdq}}$) as well as the positive and zero sequence current ($i^{+}{}_{\mathrm{vdq}}$, $i^{0}{}_{\mathrm{vdq}}$). Detailed calculations of U_{va}, U_{vb}, and U_{vc} are listed in the appendix. After the reference generation, the second harmonic voltages in the converter are measured from the dc side of each phase and further controlled in the *dq* synchronous reference frame to follow the reference value $u^{-*}_{\mathrm{h,dq}}$.

VI. Simulation Verification

A. Simulation Results

To verify the effectiveness of the proposed method, an 800 kV/733.3 MW SC-MMC is simulated in MATLAB/Simulink. The structure of the simulated SC-MMC is shown in Fig. 1. The ac side of the SC-MMC is connected to an equivalent three-phase ac voltage source, and the dc side is connected to an equivalent dc voltage source. Both the parameters of the NR SC-MMC and HR SC-MMC are designed, summarized, and compared in Table III.

Fig. 10 shows the simulation results of NR SC-MMC and HR SC-MMC under different steady-state operation conditions. Fig. 10(a) illustrates the simulation results of outputting a rated capacitive reactive power. The waveform of the single SM capacitor voltage in the A1 arm is shown in the top figure. It can be seen that the dc value of the capacitor voltage is decreased and the ripple rate is increased in the HR SC-MMC. And the peak capacitor voltage of the HR SC-MMC is the same as that of the NR SC-MMC. The waveforms of the summed capacitor voltages of all the SMs in the A1 arm and the output voltage of the A1 arm are shown in the middle figure. In this condition, the arm output voltage is in phase with the capacitor voltage ripple. Due to the minimum value of the arm voltage in NR SC-MMC being 8.59 kV, which is lower than the designed constant $u_{\mathrm{min}} \times U_{\mathrm{dc}}/3 = 0.05 \times 800\ \mathrm{kV}/3 = 13.3\ \mathrm{kV}$, a small part of the second harmonic voltage is reversely injected into the arm output voltage to increase the minimum value of the arm voltage in HR SC-MMC. The waveforms of the arm current in HR-MMC and NR-MMC are shown in the bottom figure. The higher capacitor voltage ripple does not influence the control accuracy of the arm current.

TABLE III
Circuit Parameters of the Simulation Model

Parameter	Symbol	NR SC-MMC	HR SC-MMC
Rated capacity	S	733.3 MVA	733.3 MVA
Rated ac rms voltage at converter side of transformers	U_{v}	160.12kV	160.12kV
Rated dc link voltage	U_{dc}	800 kV	800 kV
Modulation ratio when φ=0	m_0	0.85	0.85
Number of SMs in each arm	N	133	133
SM capacitance	C_{sm}	11.21 mF	8.18 mF
Rated energy storage	E	43.50 MJ	31.74 MJ
Rated SM capacitor voltage	U_{cap}	2 kV	1.92 kV
Peak SM capacitor voltage	U_{peak}	2.2 kV	2.2 kV
Capacitor voltage ripple rate	ε	10%	14.78%
Arm inductance	L	33.4 mH	33.4 mH
Factor	u_{min}	—	0.05

Fig. 10(b) illustrates the simulation results of outputting a rated active power. Similarly, the decrease in the dc capacitor voltage and the increase in the ripple rating are realized. In this condition, the second harmonic voltage with a higher amplitude is injected to reduce the maximum and minimum values of the arm output voltage in HR SC-MMC. After the injection, the minimum value of the arm output voltage is decreased from 19.51 kV to 13.02 kV, which equals the designed constant $u_{\mathrm{min}} \times U_{\mathrm{dc}}/3 = 13.3$ kV. Meanwhile, the maximum value of the arm output voltage is also reduced from 247.34 kV to 240.87 kV, avoiding the overmodulation caused by the high capacitor voltage ripple. The result is consistent with the theoretical analysis and the higher capacitor voltage ripple also does not influence the arm current.

Fig. 10(c) illustrates the simulation results of outputting a rated inductive reactive power. In this condition, the capacitor voltage ripple is opposite to the phase angle of the arm output voltage, and the second harmonic voltage with a considerable amplitude is injected in HR SC-MMC. After the injection, the minimum value of the arm output voltage is decreased from 31.23 kV to 13.453 kV, which equals the designed constant $u_{\mathrm{min}} \times U_{\mathrm{dc}}/3 = 13.3$ kV. And the maximum value of the arm output voltage is also reduced from 235.18 kV to 217.38 kV, effectively avoiding the overmodulation caused by the high capacitor voltage ripple. The arm current remains unaffected.

Under all operation conditions, the minimum arm output voltage is controlled around the designed constant. Meanwhile,

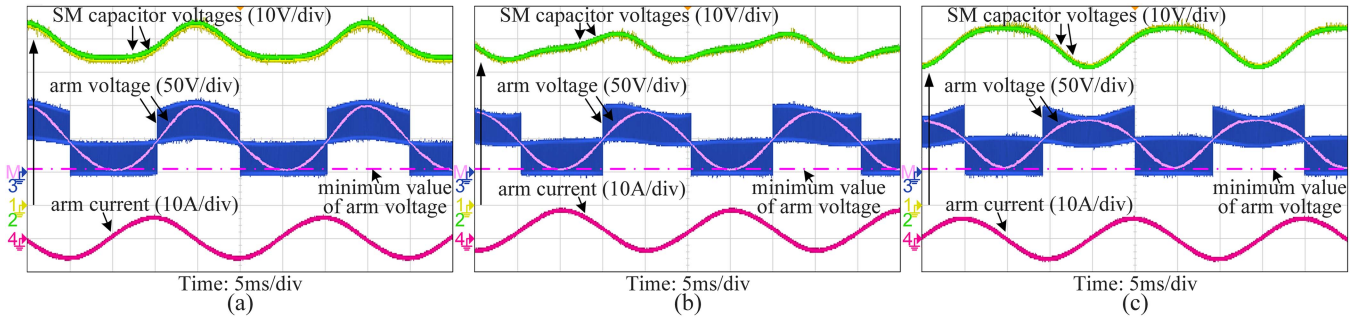

Fig. 14. Experiment results of HR SC-MMC under different steady-state operation conditions. (a) Rated capacitive reactive power output condition. (b) Rated active power output condition. (c) Rated inductive reactive power output condition.

owing to the proposed second harmonic voltage injection, the SM capacitance reduction does not cause overmodulation or the operation range reduction within the full operation range, which is consistent with the theoretical analysis. Furthermore, the fast fourier transform (FFT) results of the ac side current and the arm output voltage are obtained and shown in Fig. 11. The harmonic components of the ac side current are relatively small and meet the IEEE 519-2022 standard. Meanwhile, the FFT results of the arm output voltage are consistent with the theoretical analysis.

Fig. 12 illustrates the simulation results of HR SC-MMC under the single line-to-ground (SLG) fault on the grid side.

At 0.305 s, a SLG fault occurs on the A phase of the ac grid. Fig. 12(a) and (b) shows the three voltages and currents at the grid side of the transformers. It can be seen that the grid-side currents can remain balanced during the fault. Fig. 12(c) and (d) shows the three voltages and currents at the converter side of the transformers. As the SLG fault causes double-phase voltage sag at the converter side of transformers, the current magnitudes of the two phases with voltage sag will be increased to maintain the balanced active power input of each phase, as shown in Fig. 12(d). The output voltage and summed capacitor voltage of the A1 arm, B1 arm, and C1 arm are shown in Fig. 12(e), (f), and (g), respectively. It can be seen that the HR SC-MMC can remain in normal operation under the SLG fault condition.

VII. Experimental Verification

To further verify the effectiveness of the proposed method, a downscaled prototype has been constructed in a laboratory, as shown in Fig. 13. The detailed circuit parameters are listed in Table IV. Carrier phase-shift modulation is employed in the experiments, and the carrier frequency is set to 10 kHz. The dc side of the converter is connected to a programmable dc voltage source, and the ac side of the converter is connected to a regenerative grid simulator. The dc voltage source is operated in constant dc mode, and the HR SC-MMC is set to control the active and reactive power. Experimental results are shown in Figs. 14 –16.

Fig. 14(a) shows the steady-state experiment waveforms of the HR SC-MMC when outputting rated capacitive reactive power. The capacitor voltages of the two SMs in the A3 arm are shown in channels 1 and 2, respectively. The dc value of the capacitor voltage decreases to 47.9 V and the peak capacitor voltage reaches

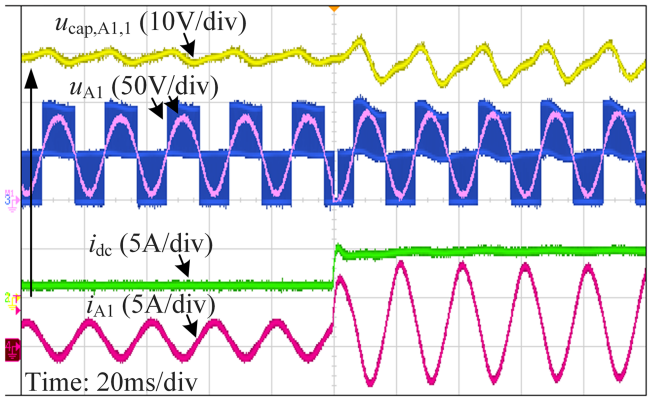

Fig. 15. Experiment results of HR SC-MMC under a transient-state operation condition when reference active power is stepped from 0.3 p.u to 0.9 p.u.

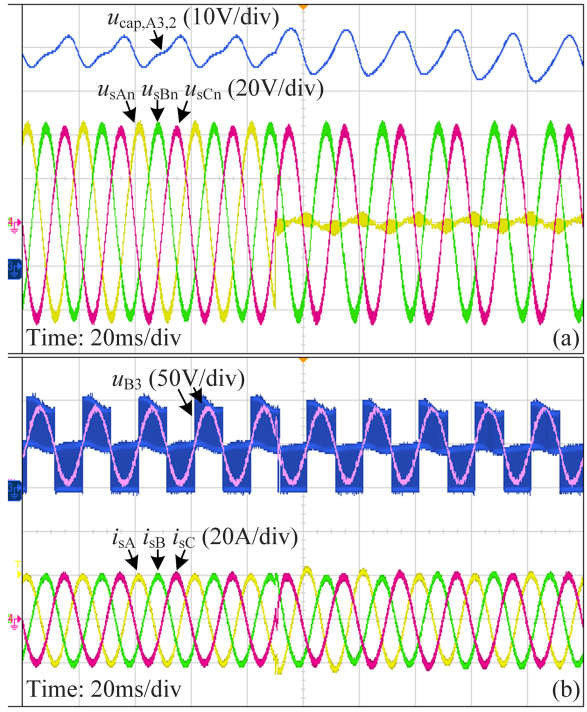

Fig. 16. Experiment results of HR SC-MMC under the SLG fault on the grid side. (a) Three-phase ac phase-neutral voltages at the gird side of transformer and the SM capacitor voltage of the A3 arm. (b) Three-phase gird current and output voltage of the B3 arm.

TABLE IV
CIRCUIT PARAMETERS OF THE EXPERIMENTAL SETUP

Parameter	Symbol	Values
Rated capacity	S	1.6 kVA
Rated ac rms voltage at converter side of transformers	$U_{\rm v}$	60 V
Rated dc link voltage	$U_{\rm dc}$	300 V
Modulation ratio when φ=0	m_0	0.85
Number of SMs in each arm	N	2
SM capacitance	$C_{\rm sm}$	1.8 mF
Rated SM capacitor voltage	$U_{\rm cap}$	47.92 V
Peak SM capacitor voltage	$U_{\rm peak}$	55 V
Upper limit of capacitor voltage ripple rate	ε	14.78%
Arm inductance	L	2.1 mH
Factor	$u_{\rm min}$	0.05

approximately 55 V. Therefore, the capacitor voltage ripple is 14.82%. The arm voltage of the A3 arm is shown in channel 3, and it is further filtered by the math function in the oscilloscope to observe the low-frequency components. The low-pass filter with a cut-off frequency of 7 kHz is implemented, and the result is shown in channel M of the oscilloscope. As is consistent with the simulation, the capacitor voltage ripple is in phase with the arm voltage. The second harmonic voltage is reversely injected into the arm voltage to control the minimum arm voltage around 5 V, which is equal to $u_{\rm min} \times U_{\rm dc}/3 = 0.05 \times 100$ V. The decreased dc value of the capacitor voltage and the higher capacitor voltage ripple do not influence the arm current.

Fig. 14(b) shows the steady-state experiment waveforms of the HR SC-MMC when outputting rated active power. The dc value of the capacitor voltage decreases to 47.9 V. The maximum and minimum values of the capacitor voltage are approximately 51 V and 43 V, respectively. Therefore, the capacitor voltage ripple is 9.28%. As is consistent with the simulation, the phase difference between the capacitor voltage ripple and the arm voltage is approximately $\pi/2$. The second harmonic voltage is injected into the arm voltage to reduce the maximum arm output voltage to 90 V and control the minimum arm voltage around 5 V.

Fig. 14(c) shows the steady-state experiment waveforms of the HR SC-MMC when outputting rated inductive reactive power. The dc value of the capacitor voltage decreases to 47.9 V. And the minimum capacitor voltage is approximately 41 V. Therefore, the capacitor voltage ripple is 14.4%. As is consistent with the simulation, the capacitor voltage ripple is in the opposite phase with the arm voltage. Meanwhile, the second harmonic voltage is injected into the arm, which lowers the maximum arm output voltage to 80 V and regulates the minimum arm voltage to approximately 5 V. Owing to the proposed second harmonic voltage injection, the HR SC-MMC can output rated inductive reactive power without causing overmodulation.

Fig. 15 shows the transient-state experiment waveforms of the HR SC-MMC. In this experiment, the HR SC-MMC is required to output pure active power to the grid simulator. When the converter operates in a steady state, the reference output active power is suddenly changed from 0.3 p.u. to 0.9 p.u. As soon as the reference is increased, the converter responds immediately and increases the dc input current and ac output currents to follow the change. Meanwhile, the second harmonic voltage is also controlled to maintain the minimum value of the arm voltage as the design value. During this dynamic process, the SM capacitor voltage is well balanced, and no evident overvoltage occurs during the transient phase.

Fig. 16 shows the experiment waveforms of HR SC-MMC under the SLG fault condition. In this experiment, the converter outputs rated active power to the grid. When the converter operates in a steady state, an SLG fault occurs on the A phase of the ac grid. As soon as the fault happens, the converter responds immediately, the positive sequence current is limited to the rated value, the negative sequence current is controlled to zero, and the zero-sequence current is controlled to a certain value to balance the output power of three phases. During this dynamic process, the grid-side currents can remain balanced. Meanwhile, the three-phase SM capacitor voltage is well balanced, and no evident overvoltage occurs during the transient phase.

VIII. CONCLUSION

This article proposes a low-capacitance SC-MMC with second harmonic voltage injection and high capacitor voltage ripples for HVdc applications. By injecting the proposed second harmonic voltage, the arm output voltage is shaped and the lower limit of the capacitor voltage is reduced, which provides additional space for the capacitor voltage. Then, the high capacitor voltage ripple operation can be achieved by utilizing this additional voltage space. By slightly decreasing the dc value of the capacitor voltage, the SC-MMC can operate under higher capacitor voltage ripples without changing the peak capacitor voltage. Therefore, the SM capacitance can be considerably reduced. The operation principle, design, and control methods of the HR SC-MMC are presented. The impacts of the proposed method on the rms current, power loss, and temperature rise of the SM capacitor are also analyzed. Based on the detailed comparison results, the proposed method effectively reduces the valve volume and cost, avoids a significant increase in the total power loss, and keeps the switch installation capacity and P-Q capability unchanged. Although the rms current and power loss of SM capacitors are increased, this may be acceptable, as the capacitor ripple current capability is underutilized and the increase in total power loss is small compared to existing methods. The effectiveness of HR SC-MMC is verified by simulation and experimental results.

APPENDIX

The amplitude of the converter's three-phase output voltages $U_{\rm va}$, $U_{\rm vb}$, and $U_{\rm vc}$ can be calculated as

$$U_{\rm va} = \sqrt{\left(u_{\rm vd}^{+} + u_{\rm vd}^{-} + u_{\rm vd}^{0}\right)^2 + \left(u_{\rm vq}^{+} - u_{\rm vq}^{-} + u_{\rm vq}^{0}\right)^2}$$

$$U_{\rm vb} = \frac{1}{2}\sqrt{\begin{matrix}\left(-u_{\rm vd}^{+} + \sqrt{3}u_{\rm vq}^{+} - u_{\rm vd}^{-} + \sqrt{3}u_{\rm vq}^{-} + 2u_{\rm vd}^{0}\right)^2 \\ +\left(-\sqrt{3}u_{\rm vd}^{+} - u_{\rm vq}^{+} + \sqrt{3}u_{\rm vd}^{-} + u_{\rm vq}^{-} + 2u_{\rm vq}^{0}\right)^2\end{matrix}}$$

$$U_{\rm vc} = \frac{1}{2}\sqrt{\begin{matrix}\left(-u_{\rm vd}^{+} - \sqrt{3}u_{\rm vq}^{+} - u_{\rm vd}^{-} - \sqrt{3}u_{\rm vq}^{-} + 2u_{\rm vd}^{0}\right)^2 \\ +\left(\sqrt{3}u_{\rm vd}^{+} - u_{\rm vq}^{+} - \sqrt{3}u_{\rm vd}^{-} + u_{\rm vq}^{-} + 2u_{\rm vq}^{0}\right)^2\end{matrix}}$$

where the $u^{+}{}_{\mathrm{vd}}$, $u^{+}{}_{\mathrm{vq}}$, $u^{-}{}_{\mathrm{vd}}$, $u^{-}{}_{\mathrm{vq}}$, $u^{0}{}_{\mathrm{vd}}$, and $u^{0}{}_{\mathrm{vq}}$ represent the positive, negative, and zero sequence components of the converter output voltage, respectively. They can be further calculated as

$$\begin{bmatrix} u_{\mathrm{vd}}^{+} \\ u_{\mathrm{vq}}^{+} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{sd}}^{+} \\ u_{\mathrm{sq}}^{+} \end{bmatrix} + X \begin{bmatrix} -i_{\mathrm{vq}}^{+} \\ i_{\mathrm{vd}}^{+} \end{bmatrix} \begin{bmatrix} u_{\mathrm{vd}}^{-} \\ u_{\mathrm{vq}}^{-} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{sd}}^{-} \\ u_{\mathrm{sq}}^{-} \end{bmatrix} \begin{bmatrix} u_{\mathrm{vd}}^{0} \\ u_{\mathrm{vq}}^{0} \end{bmatrix} = X_0 \begin{bmatrix} -i_{\mathrm{vq}}^{0} \\ i_{\mathrm{vd}}^{0} \end{bmatrix}$$

X and X_0 represent the inductances of the positive and zero sequences, respectively.

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