Isolated Three-Phase Soft-Switching DC-DC Converter With Reduced Voltage Stress on Rectifier Diodes for Off-Board Chargers

Raimundo Nonato Moura de Oliveira, José Willamy Medeiros de Araújo, Luiz Henrique Silva Colado Barreto, *Senior Member, IEEE*, Dalton de Araujo Honorio, *Senior Member, IEEE*, and Demercil de Souza Oliveira, Jr., *Senior Member, IEEE*

***Abstract*—This article presents a novel high-frequency isolated dc–dc converter feasible for level 2 and level 3 electric vehicle (EV) chargers. It exhibits pulsewidth modulation characteristics on high-frequency rectification semiconductors, enabling the use of low-voltage diodes. The steady-state analysis is derived in terms of the operating stages, voltage gain behavior, soft-switching regions, and loss mechanism. A laboratory prototype is designed with a rated power of 10 kW and dc output voltage ranging between 200 V and 920 V, aiming to validate the theoretical assumptions. Under nominal operating conditions, the maximum obtained efficiency is above 98% while presenting good performance across the entire operating range for EV chargers.**

***Index Terms*—Battery chargers, DC-DC power converters, electric vehicles, soft switching.**

I. Introduction

THE constant increase in the number of electric vehicles (EVs) requires adequate charging infrastructure, making the implementation of public battery charging points fundamentally important. However, long charging times and limited range still challenge the expansion of this market [1], [2], [3]. For instance, the voltage levels of battery packs typically vary between 200 V and 920 V, depending on the size and performance of the EV. Generally, increasing pack voltage is required to boost charging power without raising current levels [4]. Therefore, commercial chargers must be designed to provide fast charging (FC) over a wide range of voltage ratings, while keeping compatibility with the broadest possible range of models and manufacturers. Various technical standards have been established, such as the combined charging system (CCS) standard, which integrates ac or dc charging into a single plug and enables data communication between EVs and charging stations. Notably, this is a worldwide regulation, offering global compatibility, interoperability, and a streamlined charging experience for EV owners.

The most established solutions for conventional level 2 and level 3 charger topologies have two stages: an ac–dc converter responsible for providing power factor correction and a regulated dc voltage for meeting grid requirements; and the dc–dc stage with galvanic isolation at high frequency and controlled power flow to the battery pack [5], [6]. The main alternatives for dc–dc conversion are the dual active bridge (DAB) converter, families of resonant inductor-inductor-capacitor (*LLC*) converters, and traditional pulsewidth modulation (PWM) converters. DAB-based solutions typically feature bidirectional power flow with a restricted soft-switching range and a limited voltage gain range due to efficiency decrease when the output voltage deviates from its optimal value [7], [8]. The resonant *LLC* approach has soft-switching behavior for a certain operating range, with voltage regulation capacity that avoids dc bias in the high-frequency transformer. However, these solutions have limitations in the design of the resonant tank and in the variation of switching frequency for applications with a wide output voltage range. In addition, a more complex control methodology is required, typically involving a variable switching frequency [9], [10], [11]. Then, to accommodate wider voltage ranges supplied to battery packs, more complex topologies have been proposed to minimize the undesirable characteristics of these converters. For instance, a three-level resonant topology is presented in [12]. Although a 3.5 kW downscale prototype relies on a voltage range of up to 700 V, the article presents an algorithm for selecting the working mode based on the root mean square current of the high-frequency transformer. This allows for optimizing the performance and efficiency of the converter across different operating conditions.

Furthermore, a reconfigurable two-stage dc–dc resonant converter rated at 11 kW is proposed in [13]. It is based on a voltage-doubler/current-doubler reconfigurable structure, which

Received 25 July 2024; revised 21 October 2024 and 3 January 2025; accepted 10 February 2025. Date of publication 21 February 2025; date of current version 14 April 2025. This work was supported in part by Fundep/Mover, WEG Automation & Control under Grant 27192-56 and in part by the National Council for Scientific and Technological Development under Grant 404021/2023-9. Recommended for publication by Associate Editor T. Jimichi. *(Corresponding author: Dalton de Araujo Honorio.)*

Raimundo Nonato Moura de Oliveira is with the Raimundo Nonato Moura de Oliveira, Instituto Federal do Ceará, Instituto Federal do Ceará Campus Limoeiro do Norte, Limoeiro do Norte, Ceará 62930-000, Brazil (e-mail: nonato.oliveira@ifce.edu.br).

José Willamy Medeiros de Araújo, Luiz Henrique Silva Colado Barreto, Dalton de Araujo Honorio, and Demercil de Souza Oliveira, are with the Departamento de Engenharia Elétrica, Universidade Federal do Ceará, Fortaleza, Ceará 60020-181, Brazil (e-mail: willamy@dee.ufc.br; lbarreto@dee.ufc.br; dalton@dee.ufc.br; demercil@dee.ufc.br).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3544514.

Digital Object Identifier 10.1109/TPEL.2025.3544514

requires additional switches to enable reconfiguration and achieve a wide output voltage range. Although the resonant power converter achieves a wide output voltage range, it experiences a significant efficiency drop during heavy charging periods and when operating at a lower voltage rating due to turn-ON switching losses and the small duty cycle.

The two-stage, three-level converter with inherent dc voltage balance across series capacitors on the ac side (stage 2 of the proposed study) proposed in [14] simplifies control requirements and reduces costs. While the converter inherently balances dc voltages without the need for additional balancing techniques, the design requirements for achieving this balance and ensuring soft switching at the dc side (stage 1 of the proposed study) may involve complex calculations and considerations. Wide output voltage range is achieved due to reconfiguration and use of a buck converter in the second stage. However, the hard-switching characteristic of the buck stage limits the switching frequency, yielding an output filter with high dimensions.

Solutions PWM-based topologies are relatively simple, but they must however address the challenges of inductor-capacitor (*LC*) filters at the output, which do not guarantee voltage clamping on the rectifier diodes [15]. Additionally, the leakage inductance causes a reduction in the effective duty cycle, resulting in a decrease in voltage gain. Due to the absence of voltage clamping on the rectifier diodes, these solutions may require either semiconductors in series or high-voltage-rated components, which are typically more expensive and offer poor performance. In this context, the topology proposed for fast charger applications retains the advantages of PWM converters, while extending the required output voltage range and reducing voltage stress on the rectifier diodes.

This rest of this article is organized as follows. Section II describes the proposed three-level dc–dc architecture and its operation regions, namely region 01, region 02, and region 03, along with a thorough theoretical analysis. Section III is dedicated to the experimental verification of the proposed converter, covering operation stages, behavior of the voltage gain, soft-switching regions, and loss analysis. A 10 kW test bench is built to provide a wide output voltage range from 200 to 920 V.

II. Proposed Topology

A. Conception

The proposed converter presented in Fig. 1 consists of two three-phase inverter bridges (bridge 01 and bridge 02) composed of active semiconductors; six single-phase high-frequency transformers (T_{a1}, T_{b1}, T_{c1}, T_{a2}, T_{b2}, and T_{c2}), which provide galvanic isolation and allow for adjusting the voltage gain between the primary and secondary; a rectifier with current multiplier characteristics with six diodes (D_1, D_2, D_3, D_4, D_5 and D_6) connected to the secondary windings of the transformers; and three filter inductors (L_1, L_2 and L_3), which together with the capacitor C_o form an *LC* filter. The leakage inductances of the transformers ($L_{da1}, L_{db1}, L_{dc1}, L_{da2}, L_{db2}$, and L_{dc2}) are referred to their respective primary sides.

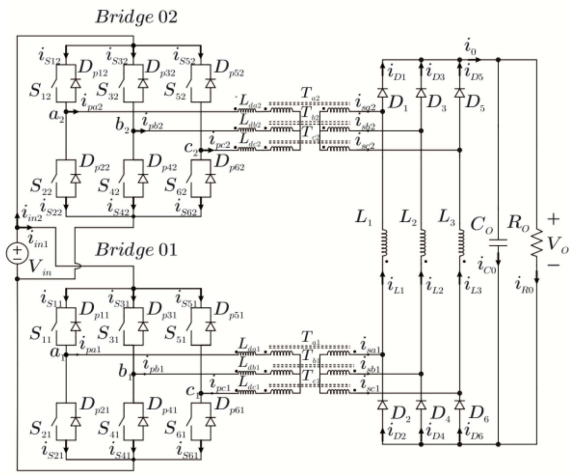

Fig. 1. Proposed converter.

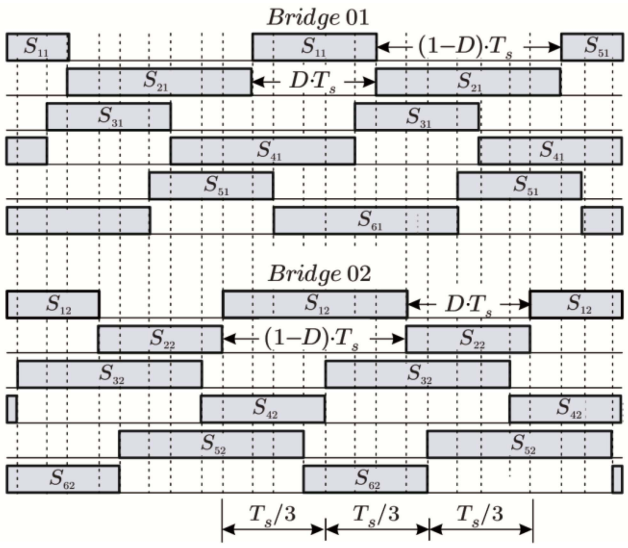

Fig. 2. Asymmetric command of the proposed converter.

PWM based on complementary signals is used to drive the switches in each module [16], [17], as shown in Fig. 2. The upper-side semiconductors of bridge 01 are driven with a duty cycle *D* while the lower-side semiconductors are driven with a complementary signal. Similarly, the upper-side semiconductors of bridge 02 are driven with a duty cycle (1-*D*), with the lower-side semiconductors driven with a complementary signal. Both modules use the same carriers, which are phase-shifted by 120°.

B. Operation

Analyzing the switching states and the line currents reveals that the converter has three well-defined operational regions. Using the semiconductors of bridge 01 as a reference, the converter operates in region 01 when there is no overlapping of the upper-side semiconductors, which occurs when $D \leq 0.33$. The converter operates in region 02 when two upper-side semiconductors overlap within the range $0.33 \leq D \leq 0.66$. Finally, region

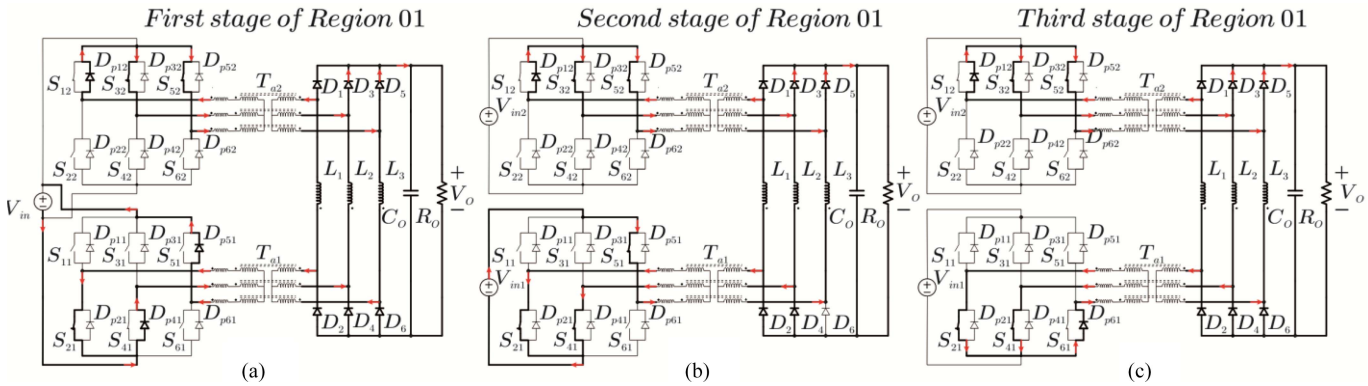

Fig. 3. Operating stages of the converter operating in region 01. (a) First stage. (b) Second stage. (c) Third stage.

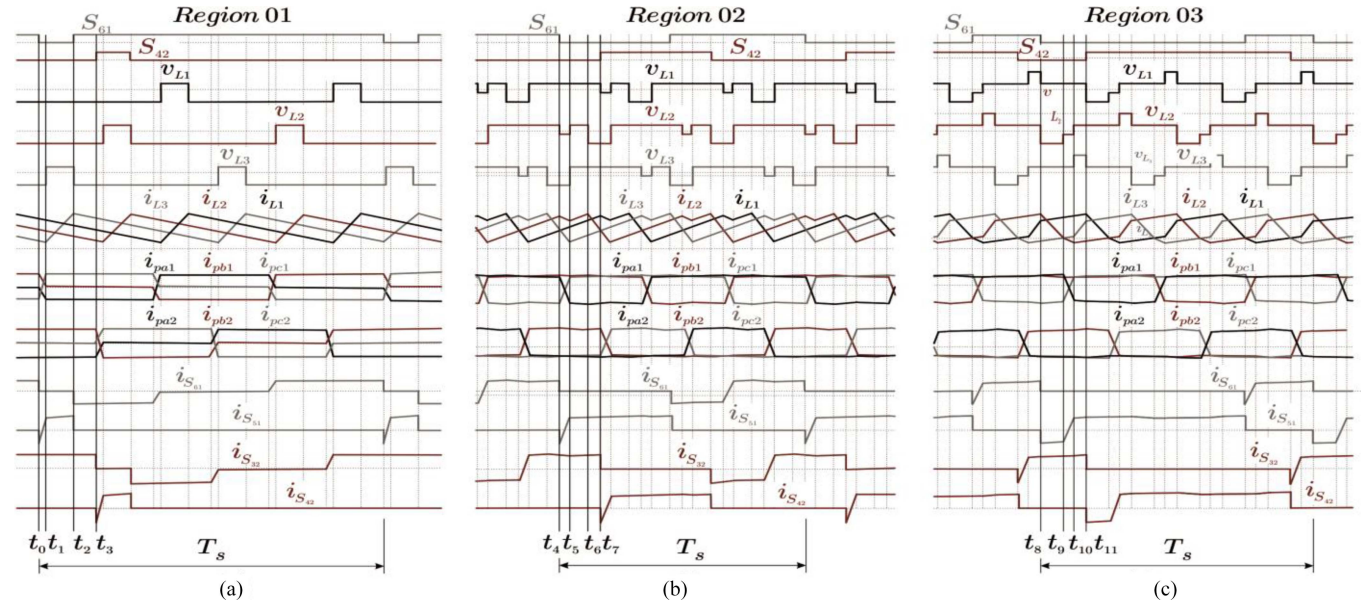

Fig. 4. Main theoretical waveforms of the proposed converter in (a) region 01, (b) region 02, and (c) region 03.

03 occurs when all three upper-side semiconductors overlap, which occurs when $0.66 \leq D \leq 1$. It should be noted that these limits do not take into account the duty cycle loss due to leakage inductances.

In addition, a sub-region occurs during the transition between regions 01 and 02, characterized by a constant voltage gain. Each region has 18 operating stages within the same switching period. Owing to the symmetry of the waveforms, only three stages per region must be analyzed, as their behaviors can be used to understand the remaining operating stages. Therefore, it is possible to analyze the converter operation considering ideal and lossless elements. For this purpose, let us define the output current as I_o, the switching period as T_s, and the common dc input power supply as $V_{\text{in1}} = V_{\text{in2}} = V_{\text{in}}$. The dc output voltage corresponds to V_o, the leakages inductances of the transformers ($L_{da1}, L_{db1}, L_{dc1}, L_{da2}, L_{db2}$, and L_{dc2}) are equal to L_d, the filter inductances (L_1, L_2, and L_3) are equal to L, and the turn ratio is $n = 1$.

1) Region 01: For simplicity, the turn-ON instant of switch S_{61} is considered the initial moment t_0. Fig. 3 shows the resulting states of the semiconductors and the current path in the converter for the first three stages, while the main voltage and current waveforms are represented in Fig. 4(a).

a) First stage (linear current) [t_0, t_1]: From Figs. 3(a) and 4(a), it can be seen that when S_{61} turns OFF, the currents through the leakage inductors of *bridge 01* vary linearly. In *bridge 02*, the transformers' primary sides are short-circuited, and all rectifier diodes are directly biased, thus resulting in a voltage $-V_o$ applied to the three filter inductors, v_{L1}, v_{L2}, and v_{L3}. The duration of this stage is given by

$$\Delta t_1 = \frac{L_d \cdot I_o}{V_{\text{in}}}. \tag{1}$$

b) Second stage (energy transfer) [t_1, t_2]: After the linear stage ends, this stage begins with the turn-ON of S_{51} under zero-voltage switching (ZVS) conditions. A direct energy transfer

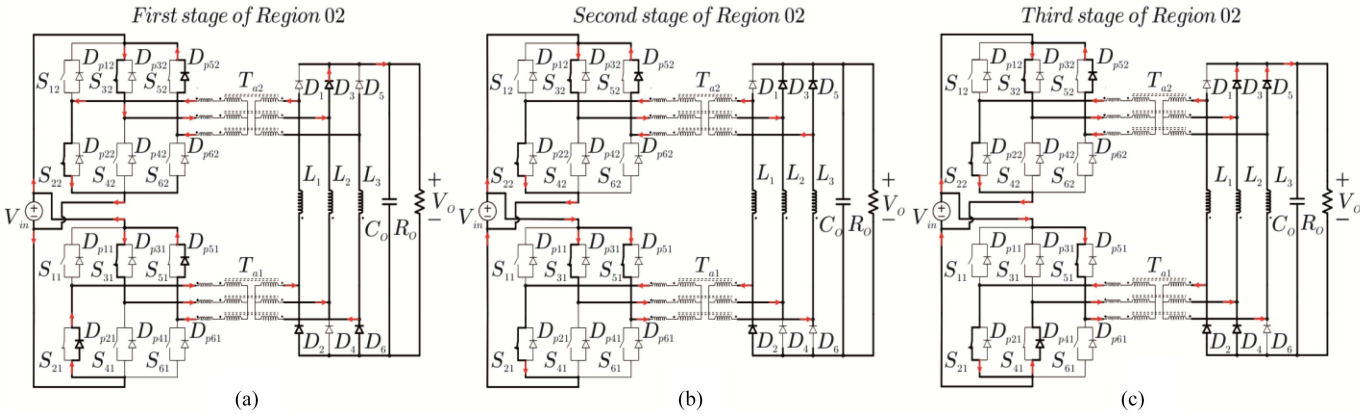

Fig. 5. Operating stages of the converter operating in region 02. (a) First stage. (b) Second stage. (c) Third stage.

occurs through L_3 when D_6 is reverse biased in Fig. 3(b). Then, the voltage across L_3 is $V_{\text{in}}-V_o$, while the voltages across L_1 and L_2 remain constant. The duration of this stage is given by

$$\Delta t_2 = D \cdot T_s - \frac{L_d \cdot I_o}{V_{\text{in}}}. \tag{2}$$

c) Third stage (freewheeling) [t_2, t_3]: With the turn-OFF of S_{51} and the direct biasing of D_{p61}, the freewheeling behavior begins. As shown in Fig. 3(c), this transition results in a short-circuit of the transformer primary sides associated with *bridge 01*. During this stage, the currents through all filter inductors decrease because the transformers are short-circuited and no energy transfer occurs. Diode D_6 becomes directly biased again, and all inductors are subjected to the voltage $-V_o$. The duration of this stage is given by

$$\Delta t_3 = T_s \cdot \left(\frac{1}{6} - D\right). \tag{3}$$

2) Region 02: The linear current transition occurs in only two energy transfer stages in this region.

a) First stage (linear current) [t_4, t_5]: This stage begins with the turn-OFF of S_{61}, corresponding to the linear transition between the currents of phases *a* and *c* of *bridge 01* as shown in Figs. 4(b) and 5(a). Then, diode D_4 is reverse biased and submitted to a reverse voltage around $V_{\text{in}}/2$, since diodes D_2 and D_6 are directly biased, and the phases *a* and *c* of *bridge 01* represent the current paths at the primary side.

This stage ends when the current flowing through phase *c* equals the current through L_3. Therefore, the voltages across inductors for L_1, L_2, and L_3 are $V_{\text{in}}-V_o$, $V_{\text{in}}/2-V_o$, and $-V_o$, respectively. The duration of this stage is given by

$$\Delta t_4 = 2 \cdot \frac{L_d \cdot I_o}{V_{\text{in}}}. \tag{4}$$

b) Second stage (energy transfer) [t_5, t_6]: In this stage, energy is transferred from the source to filter inductors, L_1, L_2, and L_3, as well as to the load. Furthermore, diode D_6 is reverse biased, as the voltages across all inductors are equal to $V_{\text{in}}-V_o$, as shown in Figs. 4(b) and 5(b). The duration of this stage is given by

$$\Delta t_5 = T_s \cdot \left(D - \frac{1}{3}\right) - 2 \cdot \frac{L_d \cdot I_o}{V_{\text{in}}}. \tag{5}$$

c) Third stage (freewheeling) [t_6, t_7]: The partial energy transfer condition occurs after D_4 is directly biased, involving inductors L_1 and L_3. Then, the energy stored in L_2 is transferred to the load, as the voltage across it, equals $-V_o$, while the voltages across the remaining inductors remain constant at $V_{\text{in}}-V_o$. The duration of the stage is given by

$$\Delta t_6 = T_s \cdot \left(D - \frac{1}{2}\right). \tag{6}$$

3) Region 03: The switching states and the path in the converter operating in region 03 are shown in Fig. 6, as the respective instantaneous waveforms are given in Fig. 4(c).

a) First Stage (Freewheeling) [t_8, t_9]: This stage begins with the turn-OFF of S_{61} and is characterized by a short-circuit in the primaries of the transformers in *bridge 01*, creating a freewheeling path for the current. As shown in Fig. 6(a), energy is transferred from *bridge 02* to inductors L_1 and L_3, with their voltages being $V_{\text{in}}-V_o$, while the voltage across L_2 is $-V_o$. The duration of this stage is given by

$$\Delta t_7 = T_s \cdot \left(D - \frac{2}{3}\right). \tag{7}$$

b) Second Stage (Linear Current) [t_9, t_{10}]: The second stage begins with the turn-OFF of S_{11} due to the linear transition of the current flowing between phases *a* and *c* of *bridge 01*, as in Fig. 6(b). Then, the voltages across L_1 and L_3 remain constant at $V_{\text{in}}-V_o$, while the voltage across L_2 is $V_{\text{in}}/2-V_o$. The duration of this stage is given by

$$\Delta t_8 = 2 \cdot \frac{L_d \cdot I_o}{V_{\text{in}}}. \tag{8}$$

c) Third Stage (Energy Transfer) [t_{10}, t_{11}]: This stage begins when D_6 is reverse biased and ends with the turn-OFF of S_{42}. From Fig. 6(c), it is observed that energy transfer occurs through the filter inductors L_1, L_2, and L_3. Therefore, the voltages across L_2 and L_1 is equal to $V_{\text{in}}-V_o$, while the one across L_3 is now

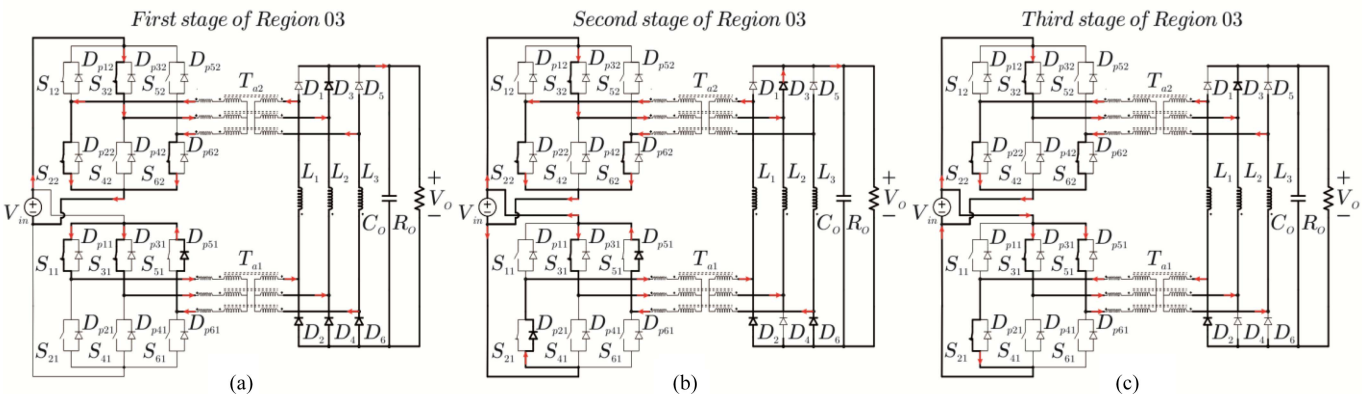

Fig. 6. Operating stages of the converter operating in region 03. (a) First stage. (b) Second stage. (c) Third stage.

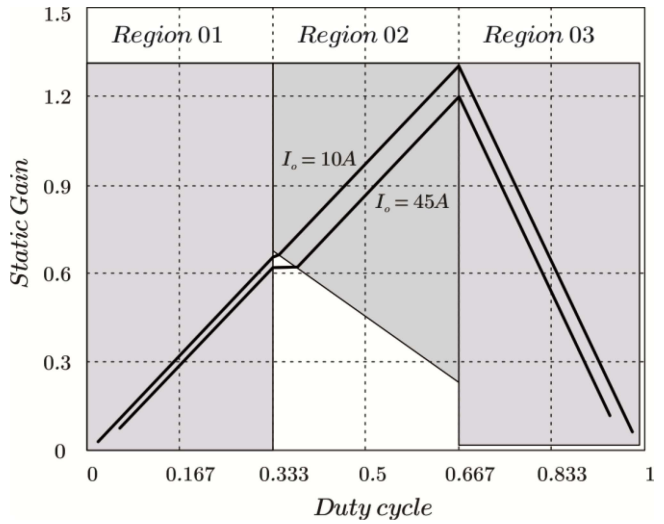

Fig. 7. Behavior of the theoretical voltage gain as a function of the duty cycle.

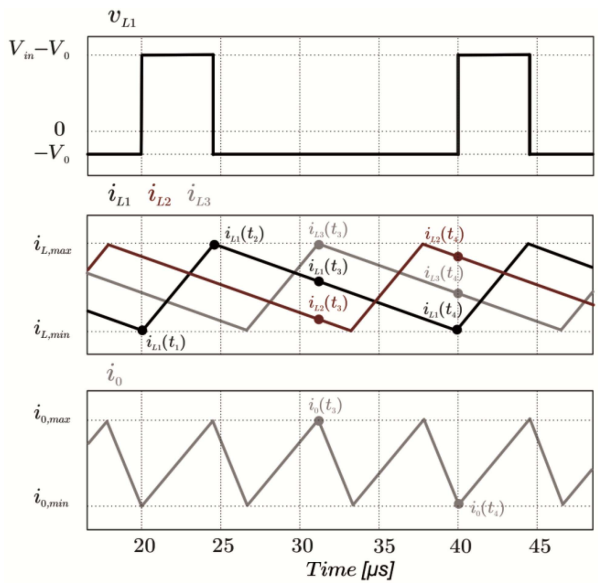

Fig. 8. Current ripples in the filter components. (a) Voltage across output filter inductor L_1. (b) Currents through the output filter inductors L_1, L_2, and L_3. (c) Ripple before the output capacitor filter C_o.

equal to $2{\cdot}V_{\rm in}-V_o$. The duration of this stage is given by

$$\Delta t_9 = T_s \cdot \left(\frac{5}{6} - D\right) - 2 \cdot \frac{L_d \cdot I_o}{V_{\rm in}}. \tag{9}$$

C. Mathematical Analysis

1) Voltage Gain: Since the average voltages across the inductors are zero over one switching period comprising 18 stages, the voltage gain corresponding to G, can be obtained from (10), yielding the plots represented by Fig. 7.

$$G = \begin{cases} \left(2 \cdot D - \frac{2{\cdot}I_o{\cdot}L_d}{T_s{\cdot}V_{\rm in}}\right) \; if \; \frac{1}{6} - \frac{2{\cdot}I_o{\cdot}L_d}{T_s{\cdot}V_{\rm in}} < D \leq \frac{1}{3} \\ \left(2 \cdot D - \frac{6{\cdot}I_o{\cdot}L_d}{T_s{\cdot}V_{\rm in}}\right) \; if \; \frac{1}{3} + \frac{2}{3} \cdot \frac{2{\cdot}I_o{\cdot}L_d}{T_s{\cdot}V_{\rm in}} < D \leq \frac{2}{3} \\ \left(4 - 4 \cdot D - \frac{6{\cdot}I_o{\cdot}L_d}{T_s{\cdot}V_{\rm in}}\right) \; if \; \frac{2}{3} < D \leq 1 - \frac{2{\cdot}I_o{\cdot}L_d}{T_s{\cdot}V_{\rm in}} \end{cases}. \tag{10}$$

2) Filter Inductance and Output Currents Ripple: The current ripples in the inductors and filter capacitors are crucial for designing these components. Additionally, the information from the previous sections allows for defining the behavior of the current ripples for the filter inductors L_1, L_2, and L_3, as well as the output current across all operational regions. Thus, the voltage across inductor L_1, v_{L1}, the inductors currents, i_{L1}, i_{L2}, and i_{L3}, and their sum, i_0, all of them for Region 01 are considered only. To simplify the calculation of the current ripple through L_1, its lowest value in Fig. 8, $i_{L,\rm min}$, is considered null, i.e., $i_{L1}(t_1) = 0$. From Fig. 8, one can also obtain the curves representing the current ripple considering different operating conditions.

3) Operational Regions Complete Behavior: To address and verify these behaviors in terms of the voltage gain and current ripples, a simulation analysis was performed using the information in Table II and compared with theoretical findings. Fig. 9 shows both the analytical and simulation results. In Fig. 9(a), the entire range of the normalized voltage gain as a function of D for the considered operational regions is displayed. Additionally, due to the wider range of D, regions 01 and 02 are advantageous because they offer better resolution, particularly for digital drive and control approaches.

TABLE I
COMPARISON OF THE PROPOSED TOPOLOGY WITH THE EXISTING WIDE-VOLTAGE RANGE TOPOLOGIES

Topology identifier	Type	Switches / Diodes	Reconfiguration	Gain control method	Frequency range (kHz)	Output range (V)	Maximum output power (kW)	Peak efficiency (%)
T1 [19]	LLC + Buck	5 SiC MOSFETs 8 Si diodes + 1 SiC diode	DC relays 0	FM+ PWM	120 LLC 50 Buck	50 - 650	20	97.03
T2 [20]	LCL - T	8 GaN FETs 0 diode	DC relays 3	PS	500	150 - 950	6.6	98,20
T3 [1]	LLC	4 SiC MOSFETs 8 SiC diodes	DC relays 3	FM	80 - 350	200 - 1000	10	98,70
T5 [21]	PWM	4 SiC MOSFETs 8 SiC diodes	DC relays 3	PS	15	250-1000	11	98,30
T4 [22]	LLC	6 SiC MOSFETs 6 Sic diodes	DC relays 0	FM + PS	50 - 155	100 - 1100	0.7	Not presented
Proposed	PWM	12 SiC MOSFETs 6 SiC diodes	DC relays 0	PWM	40	200 - 920	10	98.13

TABLE II
PARAMETERS ADOPTED IN THE DESIGN OF THE EXPERIMENTAL PROTOTYPE

Parameters	Value
Switching frequency, f_s	50 kHz
Dead time, t_d	70 ns
Leakage inductance, L_d	5 μH
Capacitances of the primary-side switches, C_{51},… and C_{62}	110 pF
Filter inductances, L_1, L_2 and L_3	1 mH
Filter capacitance, C_o	100 μH
Equivalent series resistance, r_{se}	100 mΩ
DC-bus voltage, V_{in}	600 V
Rated output voltage, V_o	920 V
Rated output power, P_o	10 kW
Maximum output current, I_o	14.28 A

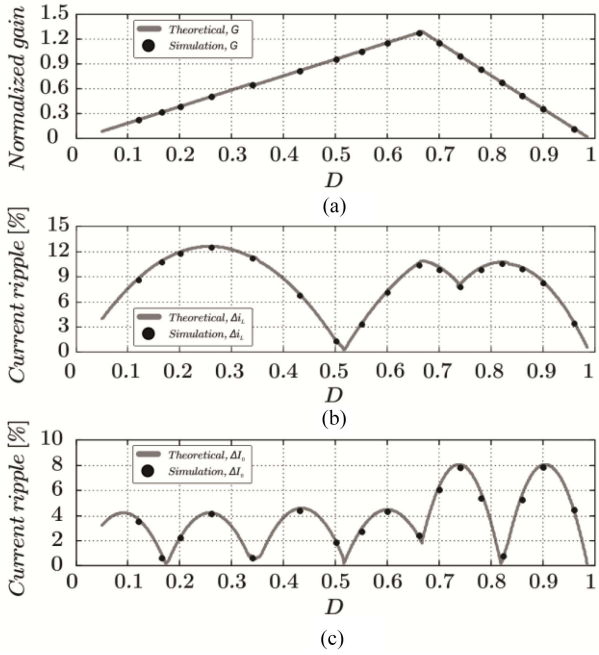

Fig. 9. Result obtained from the simulation and theoretical analysis. (a) Voltage gain. (b) Current ripple in the filter inductors. (c) Output current ripple.

Fig. 9(b) shows the current ripples in the filter inductors, while Fig. 9(c) shows the output current. The values presented in the plots are related to the maximum converter current, which occurs at the rated power with a voltage of 700 V. Thus, it is observed that regions 01 ($0 \leq D < 0.33$) and 02 ($0.33 \leq D < 0.66$) have smaller output current ripples than those for region 03 ($D < 0.66$). In regions 01 and 02, the current ripples reach their maximum at $D = 0.25$ and their minimum at $D = 0.5$.

D. Soft-Switching Analysis

During the dead time interval of one leg, the energy stored in the leakages inductor is responsible for charging and discharging the intrinsic capacitances of the switches. A proper amount of energy accumulated in the parasitic capacitances, combined with an adequate dead time can yield favorable ZVS conditions, thereby improving the overall efficiency. Fig. 10 presents the ZVS range in terms of the adopted dead time, t_d, and the normalized output current, I_o, for all operational regions. It is worth mentioning that parameters in Table II and the maximum output current, $I_{o,\max}$, were considered in the largest ZVS switching area for all semiconductors. This characteristic reinforces the advantage of operating in regions 01 and 02, especially within the range 30 ns $< t_d <$ 90 ns and at least 50% of the rated power condition.

E. Dynamic Analysis

The dynamic analysis was conducted for the three operating regions of the converter elaborated similarly to the study of the Hybridge converter presented in [18]. The study was carried out for the three operating regions of the converter. Considering that L is the equivalent inductance of the output filter, i_L is the sum of the currents of the filter inductors, C is the output capacitive filter, r_{se} is the equivalent series resistance of the capacitive filter, v_c is the voltage across the capacitor C, R_0 is the load resistance, V_{in} is the input voltage, and that the converter operates in the first region, the state space equations are represented as

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = A \cdot \begin{bmatrix} i_L \\ v_c \end{bmatrix} + B \cdot V_{\text{in}} \tag{11}$$

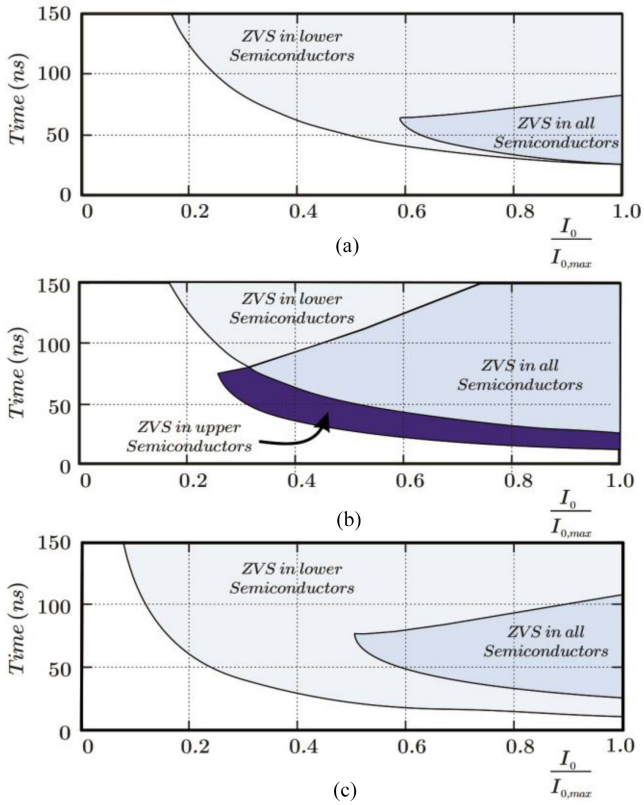

Fig. 10. ZVS ranges in (a) region 01, (b) region 02, and (c) region 03.

where A is the state variable matrix (12) and B is the input matrix (13)

$$A = \begin{bmatrix} -\frac{1}{L}\cdot\frac{R_0\cdot r_{se}}{R_0+r_{se}} - \frac{R_d}{L} & -\frac{1}{L}\cdot\frac{R_0}{R_0+r_{se}} \\ \frac{1}{C}\cdot\frac{R_0}{R_0+r_{se}} & -\frac{1}{C}\cdot\frac{1}{R_0+r_{se}} \end{bmatrix}. \quad (12)$$

$$B = \begin{bmatrix} \frac{2\cdot D}{L} \\ 0 \end{bmatrix}. \quad (13)$$

In (12), $R_d = 2{\cdot}f_s{\cdot}L_d$ is related to the duty cycle loss due to transformer leakage. For the second operating region, the state matrices remain the same as in (11). However, the term corresponding to the duty cycle loss (R_d) is three times greater, due to the change in the converter's equivalent circuit for this region. The duty cycle loss factor for the third region remains the same as in the second region. Still, the input matrix in (13) is given by (14), as the absolute value of the derivative of the voltage gain in this region is greater than in the other two regions

$$B_i = \begin{bmatrix} \frac{4-4\cdot D}{L} \\ 0 \end{bmatrix}. \quad (14)$$

Considering a function point of I_L, V_c, D, V_{in}, and R_0, by linearizing (11), the transfer function that relates the output voltage and the duty cycle is given by

$$G_{v/d}(s) = 2\cdot V_{\text{in}}\cdot\frac{r_{se}\cdot C_0\cdot s+1}{a_2\cdot s^2+a_1\cdot s+a_0} \quad (15)$$

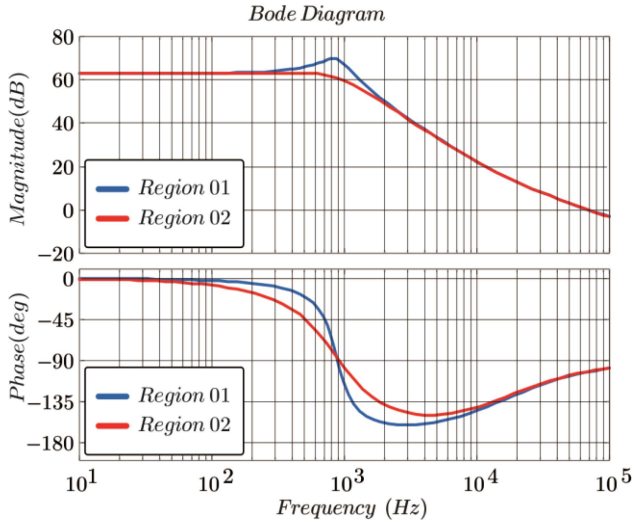

Fig. 11. Dynamic behavior of the converter output voltage as a function of the duty cycle for regions 01 and 02.

where

$$a_2 = L\cdot C_0\left(1+\frac{r_{se}}{R_0}\right) \quad (16)$$

$$a_1 = \left[r_{se}+R_d\cdot\left(1+\frac{r_{se}}{R_0}\right)\right]\cdot C_0+\frac{L}{R_0} \quad (17)$$

and

$$a_0 = \frac{R_d}{R_0}+1. \quad (18)$$

Fig. 11 shows the dynamic behavior of the converter for the transfer function presented in (15) for the first two regions. It is observed that both magnitude and phase are equivalent at low and high frequencies.

The dynamic behavior for frequencies close to 1 kHz shows slight differences in magnitude and phase; however, it was found that a single well-tuned proportional-integral/proportional-integral-derivative controller can ensure system stability in both regions. The transfer functions can be validated by simulation using the ac sweep method. Fig. 12 shows the theoretical and simulated behaviors of the converter based on the parameters listed in Table II. It is verified that the model accurately represents the simulated result.

III. Comparative Analysis

The proposed topology is compared with resonant *LLC* topologies, as outlined in Table I. The T1 topology [19] features a two-stage design: the first stage is an unregulated resonant converter operating at its resonance frequency, while the second stage is a non-isolated step-down converter. In T1, the active switches in the first stage always achieve ZVS. However, the rectifier stage includes four diodes in series, and the cascaded buck converter processes the entire power supplied to the load. This results in switching losses that limit the switching frequency of this stage. Other solutions designed to accommodate a wide output voltage range, such as those in T2 [20], T3 [1], and

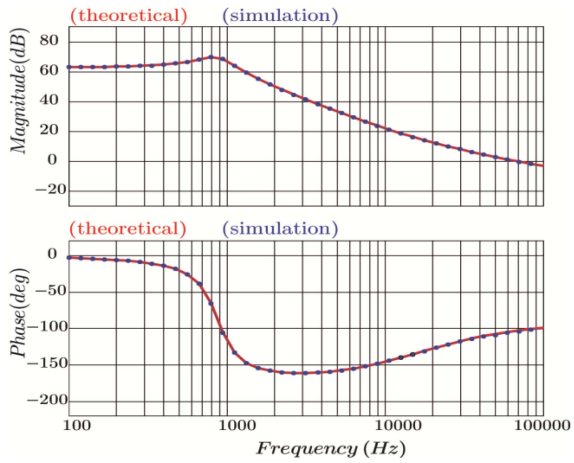

Fig. 12. Simulations of the dynamic behavior of the converter output voltage as a function of the duty cycle for region 01.

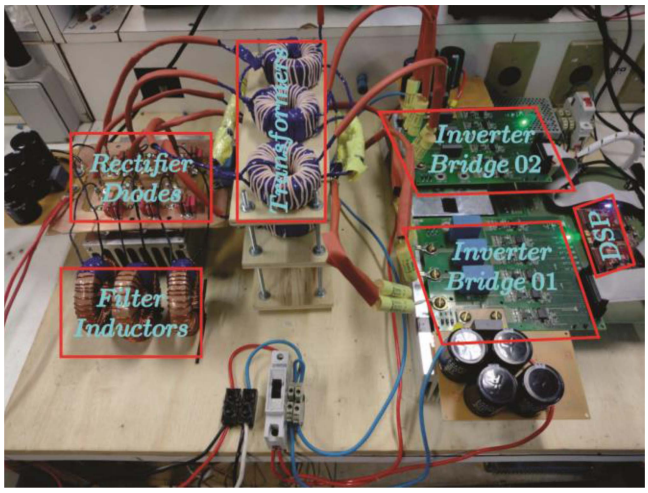

Fig. 13. 10 kW experimental prototype.

T4 [21], are based on resonant converters with reconfigurable rectifier stages. When compared to the proposed topology, these alternatives not only have higher costs due to the inclusion of dc contactors or relays, but they also risk operational discontinuity during reconfiguration.

Particularly, T2 and T3 are resonant converters and require a wide switching frequency range. In contrast, T4 features a PWM-based design with a fixed duty cycle and switching frequency, utilizing phase-shift modulation. This topology is based on the phase-shift full-bridge architecture and requires snubbers to minimize voltage stress on the rectifier diodes. However, the need for snubber circuits can negatively impact the converter's efficiency, especially at lower voltage levels. Despite this, T4 achieved a peak efficiency of 98.3% at higher voltages, making PWM converters a competitive option compared to conventional resonant solutions. In T5 [22], reconfigurations are achieved without the use of contactors or relays, relying instead on two metal-oxide field-effect transistor (MOSFETs) and two power diodes. This topology supports both half-bridge and full-bridge operations on the primary side, along with reconfigurable options on the secondary side, resulting in six distinct operating modes, each determined by the voltage requirements of the load. However, the need to accommodate a wide output voltage range through multiple operating modes introduces several discontinuities in operation. Additionally, the complexity of the design increases significantly, especially when considering the operational scope required to comply with the CCS standard for chargers. The operating modes were validated using a prototype with a power rating of only 700 W, without a detailed loss analysis, raising concerns about the converter's ability to handle higher power levels effectively. The proposed topology not only supports a wide range of output voltages but also operates with a fixed modulation frequency and avoids any load discontinuities throughout the operating range. In terms of scalability, it enables the design of a high-power FC within a single module, which justifies the inclusion of more converter components, such as a higher number of magnetic elements. While other studies report the use of fewer semiconductors, they face scalability challenges, often requiring multiple parallel converters to meet high-power FC demands. For instance, the 50 kW ABB Terra 53/54 FC employs five 10 kW modules in parallel to achieve the required power level [22].

Although the other studies use a smaller number of semiconductors, they also have limitations in terms of scalability, which implies the use of several parallel converters to meet the higher power FC requirements. The proposed converter operates with ZVS, approximately, 30% of the nominal load. It has lower voltage stress in the rectifier diodes a characteristic of the hybridge topology.

IV. Experimental Setup and Results

Experimental results were obtained from the 10 kW laboratory prototype shown in Fig. 13, whose main parameters are listed in Table II. Fig. 14 shows the behavior of the voltage across the rectifier diodes, the currents through the filter inductors, and the output voltage for $D = 0.25$, $D = 0.50$, and $D = 0.658$.

The plateau voltages across the diodes is about 720 V for all conditions, what gives room for the voltage oscillations due to the diodes reverse recovery, as shown in Fig. 14(a), (b), and (c), whilst allowing the use of 1.2 kV diodes.

Although there are some voltage spikes due to resonance involving the energy stored in the transformer's leakage inductances and parasitic elements, they do not exceed 1.2 kV. The current ripple behavior matches the theoretical analysis presented in Section III. Fig. 14(d) shows that the highest current ripple occurs at $D = 0.25$, while Fig. 14(e) shows the lowest ripple at $D = 0.50$. The current ripple increases until the end of Region 02, as shown in Fig. 14(f) for $D = 0.658$.

To evidence the soft-switching operation of the proposed converter, Fig. 15 presents the current and voltage waveforms of S_{51} and S_{61}. Fig. 15(a) represents the operation for $I_o = 11.3$ A, while the results $I_o = 3.8$ A are given in Fig. 15(b). It is noteworthy that only S_{51} operates under ZVS conditions. This result corroborates the previous theoretical analysis since

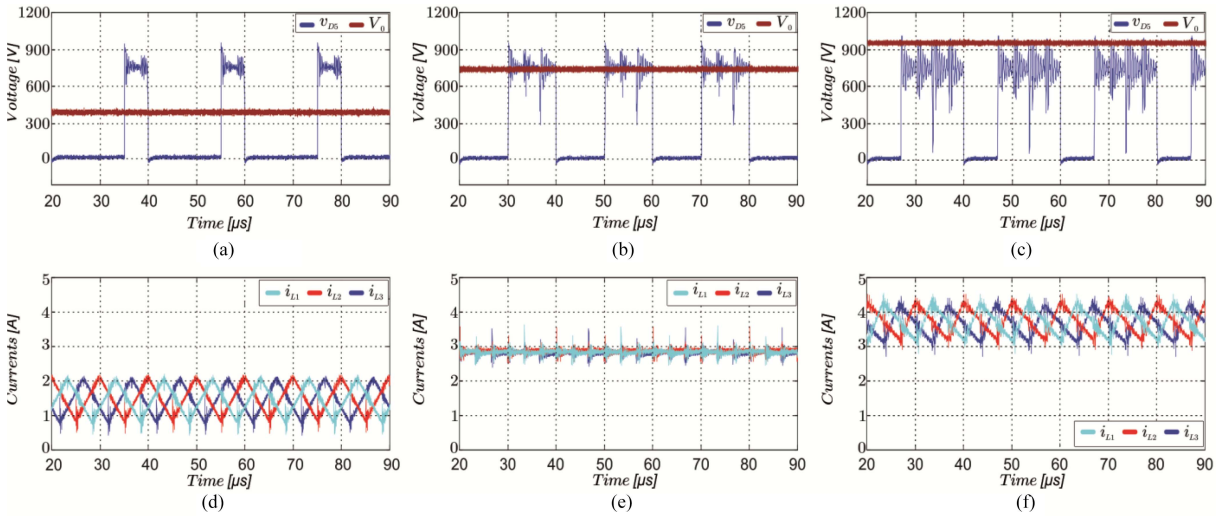

Fig. 14. Experimental waveforms of the reverse voltages across the rectifier diodes, currents through the filter inductors, and output voltage under distinct conditions. (a) $D = 0.25$. (b) $D = 0.50$. (c) $D = 0.658$. Currents through the filter inductors under distinct conditions. (d) $D = 0.25$. (e) $D = 0.50$. (f) $D = 0.658$.

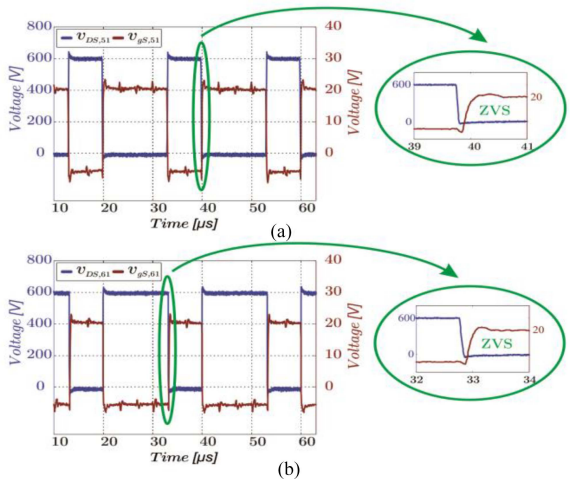

Fig. 15. Experimental results for the commutation of switches S_{51} and S_{61} in *region* 02 under distinct load conditions. (a) $I_o = 11.3$ A. (b) $I_o = 3.8$ A.

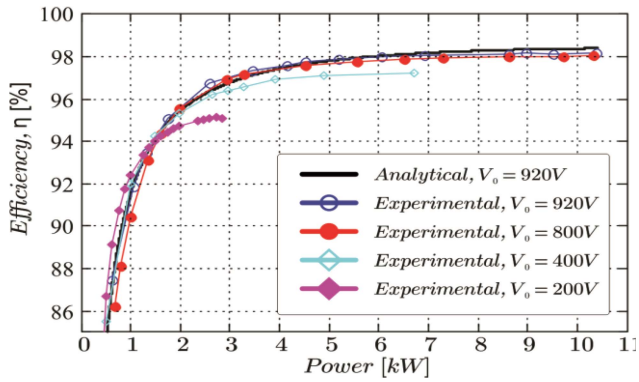

Fig. 16. Experimental results of the efficiency of the proposed converter considering multiple scenarios.

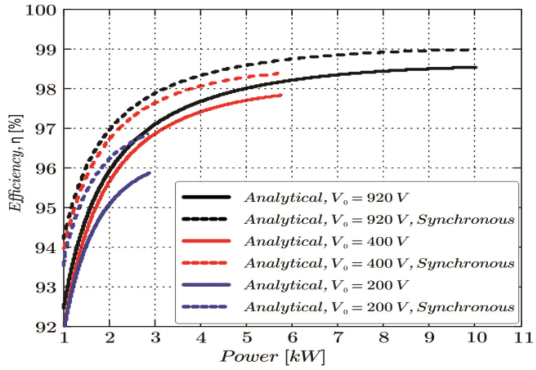

Fig. 17. Analytical efficiency of the proposed converter considering an active semiconductor at the secondary side and multiple scenarios.

the scenario in Fig. 15(b) corresponds to a dead-time interval of 70 ns and the normalized output current of 0.27.

Fig. 16 represents the converter efficiency for the rated conditions and three additional voltage levels: 800 V; 400 V; and 200 V. It reaches a maximum efficiency of 98.13% at the rated voltage. Furthermore, when the voltage reduces to 800 V, the maximum efficiency is 98.01%, while 97.17% and 95.04% are achieved when the voltage is 400 and 200 V, respectively. These results validate the PWM characteristics of the converter enabling operation over a wide range of output voltage variations with acceptable efficiency.

To minimize converter losses, a thorough analysis was conducted while replacing the power diodes with model G3R12MT12KA, aiming to provide synchronous rectification, as well as reducing the turn-OFF resistor from 6.67 Ω to 2.5 Ω to decrease switching losses.

Fig. 17 shows that under nominal conditions, the efficiency of the new design with synchronous rectification is approximately

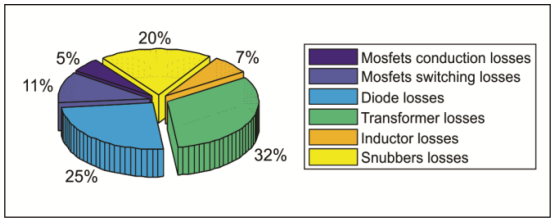

Fig. 18. Loss breakdown at the rated operating conditions.

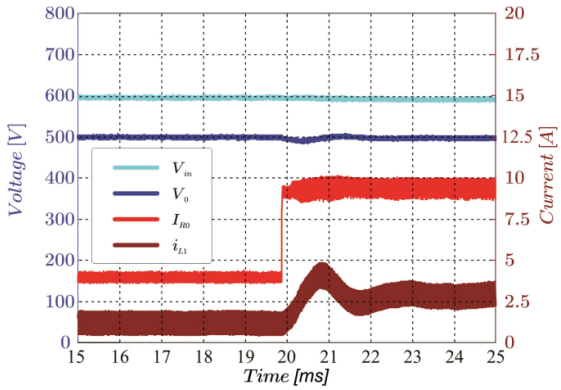

Fig. 19. Experimental results for a step-load from 1.8 kW to 4.6 kW with $Vo = 500$ V.

98.82%, representing a 0.45% improvement over the original design.

Fig. 18 presents the loss breakdown under rated conditions. It is assumed that all semiconductors achieve ZVS operation and that the reverse recovery losses of power diodes are neglected. The losses in magnetic cores were calculated using the Steinmetz coefficients provided by manufacturers. It is reasonable to state that optimizing parameters such as current ripple, switching frequency, and maximum magnetic field density in the transformer results in higher efficiencies in the design.

Based on the dynamic analysis of the converter performed in Section II, a controller was designed to assess system stability.

The transfer function presented in (15) was adopted, where the control variable is the output voltage, *Vo*. The controller was designed based on the pole placement technique, including an integrator, a pole placed at half the switching frequency, and a zero close to the resonance frequency of 1 kHz. Fig. 19 shows the step response considering a load step up from 1.8to 4.6 kW. It is observed satisfactory voltage regulation is achieved within acceptable settling time.

V. Conclusion

This article has presented a dc–dc converter topology for medium- and high-power applications involving level 2 and level 3 EV chargers. It supports a wide output voltage range (200 V to 920) without significant efficiency loss or the need for relays to change configurations. The reduction in voltage stresses on the rectifier diodes allows for the use of 1.2 kV Sic diodes, which decreases production costs and improves performance compared to using series diodes or higher peak inverse voltages (PIVs). The experimental efficiency of 98.13% and the resulting loss breakdown confirm the feasibility of this topology for high-power applications. Further efficiency improvements could be achieved by using high-quality magnetic cores.

References

[1] A. Elezab, O. Zayed, A. Abuelnaga, and M. Narimani, "High efficiency LLC resonant converter with wide output range of 200–1000 V for DC-connected EVs ultra-fast charging stations," *IEEE Access*, vol. 11, pp. 33037–33048, 2023, doi: 10.1109/ACCESS.2023.3263486.

[2] S. Mukherjee, J. M. Ruiz, and P. Barbosa, "A high power density wide range DC-DC converter for universal electric vehicle charging," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1998–2012, Feb. 2023, doi: 10.1109/TPEL.2022.3217092.

[3] M. Jahnes, L. Zhou, M. Eull, W. Wang, and M. Preindl, "Design of a 22-kW transformerless EV charger with V2G capabilities and peak 99.5% efficiency," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, pp. 5862–5871, Jun. 2023, doi: 10.1109/TIE.2022.3192697.

[4] H.-W. Jeong and C.-Y. Lim, "Hybrid DC-DC converter with novel clamp circuit in wide range of high output voltage," *IEEE Access*, vol. 12, pp. 7775–7785, 2024, doi: 10.1109/ACCESS.2024.3352443.

[5] N. Peng, Y. Yuan, Y. Huang, T. Tao, and W. Liu, "A boost-LC resonance multimode DC–DC converter for EV charger application," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 1, pp. 901–910, Mar. 2024, doi: 10.1109/TTE.2023.3291432.

[6] J. Yuan, L. Dorn-Gomba, A. D. Callegaro, J. Reimers, and A. Emadi, "A review of bidirectional on-board chargers for electric vehicles," *IEEE Access*, vol. 9, pp. 51501–51518, 2021, doi: 10.1109/ACCESS.2021.3069448.

[7] Y. Du, S. Lukic, B. Jacobson, and A. Huang, "Review of high power isolated bi-directional DC-DC converters for PHEV/EV DC charging infrastructure," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 553–560, doi: 10.1109/ECCE.2011.6063818.

[8] S. S. G. Acharige, M. E. Haque, M. T. Arif, N. Hosseinzadeh, K. N. Hasan, and A. M. T. Oo, "Review of electric vehicle charging technologies, standards, architectures, and converter configurations," *IEEE Access*, vol. 11, pp. 41218–41255, 2023, doi: 10.1109/ACCESS.2023.3267164.

[9] H. Wang and Z. Li, "A PWM LLC type resonant converter adapted to wide output range in PEV charging applications," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3791–3801, May 2018, doi: 10.1109/TPEL.2017.2713815.

[10] X. Li, H. Ma, S. Ren, J. Yi, S. Lu, and Q. Feng, "A novel LCL resonant converter with inherent CC-CV output for on-board chargers of plug-in electric vehicles," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 4212–4217, Apr. 2023, doi: 10.1109/TPEL.2022.3229025.

[11] J. Deng, S. Li, S. Hu, C. C. Mi, and R. Ma, "Design methodology of LLC resonant converters for electric vehicle battery chargers," *IEEE Trans. Veh. Technol.*, vol. 63, no. 4, pp. 1581–1592, May 2014, doi: 10.1109/TVT.2013.2287379.

[12] Y. Xuan, X. Yang, W. Chen, T. Liu, and X. Hao, "A novel three-level CLLC resonant DC–DC converter for bidirectional EV charger in DC microgrids," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2334–2344, Mar. 2021, doi: 10.1109/TIE.2020.2972446.

[13] B. O. Aarninkhof, D. Lyu, T. B. Soeiro, and P. Bauer, "A reconfigurable two-stage 11 kW DC–DC resonant converter for EV charging with a 150–1000 V output voltage range," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 1, pp. 509–522, Mar. 2024, doi: 10.1109/TPEL.2017.2713815.

[14] D. Elizondo-Martinez, E. L. Barrios, M. Galdeano, A. Ursúa, and P. Sanchis, "Novel two-stage three-level converter with inherently-balanced DC voltage for EV fast-charging applications," *IEEE Trans. Transp. Electrific.*, vol. 10, no. 3, pp. 6418–6433, Sep. 2024, doi: 10.1109/TTE.2023.3339583.

[15] B. Gu, J.-S. Lai, N. Kees, and C. Zheng, "Hybrid-switching full-bridge DC–DC converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1132–1144, Mar. 2013, doi: 10.1109/TPEL.2012.2210565.

[16] D. de Souza Oliveira and I. Barbi, "A three-phase ZVS PWM DC/DC converter with asymmetrical duty cycle for high power applications," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 370–377, Mar. 2005, doi: 10.1109/TPEL.2004.842988.
[17] D. S. Oliveira and I. Barbi, "A three-phase ZVS PWM DC/DC converter with asymmetrical duty cycle associated with a three-phase version of the hybridge rectifier," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 354–360, Mar. 2005, doi: 10.1109/TPEL.2004.842996.
[18] D. S. Oliveira Jr, R. P. T. Bascopé, I. Barbi, and C. E. A. Silva, "On the study of the dynamics of the Zvs three-phase dc/dc converter," *Eletrônica de Potência*, vol. 11, no. 1, pp. 69–76, Mar. 2006, doi: 10.18618/REP.2006.1.069076.
[19] W.-S. Lee, J.-H. Kim, J.-Y. Lee, and I.-O. Lee, "Design of an isolated DC/DC topology with high efficiency of over 97% for EV fast chargers," *IEEE Trans. Veh. Technol.*, vol. 68, no. 12, pp. 11725–11737, Dec. 2019, doi: 10.1109/TVT.2019.2949080.
[20] S. Mukherjee, J. M. Ruiz, and P. Barbosa, "A high power density wide range DC–DC converter for universal electric vehicle charging," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1998–2012, Feb. 2023, doi: 10.1109/TPEL.2022.3217092.
[21] D. Lyu, T. B. Soeiro, and P. Bauer, "Design and implementation of a reconfigurable phase shift full-bridge converter for wide voltage range EV charging application," *IEEE Trans. Transp. Electrific.*, vol. 9, no. 1, pp. 1200–1214, Mar. 2023, doi: 10.1109/TTE.2022.3176826.
[22] S. B. Althurthi, K. Rajashekara, and T. Debnath, "A novel ultrawide output range DC–DC converter for EV fast charging," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 5, no. 2, pp. 586–596, Apr. 2024, doi: 10.1109/JESTIE.2024.3376291.

Raimundo Nonato Moura de Oliveira was born in Limoeiro do Norte, Ceará, Brazil, in 1978. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Ceará, Sobral, Brazil, in 2015 and from the UFC, Fortaleza, Brasil, in 2018, respectively.

He is currently a Professor with the Federal Institute of Ceará, Limoeiro do Norte, Brazil. His research interests include static power converters, renewable energy applications, softcommutation, and solid-state transformers.

José Willamy Medeiros de Araújo was born in Fortaleza-CE, Brazil, in 1988. He received the Ph.D. degree in electrical engineering from the Federal University of Ceará, Fortaleza, Brazil, in 2022.

He is a Researcher with the Group of Power Processing and Control, Federal University of Ceará, where he is currently working on vehicle chargers. His research interests include static power converters, soft commutation and renewable energy applications.

Luiz Henrique Silva Colado Barreto (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 2003.

He is currently a Full Professor with the Federal University of Ceará, which is the Head of the Department of Electrical Engineering. He is working in electrical engineering with emphasis in power electronic and has been an Academic Advisor of masters and Ph.D. students in the Graduate Program in Electrical Engineering from UFC since 2003. He was the Coordinator of the Graduate Program in electrical engineering with the UFC, from 2009 to 2011. He was a Reviewer for the journals IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, and IEEE TRANSACTIONS ON INDUSTRY APPLICATION and the *Journal of SOBRAEP*. Was the Chair of 10th IAS/IEEE/INDUSCON held in 2012. In 2015, he was the Vice-Chair of the 1st IEEE/PELS SPEC/COBEP held in Fortaleza, Brazil. He was Brazilian Society of Power Electronics treasurer for two terms (from 2010 to 2011 and from 2021 to 2023). He is the IEEE/PELS Region 9 Membership Chair and a Member of the Brazilian Society of Power Electronics (SOBRAEP) and Power Electronics (IEEE / PELS). His field of research interest includes ZVS and ZCS techniques, structures of dc–dc converter control, power factor and harmonics, UPS systems and multilevel converters.

Dalton de Araujo Honorio (Senior Member, IEEE) received the B.Sc., M.Sc. and Ph.D. degrees in electrical engineer from the Federal University of Ceará, Fortaleza, Brazil, in 2011, 2013 and 2018, respectively.

He did a sandwich Ph.D. period with Oak Ridge National Laboratory in 2015. He is currently an Adjunct Professor with the Federal University of Ceará, where he participates in research focused on power conditioners, being the Head of the Power Conditioners Laboratory and a Member of the Power Processing and Control Group. He has been a Member of the Brazilian Power Electronics Society (SOBRAEP) since 2011, and he served as its first Secretary during the biennium 2022–2023. He has been a Member of the IEEE Power Electronics Society since 2016, located in the Northeast Brazil Section, R-9. His research focuses on power electronics applications, specifically on high conversion ratio dc–dc converters, as well as cascaded multilevel converters and modular multilevel converters applied in solid-state transformers.

Demercil de Souza Oliveira (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Uberlândia, Uberlândia, Brazil, in 1999 and 2001, respectively, and the Ph.D. degree in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 2004.

Since 2005, he has been a Professor with the Federal University of Ceará, Fortaleza, Brazil. His research interests include power converter topologies, soft switching techniques, three-phase dc–dc power conversion, solid-state transformers, and renewable energy applications.