Asymmetrical Quasi-Two-Level Modulation of a Compact Modular Multilevel DC–DC Converter (MMDC) With Reduced SM Number

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***Abstract*—As a pivotal role in interconnecting the medium-voltage dc (MVDC) and low-voltage dc (LVDC) grids, the modular multilevel dc–dc converter (MMDC) with compact size over a wide voltage range is a trending concern. This article thus proposes an asymmetrical quasi-two-level (AQ2L) modulation for a compact MMDC, which enables asymmetrical duty cycle control of the submodules (SMs). The equivalent circuit of the compact MMDC is built first, and its Boost-alike dc loop characteristic is revealed, which contributes to the reduction of SM number and converter size. Then, the power transfer characteristic under the AQ2L modulation is derived, and the favorable flatness of the transferred power over a wide voltage range is found. Besides, the proposed AQ2L modulation also achieves zero-voltage switching to ensure low switching losses. Comparison between the proposed AQ2L and conventional Q2L modulations is also demonstrated, and finally, the simulation results at 10 kV/1MW and the experimental results at 2.6 kV/50 kW verify the effectiveness and advantages of the proposed modulation.**

***Index Terms*—DC–DC conversion, modular multilevel converter (MMC), quasi-two-level (Q2L) modulation, wide voltage range.**

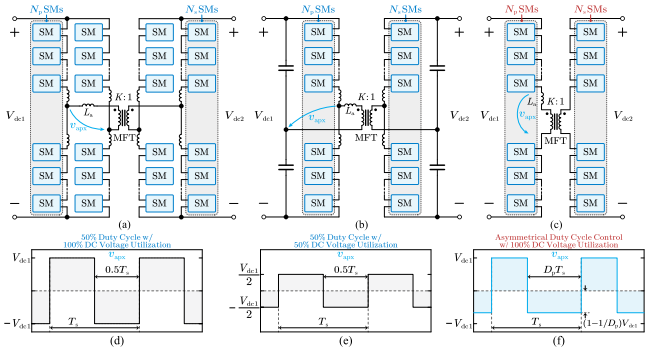

Fig. 1. (a) FTF H-bridge MMDC topology. (b) FTF HB MMDC topology. (c) Compact MMDC topology. (d) Conventional Q2L modulation with 50% duty cycle for the FTF H-bridge MMDC and compact MMDC topologies. (e) Conventional Q2L modulation with 50% duty cycle for the FTF HB MMDC topology. (f) Proposed AQ2L modulation that enables asymmetrical duty cycle control for the compact MMDC topology.

I. Introduction

FEATURING higher efficiency, smaller conductor size, better load compatibility, and lower system complexity, medium-voltage dc (MVDC) systems have gained traction over medium-voltage ac alternatives in emerging scenarios such as shipboard microgrid, all-electric aircraft, electric vehicle charging, and renewable energy collection [1], [2], [3], [4]. In the abovementioned applications, terminal loads and sources (e.g., batteries and photovoltaic plants, etc.) are typically connected to the low-voltage dc (LVDC) bus. Therefore, dc–dc converters are indispensable for the interconnection and voltage level matching between MVDC and LVDC buses.

Interfacing with MVDC and LVDC buses, the dc–dc converter demands bidirectional power flow, high voltage tolerance, well galvanic isolation, high power density and a load-independent fixed voltage ratio, which is also known as the dc transformer or dc solid-state transformer (DC SST) [5]. In contrast to the input-series output-parallel solution with high insulation costs [5], [6], [7], [8], the modular multilevel dc–dc converter (MMDC) is another promising solution [9], [10], [11], [12], [13], [14]. The traditional MMDC topology is formed by connecting two H-bridge configuration modular multilevel converters (MMCs) in a front-to-front (FTF) manner with an isolation transformer [9], [10], as shown in Fig. 1(a). It utilizes the medium-frequency (several hundred Hz to tens of kHz) ac power transmission chain and only a single medium-frequency transformer (MFT) is required, which significantly improves the power density, and also simplifies the system design. However, it still adheres to the sinusoidal modulation in conventional MMCs [9], [10], [11], [12], which not only shrinks the power capacity, but also leads to the soft-switching failure of partial switching devices [13]. To alleviate this concern, a quasi-square-wave (QSW) modulation has been proposed for the FTF H-bridge MMDC, where only partial SMs are engaged in the inserting or bypassing statuses [15], [16], [17]. The switching actions of SMs in an arm are performed within a very short interval so that the MFT is excited by a QSW. In this way, similar to the single phase-shifting control of the dual active bridges (DABs), all SMs involved can achieve zero-voltage switching (ZVS) [17]. In [18], the rise and fall time

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of the QSW are also employed as a degree of freedom (DoF) for the circulating current stress reduction, whereas it is revealed that the increase in the rise and fall time diminish the ZVS region of the SMs [19]. Replacing the ac inductor with the resonant tanks, the MMDC resonant topologies are also proposed drawing on the operating principle of *LLC* and *CLLC* converters [20], [21], [22], [23], [24], [25], [26], which features lower turn-OFF loss. However, its variable frequency control characteristics are not favorable for the MFT design in high-power situations. Besides, the size of the resonant capacitor, which withstands MV and large current stress in high-power conversion applications, remains a challenging issue.

Further enhancing performance, a quasi-two-level (Q2L) modulation has been proposed [27], [28], [29], directly inserting or bypassing all the SMs in an arm to generate a full amplitude QSW as shown in Fig. 1(d), thus maximizing the power transfer capability of the converter. In the light of the analysis in [29], the FTF H-bridge MMDC under Q2L modulation is approximately equivalent to a Q2L DAB, and the SM is essentially simplified to an active clamp circuit, while the SM capacitor acts as the energy buffer, thus, the sizes of the SM capacitor and the bulky arm inductor are dramatically reduced, which facilitates the overall power density enhancement. Nevertheless, the duty cycle of the SMs has to be fixed at 50% in the Q2L modulation to ensure no dc magnetic flux in the MFT. A quasi-three-level (Q3L) modulation is proposed in [30] and [31], and it introduces a short-through in the dc loop by symmetrically adjusting the duty cycle of SMs, thus enabling dc-loop current control. Similarly, a chopping phase shift square modulation adopting the Q3L voltage wave is presented in [32], which achieves output power enhancement and ac current optimization. Nevertheless, the duty cycle control DoF in [31] and [32] is obtained at the expense of introducing bulky dc choke inductors in arms, which inevitably compromises the power density.

For the power density of the MMDC, the dc-bus capacitors, the volume and number of the magnetic components, and the SM number are all important factors. The dc-bus capacitors serve as terminal filtering, cable parasitic inductance decoupling and transient energy support (e.g., for sudden load changes, temporary faults, etc.), and the capacitance required for the latter is usually much larger than the former two, which is related only to the converter power capacity and bus voltages [33]. The volume of the MFT is also dominated by its power capacity and operating frequency according to the product areas method [34]. While the reduction of the SM number can notably reduce the modularization space penalty (i.e., the insulation and mounting space between SMs), and the volume occupation of auxiliary components (e.g., communication cables, heat sinks, structural members, etc.) [35], [36]. Therefore, reducing the SM number is a more effective way to boost the power density.

Accordingly, the FTF half-bridge (HB) MMDC topology [37], [38] as shown in Fig. 1(b) and single-arm MMDC topology [39], [40], [41] are presented for the SM reduction purpose, whose SM number ($N_\mathrm{p}+N_\mathrm{s}$ SMs required) is halved compared with that of the FTF H-bridge MMDC ($2N_\mathrm{p}+2N_\mathrm{s}$ SMs required) at the same bus voltage. However, as shown in Fig. 1(e), they attain only 50% dc voltage utilization of the FTF H-bridge MMDC, and thus, their current stress has to be doubled to achieve the same power transfer capacity. As depicted in Fig. 1(c), integrating the dc common-mode loop and the ac difference-mode loop into a unified loop, the compact MMDC topology with the series structure of the arms and MFT is established in [42], [43], [44], and [45], which also uses only half of the SM number ($N_\mathrm{p}+N_\mathrm{s}$) and shares the same 100% dc voltage utilization as the FTF H-bridge MMDC. Meanwhile, the magnetizing inductance of the MFT can naturally act as the dc choke inductor, and the dc magnetic fluxes generated by the dc current in the primary and secondary windings can be canceled with each other, thus avoiding the core saturation issue [45]. However, larger winding current stresses are incurred, therefore, a larger core window is required, leading to a modest increase in MFT volume. Nevertheless, the total size is still reduced due to the halving of the SM number and the reduction of arm inductors.

Yet, the 50% duty-cycle Q2L modulation is still utilized in such a compact MMDC, as depicted in Fig. 1(c), which hinders the performance improvement of the compact MMDC in wide voltage range applications [46], [47]. To fill this gap, this article proposes an asymmetrical Q2L (AQ2L) modulation for such a compact MMDC, which enables the asymmetrical duty cycle control of SMs, as indicated in Fig. 1(f). Compared with the conventional Q2L modulation, the main advantages of the proposed AQ2L modulation are as follows.

1) The SM number can be further reduced. When the MV bus voltage is high, the voltage stress on the SMs can be restricted by enlarging their duty cycle, thus, the additional SMs for withstanding the high voltage can be discarded.
2) The favorable flatness of the transferred power is obtained. As the MV bus voltage drops to low voltage, it can effectively boost the power transfer capability of the converter by lowering the SM duty cycle.
3) The AQ2L modulation retains the bipolar trapezoidal waveform of the arm current, which establishes the ZVS conditions for SMs. Thus, all the SMs can achieve the ZVS turning-ON, enabling low switching losses.

The abovementioned enhancements promote the compact MMDC to achieve a smaller size. The rest of this article is organized as follows. The equivalent circuit of the compact MMDC is revealed, and then the operating principle of the proposed AQ2L modulation is elaborated in Section II. In Section III, the steady-state characteristics of the compact MMDC under the proposed AQ2L modulation are carried out. A design case and the performance comparison between the proposed AQ2L and the conventional Q2L modulations are also presented. Section IV provides the simulation and experimental results. Finally, Section V concludes this article.

II. Proposed AQ2L Modulation for the Compact MMDC

A. Equivalent Circuit of the Compact MMDC

To facilitate illustration, the topology of the compact MMDC exhibited in Fig. 1(c) is simplified by merging two identical series SM chains and reshown in Fig. 2(a), which interconnects the MVDC and LVDC buses with voltages V_dc1 and V_dc2, respectively. L_cp and L_cs are the cable parasitic inductances

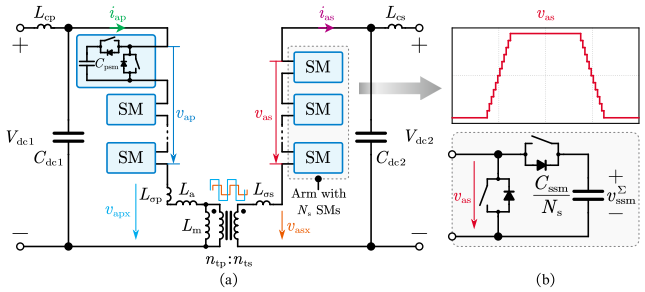

Fig. 2. (a) Compact MMDC topology. (b) Q2L waveform of the secondary-side arm voltage, and the SM chain equivalent circuit.

on the MVDC and LVDC sides, respectively. They can be decoupled from the two arms by the dc-bus capacitors $C_{\rm dc1}$ and $C_{\rm dc2}$, so their effect on the ac and dc loops of the converter is ignored in the subsequent analysis. $L_{\sigma\rm p}$ and $L_{\sigma\rm s}$ are the line stray inductances of the primary and secondary arms, respectively. The arm inductor $L_{\rm a}$ is the aggregate of the additional arm inductance and the leakage inductance of the MFT referred to the primary side. Apart from the decoupling capability, the dc-bus capacitors $C_{\rm dc1}$ and $C_{\rm dc2}$ also serve as terminal filtering and transient energy support for the MVDC and LVDC buses, respectively. The primary-side arm is formed by an SM chain with $N_{\rm p}$ HB SMs connected in series, while the secondary-side arm contains $N_{\rm s}$ HB SMs in series. The turn ratio of the MFT is $K = n_{\rm tp} : n_{\rm ts}$, where $n_{\rm tp}$ and $n_{\rm ts}$ are the turn numbers of the primary and secondary windings, respectively, and $K = V_{\rm dc1}/V_{\rm dc2}$ is mandatory to cancel out the dc magnetic flux in the core. $L_{\rm m}$ is the magnetizing inductance of the MFT, which is referred to the primary side.

The top of Fig. 2(b) demonstrates the secondary-side arm voltage waveform of the compact MMDC under the Q2L modulation. It is seen that the secondary-side arm voltage $v_{\rm as}$ is a multilevel wave, which is composed of $(N_{\rm s}-1)$ dwell steps during level transitions. The transition time is small with respect to the switching period $T_{\rm s}$, so the arm voltages $v_{\rm ap}$ and $v_{\rm as}$ are QSWs. Thereby, the SM chain equivalent circuit of the compact MMDC can be approximately obtained in the form of HB circuit, as shown at the bottom of Fig. 2(b), whose capacitor voltage is the sum of all SM capacitor voltages in an arm

$$\begin{cases} v_{\rm psm}^{\Sigma} = \sum_{i=1}^{N_{\rm p}} v_{{\rm psm}i} \\ v_{\rm ssm}^{\Sigma} = \sum_{j=1}^{N_{\rm s}} v_{{\rm ssm}j} \end{cases} \tag{1}$$

where $v_{\rm psm}^{\Sigma}$ and $v_{\rm ssm}^{\Sigma}$ are the capacitor voltages of the primary and secondary SM chain equivalent circuits, respectively; $v_{{\rm psm}i}$ and $v_{{\rm ssm}j}$ denote the capacitor voltages of the ith and jth SMs ($i = 1, 2, \ldots, N_{\rm p}$ and $j = 1, 2, \ldots, N_{\rm s}$) in the primary-side and secondary-side arms, respectively.

Substituting the arms in the compact MMDC with the SM chain equivalent circuit illustrated in Fig. 2(b) and removing the ideal transformer since it is an ac component, the primary and secondary dc equivalent circuits of the compact MMDC

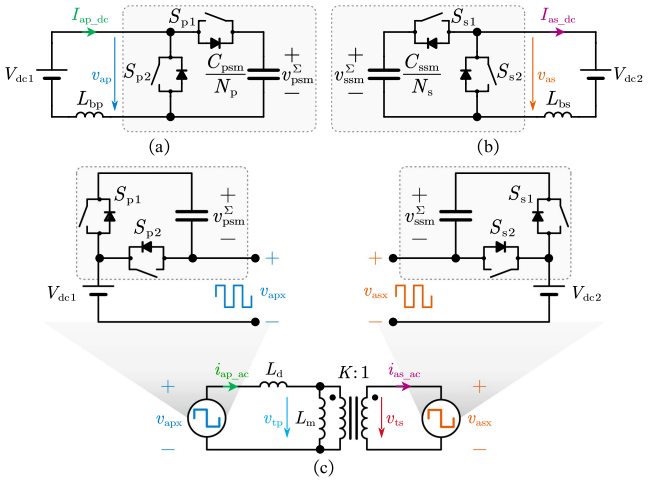

Fig. 3. Equivalent circuits of the compact MMDC. (a) Boost-alike dc equivalent circuit of the primary side. (b) Boost-alike dc equivalent circuit of the secondary side. (c) DAB-alike ac equivalent circuit.

can be derived as shown in Fig. 3(a) and (b), respectively, where $L_{\rm bp} = L_{\rm a} + L_{\rm m} + L_{\sigma\rm p}$ and $L_{\rm bs} = L_{\rm m}/K^2 + L_{\sigma\rm s}$ are the dc equivalent inductances, respectively. Evidently, the dc equivalent circuit of the compact MMDC is a Boost-alike circuit, where the bus voltages $V_{\rm dc1}$ and $V_{\rm dc2}$ are pumped up into the SM capacitors by the control of the lumped equivalent switches. Assuming that the duty cycles of the lumped equivalent switches $S_{\rm p1}$ and $S_{\rm s1}$ (note that $S_{\rm p1}$ and $S_{\rm p2}$, $S_{\rm s1}$ and $S_{\rm s2}$ operate in a complementary way, respectively) in the primary-side and secondary-side SM chain equivalent circuits are $D_{\rm p}$ and $D_{\rm s}$ ($0 < D_{\rm p} < 1$, $0 < D_{\rm s} < 1$), respectively, then the voltages in the equivalent capacitors are governed by

$$\begin{cases} v_{\rm psm}^{\Sigma} = \frac{V_{\rm dc1}}{D_{\rm p}} \\ v_{\rm ssm}^{\Sigma} = \frac{V_{\rm dc2}}{D_{\rm s}}. \end{cases} \tag{2}$$

Assuming that the SM capacitor voltages in the same arm are equal as a result of the voltage balancing strategy, the steady-state average SM capacitor voltages can be obtained by combining (1) and (2), as

$$\begin{cases} V_{\rm psm} = \frac{v_{\rm psm}^{\Sigma}}{N_{\rm p}} = \frac{V_{\rm dc1}}{D_{\rm p}N_{\rm p}} \\ V_{\rm ssm} = \frac{v_{\rm ssm}^{\Sigma}}{N_{\rm s}} = \frac{V_{\rm dc2}}{D_{\rm s}N_{\rm s}} \end{cases} \tag{3}$$

where $V_{\rm psm}$ and $V_{\rm ssm}$ denote the steady-state average SM capacitor voltages in the primary-side and secondary-side arms, respectively.

According to Kirchhoff's voltage law, the dynamics of the compact MMDC are given by

$$V_{\rm dc1} = v_{\rm ap} + v_{\rm apx} \tag{4}$$

$$V_{\rm dc2} = v_{\rm as} + v_{\rm asx} \tag{5}$$

$$v_{\rm apx} = K v_{\rm asx} + L_{\rm d}\frac{{\rm d}i_{\rm ap}}{{\rm d}t} \tag{6}$$

where $v_{\rm ap}$ and $v_{\rm as}$ are the arm voltages in the primary and secondary sides, respectively; $v_{\rm apx}$ and $v_{\rm asx}$ denote port voltages in the primary and secondary sides of the MFT and inductor

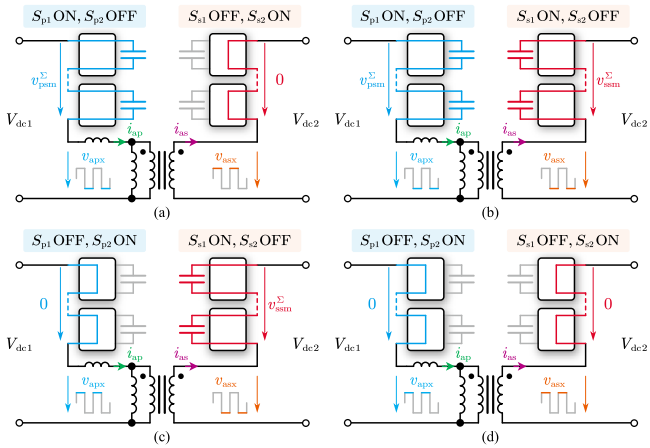

Fig. 4. Simplified model analysis of the compact MMDC under the proposed AQ2L modulation. (a) Mode A. (b) Mode B. (c) Mode C. (d) Mode D.

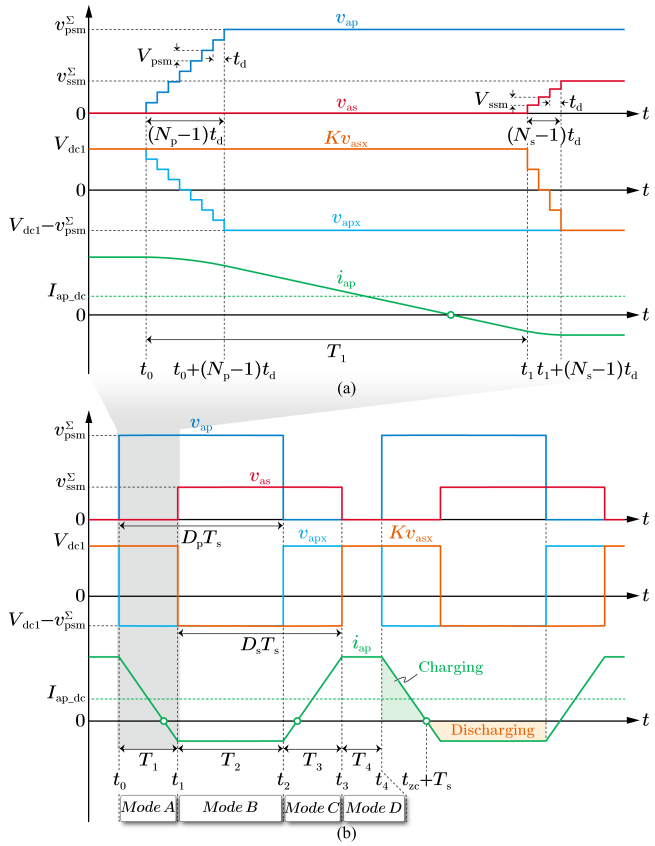

Fig. 5. Typical waveforms of the compact MMDC under the AQ2L modulation. (a) Magnified waveforms in detail. (b) Steady-state key waveforms.

as a whole, respectively. Following (4)–(6), the ac equivalent circuit of the compact MMDC can be theoretically constructed. Alternatively, it can also be derived by substituting the SM chain equivalent circuit, as shown in Fig. 3(c), where is a DAB-alike circuit and the ac equivalent inductance $L_d = L_a + L_{\sigma p} + K^2 L_{\sigma s}$. Taking the primary side as an example, when the equivalent switch S_{p1} is OFF and the equivalent switch S_{p2} is ON, the primary side excitation voltage $v_{apx} = v_{dc1}$; on the contrary, when the equivalent switch S_{p1} is ON and the equivalent switch S_{p2} is OFF, $v_{apx} = v_{dc1} - v^{\Sigma}_{psm}$. According to (2), $v^{\Sigma}_{psm} > v_{dc1}$ is always held and hence, the bipolar excitation voltage v_{apx} is generated for the primary side. The same conclusion can be drawn for the secondary excitation voltage v_{asx}.

To this point, it is clear that the compact MMDC shares a similar ac equivalent circuit and mechanism of transferring power with the DAB, while the amplitude and duty cycle of its excitation voltages can be flexibly adjusted by controlling the inserting and bypassing of the SMs, i.e., their duty cycles.

B. Operating Principle

Owing to the presence of the Boost-alike dc equivalent circuit, the compact MMDC can achieve performance enhancement by adjusting the duty cycle of SMs.

Figs. 4 and 5 demonstrate the simplified mode analysis and typical waveforms of the compact MMDC under the proposed AQ2L modulation, respectively. As illustrated by the magnified waveforms in Fig. 5(a), when the SMs in the arm are required to be inserted, all SMs in the arm will be centrally inserted within a short interval, e.g., t_0–$t_0 + (N_p - 1)t_d$ and t_1–$t_1 + (N_s - 1)t_d$. Besides, the insertion actions between SMs are staggered by a dwell time of t_d, respectively, in order to limit the excessively high dv/dt and introduce a control DoF to balance the SM capacitor voltages. When the SM is required to be bypassed, a similar operation will be performed as well. Since the dwell time t_d is tiny and the interval of level transitions is typically less than 3% of the switching period T_s, the short intervals $(N_p - 1)t_d$ and $(N_s - 1)t_d$ between QSW level transitions are neglected during the following analysis of mode and typical waveforms.

Mode A $(t_0 - t_1)$: As shown in Fig. 4(a), the primary-side SM chain is inserted into the arm and the secondary-side SM chain is bypassed from the arm, which indicates the primary-side equivalent switch S_{p1} is ON and the secondary-side equivalent switches S_{s1} is OFF in Fig. 3(c). In this way, the arm voltages of the primary and secondary sides in this mode are

$$\begin{cases} v_{ap}(t) = v^{\Sigma}_{psm}, & t \in [t_0, t_1) \\ v_{as}(t) = 0, & t \in [t_0, t_1) \end{cases}. \tag{7}$$

Then, based on (4) and (5), v_{apx} and v_{asx} in this mode are

$$\begin{cases} v_{apx}(t) = V_{dc1} - v^{\Sigma}_{psm}, & t \in [t_0, t_1) \\ v_{asx}(t) = V_{dc2}, & t \in [t_0, t_1) \end{cases}. \tag{8}$$

Substituting (2) into (8) yields

$$\begin{cases} v_{apx}(t) = \left(1 - \frac{1}{D_p}\right) V_{dc1}, & t \in [t_0, t_1) \\ v_{asx}(t) = V_{dc2}, & t \in [t_0, t_1) \end{cases}. \tag{9}$$

Combining (6) and (9), the dynamics of the primary-side arm current i_{ap} in this mode can be obtained

$$i_{ap}(t) = i_{ap}(t_0) - \frac{V_{dc1}}{L_d D_p}(t - t_0) \quad t \in [t_0, t_1). \tag{10}$$

As illustrated in Fig. 5(b), the duration of *Mode A* is T_1, and in this mode, $i_{\rm ap}(t)$ decreases linearly, turning from positive at t_0 to negative at t_1. $i_{\rm ap}(t_0) > 0$ provides the ZVS turning-ON condition for the upper switches in the primary-side SMs (equivalent to $S_{\rm p1}$), while $i_{\rm ap}(t_1) < 0$ lays the ZVS turning-ON foundation in *Mode B* for the upper switches in the secondary-side SMs (equivalent to $S_{\rm s1}$).

Mode B $(t_1 - t_2)$: As shown in Fig. 4(b), the SM chains of the primary and secondary sides are both inserted into the arms, indicating $S_{\rm p1}$ and $S_{\rm s1}$ are both ON in this mode. Therefore, the converter dynamics in this mode is

$$\begin{cases} v_{\rm ap}(t) = v_{\rm psm}^{\Sigma}, & t \in [t_1, t_2) \\ v_{\rm as}(t) = v_{\rm ssm}^{\Sigma}, & t \in [t_1, t_2) \end{cases} \tag{11}$$

$$\begin{cases} v_{\rm apx}(t) = \left(1 - \frac{1}{D_{\rm p}}\right) V_{\rm dc1}, & t \in [t_1, t_2) \\ v_{\rm asx}(t) = \left(1 - \frac{1}{D_{\rm s}}\right) V_{\rm dc2}, & t \in [t_1, t_2) \end{cases} \tag{12}$$

$$i_{\rm ap}(t) = i_{\rm ap}(t_1) + \left(\frac{1}{D_{\rm s}} - \frac{1}{D_{\rm p}}\right) \frac{V_{\rm dc1}}{L_{\rm d}} (t - t_1) \;\; t \in [t_1, t_2). \tag{13}$$

If $D_{\rm p} = D_{\rm s}$, $i_{\rm ap}(t)$ will remain constant in this mode. Then, the ZVS turning-ON conditizon in *Mode C* for the lower switches in the primary-side SMs (equivalent to $S_{\rm p2}$) can thus be supported by $i_{\rm ap}(t_2) < 0$.

Mode C $(t_2 - t_3)$: As shown in Fig. 4(c), the primary-side SM chain is bypassed from the arm and the secondary-side SM chain is inserted into the arm, i.e., $S_{\rm p1}$ is OFF and $S_{\rm s1}$ is ON in this mode. The converter dynamics in this mode is

$$\begin{cases} v_{\rm ap}(t) = 0, & t \in [t_2, t_3) \\ v_{\rm as}(t) = v_{\rm ssm}^{\Sigma}, & t \in [t_2, t_3) \end{cases} \tag{14}$$

$$\begin{cases} v_{\rm apx}(t) = V_{\rm dc1}, & t \in [t_2, t_3) \\ v_{\rm asx}(t) = \left(1 - \frac{1}{D_{\rm s}}\right) V_{\rm dc2}, & t \in [t_2, t_3) \end{cases} \tag{15}$$

$$i_{\rm ap}(t) = i_{\rm ap}(t_2) + \frac{V_{\rm dc1}}{L_{\rm d} D_{\rm s}} (t - t_2) \;\; t \in [t_2, t_3). \tag{16}$$

$i_{\rm ap}(t)$ increases linearly, turning from negative at t_2 to positive at t_3. Similarly, $i_{\rm ap}(t_3) > 0$ provides the ZVS turning-ON condition in *Mode D* for the lower switches in the secondary-side SMs (equivalent to $S_{\rm s2}$).

Mode D $(t_3 - t_4)$: As shown in Fig. 4(d), the SM chains of the primary and secondary sides are both bypassed from the arms, i.e., $S_{\rm p1}$ and $S_{\rm s1}$ are both OFF in this mode, so the converter dynamics is

$$\begin{cases} v_{\rm ap}(t) = 0, & t \in [t_3, t_4) \\ v_{\rm as}(t) = 0, & t \in [t_3, t_4) \end{cases} \tag{17}$$

$$\begin{cases} v_{\rm apx}(t) = V_{\rm dc1}, & t \in [t_3, t_4) \\ v_{\rm asx}(t) = V_{\rm dc2}, & t \in [t_3, t_4) \end{cases} \tag{18}$$

$$i_{\rm ap}(t) = i_{\rm ap}(t_3) \;\; t \in [t_3, t_4). \tag{19}$$

It can be seen that $i_{\rm ap}(t)$ keeps constant in this mode, and thus $i_{\rm ap}(t_4) > 0$ (i.e., $i_{\rm ap}(t_0)$ in *Mode A* since the next cycle begins) enables the ZVS turning-ON condition of the upper switches in the primary-side SMs.

As can be seen in Fig. 5, the duty cycles of the SMs in the primary and secondary-side arms $D_{\rm p}$ and $D_{\rm s}$ are no longer fixed at 50%, but are determined by

$$\begin{cases} D_{\rm p} T_{\rm s} = T_1 + T_2 \\ D_{\rm s} T_{\rm s} = T_2 + T_3. \end{cases} \tag{20}$$

Since $V_{\rm dc1} = K V_{\rm dc2}$, $D_{\rm p}$ and $D_{\rm s}$ should be kept equal to avoid the voltage mismatch between the primary and secondary-side SM chains, which may result in a large arm current, namely

$$T_1 = T_3. \tag{21}$$

As a result, the bipolar trapezoidal waveforms of the arm currents $i_{\rm ap}$ and $i_{\rm as}$ are retained under the proposed AQ2L modulation, and thus, the ZVS features under the conventional Q2L modulation are also inherited to achieve low switching losses. The following requirements should be fulfilled to achieve the ZVS turning-ON of all SMs [14], [15]

$$\begin{cases} i_{\rm ap}(t_0) > I_{\rm pz} \\ i_{\rm ap}(t_1) < -\frac{I_{\rm sz}}{K} \\ i_{\rm ap}(t_2) < -I_{\rm pz} \\ i_{\rm ap}(t_3) > \frac{I_{\rm sz}}{K} \end{cases} \tag{22}$$

where $I_{\rm pz}$ and $I_{\rm sz}$ are the threshold currents of the SMs in the primary and secondary sides to achieve ZVS turning-ON

$$\begin{cases} I_{\rm pz} = \frac{2 V_{\rm psm} C_{\rm po}}{T_{\rm dz}} \\ I_{\rm sz} = \frac{2 V_{\rm ssm} C_{\rm so}}{T_{\rm dz}} \end{cases}. \tag{23}$$

$C_{\rm po}$ and $C_{\rm so}$ in (23) are the output capacitances of the switches in the primary-side and secondary-side SMs, respectively, and $T_{\rm dz}$ is the dead time of the HB SM.

C. MFT Magnetic Flux Analysis

In the compact MMDC, the Boost-alike dc equivalent circuit and DAB-alike ac equivalent circuit share the same physical circuit. It results in both the primary and secondary windings of the MFT being forced to flow the arm currents that contain dc components, which can be expressed in the form of the dc and ac components

$$\begin{cases} i_{\rm ap} = I_{\rm ap\_dc} + i_{\rm ap\_ac} \\ i_{\rm as} = I_{\rm as\_dc} + i_{\rm as\_ac} \end{cases} \tag{24}$$

where $I_{\rm ap\_dc}$ and $I_{\rm as\_dc}$ denote the dc components of $i_{\rm ap}$ and $i_{\rm as}$, respectively. $i_{\rm ap\_ac}$ and $i_{\rm as\_ac}$ denote the ac components of $i_{\rm ap}$ and $i_{\rm as}$, respectively.

By Ampere's law, the total magnetic flux Φ of the MFT can also obtained in the form of the dc and ac components

$$\begin{aligned} \Phi &= \Phi_{\rm dc} + \Phi_{\rm ac} \\ \Phi_{\rm dc} &= \frac{1}{R_{\rm m}} \left(n_{\rm tp} I_{\rm ap\_dc} - n_{\rm ts} I_{\rm as\_dc}\right) \\ \Phi_{\rm ac} &= \frac{1}{R_{\rm m}} \left(n_{\rm tp} i_{\rm ap\_ac} - n_{\rm ts} i_{\rm as\_ac}\right) \end{aligned} \tag{25}$$

where R_{m} denotes the magnetic core reluctance of the MFT. It is worth mentioning that since the reference directions of i_{ap} and i_{as} are opposite, the subtraction rather than the addition of the primary and secondary magnetomotive forces in (25) are performed. Furthermore, due to the conservation of power

$$\frac{V_{\mathrm{dc1}}}{V_{\mathrm{dc2}}} = \frac{I_{\mathrm{as\_dc}}}{I_{\mathrm{ap\_dc}}} = K. \tag{26}$$

Hence, substituting (26) into (25) gives $\Phi_{\mathrm{dc}} = 0$. It indicates that even though the arm currents containing dc components pass through the windings of the MFT, the dc magnetic fluxes generated by them can still be canceled out by each other in the magnetic core.

As for the ac component Φ_{ac}, it is characterized by the volt-second product λ_{p} and λ_{s} applied to the primary and secondary windings. λ_{p} and λ_{s} in a switching cycle can be calculated as

$$\lambda_{\mathrm{p}} = \int_{t_0}^{t_0+T_{\mathrm{s}}} v_{\mathrm{apx}}(t)\mathrm{d}t = 0 \tag{27}$$

$$\lambda_{\mathrm{s}} = \int_{t_0}^{t_0+T_{\mathrm{s}}} v_{\mathrm{asx}}(t)\mathrm{d}t = 0. \tag{28}$$

Consequently, the average value of Φ_{ac} in a switching cycle is zero as well, which implies that even though the applied excitation voltages on both sides of the MFT are no longer symmetrical, their volt-second product is still zero, thus avoiding the magnetic core saturation issue.

It can be concluded that under the proposed AQ2L modulation, the MFT in the compact MMDC can also operate as normally as in the conventional FTF H-bridge MMDC. However, due to the dc component of the arm currents flowing through its windings, larger winding current root-mean-square (RMS) values are incurred. Therefore, a larger core window is required, leading to a modest increase in MFT volume.

III. Steady-State Characteristics Analysis and Performance Comparison

A. Steady-State Characteristics Analysis

To facilitate the subsequent performance comparison with the conventional Q2L modulation, the steady-state characteristics under the proposed AQ2L modulation are investigated as follows.

1) Transferred Power: The power transfer characteristics of the compact MMDC under the AQ2L modulation can be found by integrating the MFT excitation voltage and current

$$\begin{aligned} P &= \frac{1}{T_{\mathrm{s}}}\int_{t_0}^{t_4} v_{\mathrm{apx}}(t) i_{\mathrm{ap}}(t)\mathrm{d}t \\ &= \frac{K V_{\mathrm{dc1}} V_{\mathrm{dc2}}}{2L_{\mathrm{d}}(T_1+T_2)^2} T_1\left[2T_2T_4 + T_1(T_2+T_4)\right]. \end{aligned} \tag{29}$$

Following (21), it gives $T_{\mathrm{s}} = 2T_1 + T_2 + T_4$. Hence, it can be observed that for any given transferred power, an infinite number of solutions to $\{T_1, T_2, T_4\}$ are available, since they are constrained by only two equations. At the same time, it also provides a DoF to enable performance enhancement of the compact MMDC.

2) SM Voltage Stress: The SM voltages under the AQ2L modulation are determined by (3), which can be regulated by D_{p} and D_{s}. When the bus voltage V_{dc1} (or V_{dc2}) is high, the SM voltage stress can be lowered by enlarging D_{p} (or D_{s}), thus minimizing the demand for the SM number; when the bus voltage V_{dc1} (or V_{dc2}) is low, it enables to effectively enhance the power transfer capability by decreasing D_{p} (or D_{s}) to increase the SM capacitor voltages. As a result, these efforts contribute to the further improvement of the converter power density and thus enable a smaller converter size.

Due to the duality of the primary-side and secondary-side SMs, only the primary-side SMs are considered as an illustration to analyze the regulation of the SM voltage in the following. Suppose the maximum voltage stress allowed by the primary-side SM is V_{psmmax}, the constraint on $\{T_1, T_2, T_4\}$ can be determined by

$$V_{\mathrm{psm}} \le V_{\mathrm{psm\,max}}. \tag{30}$$

Substituting (3) and (20) into (30) yields

$$T_1 + T_2 \ge \frac{V_{\mathrm{dc1}} T_{\mathrm{s}}}{N_{\mathrm{p}} V_{\mathrm{psm\,max}}}. \tag{31}$$

Assuming that the desired transferred power is P_{t}, T_2 can be derived from (29) as

$$T_2 = -T_1 + \frac{1}{2}\lambda + \frac{1}{2}\sqrt{\lambda(\lambda - 2T_1)} \tag{32}$$

$$\lambda = \frac{T_1 T_{\mathrm{s}} V_{\mathrm{dc1}}^2}{L_{\mathrm{d}} P_{\mathrm{t}} + T_1 V_{\mathrm{dc1}}^2}. \tag{33}$$

Then, the boundary constraints for T_1 can be attained by combining (31) and (32)

$$T_1 \in \left[\gamma - \sqrt{\gamma^2 - \frac{2L_{\mathrm{d}}P_{\mathrm{t}}T_{\mathrm{s}}}{N_{\mathrm{p}}^2 V_{\mathrm{psm\,max}}^2}}, \gamma + \sqrt{\gamma^2 - \frac{2L_{\mathrm{d}}P_{\mathrm{t}}T_{\mathrm{s}}}{N_{\mathrm{p}}^2 V_{\mathrm{psm\,max}}^2}}\right] \tag{34}$$

$$\gamma = \frac{T_{\mathrm{s}} V_{\mathrm{dc1}}\left(N_{\mathrm{p}} V_{\mathrm{psm\,max}} - V_{\mathrm{dc1}}\right)}{N_{\mathrm{p}}^2 V_{\mathrm{psm\,max}}^2}. \tag{35}$$

Consequently, depending on the operating condition of the compact MMDC, a proper value of T_1 can be selected within the range indicated in (34) to implement the regulation of the transferred power and SM capacitor voltages.

3) SM Current Stresses: The SM current stresses include the switch current stresses (the upper and lower switches) and the SM capacitor current stress, while the upper switch current stress is the same as that of the SM capacitor.

In the form of rms value, the upper switch and SM capacitor current stresses I_{SpuRMS} and I_{CpRMS} of the primary-side arm can be determined

$$\begin{aligned} I_{\mathrm{SpuRMS}} = I_{\mathrm{CpRMS}} &= \sqrt{\frac{1}{T_{\mathrm{s}}}\int_{t_0}^{t_2} i_{\mathrm{ap}}^2(t)\mathrm{d}t} \\ &= \frac{V_{\mathrm{dc1}} T_1}{L_{\mathrm{d}}(T_1+T_2)}\sqrt{\frac{T_1(T_1+4T_2)T_{\mathrm{s}}V_{\mathrm{dc1}}^2}{12(T_1+T_2)}}. \end{aligned} \tag{36}$$

Similarly, the lower switch current stress in the primary-side arm can be obtained

$$I_{\mathrm{SplRMS}} = \sqrt{\frac{1}{T_\mathrm{s}}\int_{t_2}^{t_4} i_{\mathrm{ap}}^2(t)\mathrm{d}t} = \frac{V_{\mathrm{dc1}}T_1}{L_\mathrm{d}\left(T_1+T_2\right)^2}\sqrt{\frac{T_\mathrm{s}\left(M_1+M_2+M_3+M_4\right)}{12}} \tag{37}$$

where M_1, M_2, M_3, and M_4 are

$$\begin{cases} M_1 = T_1^2\left(3T_\mathrm{s}-25T_2\right) \\ M_2 = 12T_2^2\left(T_\mathrm{s}-T_2\right) \\ M_3 = -5T_1^3 \\ M_4 = -4T_1T_2\left(8T_2-3T_\mathrm{s}\right). \end{cases} \tag{38}$$

The SM current stresses of the secondary-side arm can be derived by directly mapping those of the primary-side arm

$$\begin{cases} I_{\mathrm{SsuRMS}} = I_{\mathrm{CsRMS}} = KI_{\mathrm{SpuRMS}} \\ I_{\mathrm{SslRMS}} = KI_{\mathrm{SplRMS}}. \end{cases} \tag{39}$$

4) Arm Current Stress: The primary-side arm current stress I_{apRMS} can be given by

$$I_{\mathrm{apRMS}} = \sqrt{\frac{1}{T_\mathrm{s}}\int_{t_0}^{t_0+T_\mathrm{s}} i_{\mathrm{ap}}^2(t)\mathrm{d}t} = \frac{V_{\mathrm{dc1}}T_1}{L_\mathrm{d}\left(T_1+T_2\right)^2}\sqrt{\frac{T_\mathrm{s}\left(M_2+M_5+M_6+M_7\right)}{12}} \tag{40}$$

where M_5, M_6, and M_7 are

$$\begin{cases} M_5 = T_1^2\left(3T_\mathrm{s}-20T_2\right) \\ M_6 = -4T_1^3 \\ M_7 = -4T_1T_2\left(7T_2-3T_\mathrm{s}\right). \end{cases} \tag{41}$$

The secondary-side arm current stress I_{asRMS} is

$$I_{\mathrm{asRMS}} = KI_{\mathrm{apRMS}}. \tag{42}$$

According to (36)–(42), no matter the current stresses of the SM or the arm, they are all determined by T_1 and T_2, together. Therefore, the optimal selection of T_1 and T_2 can be further carried out with the aim of minimizing the current stresses.

5) SM Capacitance and Voltage Ripple: The SM capacitance is determined by the tolerance of the capacitor voltage ripple. Taking the primary-side SM as an example, its capacitor is charged by i_{ap} between t_0 and t_{zc}, where t_{zc} is the first zero-crossing time after t_0 of i_{ap}. Therefore, the ripple magnitude ΔV_{psm} of the primary-side SM capacitor voltage is

$$\Delta V_{\mathrm{psm}} = \frac{1}{C_{\mathrm{psm}}}\int_{t_0}^{t_{\mathrm{zc}}} i_{\mathrm{ap}}(t)\mathrm{d}t = \frac{V_{\mathrm{dc1}}}{8L_\mathrm{d}C_{\mathrm{sm}}}\frac{T_\mathrm{s}}{T_1+T_2}\left[\frac{T_1\left(T_1+2T_2\right)}{T_1+T_2}\right]^2 \tag{43}$$

$$t_{\mathrm{zc}} = \frac{T_1}{2}\left(1+\frac{T_2}{T_1+T_2}\right). \tag{44}$$

Assuming that the percentage tolerance of the capacitor voltage ripple is ε, the minimum primary-side SM capacitance can be derived by combining (3) and (43) as

$$C_{\mathrm{psm}} \geq N_\mathrm{p}\tau \tag{45}$$

$$\tau = \frac{1}{8\varepsilon L_\mathrm{d}}\left[\frac{T_1\left(T_1+2T_2\right)}{T_1+T_2}\right]^2. \tag{46}$$

Similarly, the secondary-side SM capacitor voltage ripple ΔV_{ssm} and the minimum secondary-side SM capacitance can be obtained as

$$\Delta V_{\mathrm{ssm}} = \frac{KV_{\mathrm{dc1}}}{8L_\mathrm{d}C_{\mathrm{ssm}}}\frac{T_\mathrm{s}}{T_1+T_2}\left[\frac{T_1\left(T_1+2T_2\right)}{T_1+T_2}\right]^2 \tag{47}$$

$$C_{\mathrm{ssm}} \geq K^2N_\mathrm{s}\tau. \tag{48}$$

6) DC-Bus Capacitance for Filtering and Decoupling: Assuming that the ac component of i_{ap} is absorbed by the MV bus capacitance C_{dc1}, the minimum value of C_{dc1} considering the bus voltage ripple percentage ε_t can be derived as

$$C_{\mathrm{dc1}} \geq \frac{T_1\left[T_1\left(3T_\mathrm{s}-8T_2\right)+4T_2\left(T_\mathrm{s}-T_2\right)-4T_1^2\right]}{4\varepsilon_\mathrm{t}L_\mathrm{d}\left(T_1+T_2\right)}. \tag{49}$$

Similarly, the minimum LV bus capacitance C_{dc2} for filtering can be obtained as

$$C_{\mathrm{dc2}} \geq \frac{K^2T_1\left[T_1\left(3T_\mathrm{s}-8T_2\right)+4T_2\left(T_\mathrm{s}-T_2\right)-4T_1^2\right]}{4\varepsilon_\mathrm{t}L_\mathrm{d}\left(T_1+T_2\right)}. \tag{50}$$

To decouple the parasitic inductance caused by the long power cable at the terminals, the impedance at the switching frequency of the dc-bus capacitances should be much smaller than that of the parasitic inductances

$$C_{\mathrm{dc1}} \geq \frac{T_\mathrm{s}^2}{4\pi^2k_\mathrm{c}L_{\mathrm{cp}}} \tag{51}$$

$$C_{\mathrm{dc2}} \geq \frac{T_\mathrm{s}^2}{4\pi^2k_\mathrm{c}L_{\mathrm{cs}}} \tag{52}$$

where k_c denotes the impedance ratio between capacitance and inductance. For the MVDC scenarios, L_{cp} and L_{cs} are $75--500\,\mu$H typically [7].

B. Parameters Design

To facilitate the illustration, the design and discussion is presented with the case of a 1 MW compact MMDC-based DC SST interconnecting the 12 kV and 2 kV buses, whose main parameters are depicted in Table I. The ac equivalent inductance $L_\mathrm{d} = 960\,\mu$H is chosen to fulfill the power transfer demand of the converter at rated operating conditions. It is worth noting that, in order to indicate the difference between the same steady-state variables in two modulations, the steady-state variables under the conventional Q2L modulation are labeled with the letter "Q" in the superscript.

1) SM Numbers Design: In the design case, when the MV bus voltage V_{dc1} varies from 7.2–12 kV, the transferred power of the converter is required to be larger than 1 MW to fulfill the load demand. Besides, 1.7 kV power semiconductor devices are

TABLE I
PARAMETERS OF THE CASE STUDY AND SIMULATION

Parameters	AQ2L	Q2L
MVDC bus voltage V_{dc1}	Rated 12 kV (7.2–12 kV)	
LVDC bus voltage V_{dc2}	Rated 2 kV (1.2–2 kV)	
DC-bus capacitance C_{dc1}, C_{dc2}	556 μF, 20 mF	
Transferred power P_o	Rated 1 MW	
Switching frequency f_{sw}	10 kHz	
Turn ratio of the MFT K : 1	6 : 1	
Equivalent ac inductance L_d	960 μH	
Dwell time t_d	100 ns	
Dead time T_{dz}	1 μs	
SM numbers N_p, N_s	17, 4	20, 5
SM capacitance C_{psm}, C_{ssm}	25 μF, 210 μF	45 μF, 370 μF

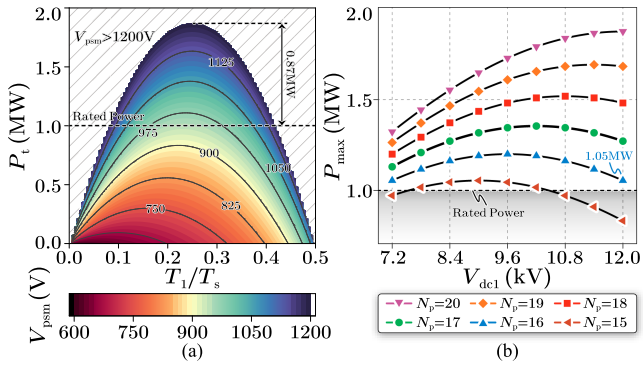

Fig. 6. (a) Variation characteristic of the primary-side SM voltage V_{psm} versus T_1 and P_t with $N_p = 20$ under the proposed AQ2L modulation. (b) Maximum transferred power P_{max} under different V_{dc1} and N_p.

utilized for the primary-side SMs, so the rated voltage stress for each SM in the primary side $V_{psmmax} = 1.2$ kV is set. Since V_{psmmax} is determined, N_p can be further identified by compromising the transferred power demand and converter size.

When V_{dc1} varies from 7.2 to 12 kV, N_p can be selected between 15 and 20 with the proper adjustment of the duty cycle D_p. In the case of $N_p = 20$ and $V_{dc1} = 12$ kV, the variation characteristic of the primary-side SM voltage V_{psm} versus T_1 and P_t is depicted in Fig. 6(a), where the colorful region indicates the feasible region that meets the constraint of $V_{psm} \le 1.2$kV, while the slash-filled region does not. From Fig. 6(a), it is observed that the boundary of the feasible region appears at $V_{psm} = V_{psmmax}$. Therefore, substituting (31) into (29) yields the boundary of P_t

$$P_{tB} = -\frac{N_p^2 V_{psm\,max}^2}{2L_d T_s} T_1^2 + \frac{V_{dc1}\left(N_p V_{psm\,max} - V_{dc1}\right)}{L_d} T_1 \tag{53}$$

where P_{tB} denotes the boundary of P_t at $V_{psm} = V_{psmmax}$. It can be seen that P_{tB} is quadratically related to T_1, which implies that the maximum transferred power P_{max} is found at $T_1 = \gamma$. Accordingly, P_{max} under different V_{dc1} can be obtained as

$$P_{max} = \frac{T_s}{2L_d} \cdot \left(V_{dc1} - \frac{V_{dc1}^2}{N_p V_{psm\,max}}\right)^2. \tag{54}$$

P_{max} should provide a margin to accommodate transient demand, i.e.,

$$P_{max} \ge (1+\xi)\, P_o \tag{55}$$

where ξ is the margin factor, and P_o is the rated output power.

Combining (54) and (55) gives the minimum N_p

$$N_p = \text{Ceil}\left[\frac{V_{dc1}^2}{\left(V_{dc1}^2 T_s - \zeta\right) V_{psm\,max}} \left(V_{dc1} T_s + \sqrt{T_s \zeta}\right)\right] \tag{56}$$

where Ceil$(\cdot)$ is the upward rounding function and $\zeta = 2(1+\xi)L_d P_o$. Then, substituting $\xi = 0.1$ and the parameters shown in Table I into (56), $N_p = 17$ can be obtained. Similarly, the SM number of the secondary side is ultimately set as $N_s = 4$ with a maximum voltage stress of 850 V.

P_{max} under different V_{dc1} and N_p ($V_{dc1} = 7.2$–12 kV, $N_p = 15$–20) is illustrated in Fig. 6(b). It is also revealed that P_{max} is in negative correlation with N_p. When $N_p = 16$, P_{max} at $V_{dc1} = 12$ kV is only 1.05 MW, and as N_p continues to decrease to 15, P_{max} is no longer able to satisfy the requirement of the load power demand 1.0 MW over the whole voltage range. As $N_p = 17$, a minimum power margin of 0.13 MW at $V_{dc1} = 7.2$ kV is achieved.

2) Control Characteristic Analysis and SM Capacitance Design: For a given transferred power P_t except for P_{max}, there are numerous T_1 available. Besides, the control characteristic under different values of T_1 is still ambiguous, so it is imperative to investigate it first.

Based on $N_p = 17$, the variation characteristics of the SM current stresses versus T_1 and P_t for $V_{dc1} = 12$ kV are exhibited in Fig. 7. As observed in Fig. 7(a) and (c), the current stresses of SM upper switch and arm in the primary side, i.e., I_{SpuRMS} and I_{apRMS} increases as P_t and T_1 rises. The profile of the lower switch current stress I_{SplRMS} is similar to I_{SpuRMS} and I_{apRMS}, but I_{SplRMS} and T_1 are no longer monotonically correlated in the light-load region ($P_t < 0.25P_o$). Fortunately, I_{SplRMS} is small in the light load condition compared with the heavy load condition, so the profile is still dominated by the heavy-load region.

Therefore, for the sake of minimizing the SM and arm current stresses, the lower bound of T_1 in (34) is supposed to be selected at a certain transferred power P_t, i.e.,

$$T_1^{opt} = \gamma - \sqrt{\gamma^2 - \frac{2L_d P_t T_s}{N_p^2 V_{psm\,max}^2}}. \tag{57}$$

With the selected T_1^{opt}, the SM capacitance can be further determined. With the aim of $\varepsilon \le 5\%$, the minimum SM capacitance in the primary-side arm at different V_{dc1} is depicted in Fig. 8. As can be observed, the maximum value of C_{psm} is obtained at $V_{dc1} = 7.2$ kV, which is 24.9 μF. For C_{ssm}, a similar phenomenon can be found. Hereby, the ultimately selected C_{psm} and C_{ssm} are exhibited in Table I.

3) DC-Bus Capacitance Design: According to (49)–(52), to meet the requirements of filtering ($\varepsilon_t \le 1.0\%$) and decoupling ($k_c \le 0.1$), $C_{dc1} \ge 48.4\,\mu$F, and $C_{dc2} \ge 1.7$mF are required. Nevertheless, as mentioned in [33], another critical role for dc-bus capacitors is to provide transient energy support or sinking, e.g., for sudden load changes, temporary faults, etc. Following this demand, the MV and LV bus capacitance C_{dc1} and C_{dc2}

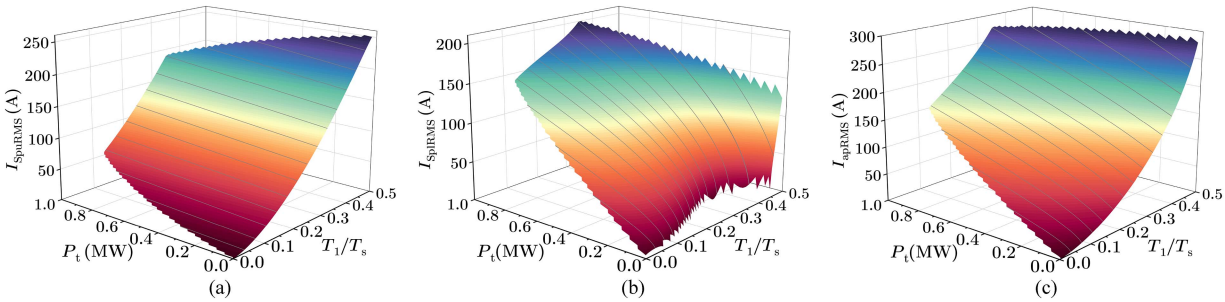

Fig. 7. Variation characteristics of the primary-side current stresses versus T_1 and P_{t} under the proposed AQ2L modulation. (a) Current stress of the upper switch I_{SpuRMS}. (b) Current stress of the lower switch I_{SplRMS}. (c) Primary-side arm current stress I_{apRMS}.

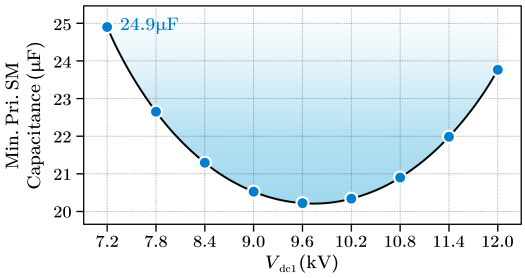

Fig. 8. Minimum SM capacitance in the primary-side arm for $\varepsilon \leq 5\%$ under $V_{\mathrm{dc1}} = 7.2$–12 kV.

can be estimated by

$$\begin{cases} C_{\mathrm{dc1}} = 2P_{\mathrm{o}}E_{\mathrm{P}}/V_{\mathrm{dc1}}^2 = 556\,\mu\mathrm{F} \\ C_{\mathrm{dc2}} = 2P_{\mathrm{o}}E_{\mathrm{P}}/V_{\mathrm{dc2}}^2 = 20\,\mathrm{mF} \end{cases} \tag{58}$$

where E_{P} is the energy-to-power ratio typically between 10 and 50 kJ/MW, and $E_{\mathrm{P}} = 40$ kJ/MW is used here. As can be seen, the capacitance requirement for energy support is much larger than the capacitance required for filtering and decoupling. Therefore, once the energy support requirement is fulfilled, the other two restrictions are satisfied naturally.

4) MFT Design: Similar to the traditional MFT design methods [34], [48], the MFT design for the compact MMDC needs to comprehensively consider the core loss, winding loss, and transformer volume to obtain the optimal parameters. Limited by the page, only the design considerations of winding loss and transient magnetic bias suppression, which differ from the traditional MFT, are discussed here.

The winding loss for the trapezoidal current waveform can calculated by fast Fourier transform as

$$\begin{cases} P_{\mathrm{wp}} = I_{\mathrm{ap\_dc}}^2 R_{\mathrm{dcp}} + \sum_{h=1}^{N_h} I_{\mathrm{ap\_ac}h}^2 R_{\mathrm{ac}ph} \\ P_{\mathrm{ws}} = I_{\mathrm{as\_dc}}^2 R_{\mathrm{dcs}} + \sum_{h=1}^{N_h} I_{\mathrm{as\_ac}h}^2 R_{\mathrm{ac}sh} \end{cases} \tag{59}$$

where P_{wp} and P_{ws} denote the primary and secondary winding loss, respectively; R_{dcp} and R_{dcs} denote the dc resistance of the primary and secondary windings, respectively; $R_{\mathrm{ac}ph}$ and $R_{\mathrm{ac}sh}$ denote the ac resistance of the primary and secondary windings at hth ($h = 1, 2, \ldots, N_h$ and N_h is determined by the calculation accuracy demand) current harmonic, respectively; $I_{\mathrm{ap\_ac}h}$ and $I_{\mathrm{as\_ac}h}$ are the rms values for hth harmonic of i_{ap} and i_{as}, respectively. It is seen that compared with the traditional MFT, the MFT in the compact MMDC has an extra dc loss term in winding loss, thus requiring about 20% more winding cross-sectional area.

According to (27), the steady-state flux density B_{ss} of the MFT can be calculated as

$$B_{\mathrm{ss}} = \frac{(T_{\mathrm{s}} - T_1 - T_2)\,V_{\mathrm{dc1}}}{2n_{\mathrm{tp}}A_{\mathrm{c}}} \tag{60}$$

where A_{c} is the effective magnetic core cross-sectional area.

Following (25), the mismatch of $I_{\mathrm{ap\_dc}}$ and $I_{\mathrm{as\_dc}}$ during the transient process will inevitably cause the transient dc magnetic bias, which can be expressed as

$$B_{\mathrm{ts}} = \frac{1}{A_{\mathrm{c}}R_{\mathrm{m}}}\left(I_{\mathrm{ap\_dc}} - \frac{I_{\mathrm{as\_dc}}}{K}\right). \tag{61}$$

The magnetic reluctance R_{m} and magnetizing inductance L_{m} are determined by the magnetic core and the air gap

$$R_{\mathrm{m}} = \frac{l_{\mathrm{c}}}{\mu_0\mu_{\mathrm{r}}A_{\mathrm{c}}} + \frac{l_{\mathrm{g}}}{\mu_0 A_{\mathrm{c}}} \tag{62}$$

$$L_{\mathrm{m}} = \frac{n_{\mathrm{tp}}^2}{R_{\mathrm{m}}} \tag{63}$$

where μ_0 is the vacuum permeability and μ_{r} is the relative permeability of the magnetic core; l_{c} and l_{g} are the mean path lengths of the magnetic core and air gap, respectively.

To avoid core saturation during the transient process such as startup and load stepping, the maximum transient flux density B_{max} should be less than the core saturation flux density B_{sat}

$$B_{\mathrm{max}} = B_{\mathrm{ss}} + |B_{\mathrm{ts}}| < B_{\mathrm{sat}}. \tag{64}$$

From (60) to (64), it is clear that the transient magnetic bias B_{ts} can be effectively suppressed by designing an appropriate air gap length l_{g} to avoid core saturation. Finally, the PC1293 nanocrystalline core of Advanced Technology and Materials is selected as the MFT core, with $l_{\mathrm{c}} = 106.7\mathrm{cm}$, $A_{\mathrm{c}} = 149.6\mathrm{cm}^2$, $\mu_{\mathrm{r}} = 80\,000$, and $B_{\mathrm{sat}} = 1.25\mathrm{T}$. The air gap length $l_{\mathrm{g}} = 0.2\mathrm{cm}$ is designed and the magnetizing inductance $L_{\mathrm{m}} = 33.6$ mH. Although the air gap is introduced to the MFT core to counteract the dc bias of the magnetizing current during transients, a large magnetizing inductance is still maintained thanks to the

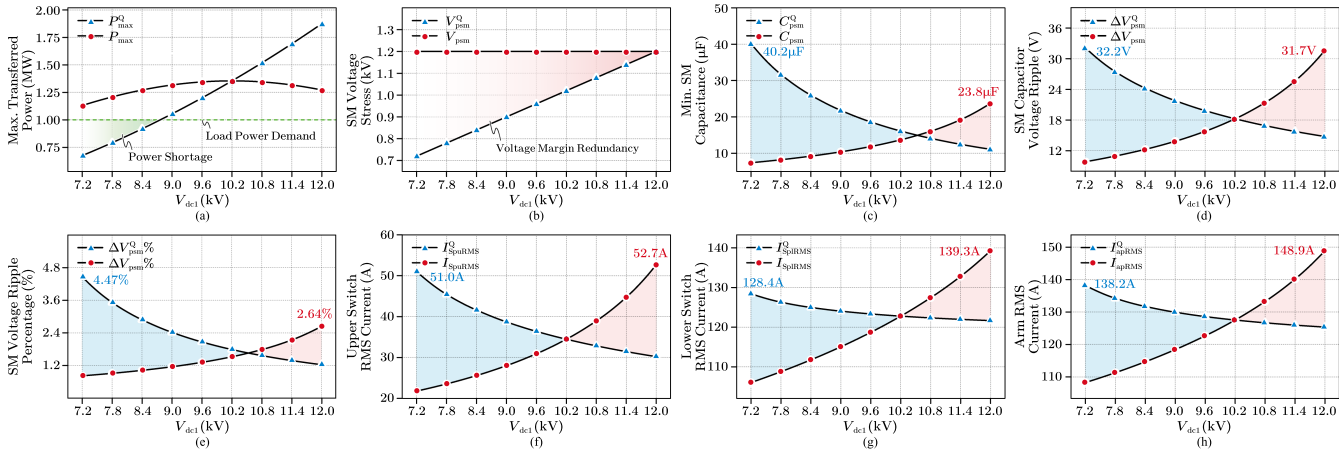

Fig. 9. Performance metrics of the compact MMDC at different V_{dc1} under the two modulations. (a) Maximum transferred power. (b) SM voltage stress in the primary-side arm. (c) Minimum SM capacitance in the primary-side arm for $\varepsilon \leq 5\%$. (d) Amplitude of the primary-side SM capacitor voltage ripple. (e) Percentage of the primary-side SM capacitor voltage ripple. (f) Upper switch rms current in the primary-side arm. (g) Lower switch rms current in the primary-side arm. (h) Primary-side arm rms current.

high permeability of the nanocrystalline ribbons. Besides, the moderate reduction of L_m contributes to the desirable increase of the magnetizing current, which facilitates the enlargement of the converter ZVS regions [14].

C. Performance Comparison

The conventional Q2L modulation is actually a special case of the proposed AQ2L modulation at $D_p = D_s = 0.5$. Therefore, the parameters design and steady-state performance metrics under the conventional Q2L modulation can be obtained by directly substituting $T_2 = T_s/2 - T_1$. Then, both modulations can be compared and evaluated.

1) SM Numbers: As previously analyzed, the SM numbers under the proposed AQ2L modulation are established as $N_p = 17$ and $N_s = 4$, while those under the Q2L modulation are $N_p = 20$ and $N_s = 5$. As a result, 16% SM number savings are achieved, facilitating the size reduction.

2) Transferred Power: The maximum transferred power P_{max} for the proposed AQ2L modulation has been revealed in (54). As for the conventional Q2L modulation, its maximum transferred power P^{Q}_{max} is obtained at $T_1 = T_s/4$, which is

$$P^{Q}_{max} = \frac{KV_{dc1}V_{dc2}T_s}{8L_d}. \tag{65}$$

The maximum transferred power at different V_{dc1} is depicted in Fig. 9(a). As can be seen, P^{Q}_{max} for the Q2L modulation declines rapidly with the drop of V_{dc1}, and when $V_{dc1} < 8.76$ kV, P^{Q}_{max} can no longer cover the rated load power demand. On the contrary, P_{max} for the proposed AQ2L modulation changes modestly and is always greater than the rated load power demand $P_o = 1$ MW as V_{dc1} varies between 7.2 and 12 kV. Therefore, the proposed AQ2L modulation can effectively improve the power transfer capability of the converter by boosting the SM capacitor voltage even under the operating condition of low bus voltage.

3) SM Voltage Stress: Fig. 9(b) demonstrates the SM voltage stress in the primary-side arm at different V_{dc1}. It indicates that under the proposed AQ2L modulation and adopting the selected optimized T_1^{opt}, the SMs always operate at the maximum voltage V_{psmmax}. While employing the Q2L modulation, the SM voltage stress decreases linearly with the drop of V_{dc1}, thus resulting in voltage margin redundancy of the high-voltage power semiconductor device in the case of low MV bus voltage. In the subsequent analysis, it is revealed that this rather increases the SM current stresses at low voltage conditions.

4) SM Capacitance and Voltage Ripple: For the sake of fairness, the SM capacitance and voltage ripple should be compared at the same transferred power. Since P^{Q}_{max} of the Q2L modulation cannot achieve the rated power P_o when $V_{dc1} < 8.76$ kV, it is, therefore, stipulated that, when V_{dc1} is dropped from 12 to 7.2 kV, the transferred power used for comparison changes also linearly from the rated 1 to 0.6 MW, i.e., $P_t = 83.33\text{A} \cdot V_{dc1}$.

Consequently, with the aim of $\varepsilon \leq 5\%$, the minimum SM capacitance in the primary-side arm at different V_{dc1} under the two modulations is illustrated in Fig. 9(c). As can be observed, under the conventional Q2L modulation, the minimum C^{Q}_{psm} grows as V_{dc1} drops and reaches a maximum value of $40.2\,\mu$F at $V_{dc1} = 7.2$ kV. With the opposite trend, utilizing the proposed AQ2L modulation, the minimum C_{psm} declines with V_{dc1}, and its maximum value is obtained at $V_{dc1} = 12$ kV, which is $23.8\,\mu$F. As a result, the proposed AQ2L modulation has a smaller SM capacitance requirement, which also contributes to reducing the converter size.

The SM capacitor voltage ripples in the primary-side arm under two modulations are compared with the same SM capacitance of $45\,\mu$F for the sake of fairness. The amplitude and percentage of the SM capacitor voltage ripples under two modulations at different V_{dc1} are shown in Fig. 9(d) and (e). It is seen that the SM capacitor voltage ripple ΔV^{Q}_{psm} under the conventional Q2L modulation increases as V_{dc1} decreases and reaches its maximum value of 32.2 V at $V_{dc1} = 7.2$ kV (corresponding to the SM capacitor voltage $V^{Q}_{psm} = 720$ V), hence, its maximum ripple percentage $\Delta V^{Q}_{psm}\%$ is 4.47%. On the contrary, under the proposed AQ2L modulation, the SM capacitor voltage ripple ΔV_{psm} is in positive correlation with V_{dc1}, and the maximum ripple is 31.69 V at $V_{dc1} = 12$ kV (corresponding to the SM capacitor voltage $V_{psm} = 1200$ V), which

is slightly smaller than the maximum ripple under conventional Q2L modulation. Therefore, its maximum ripple percentage $\Delta V_{\mathrm{psm}}\%$ is 2.64%. As for the SM capacitance and voltage ripple in the secondary-side arm, the same conclusion can be made.

5) SM Current Stresses: Similar to that of the SM capacitance, the transferred power $P_{\mathrm{t}} = 83.33\mathrm{A} \cdot V_{\mathrm{dc1}}$ is used for comparison. Accordingly, the rms current stresses of the upper switch, lower switch, and arm in the primary side are depicted in Fig. 9(f)–(h), respectively. It is noted that the three current stresses exhibit similar variation characteristics with respect to V_{dc1}. Namely, under the Q2L modulation, $I^{\mathrm{Q}}_{\mathrm{SpuRMS}}$, $I^{\mathrm{Q}}_{\mathrm{SplRMS}}$, and $I^{\mathrm{Q}}_{\mathrm{apRMS}}$ increase as V_{dc1} drops, and at $V_{\mathrm{dc1}} = 7.2$ kV, their maximum values are achieved as 51.0 A, 128.4 A, and 138.2 A, respectively. Whereas under the proposed AQ2L modulation, I_{SpuRMS}, I_{SplRMS}, and I_{apRMS} reach their maximum values at $V_{\mathrm{dc1}} = 12$ kV since they increase as V_{dc1} rises, which are 52.7 A, 139.3 A, and 148.9 A, respectively. The maximum rms current stresses with the proposed AQ2L modulation are moderately higher than those adopting the conventional Q2L modulation (3.3%, 8.5%, and 7.7% higher, respectively). Therefore, the established advantages above are obtained at the expense of a moderate increase in the maximum rms current.

6) Power Loss: Assuming that the CAS380M17HM3 (1.7 kV, $C_{\mathrm{po}} = 2.6$ nF) and CAB760M12HM3 (1.2 kV, $C_{\mathrm{so}} = 5.8$ nF, two in parallel utilized in an SM) power modules from Wolfspeed are used for the primary-side and secondary-side SMs, respectively, and the dead time $T_{\mathrm{dz}} = 1\ \mu$s is set for both primary-side and secondary-side SMs. Then, the ZVS region under the two modulations is attained and illustrated in Fig. 10.

Under the proposed AQ2L modulation, V_{psm} is fixed at $V_{\mathrm{psmmax}} = 1.2$ kV, so $I_{\mathrm{pz}} = 6.24$ A and $I_{\mathrm{sz}} = 1.64$ A, which are also fixed regardless of the change of V_{dc1}. While the Q2L modulation is employed, $V^{\mathrm{Q}}_{\mathrm{psm}}$ decreases with V_{dc1}, so I_{pz} and I_{sz} change as well, whose ranges are 3.74–6.24 A and 0.93–1.55 A as V_{dc1} ranges from 7.2 to 12 kV, respectively. It is observed in Fig. 10(a) and (c) that for the upper switches in the primary-side SMs (equivalent to S_{p1}) and the lower switches in the secondary-side SMs (equivalent to S_{s2}), their ZVS region covers almost the entire load range since $i_{\mathrm{ap}}(t_0)$ and $i_{\mathrm{ap}}(t_3)$ have a large positive magnitude. The ZVS region under the Q2L modulation is slightly larger when V_{dc1} is low since its I_{pz} and I_{sz} are smaller when V_{dc1} is low [note that I_{sz} is too small, so its curve is not illustrated in Fig. 10(a) and (c)]. For the lower switches in the primary-side SMs (equivalent to S_{p2}) and the upper switches in the secondary-side SMs (equivalent to S_{s1}), their ZVS criterion is more rigorous, as $i_{\mathrm{ap}}(t_1)$ and $i_{\mathrm{ap}}(t_2)$ are with relatively small negative magnitude compared with $i_{\mathrm{ap}}(t_0)$ and $i_{\mathrm{ap}}(t_3)$. As depicted in Fig. 10(b) and (d), the area of the ZVS region under two modulations is comparable. The proposed AQ2L modulation owns a larger ZVS region as V_{dc1} is close to 12 kV, while vice versa when V_{dc1} is close to 7.2 kV.

To further investigate the total power loss, a loss simulation is performed in the PLECS platform. Similarly, the transferred power $P_{\mathrm{t}} = 83.33\mathrm{A} \cdot V_{\mathrm{dc1}}$ is set, and the results are demonstrated in Fig. 11. The MFT core loss is calculated by the improved generalized Steinmetz equation [49]. As can be seen Fig. 11, the power loss is dominated by the conduction loss since

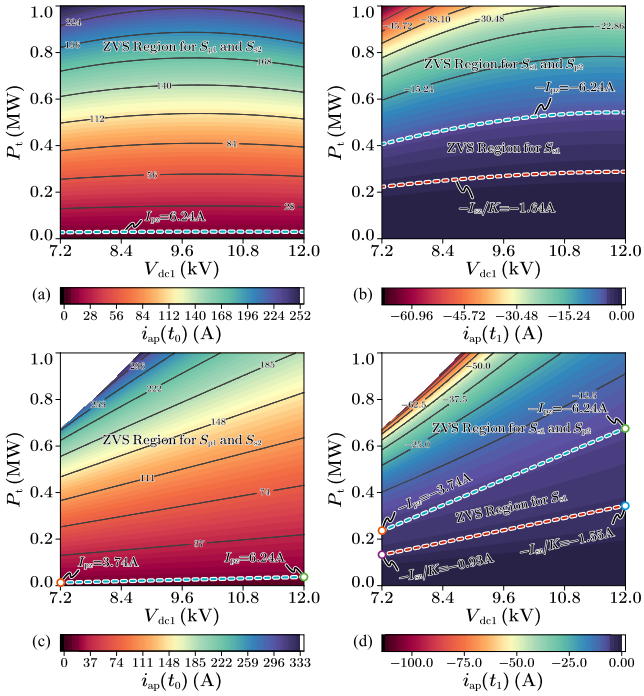

Fig. 10. ZVS regions under two modulations. Under the proposed AQ2L modulation: (a) ZVS region for the equivalent switches S_{p1} and S_{s2}, and (b) ZVS region for the equivalent switches S_{p2} and S_{s1}. Under the Q2L modulation: (c) ZVS region for the equivalent switches S_{p1} and S_{s2}, and (d) ZVS region for the equivalent switches S_{p2} and S_{s1}.

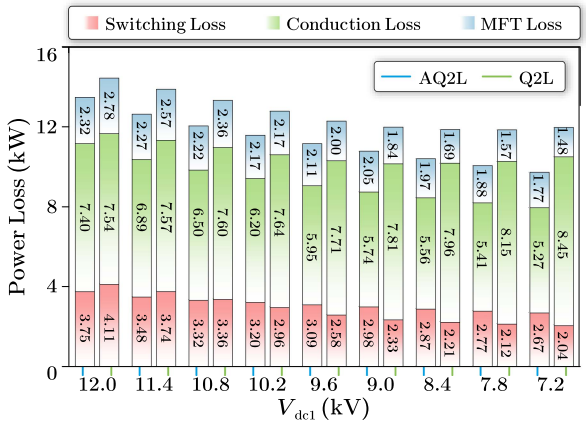

Fig. 11. Power loss of the compact MMDC for different V_{dc1} under two modulations.

most of the switching loss is conserved thanks to the achievement of ZVS turning-ON. Consequently, the power loss of the compact MMDC under the proposed AQ2L modulation is always smaller than that under the Q2L modulation because the SM number required by the AQ2L modulation is fewer.

D. Discussion

Four cases, i.e., the FTF H-bridge MMDC under conventional Q2L modulation (case I), the FTF HB MMDC under conventional Q2L modulation (case II), the compact MMDC

TABLE II
COMPARISON OF FOUR CASES

Cases		Case I: FTF H-bridge MMDC with Q2L	Case II: FTF HB MMDC with Q2L	Case III: Compact MMDC with Q2L	Proposed case: Compact MMDC with the proposed AQ2L
DC-bus capacitors	For filtering ($\varepsilon_t \leq 1.0\%$) and decoupling ($k_c \leq 0.1$)	20.1μF for MV bus 0.7mF for LV bus	72.3μF for MV bus 2.6mF for LV bus	72.3μF for MV bus 2.6mF for LV bus	48.4μF for MV bus 1.7mF for LV bus
	For energy support	556μF for MV bus 20mF for LV bus			
SM	Total number	52	26	25	21
	Pri. stress	Max. rms current 77.9A Max. voltage 1200V	Max. rms current 155.9A Max. voltage 1200V	Max. rms current 128.4A Max. voltage 1200V	Max. rms current 139.3A Max. voltage 1200V
	Sec. stress	Max. rms current 467.4A Max. voltage 667V	Max. rms current 935.4A Max. voltage 667V	Max. rms current 770.4A Max. voltage 800V	Max. rms current 835.8A Max. voltage 850V
	Pri. number	40 SMs with 1.7kV/225A modules	20 SMs with 1.7kV/380A modules	20 SMs with 1.7kV/380A modules	17 SMs with 1.7kV/380A modules
	Sec. number	12 SMs with 1.2kV/425A modules (two in parallel in an SM)	6 SMs with 1.2kV/760A modules (two in parallel in an SM)	5 SMs with 1.2kV/760A modules (two in parallel in an SM)	4 SMs with 1.2kV/760A modules (two in parallel in an SM)
	Pri. SM Cap. for 5.0% voltage ripple	42μF with 10μH arm inductance	65μF with 10μH arm inductance	45μF	25μF
	Sec. SM Cap. for 5.0% voltage ripple	320μF with 0.1μH arm inductance	540μF with 0.1μH arm inductance	370μF	210μF
	Pri.voltage ripple percentage with C_{psm}=45μF	4.13% with 10μH arm inductance	10.5% with 10μH arm inductance	4.5%	2.6%
Magnetic component	MFT volume	0.83 p.u.		1.0 p.u.	
	Arm inductors for current choking	8 pcs with each volume of 0.5 p.u.	4 pcs with each volume of 1.0 p.u.	No need	
	AC inductor for power transfer	960μH	240μH	960μH	
Performance	Max. transferred Power	1.875MW max. at V_{dc1}=12kV 0.675MW min. at V_{dc1}=7.2kV			1.35MW max. at V_{dc1}=10.2kV 1.13MW min. at V_{dc1}=7.2kV
	Power loss	16.96kW	16.62kW	14.43kW	13.47kW
	Total volume	570L	553L	448L	430L

under conventional Q2L modulation (case III), and the compact MMDC under the proposed AQ2L modulation (the proposed case) are designed, and their parameters are listed in Table II. As a premise for comparison, the same prior specifications are utilized, including the transferred power of $P_t = 83.33\text{A} \cdot V_{dc1}$, the switching frequency of 10 kHz, and the capacitor voltage ripple requirements. The main design process is as follows:

1) for the given specifications, the voltage and current profiles are first calculated under different topologies and modulations, and the SM numbers N_p and N_s are determined;
2) the suitable power devices and passive devices can then be selected so that the power loss and volume can be estimated;
3) the schemes under different topologies and modulations are evaluated and compared.

To ensure a fair comparison, the voltage and current utilizations of the SM power devices in all cases are selected to be as close as possible. Taking the power devices in the secondary-side SMs as an example, the current utilizations for four cases are 55.0%, 61.5%, 50.7%, and 55.0%, respectively, and the voltage utilizations for four cases are 55.6%, 55.6%, 66.7%, and 70.8%, respectively. The voltage utilizations in cases I and II are slightly lower since their SM numbers have to be even with the structure of the upper and lower arm, while benefiting from the single-arm structure, the SM numbers in case III and the proposed case are free from this constraint. It also shows the advantage of the compact MMDC in terms of design flexibility. For more intuition, the main performance indicators are also illustrated in Fig. 12 as a radar chart, where the better indicators are mapped to the more outlying areas so that the case with better overall performance would have a larger encompassing area. The detailed data analysis and comparison are as follows.

1) DC-Bus Capacitors: If only the voltage ripple and cable parasitic inductance decoupling are considered, the dc-bus capacitances for the four cases are different, and the dc-bus capacitances of case I and the proposed case are smaller than those of cases II and III. However, as mentioned in [33], taking the transient energy support demand into account, the capacitance requirement is much larger than that required for the other two demands, and depends only on the power capacity P_o and bus voltages, therefore, the dc-bus capacitance for all cases is the same.

2) SM Numbers and SM Voltage, Current Stresses: The SM numbers in case II (20 primary and 6 secondary SMs) and case III (20 primary and 5 secondary SMs) are halved compared with that in case I (40 primary and 12 secondary SMs). While in the proposed case, the SM voltage is always controlled to be the designed maximum value, thus reducing the SM number

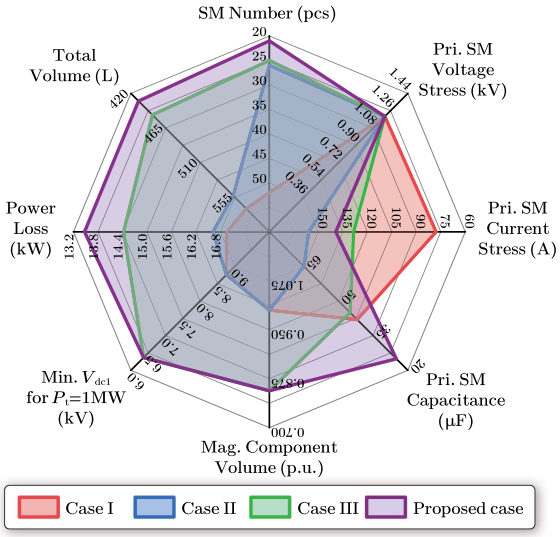

Fig. 12. Comparison for the four cases of the MMDC topologies and modulations.

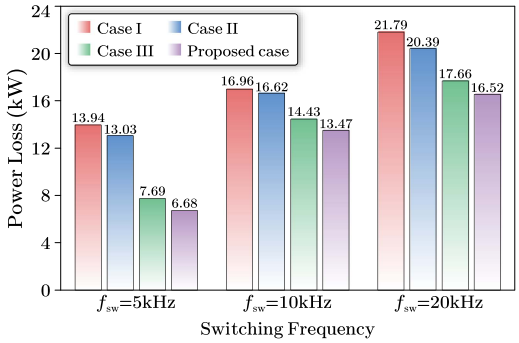

Fig. 13. Power loss for four cases at different switching frequencies.

(17 primary and 4 secondary SMs). Nevertheless, with the same power capacity and voltage level, the lower SM number inevitably implies that the larger current to be handled by each SM. Therefore, the current stress of the proposed case is 139.3 A, which is the second highest among all cases, while case II is the largest at 155.9 A since its voltage amplitude applied on the MFT is halved. Compared with the compact MMDC with the conventional Q2L modulation (i.e., case III), the proposed case avoids the increase in SM voltage stress at the expense of moderately increasing current stress, thereby reducing the SM number.

3) SM Capacitance and Voltage Ripple: The SM capacitance is governed by its voltage ripple percentage $\Delta V_{\rm psm}\%$, and $\Delta V_{\rm psm}\% = \Delta V_{\rm psm}/V_{\rm psm}$. Since the proposed case has a constant $V_{\rm psm}$, $\Delta V_{\rm psm}\%$ is only related to $\Delta V_{\rm psm}$, and $C_{\rm psm} = 25\,\mu$F can be designed to fulfill the voltage ripple percentage tolerance of 5.0% at different $V_{\rm dc1}$. While the SM capacitor voltages in cases I–III all decrease linearly with the drop of $V_{\rm dc1}$, thus leading to a larger SM capacitor voltage ripple percentage. Therefore, the SM capacitance in cases I–III needs to be larger to address the voltage ripple percentage tolerance of 5.0%. As a result, the proposed case has a smaller SM capacitance requirement, which also contributes to reducing the converter size.

4) Magnetic Components: The MFT volume for both case III and the proposed case is about 20% larger than cases I and II since the MFT winding current stresses of the compact MMDC are larger. Moreover, for current choking purposes, extra arm inductors are required for case I (8 pcs) and case II (4 pcs). While for case III and the proposed case, the magnetizing inductor of the MFT is multiplexed as the choke inductor of the dc loop, and thus, no additional arm choke inductor is required. Accordingly, the total volume of magnetic components in the proposed case is still smaller than that in cases I and II, even though its MFT volume is larger.

5) Power and ZVS Characteristics: With the Q2L modulation, cases I, II, and III exhibit the same maximum transferred power, i.e., 1.875 MW at $V_{\rm dc1} = 12$ kV and 0.675 MW at $V_{\rm dc1} = 7.2$ kV, which decreases dramatically with the drop of $V_{\rm dc1}$. While the proposed case achieves superior transferred power flatness, fulfilling the 1 MW transferred power demand over the whole voltage range. Moreover, the proposed AQ2L modulation also inherits favorable ZVS characteristics of the conventional Q2L modulation. The power loss for four cases at different switching frequencies (5 kHz, 10 kHz, and 20 kHz) is evaluated, as shown in Fig. 13. Thanks to the achievement of ZVS turning-ON, the power loss rises moderately as the switching frequency increases, and maintains at a low level. Moreover, the proposed case features the lowest power loss among the four cases since the smallest SM number is used.

6) Volume Estimation: The total volume of the key components (the dc-bus capacitor is excluded since it is the same under four cases) is estimated for the four cases. The volume of the SM capacitor is calculated based on an empirical energy density of $6.3{\rm cm}^3/{\rm J}$ [50]. Besides, it is assumed that 40% volume utilization is achieved due to insulation and mounting occupation. It is seen from Table II that the proposed case has the smallest volume footprint among the four cases.

Benefiting from the flexible SM voltage control technique, the proposed case outperforms the other cases in wide voltage range scenarios. Compared with case III, the proposed case provides a saving of about 4.0% in total volume, with 16.0% fewer in SM numbers, 44.4% smaller in SM capacitance, 20.5% smaller in magnetic component volume, and 6.7% less in power loss, while achieving superior transferred power flatness over a wide range of voltage variations. Compared with cases I and II, the proposed case provides savings of about 24.6% and 22.2% in total volume, respectively. Overall, the proposed case outperforms the other cases in terms of volume.

In general, for the MMDCs with the same power capacity and voltage level, the lower SM number inevitably implies that the larger current to be handled by each power device. However, the total area of bare semiconductor chips, which depends jointly on the voltage and current ratings [51], [52], is almost unchanged, and therefore, the total cost of bare semiconductor chips is also almost unchanged. Using a smaller number of power devices can also notably reduce the space wastage (i.e., the insulation and mounting space between components) and the volume occupation of auxiliary components (e.g., drive circuits, heat sinks, structural members, etc.). Especially in the high-power density applications, liquid-cooled heat sinks are usually configured for

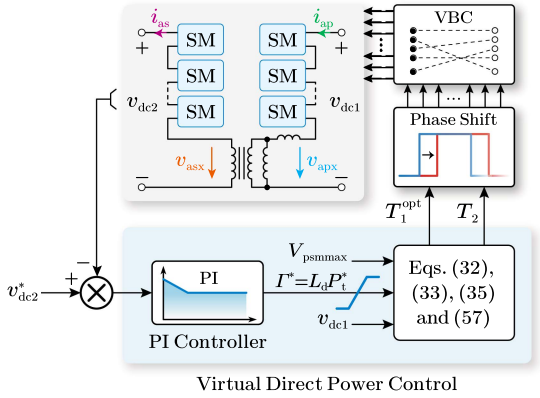

Fig. 14. Control strategy of the compact MMDC under the AQ2L modulation.

the power devices. Although the heat dissipation area is reduced since the lower number of power devices is used, the device temperature can still be maintained by increasing the flow rate of the cooling fluid. Therefore, the volume of the heat sink will not increase significantly. Nevertheless, the power device with a higher current rating also leads to new challenges in packaging processes, which might increase the cost or compromise the reliability of the device. On balance, the advantage of using power devices with lower numbers and higher current ratings would be more apparent in some specific scenarios, e.g., in megawatt power class applications [53].

IV. Simulation and Experimental Verification

A. Control Strategy

Based on (33) and (57), it is observed that the optimal values of T_1 and T_2 are affected by the inductance L_d. In practice, the value of L_d varies with i_ap due to the nonlinear permeability of the magnetic powder core, which is difficult to be obtained accurately. To this end, a virtual power control strategy is proposed which dispenses with the accurate value of L_d. In the proposed strategy, the virtual reference Γ^*, which is the product of L_d and the virtual power reference P_t^*, is directly adopted as the output of the closed-loop controller. In this way, only the approximate value of L_d and the maximum allowable value of P_t^* are required as the saturation limit for the closed-loop controller. Once Γ^* is determined, T_1^opt can be found according to (35) and (57) to ensure the minimum current stresses. In turn, T_2 can be obtained by using (32) and (33), and thereby the closed-loop control can be accomplished. Besides, the voltage balancing control method presented in [54] is applied to keep the SM capacitor voltages balanced. The control block diagram of the above control strategy is demonstrated in Fig. 14.

B. Simulation Results

To validate the abovementioned analysis, the simulations of the compact MMDC under the two modulations are performed employing the PLECS platform with the parameters shown in Table I.

The startup waveforms ($P_\mathrm{t} = 0.5$ MW, $V_\mathrm{dc1} = 12$ kV) are depicted in Fig. 15. The entire startup process consists of two

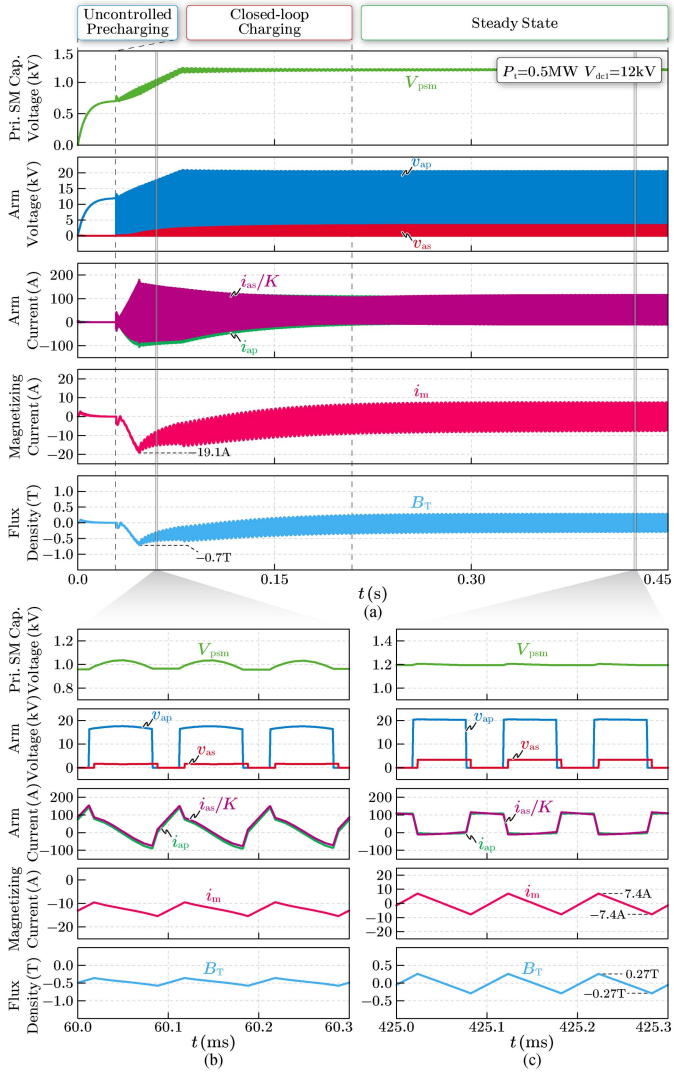

Fig. 15. Startup simulation waveforms of the compact MMDC with the proposed AQ2L modulation. (a) Entire startup process. (b) Transient waveforms during the closed-loop charging procedure. (c) Steady-state waveforms after completing the startup.

procedures, uncontrolled precharging and closed-loop charging. During the uncontrolled precharging procedure, all SM capacitors in the primary side are automatically charged by the MV bus via the freewheeling diodes. Since this procedure is uncontrolled, a resistor–contactor snubber circuit is connected in series between the MV bus and C_dc1, thus avoiding a large inrush current [55]. This process ultimately charges the SM capacitor voltage to $V_\mathrm{dc1}/N_\mathrm{p}$, and then the closed-loop charging procedure is engaged. An adaptive soft-start strategy based on the AQ2L modulation has been designed to achieve a smooth closed-loop charging procedure. The main idea is to set $V_\mathrm{psmmax} = V_\mathrm{dc1}/N_\mathrm{p}$ at the beginning of the closed-loop charging procedure, and gradually increase V_psmmax until it reaches the designed maximum value. In this way, the current spikes are avoided throughout the startup process and the converter is gradually charged to the steady state. As seen in Fig. 15(a), the magnetizing current of the MFT (i.e., $i_\mathrm{m} = i_\mathrm{ap} - i_\mathrm{as}/K$) has a dc bias during the startup process, and its maximum absolute value is -19.1 A, corresponding to a maximum flux density of -0.7 T, which is smaller

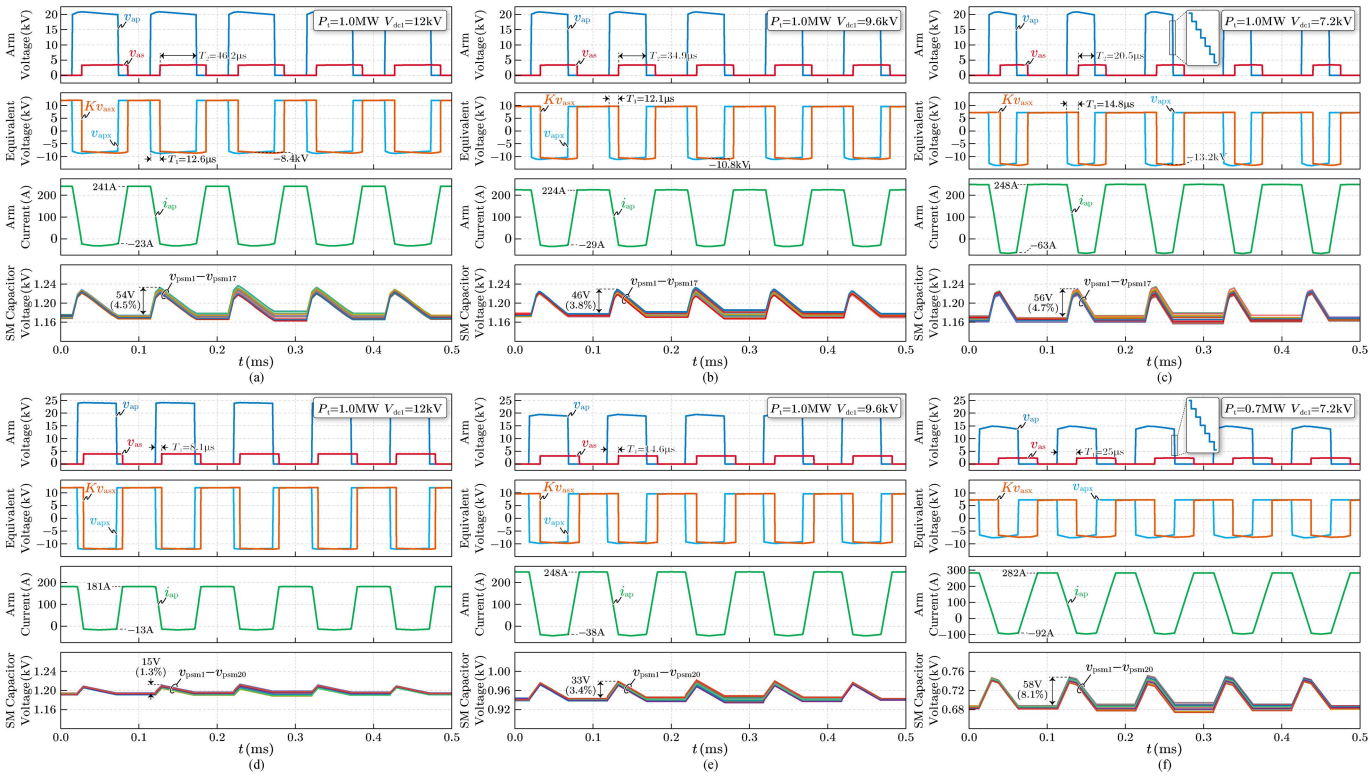

Fig. 16. Simulation waveforms of the compact MMDC under the two modulations. Under the proposed AQ2L modulation. (a) $P_t = 1.0$ MW, $V_{dc1} = 12$ kV. (b) $P_t = 1.0$ MW, $V_{dc1} = 9.6$ kV. (c) $P_t = 1.0$ MW, $V_{dc1} = 7.2$ kV. Under the Q2L modulation. (d) $P_t = 1.0$ MW, $V_{dc1} = 12$ kV. (e) $P_t = 1.0$ MW. $V_{dc1} = 9.6$ kV. (f) $P_t = 0.7$ MW, $V_{dc1} = 7.2$ kV.

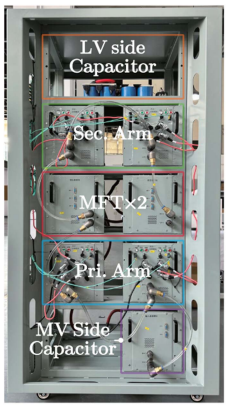

Fig. 17. Experimental prototype of the compact MMDC.

TABLE III
PARAMETERS OF THE EXPERIMENT

Parameters	Value
MVDC bus voltage V_{dc1}	Rated 2.6 kV (1.56–2.6 kV)
LVDC bus voltage V_{dc2}	Rated 1.0 kV (0.6–1.0 kV)
DC-bus capacitance C_{dc1}, C_{dc2}	120 μF, 560 μF
Transferred power P_o	Rated 50 kW
Switching frequency f_{sw}	30 kHz
Turn ratio of the MFT K : 1	2.6 : 1
Equivalent ac inductance L_d	220 μH
Dwell time t_d	300 ns
Dead time T_{dz}	1.0 μs
SM numbers N_p, N_s	5, 2
SM capacitance C_{psm}, C_{ssm}	140.5 μF, 140.5 μF

than the core saturation flux density $B_{sat} = 1.25$ T. Fig. 15(b) and (c) demonstrates the waveforms of during and after the startup process, respectively. It is seen that the maximum arm current amplitude is 179 A for i_{ap}, and the steady-state flux density after the startup is $B_{ss} = 0.27$ T.

The steady-state simulation results of the compact MMDC under the two modulations are exhibited in Fig. 16. As can be seen in Fig. 16(a)–(c), with the proposed AQ2L modulation, despite V_{dc1} decreasing from 12 kV to 9.6 kV and 7.2 kV, the duty cycle D_p of the primary-side SMs also changes to 0.59, 0.47, and 0.35, respectively, so that the primary-side SM capacitor voltages are always maintained at 1.2 kV. As a result, the converter can still retain the transferred power $P_t = 1.0$ MW over the full voltage range of V_{dc1}, while I_{apRMS} is 147.1 A, 157.2 A, and 192.4 A (corresponding to $V_{dc1} = 12$ kV, 9.6 kV, and 7.2 kV), respectively.

Fig. 16(d)–(f) shows the waveforms at $V_{dc1} = 12$ kV, 9.6 kV, and 7.2 kV under the Q2L modulation, respectively. It is seen that since D_p is always held at 0.5, the primary-side SM capacitor voltages decrease with V_{dc1}, which are 1200 V, 960 V and 720 V, respectively. Moreover, I^{Q}_{apRMS} at $V_{dc1} = 12$ kV, 9.6 kV and 7.2 kV is 125.0 A, 167.0 A, and 181.9 A, respectively. In addition, it is important to note that when $V_{dc1} = 7.2$ kV, the converter

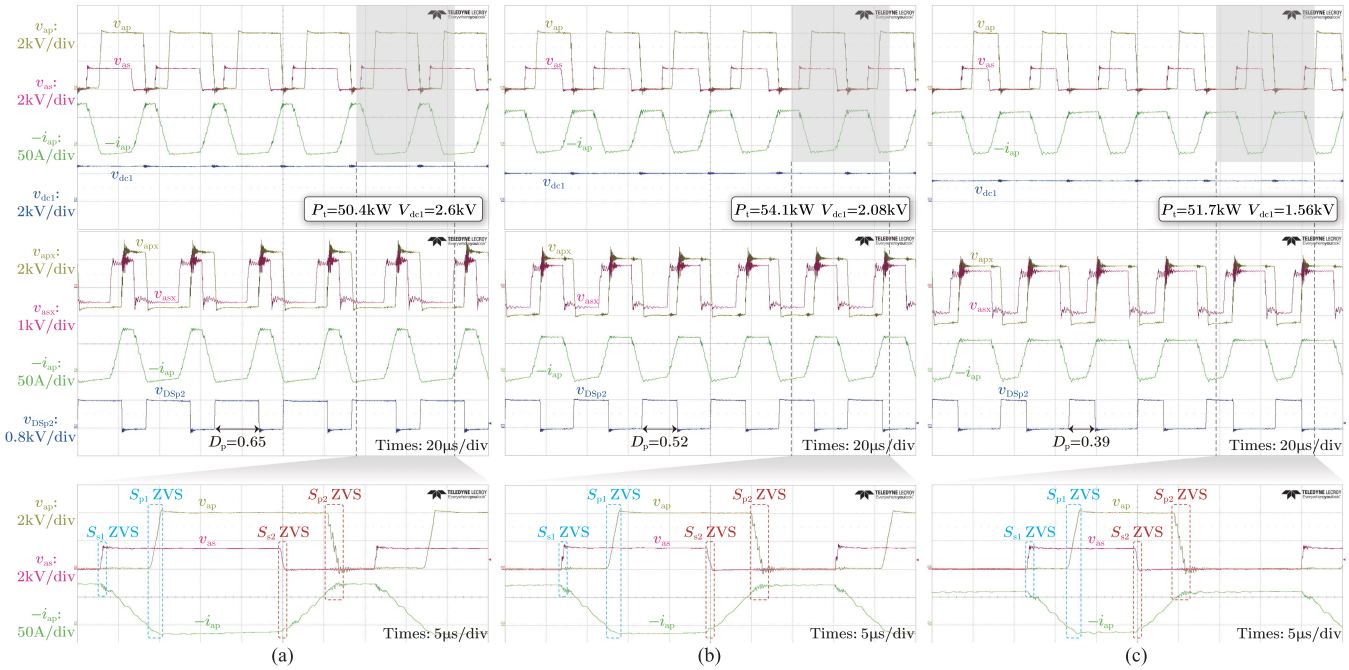

Fig. 18. Steady-state experimental waveforms of the compact MMDC under the proposed AQ2L modulation. (a) Waveforms at $P_t = 50.4$ kW, $V_{dc1} = 2.6$ kV. (b) Waveforms at $P_t = 54.1$ kW, $V_{dc1} = 2.08$ kV. (c) Waveforms at $P_t = 51.7$ kW, $V_{dc1} = 1.56$ kV.

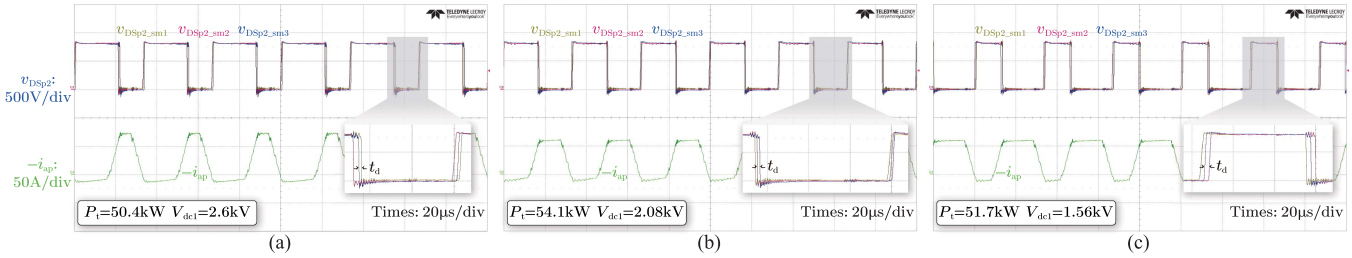

Fig. 19. Experimental waveforms of the balanced SM capacitor voltages under the proposed AQ2L modulation. (a) Waveforms at $P_t = 50.4$ kW, $V_{dc1} = 2.6$ kV. (b) Waveforms at $P_t = 54.1$ kW, $V_{dc1} = 2.08$ kV. (c) Waveforms at $P_t = 51.7$ kW, $V_{dc1} = 1.56$ kV.

transferred power has reached its maximum value under the Q2L modulation, i.e., $P_t = 0.7$ MW with $T_1 = T_s/4 = 25\,\mu$s. Comparatively, it reflects the favorable power transfer characteristic of the proposed AQ2L modulation, even though a lower SM number is used.

With the primary-side SM capacitance $C_{psm} = 25\,\mu$F under the proposed AQ2L modulation, the SM capacitor voltage ripple ΔV_{psm} at $V_{dc1} = 12$ kV, 9.6 kV and 7.2 kV are 54 V, 46 V and 56 V, respectively. Whereas with the larger primary-side SM capacitance $C^{Q}_{psm} = 45\,\mu$F, the SM capacitor voltage ripple ΔV^{Q}_{psm} under the Q2L modulation at $V_{dc1} = 12$ kV, 9.6 kV, and 7.2 kV are 15 V, 33 V, and 58 V, respectively. Consistent with the previous analysis, with the same transferred power, the SM capacitor voltage ripple under the proposed AQ2L modulation is smaller than that under the Q2L modulation when $V_{dc1} < 10.2$ kV, while the SM capacitor voltage ripple under the proposed AQ2L modulation is larger than that under the Q2L modulation when $V_{dc1} \geq 10.2$ kV. However, as V_{dc1} drops from 12 to 7.2 kV, the SM capacitor voltage V^{Q}_{psm} under the Q2L modulation also decreases from 1200 to 720 V, whereas the SM capacitor voltage V_{psm} remains unchanged at 1200 V under the proposed AQ2L modulation. Thereby, the SM capacitor voltage ripple percentage $\Delta V_{psm}\%$ at $V_{dc1} = 12$ kV, 9.6 kV, and 7.2 kV under the proposed AQ2L modulation are 4.5%, 3.8%, and 4.7%, respectively, which always satisfies the requirement of $\varepsilon \leq 5.0\%$, whereas the SM capacitor voltage ripple percentage $\Delta V^{Q}_{psm}\%$ under the Q2L modulation increases significantly with the decrease of V_{dc1}, which are 1.3%, 3.4%, and 8.1% at $V_{dc1} =$ 12 kV, 9.6 kV and 7.2 kV, respectively. Accordingly, the above-mentioned results validate the conclusion on the proposed AQ2L modulation featuring a smaller SM capacitance requirement.

C. Experimental Setup and Results

To verify the proposed scheme, a 50 kW/2.6 kV prototype was built, as shown in Fig. 17, whose parameters are depicted in

Table III. 1200 V SiC power modules CAS350M12BM3 from Wolfspeed are utilized in the experimental prototype, and $V_{\mathrm{psmmax}} = 800$ V is set. N_{p} and N_{s} are designed as 5 and 2 based on (56), respectively, while those under the conventional Q2L modulation are 7 and 3, where 30% SM number savings are achieved. Due to the lack of a high-voltage power supply, the LV bus is connected to the input power supply, while the MV bus serves as the output load.

Fig. 18 demonstrates the steady-state experimental waveforms of the compact MMDC under the proposed AQ2L modulation. As shown in Fig. 18(a), at $V_{\mathrm{dc1}} = 2.6$ kV and $P_{\mathrm{t}} = 50.4$ kW, the duty cycle D_{p} of the primary-side SMs is regulated as 0.65, so V_{psm} is kept at 800 V (indicated by the drain-source voltage v_{DSp2} of the lower switch in the primary-side SM in the waveforms), while V_{psm} would be 1040 V if the conventional Q2L modulation was used. The amplitudes of v_{ap} and v_{as} are 4 kV and 1.54 kV, respectively. Therefore, the positive and negative amplitudes of v_{apx} and v_{asx} are 2.6 kV/−1.4 kV and 1.0 kV/− 0.54 kV, respectively. It should be noted that the oscillations of v_{apx} and v_{asx} at the switching moments and their slight voltage drops when i_{ap} ramps up and down are caused by the presence of stray inductances $L_{\sigma\mathrm{p}}$ and $L_{\sigma\mathrm{s}}$ on the line.

As shown in Fig. 18(b) and (c), it is seen that when $V_{\mathrm{dc1}} = 2.08$ kV and $V_{\mathrm{dc1}} = 1.56$ kV, D_{p} is adjusted to 0.52 and 0.39, respectively, keeping $V_{\mathrm{psm}} = 800$ V, $v_{\mathrm{ap}} = 4$ kV, and $v_{\mathrm{as}} = 1.54$ kV. Hence, the positive and negative amplitudes of v_{apx} and v_{asx} at $V_{\mathrm{dc1}} = 2.08$ kV are 2.08 kV/–1.92 kV and 0.8k V/–0.74 kV, respectively, while those at $V_{\mathrm{dc1}} = 1.56$ kV are 1.56 kV/–2.44 kV and 0.6 kV/–0.94 kV, respectively. It is observed that all the SMs achieve ZVS turning-ON (note that S_{p1} and S_{p2} indicate the upper and lower switches in the primary-side SMs, respectively; S_{s1} and S_{s2} indicate the upper and lower switches in the secondary-side SMs, respectively) for all three operating conditions, as shown in the bottom waveforms of Fig. 18. Furthermore, the average value of i_{ap} in Fig. 18(c) is 33.1 A, revealing that the transferred power $P_{\mathrm{t}} = 51.7$ kW is achieved at $V_{\mathrm{dc1}} = 1.56$ kV, while the maximum value of P_{t} is only 46.0 kW with the same parameters under the conventional Q2L modulation. It validates the effectiveness of the proposed AQ2L modulation in boosting the power transfer capability at low voltage.

Experimental waveforms of the balanced SM capacitor voltages under the proposed AQ2L modulation are shown in Fig. 19. At $V_{\mathrm{dc1}} = 2.6$ kV and $P_{\mathrm{t}} = 50.4$ kW, the drain-source voltages of the lower switch in the three primary-side SM $v_{\mathrm{DSp2\_sm1}}$, $v_{\mathrm{DSp2\_sm2}}$, and $v_{\mathrm{DSp2\_sm3}}$ with the same high-level magnitude shown in Fig. 19(a) reflect the well-balanced SM capacitor voltages, i.e., v_{psm1}, v_{psm2}, and v_{psm3}. From the enlarged waveform in Fig. 19(a), the staggered dwell time t_{d} between $v_{\mathrm{DSp2\_sm1}}$, $v_{\mathrm{DSp2\_sm2}}$, and $v_{\mathrm{DSp2\_sm3}}$ can also be observed, which is used for the balancing control of SM capacitor voltages. Similarly, the waveforms in Fig. 19(b) and (c) also demonstrate the well-balanced SM capacitor voltages at the operating conditions of $V_{\mathrm{dc1}} = 2.08$ kV, $P_{\mathrm{t}} = 54.1$ kW and $V_{\mathrm{dc1}} = 1.56$ kV, $P_{\mathrm{t}} = 51.7$ kW, respectively.

Transient experimental waveforms of the compact MMDC under the proposed AQ2L modulation are illustrated in Fig. 20. As shown in Fig. 20(a), when the load power of the compact

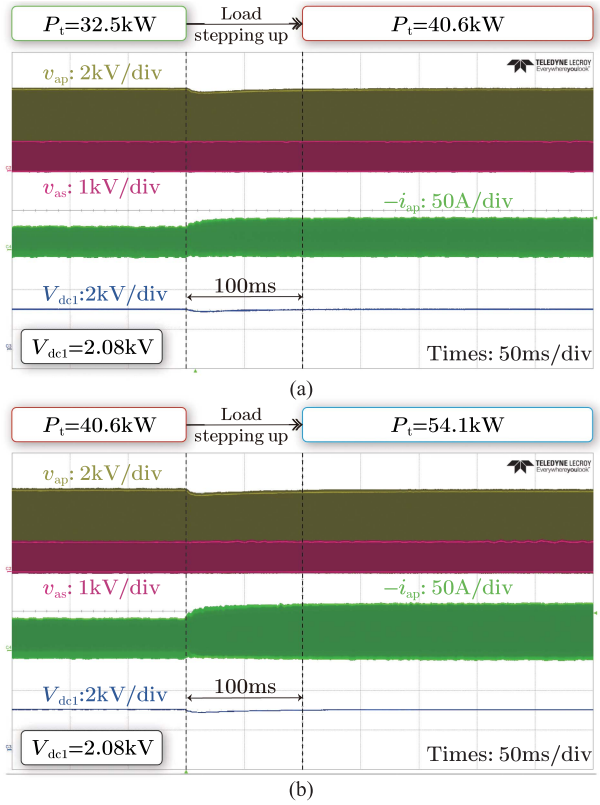

Fig. 20. Load stepping of the compact MMDC under the proposed AQ2L modulation. (a) Transient experimental waveforms for stepping up from $P_{\mathrm{t}} = 32.5$ kW to $P_{\mathrm{t}} = 40.6$ kW at $V_{\mathrm{dc1}} = 2.08$ kV. (b) Transient experimental waveforms for stepping up from $P_{\mathrm{t}} = 40.6$ kW to $P_{\mathrm{t}} = 54.1$ kW at $V_{\mathrm{dc1}} = 2.08$ kV.

MMDC steps up from $P_{\mathrm{t}} = 32.5$ kW to $P_{\mathrm{t}} = 40.6$ kW at $V_{\mathrm{dc1}} = 2.08$ kV, the MV bus voltage V_{dc1} exhibits a slight drop and recovers to the steady state after about 100 ms, showing no current spike. Similarly, the load power steps up from $P_{\mathrm{t}} = 40.6$ kW to $P_{\mathrm{t}} = 54.1$ kW at $V_{\mathrm{dc1}} = 2.08$ kV in Fig. 20(b), where the transient process also has a smooth transition and sustains about 100 ms.

Overall, the abovementioned experimental results confirm the advantages and effectiveness of the proposed AQ2L modulation in saving the number of SMs, realizing ZVS, and improving the power transfer capability.

V. Conclusion

An AQ2L modulation for the compact MMDC is proposed in this article to enable the asymmetrical duty cycle control of SMs. With the proposed AQ2L modulation, the SM capacitor voltage can be flexibly controlled to fulfill the performance requirements under different operating conditions.

As the MV bus voltage is high, the maximum SM capacitor voltage is restricted by the AQ2L modulation at the expense of the moderate increase in SM current stress, thus reducing the required SM number and lowering the converter size. As the MV bus voltage is low, the SM capacitor voltage is boosted to increase the excitation voltage amplitude of the MFT, thus effectively enhancing the power transfer capability of the converter.

In the case study, with the proposed AQ2L modulation, the compact MMDC provides a saving of about 16% in the SM number without increasing the power device current rating, and a smaller SM capacitance is required. Meanwhile, it achieves favorable transferred power flatness over a wide voltage range. Besides, the compact MMDC under the proposed AQ2L modulation exhibits a comparable ZVS region to that under conventional Q2L modulation, but achieves lower power loss since fewer SMs are used, which implies less conduction losses. All the abovementioned enhancements promote the compact MMDC to achieve a smaller size, making it particularly suitable for the applications with a wide voltage range and high space cost.

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