An Optimized Fault-Tolerant Control Strategy Based on Dynamic Modulation Voltage Adjustment for Solid-State Transformers

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***Abstract*—Solid-state transformers (SSTs) have broad application prospects in medium-voltage dc distribution systems. However, the large number of switching devices in SSTs makes it prone to failure. The cascaded structure of SSTs facilitates redundant fault-tolerant control in the event of a failure. Nevertheless, traditional redundancy-based fault-tolerant control methods will lead to current surges when bypassing or inserting a module. In this article, an optimized fault-tolerant control strategy based on modulation voltage correction is proposed. To reduce the voltage and current fluctuations caused by the removal of the faulty module, the new modulation voltage signal is calculated by the bus voltage of the normal operating modules, the bus voltage of the redundant module and the original modulation voltage signal. The principle of dynamic adjustment of modulation voltage is analyzed. Furthermore, during the fault-tolerant shifting process, the control mode is changed to achieve smooth fault-tolerant shifting while ensuring control continuity. The effectiveness of the proposed fault-tolerant control strategy is verified through simulation and experiments.**

***Index Terms*—Fault-tolerant, modulation voltage, solid-state transformers (SSTs).**

I. Introduction

With the integration of distributed power sources, such as photovoltaic and wind power, as well as dc loads like data centers and electric vehicles into the grid, solid-state transformers (SSTs) are increasingly recognized for their capabilities in reactive power compensation, power flow management, harmonic mitigation, and fault protection [1], [2], [3], [4]. Due to constraints posed by the voltage rating of semiconductor power devices, SSTs that convert medium-voltage ac to low-voltage dc typically adopt an input-series output-parallel structure [5], [6], [7], [8].

In a cascaded system like SST, the number of power switching devices used is proportional to the number of modules. Power switching devices are the susceptible components to failure in power electronic devices. Therefore, the probability of switch failure in an SST is much higher than in conventional transformers [9]. Moreover, if a module in an SST fails and is not promptly and properly handled, significant voltage and current fluctuations can easily affect the normal operation of other modules, leading to more module failures and even causing the system breakdown [10], [11]. Hence, designing reliable fault-tolerant control strategies is crucial to ensure the continuous and reliable operation of the power supply system.

Common fault-tolerance strategies mainly include circuit reconfiguration based on fault types and hardware redundancy [12]. Circuit reconfiguration typically involves isolating the faulty switch and modifying the control strategy to allow the remaining portion of the circuit to continue operating [13], [14]. Weng et al. [13] demonstrates fault-tolerant operation by converting a full-bridge converter into a half-bridge converter. Zhao et al. [14] addresses open-circuit faults in H-bridges by continuing operation with the remaining functional H-bridges. However, these methods may lead to a decline in system performance. In contrast, hardware redundancy can ensure effective system operation [15], [16], [17], [18], [19]. Julian and Oriti [15] and de Araujo Ribeiro et al. [16] add a redundant switch in series or parallel with each switch in the circuit. Costa et al. [17], Song and Wang [18], and Restrepo et al. [19] employ a redundant bridge arm strategy, incorporating an additional bridge arm for each H-bridge. However, in cascaded configurations, the cost of redundant components increases with the number of modules.

For modular cascading circuits, a commonly used fault-tolerant approach is to add a redundant module to the system. This allows for bypassing a faulty module in case of failure and replacing it with the redundant module to continue operation. According to the redundant module whether they are operating in normal operation, redundant modules are classified into two types: hot redundancy scheme [3], [20], [21], [22], [23] and cold redundancy scheme [24], [25], [26], [27], [28].

For the hot redundancy scheme, during normal operation, the redundant module runs together with the other modules. When a fault occurs, the faulty module is bypassed, the total number of modules has decreased, sometimes it is needed to raise the bus voltage to avoid the overmodulation. This will increase the voltage stress to the power switches. Moreover, the gain of

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the isolated dc-dc converters in the second stage will change, which will cause it to deviate from the rated operating point. For SSTs with isolated dc-dc converters like *LLC* in the second stage, this hot redundancy scheme will reduce the efficiency of the SST system. [3] discusses a cascaded dc-SST topology with a half-bridge configuration at the first stage. It employs a method of gradually adjusting the duty cycle to disconnect and reconnect modules. However, this method is applicable to the scenario of active shifting, and is not suitable for fault-tolerant control. Song and Huang [20] require increasing the bus voltage of the remaining normal modules after bypassing the faulty module. By increasing the modulation voltage at the shifting moment, current surges are avoided. After the bus voltage of the remaining modules rises to the specified value, the modulation voltage directly returns to the normal value. Maharjan et al. [21] reduce the modulation ratio by injecting zero-sequence voltage after bypassing the faulty module. In [22] and [23], when a submodule fails and is bypassed, the missing voltage levels of the faulty submodule are compensated by other healthy modules in the faulty phase. This method does not require modifying the modulation voltage or phase shift angle.

Unlike the hot redundancy scheme, the cold redundancy scheme keeps the number of active modules unchanged before and after the transition. The bus voltage of the normal operation module is unchanged for the cold redundancy scheme. Therefore, power switches have the same voltage stress without reducing SST efficiency. However, the redundant module must be charged to the rated bus voltage before it can operate normally in place of the faulty module. There will be an input current surge during the charging process. In [24], in the cascaded module with the first stage of cascaded H-bridge (CHB) and the second stage of dual active bridge (DAB), the DAB of the redundant module can reversely charge the bus capacitance of the redundant module during normal operation, thereby reducing the charging time and dynamic adjustment duration. However, this method is not suitable for unidirectional energy transfer circuits. In order to reduce costs, Nie et al. [25] proposed a scheme where a three-phase cascaded system shares a common cold redundant module. Based on this scheme, Tian et al. [26] improved it by pre-charging the redundant module, which results in a shorter shifting time. When the number of faulty modules exceeds the configured redundant modules, Son et al. [27] proposes a novel spare process for modular multilevel converters (MMCs) to handle such emergency situations. In [28], a method is proposed for the MMC that can seamlessly bypass a faulty module and insert a cold redundant module.

There is some other modulation schemes used to handle fault-tolerant operation after bypassing the fault submodules of MMC [29]. A method of injecting zero sequence voltage (ZSV) after bypassing the faulty module was proposed in [30] and [31], this method can avoid the rise of capacitor voltage and the configuration of redundant submodules. In [32] and [33], irregular ZSV injection-based methods are proposed to further balance line-to-line voltages. However, injecting ZSV is not suitable for single-phase systems. In [34] and [35], after bypassing the fault module, use a specific harmonic elimination method to balance the line-to-line voltages and eliminate a wide range of low order harmonics to reduce the total harmonic distortion (THD) of MMC voltage under fault conditions. In [36], a new fault tolerance strategy based on improved space vector modulation technology was proposed to enhance the performance of MMC converters under fault conditions. By using this strategy, the faulty submodule can be directly bypassed without bypassing submodules in the other two phases, and MMC can also generate balanced line-to-line voltages. In [37], by injecting third harmonic, the utilization rate of bus voltage can be improved, this method also only requires bypassing the faulty submodule of the faulty phase without bypassing the submodules of the other phases, although the phase voltages of the inverter are unbalanced, this method can maximize the balance of the line-to-line voltages. In single-phase systems, the method of injecting third harmonic modulation wave is not suitable.

In addition, there are several other fault-tolerant methods. Moradi et al. [38] adopt a fault-tolerant method using a hardware circuit. After bypassing the faulty bridge arm, an auxiliary circuit is inserted into the system to maintain its normal operation. Zhu et al. [39] proposes a fault-tolerant control strategy based on the Vienna SST system, which allows the faulty module to continue operating while ensuring three-phase balance and voltage stability in the system.

To reduce current surges during the transition from a faulty module to a redundant module, this article proposes a dynamic modulation control strategy. It is based on the idea of detecting the bus voltage of each module and feeding back to modify the modulation voltage. During the period between bypassing the faulty module and fully charging the bus capacitor of the redundant module, a computed gain is applied to the modulation voltage of the normal operational modules. The gain is dynamically adjusted according to the changes in the redundant module bus voltage to keep the grid-side inductor voltage stable, and the control mode is changed during the fault-tolerant shifting, the input current surge is suppressed to ensure smooth fault-tolerant shifting (i.e., bypassing, insertion).

The rest of this article is organized as follows. Section II analyzes the current surge when bypassing the faulty module. Section III describes the proposed fault-tolerant control strategy that dynamically adjusts the modulation voltage. Section IV analyzes the proposed fault-tolerant control strategy. Section V validates the proposed fault-tolerant control strategy through experiments. Finally, Section VI concludes this article.

II. Circuit Analysis When Bypassing the Faulty Module

In the conventional cold redundancy scheme, when the faulty module is bypassed, it will cause a sudden increase in the input inductor voltage, which will cause a surge in the input current.

To explore methods for reducing current surge during fault-tolerant shifting, it is essential to analyze the circuit working status when bypassing the faulty module. The SST with three modules and a redundant module, where each module is configured with an H-bridge circuit at the first stage and a unidirectional *LLC* circuit at the second stage. It is worth

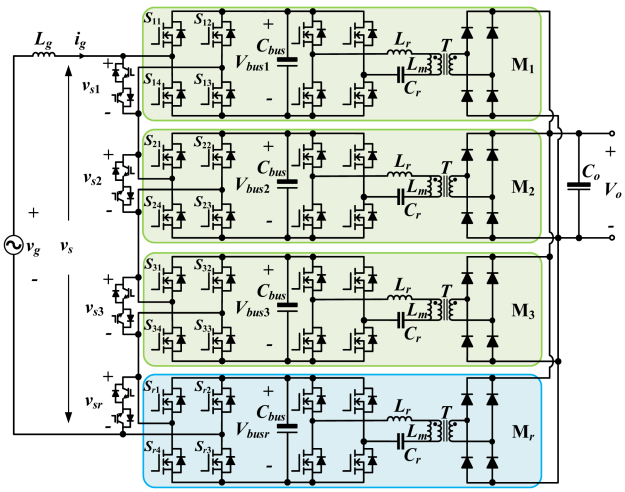

Fig. 1. Circuit structure diagram.

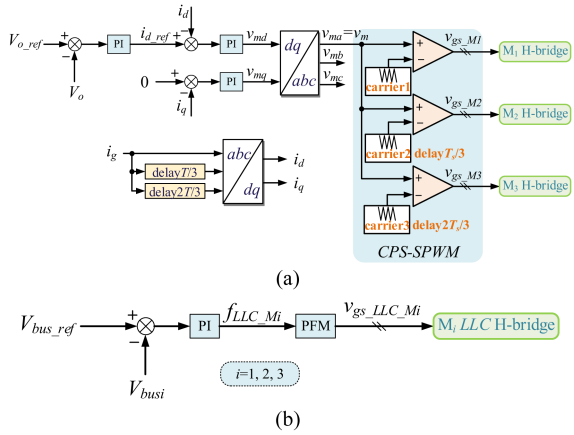

Fig. 2. Conventional SST control system diagram under normal operation conditions. (a) Diagram of the CHB control system. (b) Diagram of the *LLC* control system.

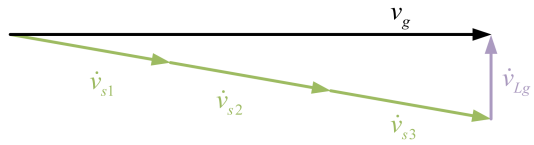

Fig. 3. Phasor diagram of the input voltage vectors under normal operating conditions.

mentioning that the application scenarios of unidirectional SST include electric vehicle charging stations and data centers.

In Fig. 1, M_1, M_2, and M_3 represent the three normal operating modules, and M_r denotes the redundant module. During normal operation, the modules M_1, M_2, M_3 are active, and redundant module M_r is bypassed on the input side. The parameters are defined as follows: v_g and i_g represent the grid voltage and current, respectively, V_o is the output voltage, v_{si} $(i = 1, 2, 3, r)$ denotes the input voltage of each module; v_s is the total input voltage of all modules, $V_{\text{bus}i}$ $(i = 1, 2, 3, r)$ represents the bus voltage of each module, L_g is the grid-side inductor, C_{bus} is the bus capacitor, L_r is the resonant inductance, C_r is the resonant capacitor, L_m is the magnetizing inductance, C_o is the output capacitor, T is the transformer turn ratio, and S_{ij} $(i = 1, 2, 3, r; j = 1, 2, 3, 4)$ denotes the switches in the H-bridge of each module's first stage.

A. Normal Operating Conditions

During normal operation, modules M_1, M_2, and M_3 are active, while the input side of the redundant module is bypassed by the insulated gate bipolar transistors (IGBTs). At this time, the control block diagrams for the system's first stage and second stage are shown in Fig. 2, where v_{gs_Mi} and $v_{gs\_\text{LLC}\_Mi}$ represent the drive signals for the first and second stages of the H-bridge in modules M_i $(i = 1, 2, 3)$, respectively.

Fig. 2(a) depicts the diagram for the CHB control system. The CHB controller utilizes a dual-loop control strategy, incorporating an outer voltage control loop and an inner current control loop. The outer loop regulates the output voltage V_o, while the inner loop manages the input current i_g, with the output of the outer loop i_{d_ref} serving as the reference for the d-axis component i_d of the current in the inner loop. The modulation scheme employed by the CHB controller is carrier phase-shifted sinusoidal pulse width modulation (CPS-SPWM), in which the modulation waves for each module are identical, but the carrier waves are phase-shifted relative to one another. Fig. 2(b) presents the *LLC* control system diagram for each module. Each module's bus voltage is controlled by an *LLC* controller, which operates using pulse frequency modulation. This technique adjusts the gain by varying the operating frequency of the *LLC* stage, thereby ensuring the stability of the module's bus voltage.

Fig. 3 illustrates the phasor diagram of the voltage vectors on the input side under normal operating conditions, where v_{Lg} represents the grid-side inductor voltage.

Based on the phasor diagram presented in Fig. 3, the phasor representation of the grid-side inductor voltage v_{Lg} for each module under normal operating conditions can be expressed as

$$\dot{v}_{Lg} = \dot{v}_g - \dot{v}_s = \dot{v}_g - (\dot{v}_{s1} + \dot{v}_{s2} + \dot{v}_{s3}). \tag{1}$$

B. Transient Analysis of Faulty Module Removal

The conventional SST control system diagram under fault operation conditions is shown in Fig. 4. The overall control loop remains consistent with normal operation. However, the drive signal v_{gs_M3} is redirected to the H-bridge of the first stage of redundant module. The second stage of redundant module, similar to other modules, continues to regulate its own bus voltage $V_{\text{bus}r}$.

The phasor diagram of the input side at this moment can be depicted as shown in Fig. 5. When module M_3 has been bypassed, it results in its input voltage v_{s3} being zero. Since the redundant module has just been inserted into the system, its bus capacitor has not yet begun charging, therefore it does not contribute to the input-side voltage v_s. Assuming the grid voltage v_g remains unaffected by external factors and remains constant and considering that the bus voltages $V_{\text{bus}1}$ and $V_{\text{bus}2}$ of modules M_1 and M_2 will not exhibit abrupt changes due to the presence of bus capacitors.

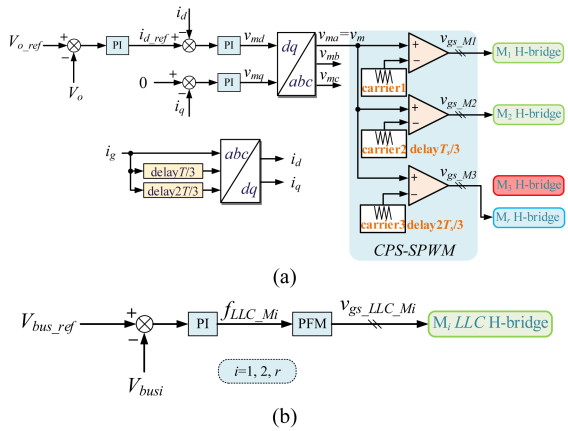

Fig. 4. The conventional SST control system diagram under fault operation conditions. (a) Diagram of the CHB control system. (b) Diagram of the *LLC* control system.

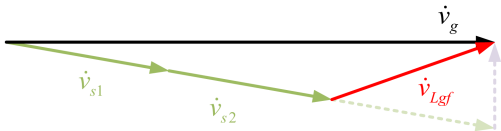

Fig. 5. Phasor diagram of the input side at the instant of faulty module removal.

Under these conditions, the phasor of the grid-side inductor voltage v_{Lgf} for all modules can be expressed as

$$\dot{v}_{Lgf} = \dot{v}_g - \dot{v}_s = \dot{v}_g - (\dot{v}_{s1} + \dot{v}_{s2}) . \tag{2}$$

By comparing (1) with (2) as well as Fig. 3 with Fig. 5, it is evident that the voltage previously borne by module M_3 is entirely transferred to the inductor at the moment of the fault. This results in a sudden increase in the inductor voltage. The change of inductor voltage Δv_{Lg} is

$$\Delta v_{Lg} = v_{Lgf} - v_{Lg} = \omega_g L_g i_{gf} - \omega_g L_g i_g = \omega_g L_g \Delta i_g \tag{3}$$

where ω_g is the angular frequency of the grid voltage, i_{gf} is the instantaneous input current of the bypass faulty module, Δi_g is the change in input current after bypassing the faulty module.

It can be seen from (3) that a sudden increase Δv_{Lg} in the inductor voltage will result in a sudden increase Δi_g in the input current. In the SST system, since the input current is the same across all modules, such a sudden change in current can affect normally operating modules and potentially cause damage to additional modules. Therefore, it is necessary to improve the control strategy during the shift process to ensure system stability.

III. Proposed Fault-Tolerant Control Strategy

To reduce the current stress in the conventional fault-tolerant control strategy when bypassing the faulty module and inserting the redundant module, this section studies an optimized fault-tolerant control strategy, which dynamically adjusts the modulation voltage v_{mn} according to the bus voltage $V_{\text{bus}i}$ ($i = 1, 2, r$) of each module and the original modulation voltage v_m. Therefore, the fluctuation of the input voltage can be reduced, thereby avoiding input current surge.

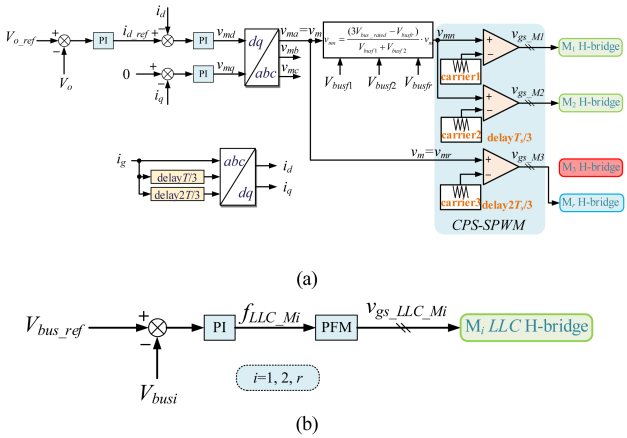

Fig. 6. Proposed SST control system diagram under fault operation conditions. (a) Diagram of the CHB control system. (b) Diagram of the *LLC* control system.

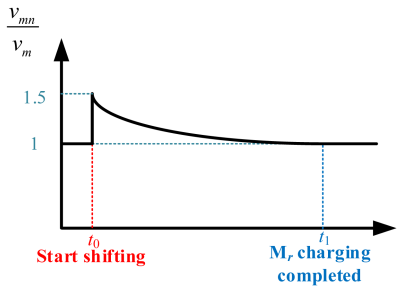

Fig. 7. Variation curve of the v_{mn} / v_m ratio during the fault-tolerant control shifting process.

A. Fault-Tolerant Control Strategy

The optimized control system diagram of SST using the dynamic voltage adjustment scheme studied in this article during the process of shifting is shown in Fig. 6. Compared with the control system diagram in Fig. 4, the main difference lies in the modulation part. In Fig. 6, on the basis of the modulation voltage v_m calculated by the control loop, the optimized fault-tolerant strategy adjusts the modulation voltage actually given to modules M_1, M_2 and redundant module. The modulation voltage v_{mr} of redundant module M_r remains unchanged, while the modulation voltage v_{mn} of module M_1 and module M_2 is calculated by the dc bus voltage $V_{\text{bus}i}$ ($i = 1, 2, r$) of each module and v_m.

The ratio between the modulation voltage v_{mn} and the modulation voltage v_m is shown in Fig. 7. In order to compensate for the voltage loss caused by the faulty module being bypassed, the modulation voltage v_{mn} of the normally operating modules M_1 and M_2 increases suddenly after the shifting. After time t_0, the bus capacitor of the redundant module is charged, the value of v_{mn} gradually decreases until the bus capacitor of the redundant module is fully charged and the value of v_{mn} returns to be equal to v_m.

B. Improved Fault-Tolerant Control Strategy

Based on the proposed control method, some further improvements have been made to reduce the fluctuations in the

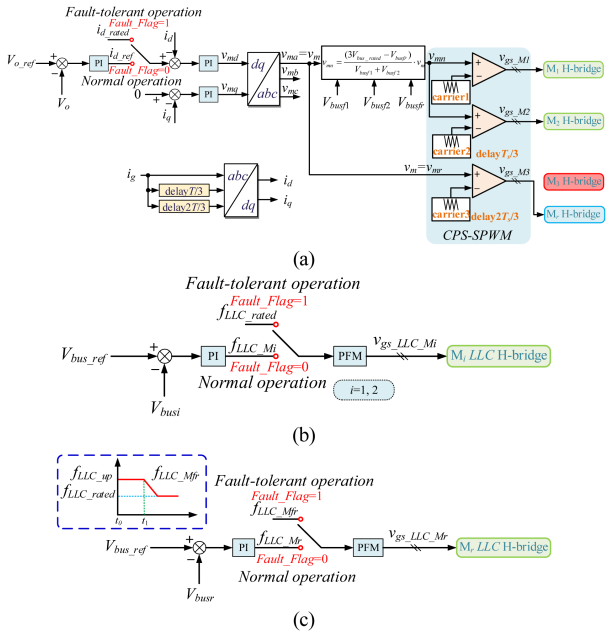

Fig. 8. SST control system diagram after further improvement of the proposed control method under fault operation conditions. (a) Diagram of the CHB control system. (b) *LLC* control system diagram for healthy modules. (c) *LLC* control system diagram for redundant module.

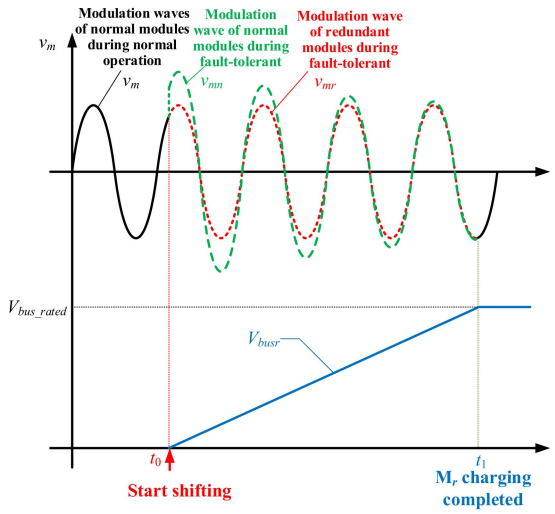

Fig. 9. Variation curves of each module's modulation voltage waveforms during the fault-tolerant control process.

input current i_g and effectively prevent the overshoot of redundant module's bus voltage V_{busr} during the shifting process, thus achieving a smooth fault-tolerant shifting. The proposed fault-tolerant control system diagram is shown in Fig. 6, while the further improved fault-tolerant control system diagram is illustrated in Fig. 8. As shown in Fig. 8(a), compared with the fault-tolerant control strategy in Fig. 6(a), at the beginning of the fault-tolerant shifting, the Fault_Flag is set from 0 to 1, the first stage CHB controller changes from the original dual-loop control mode (output voltage outer loop and input current inner loop) to a single-loop control mode using only the input current. Applying a single current loop to control the input current during the fault-tolerant shifting can significantly reduce the surge of input current. It is worth noting that the reference value i_{d_rated} of the current loop is set to the current reference value i_{d_ref} calculated by the output voltage loop at the moment before shifting. When the fault-tolerant shifting is completed, the Fault_Flag is set from 1 to 0, the control mode changes to dual loop mode, the parameter values of the voltage loop PI controller are assigned to their values at the moment before shifting. Additionally, for the second stage *LLC* controllers, their switching frequency f_{LLC_Mi} experiences an upward transient overshoot during the shifting process, especially in the redundant module, the switching frequency f_{LLC_Mfr} may reach its upper limit. Therefore, as shown in Fig. 8(b) and (c), at the beginning of fault-tolerant shifting, set the Fault_Flag to 1, all second-stage *LLC* controllers are adjusted to operate in an open-loop fixed-frequency mode. Specifically, in Fig. 8(b), the healthy modules M_1 and M_2 maintain the rated switching frequency $f_{\mathrm{LLC\_rated}}$ throughout the shifting process. In Fig. 8(c), the redundant module M_r starts with a higher switching frequency f_{LLC_up} and operates at this higher value until its bus voltage V_{busr} reaches the rated level, after which the frequency f_{LLC_Mfr} gradually decreases linearly back to the rated value required for normal operation. Finally, after the system returns to normal operation, the Fault_Flag is set from 1 to 0, all LLC controllers revert to closed-loop control mode.

C. Analysis of SST Fault-Tolerant Shifting Process

Fig. 9 shows each module's modulation voltage waveforms during the fault-tolerant control shifting process.

The following result shown in Fig. 9.

1) Before time t_0, the system operates normally. Since the CHB controller uses CPS-SPWM modulation, all modules have identical sinusoidal modulation signals before shifting.
2) After detecting the fault at time t_0, the modulation voltage v_{mr} of the newly activated redundant module is the same as the normal operating modulation voltage v_m. To compensate for the input voltage originally handled by the faulty module M_3, the modulation voltage v_{mn} of the normal modules M_1 and M_2 is adjusted according to the proposed control strategy.
3) Between time t_0 and t_1, the bus capacitor of the redundant module is charged, the modulation voltage v_{mn} of modules M_1 and M_2 gradually decreases and finally returns to its normal value v_m. This is because the contribution of the redundant module to the input voltage v_s gradually increases, and the additional input voltage borne by modules M_1 and M_2 decreases, so their modulation voltage needs to be reduced.

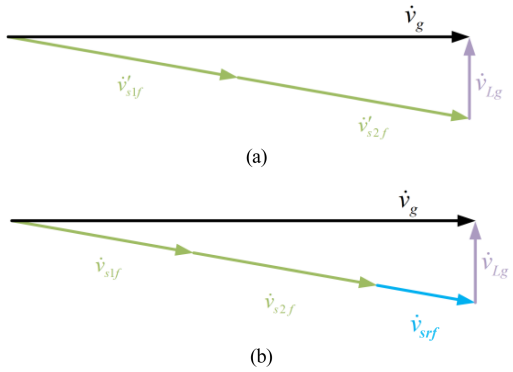

Fig. 10. Phasor diagrams of the input side under ideal conditions during the shifting process. (a) Moment of faulty module removal. (b) During the charging process of the redundant module.

4) After time t_1, all modules' modulation voltages return to their normal operating value v_m. The redundant module charging is complete, and it fully replaces the faulty module.

IV. Analysis of Proposed Fault-Tolerant Control Strategy

A. Analysis of Circuit State During SST Shifting Process

In order to reduce the current stress during the shifting process, the voltage v_{Lg} on inductor L_g should be same as before the shifting, the phasor diagram of the inductor voltage v_{Lg}, the grid voltage v_g, each module's input voltage v'_{sif} ($i = 1, 2, r$) at the moment of faulty module removal and each module's input voltage v_{sif} ($i = 1, 2, r$) during the charging process of the redundant module is shown in Fig. 10. Fig. 10(a) is the phasor diagram at the moment of faulty module removal, Fig. 10(b) is the phasor diagram during the charging process of the redundant module.

Based on Fig. 10(a), the phasor expressions for the inductor voltage v_{Lg}, the grid voltage v_g and each module's input voltage v'_{sif} ($i = 1, 2, r$) at the moment of faulty module removal can be derived as follows:

$$\dot{v}'_{s1f} + \dot{v}'_{s2f} = \dot{v}_g - \dot{v}_{Lg}. \tag{4}$$

Based on Fig. 10(b), the expressions for the inductor voltage v_{Lg}, the grid voltage v_g and each module's input voltage v_{sif} ($i = 1, 2, r$) during the charging process of the redundant module are as follows:

$$\dot{v}_{s1f} + \dot{v}_{s2f} + \dot{v}_{srf} = \dot{v}_g - \dot{v}_{Lg}. \tag{5}$$

Rewrite the input phasor expression under normal operating conditions (1) as follows:

$$\dot{v}_{s1} + \dot{v}_{s2} + \dot{v}_{s3} = \dot{v}_g - \dot{v}_{Lg}. \tag{6}$$

Substitute (6) into (4) and (5), respectively,

$$\dot{v}'_{s1f} + \dot{v}'_{s2f} = \dot{v}_{s1} + \dot{v}_{s2} + \dot{v}_{s3} \tag{7}$$

$$\dot{v}_{s1f} + \dot{v}_{s2f} + \dot{v}_{srf} = \dot{v}_{s1} + \dot{v}_{s2} + \dot{v}_{s3}. \tag{8}$$

Since the voltage directions of all modules are the same during normal operation and fault-tolerant control, (7) and (8) can be expressed in scalar form as follows:

$$v'_{s1f} + v'_{s2f} = v_{s1} + v_{s2} + v_{s3} \tag{9}$$

$$v_{s1f} + v_{s2f} + v_{srf} = v_{s1} + v_{s2} + v_{s3}. \tag{10}$$

Equation (9) can be considered as a special case of (10) where the redundant module input voltage v_{srf} is zero. Therefore, the situations of faulty module removal and redundant module charging can be treated uniformly. Taking the switch cycle average of both sides of (10) yields

$$\begin{aligned} &< v_{s1f} >_{Ts} + < v_{s2f} >_{Ts} + < v_{srf} >_{Ts} \\ &=< v_{s1} >_{Ts} + < v_{s2} >_{Ts} + < v_{s3} >_{Ts}. \end{aligned} \tag{11}$$

Taking M_1 as a case study. The relationship between the input voltage v_{s1} and the bus voltage V_{bus1} is derived as follows.

Firstly, the input voltage v_{s1} under various switching states can be expressed as

$$v_{s1} = \begin{cases} V_{\text{bus1}},\ S_{11},\ S_{13} \text{ on} \\ -V_{\text{bus1}},\ S_{12},\ S_{14} \text{ on} \end{cases}. \tag{12}$$

Assuming the duty cycle of S_{11} is D, (12) can be expressed as

$$v_{s1} = \begin{cases} V_{\text{bus1}},\ DT_s \\ -V_{\text{bus1}},\ (1-D)T_s \end{cases} \tag{13}$$

where T_s denotes the switching period.

Taking the average of (13) over the switching period T_s

$$\begin{aligned} < v_{s1} >_{Ts} &= V_{\text{bus1}} \cdot D + (-V_{\text{bus1}}) \\ &\quad \cdot (1-D) = V_{\text{bus1}}(2D-1). \end{aligned} \tag{14}$$

Assuming the amplitude of the modulation wave remains approximately constant within a switching period, the duty cycle can be expressed as follows according to [40]

$$D = \frac{v_m + V_{\text{tri}}}{2V_{\text{tri}}} \tag{15}$$

where v_m represents the amplitude of the modulation wave, and V_{tri} denotes the amplitude of the triangular carrier wave.

Substituting (15) into (14)

$$< v_{s1} >_{Ts} = V_{\text{bus1}} \frac{v_m}{V_{\text{tri}}}. \tag{16}$$

If the amplitude of the carrier wave V_{tri} is normalized to 1, (16) can be simplified to

$$< v_{s1} >_{Ts} = V_{\text{bus1}} \cdot v_m. \tag{17}$$

Similar to the derivation of (17), the relationship between each module's input voltage v_{sif}($i = 1, 2, 3, r$), modulation voltage v_{mfi}($i = 1, 2, 3, r$), and bus voltage $V_{\text{bus}fi}$($i = 1, 2, 3, r$) during

the shifting process are as follows:

$$\begin{cases} < v_{s1f} >_{Ts} = V_{\text{bus}f1} \cdot v_{mf1} \\ < v_{s2f} >_{Ts} = V_{\text{bus}f2} \cdot v_{mf2} \\ < v_{s3f} >_{Ts} = V_{\text{bus}f3} \cdot v_{mf3} \\ < v_{srf} >_{Ts} = V_{\text{bus}fr} \cdot v_{mfr} \end{cases}. \tag{18}$$

Substituting (18) into (11)

$$\begin{aligned} &V_{\text{bus}f1} \cdot v_{mf1} + V_{\text{bus}f2} \cdot v_{mf2} + V_{\text{bus}fr} \cdot v_{mfr} \\ &\quad = (V_{\text{bus}1} + V_{\text{bus}2} + V_{\text{bus}3}) \cdot v_m \end{aligned} \tag{19}$$

where $V_{\text{bus}i}(i = 1, 2, r)$ and v_m are the bus voltage of each module and the modulation voltage of the first-stage H-bridge, respectively, under normal operating conditions.

As the bus voltage $V_{\text{bus}i}(i = 1, 2, 3, r)$ is controlled by the second-stage *LLC* controller and remains nearly constant at the rated value under normal operating conditions, it can be treated as a constant. Thus, (19) can be expressed as follows:

$$\begin{aligned} &V_{\text{bus}f1} \cdot v_{mf1} + V_{\text{bus}f2} \cdot v_{mf2} + V_{\text{bus}fr} \cdot v_{mfr} \\ &\quad = 3V_{\text{bus\_rated}} \cdot v_m \end{aligned} \tag{20}$$

where $V_{\text{bus\_rated}}$ is the rated bus voltage for each module.

Therefore, based on the above analysis, the objective of fault-tolerant control can be seen as adjusting the modulation voltage $v_{mfi}(i = 1, 2, r)$ of each module to maintain the validity of (20) despite variations in the bus voltage $V_{\text{bus}fr}$ of the redundant module.

B. Optimized Scheme for Dynamically Adjusting Modulation Voltage

In (20), the only variable affected by external factors is the bus voltage $V_{\text{bus}fr}$, which increases as the redundant module charges. The controllable variables are the modulation waves $v_{mfi}(i = 1, 2, r)$. To simplify calculations, some constraints on the modulation waves can be introduced, such as

$$\begin{cases} v_{mf1} = v_{mf2} = v_{mn} \\ v_{mfr} = v_m \end{cases}. \tag{21}$$

Set the modulation voltage v_{mfr} of the charging redundant module to its nominal value v_m. Ensure that the modulation voltages of modules M_1 and M_2 are both v_{mn}. Therefore, only v_{mn} needs to be determined.

Substituting (21) into (20)

$$(V_{\text{bus}f1} + V_{\text{bus}f2}) \cdot v_{mn} + V_{\text{bus}fr} \cdot v_m = 3V_{\text{bus\_rated}} \cdot v_m. \tag{22}$$

From (22), the expression for the modulation voltage v_{mn} can be derived as follows:

$$v_{mn} = \frac{(3V_{\text{bus\_rated}} - V_{\text{bus}fr})}{V_{\text{bus}f1} + V_{\text{bus}f2}} \cdot v_m \tag{23}$$

where $V_{\text{bus}fr}$ is the bus voltage of the redundant module, varying with its charging during fault-tolerant shifting, $V_{\text{bus}f1}$ and $V_{\text{bus}f2}$ are the bus voltages of normally operating modules M_1 and M_2, respectively, $V_{\text{bus\_rated}}$ is the rated bus voltage, and v_m is the modulation voltage calculated by the normal control loop.

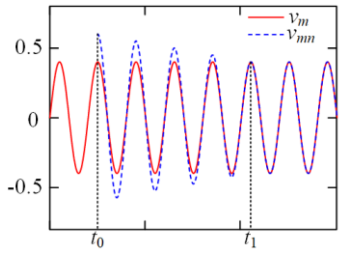

Fig. 11. Waveform of the modulation voltage during the fault-tolerant shifting period.

The waveform of the modulation voltage during the fault-tolerant shifting period, which is derived from (23), is shown in Fig. 11. t_0 indicates the start of shifting, and at the same time, the redundant module starts charging, t_1 indicates that the redundant module is fully charged, and the charging time of the redundant module is related to the control speed and the capacitance value of the bus capacitor.

C. Situation of N Modules

The above analysis is based on a system with three modules in cascade and one redundant module. The optimal fault-tolerant control scheme studied in this article is also applicable to the case of multiple modules. Therefore, the above conclusions will be extended to the case of *N* modules.

Consider a system consisting of N modules $(M_1, M_2, \ldots M_N)$ cascaded with a redundant module. During normal operation, the redundant module is bypassed. Assuming that a module M_F in SST is bypassed due to a fault, insert the redundant module into SST operation and charge it until the bus capacitor voltage of the redundant module stabilizes at the rated value.

Similar to the previous derivations, let the modulation voltage of the redundant module be equal to the modulation wave v_m during normal operation, and set the modulation voltage of the *N*-1 modules in normal operation to v_{mn}. Under these conditions, the relationship among the variable v_{mn}, the bus voltage $V_{\text{bus}fi}(i = 1, 2, \ldots N, r)$ of each module during fault-tolerant control, and the modulation voltage v_m during normal operation are as follows:

$$v_{mn} = \frac{N \cdot V_{\text{bus\_rated}} - V_{\text{bus}fr}}{\sum_{\substack{i=1 \\ i \neq F}}^{N} V_{\text{bus}fi}} \cdot v_m. \tag{24}$$

Therefore, during the fault-tolerant shifting process, by keeping the modulation voltage of the redundant module unchanged and dynamically adjusting the modulation voltages of the remaining *N*-1 modules according to (24), a smooth shift in the SST fault-tolerant control process can be achieved.

Typically, the capacitance of the bus capacitor in each module is large, and with the effect of the second-stage *LLC* controller, the variation in the bus voltage $V_{\text{bus}fi}(i = 1, 2, \ldots N, i \neq F)$ of each normal module during fault-tolerant shifting is relatively small. Therefore, it can be approximated as the rated value $V_{\text{bus\_rated}}$.

Consequently, (24) can be written as

$$\frac{v_{mn}}{v_m} = \frac{N \cdot V_{\text{bus\_rated}} - V_{\text{bus}fr}}{(N-1) \cdot V_{\text{bus\_rated}}}. \tag{25}$$

According to (25), the ratio of v_{mn} to the normal modulation wave v_m decreases as $V_{\text{bus}fr}$ increases during fault-tolerant control. As the redundant module charges, v_{mn} gradually approaches to v_m under normal conditions. Thus, at the moment of shifting, when $V_{\text{bus}fr}$ is zero, the ratio of v_{mn} to v_m is at its maximum, which is

$$\frac{v_{mn}}{v_m} = \frac{N}{N-1}. \tag{26}$$

From (26), it can be seen that the magnitude of the modulation voltage v_{mn} at the moment of shifting depends on the number of cascaded modules N during normal operation, and decreases as N increases. In other words, with more cascaded modules, the increase of v_{mn} is smaller during the fault-tolerant control process, whereas with fewer modules, the increase of v_{mn} is larger, which may lead to overmodulation issues. Therefore, when designing an SST with fewer cascaded modules, it is essential to provide a larger margin for the modulation ratio.

D. Comparison Between the Proposed Fault-Tolerant Control Strategy and the Improved Fault-Tolerant Control Strategy Through Simulation

To quantitatively assess the effectiveness of the improved fault-tolerant control strategy, the fluctuations in input current and the bus voltage of redundant module were compared between direct shifting strategy, the proposed fault-tolerant control strategy and the improved fault-tolerant control strategy.

Since the input current is ac, its fluctuation is represented by the difference ΔI_{pp} between its peak-to-peak value I_{ppf} during the fault-tolerant shifting process and its peak-to-peak value I_{ppn} during normal operation. For the bus voltage of redundant module M_r, the fluctuation is represented by the difference $\Delta V_{\text{bus}r}$ between its maximum value $V_{\text{bus}r\_\max}$ and its rated value $V_{\text{bus\_rated}}$ during the fault-tolerant shifting process

$$\begin{aligned} \Delta I_{pp} &= I_{ppf} - I_{ppn} \\ \Delta V_{\text{bus}r} &= V_{\text{bus}r\_\max} - V_{\text{bus}r\_\text{rated}}. \end{aligned} \tag{27}$$

The comparison of simulation results between direct shifting, proposed fault-tolerant strategy, and further improved fault-tolerant strategy are shown in Fig. 12. In Fig. 12(a), with direct shifting, the input current fluctuation ΔI_{pp} is 17.55 A, and the fluctuation $\Delta V_{\text{bus}r}$ of the bus voltage of the redundant module relative to the rated value is 25.12 V. In Fig. 12(b), with applying the proposed fault-tolerant control strategy, the input current fluctuation ΔI_{pp} is 15.54 A, and the redundant module bus voltage fluctuation $\Delta V_{\text{bus}r}$ is 26.85 V. In Fig. 12(c), with applying the further improved fault-tolerant control strategy, the input current fluctuation ΔI_{pp} is 4.92A, and the redundant module bus voltage fluctuation $\Delta V_{\text{bus}r}$ is 5.24 V. Therefore, after adopting the improved fault-tolerant strategy, the fluctuations of input current and the redundant module bus voltage are significantly reduced, and smooth shifting is basically achieved.

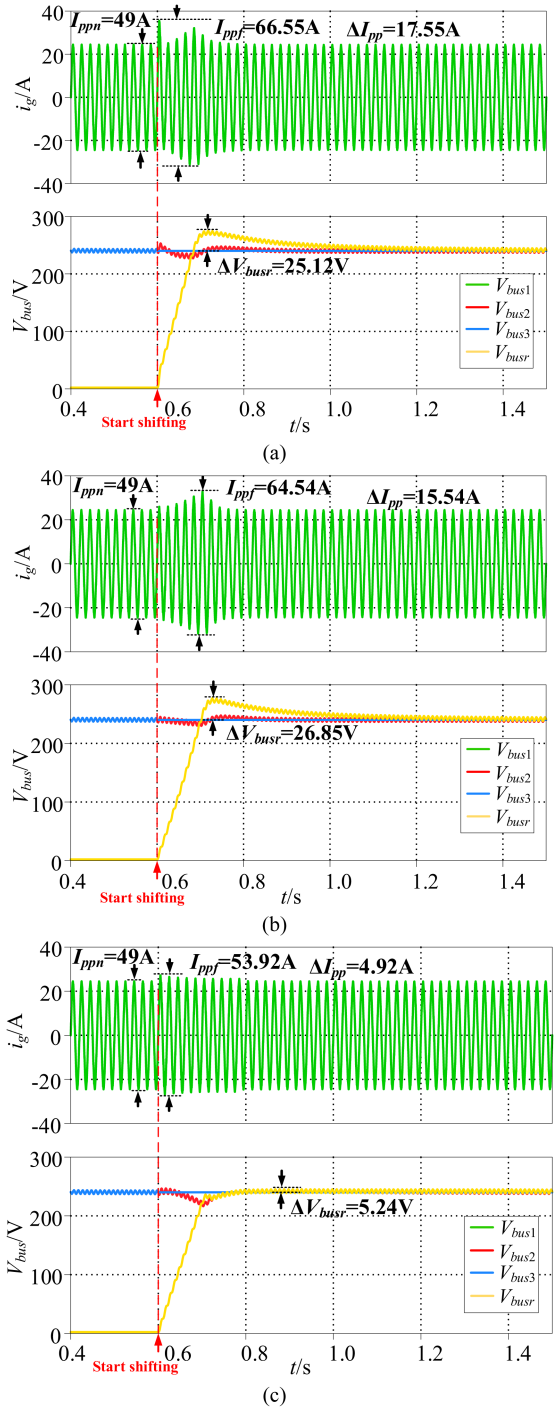

Fig. 12. Comparison of simulated waveforms. (a) Direct shifting. (b) Proposed fault-tolerant control strategy. (c) Improved fault-tolerant control strategy.

E. The Simulation Verification Under N = 4

To demonstrate the scalability of the proposed method with a larger number of modules, simulation verification of the improved method was conducted with the number of modules N set to 4. The simulation results are shown in Fig. 13.

As can be seen from Fig. 13, the input current fluctuation ΔI_{pp} is 2.39 A, and the redundant module bus voltage fluctuation $\Delta V_{\text{bus}r}$ is 4.5 V. The proposed method remains effective even

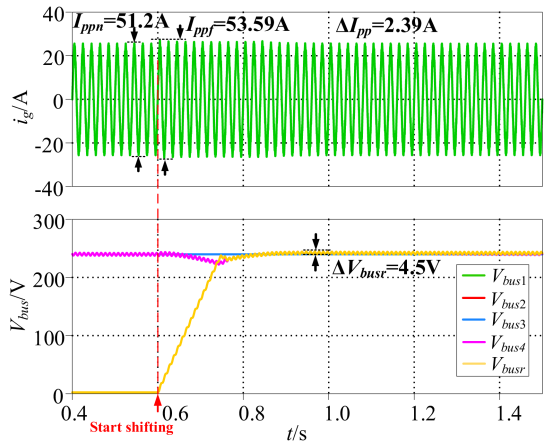

Fig. 13. Simulation verification results of the proposed improved method under the condition of the number of modules N is 4.

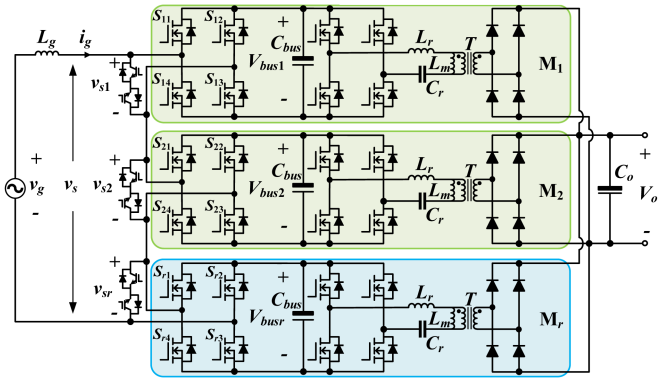

Fig. 14. Hardware prototype circuit diagram.

when the number of modules is increased, which demonstrates its scalability. Moreover, when there are more modules, the current and voltage fluctuations generated during the shifting process are smaller.

V. Experimental Verification

To validate the effectiveness of the optimized fault-tolerant control strategy proposed in this article under actual operating conditions, a hardware prototype was constructed, consisting of two cascaded modules and one redundant module. The circuit diagram of the prototype is shown in Fig. 14, and the circuit parameters are given in Table I. The photo of the experimental prototype is shown in Fig. 15. It is assumed that the fault occurs in module M_2.

Faults occurring at different input current positions within a power frequency cycle can affect the SST differently. To explore these effects, experiments were conducted with faults occurring at the peak current, at half of the peak current, and at the zero-crossing point. Each scenario impacts the SST circuit's voltages and currents in distinct ways. Fault-tolerant shifting experiments were performed under these conditions to validate the effectiveness of the optimized fault-tolerant control strategy proposed in this article.

TABLE I
Parameters of Solid-State-Transformer

Items	Descriptions	Specifications
v_g	Grid voltage	100Vrms / 50Hz
V_{bus}	Bus voltage	120V
V_o	Output voltage	120V
L_g	Grid inductance	415μH
C_{bus}	Bus capacitor	2.45mF
C_o	Output capacitor	24μF
C_r	Resonant capacitor	297.1nF
L_r	Resonant inductance	34.3μH
L_m	Magnetizing inductance	623.8μH
T	Turn ratio	1:1

Fig. 15. Photograph of the three-module SST prototype.

The experimental results are shown in Figs. 16, 17 and 18, respectively.

Fig. 16 shows the experimental comparison results for shifting at the current zero-crossing point. In Fig. 16(a), with direct shifting, the input current fluctuation ΔI_{pp} is 20.6 A and the output voltage fluctuation ΔV_o is 34.8 V. In Fig. 16(b), after applying the optimized fault-tolerant control strategy, the input current fluctuation ΔI_{pp} and the output voltage fluctuation ΔV_o are reduced to 14.6 A and 23.2 V, respectively. Fig. 17 shows the experimental comparison results for shifting at half of the peak current. In Fig. 17(a), with direct shifting, the input current fluctuation ΔI_{pp} is 20.4 A and the output voltage fluctuation ΔV_o is 34.4 V. In Fig. 17(b), after applying the optimized fault-tolerant control strategy, the input current fluctuation ΔI_{pp} and the output voltage fluctuation ΔV_o are reduced to 14.8 A and 23.6 V, respectively. Fig. 18 shows the experimental comparison results for shifting at the peak current. In Fig. 18(a), with direct shifting, the input current fluctuation ΔI_{pp} is 21.8A and the output voltage fluctuation ΔV_o is 31.4 V. In Fig. 18(b), after applying the optimized fault-tolerant control strategy, the input current fluctuation ΔI_{pp} and the output voltage fluctuation ΔV_o are reduced to 15.3 A and 22.8 V, respectively.

Based on the above analysis, there is an instantaneous surge in input current during direct shifting in all three cases. As shown in Fig. 18(a), shifting at peak current results in a surge that nearly doubles the normal operating current amplitude, which could

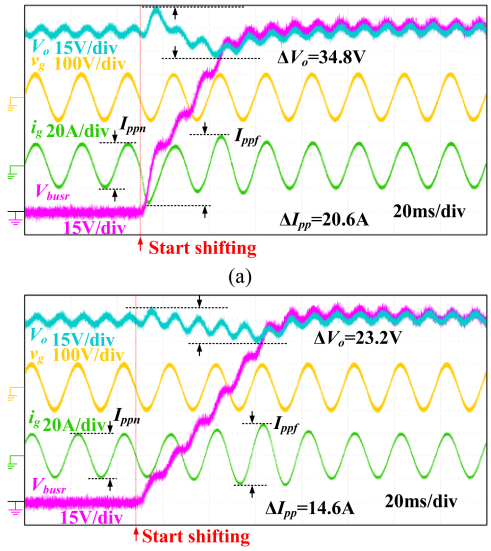

Fig. 16. Comparison of experimental results for shifting at the current zero-crossing point. (a) Direct shifting. (b) Optimized fault-tolerant control strategy.

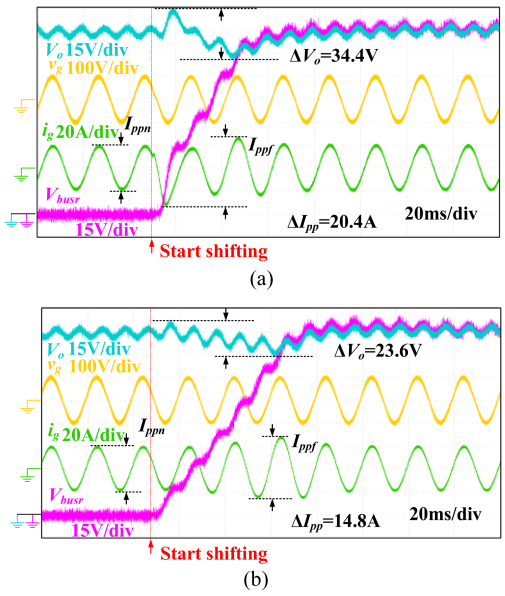

Fig. 17. Comparison of experimental results for shifting at half of the peak current. (a) Direct shifting. (b) Optimized fault-tolerant control strategy.

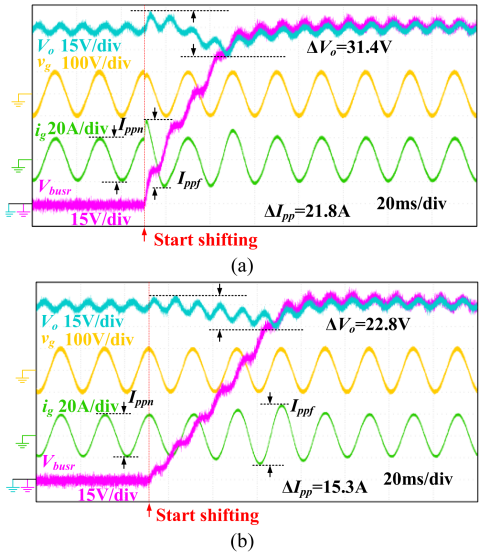

Fig. 18. Comparison of experimental results for shifting at the peak current. (a) Direct shifting. (b) Optimized fault-tolerant control strategy.

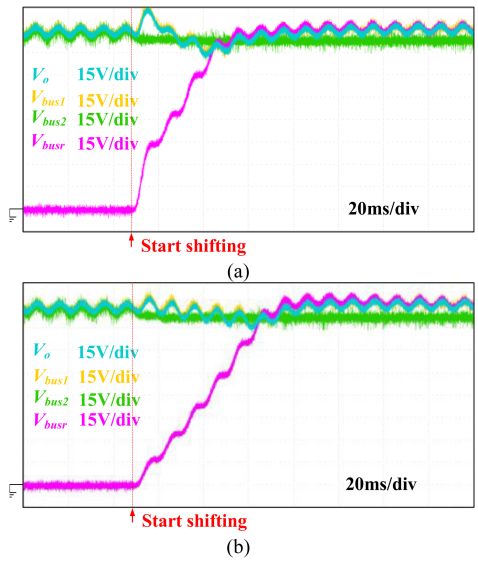

Fig. 19. Bus voltage waveforms of each module during shifting at the current zero-crossing point. (a) Direct shifting. (b) Optimized fault-tolerant control strategy.

potentially damage other SST modules in practical applications. In contrast, with the optimized fault-tolerant control strategy proposed in this article, current fluctuations ΔI_{pp} at the moment of shifting are minimal, and output voltage fluctuations ΔV_o are also effectively reduced. This ensures a smooth shifting process and demonstrates the advantages of the proposed control strategy.

The fluctuations of the SST input current and output voltage during fault-tolerant shifting have been analyzed above. The next step is to examine the variations in bus voltage of each module at different shifting moments. The experimental results for shifting at the current zero-crossing point are shown in Fig. 19.

In Fig. 19, after bypassing the faulty module M_2 and locking the drives of its H-bridge and *LLC* at the same time, the bus voltage V_{bus2} of module M_2 remains unchanged. In contrast, the bus voltage V_{bus1} of the normally operating module M_1 follows a variation trend similar to that of the output voltage V_o. This indicates that fluctuations in the output voltage during fault-tolerant shifting also impact the bus voltage of the normally operating module through the second-stage *LLC*. Therefore, with the optimized fault-tolerant control strategy proposed in this article, the fluctuations in the bus voltage of the normal module are reduced, thus minimizing the risk of fault propagation to other modules.

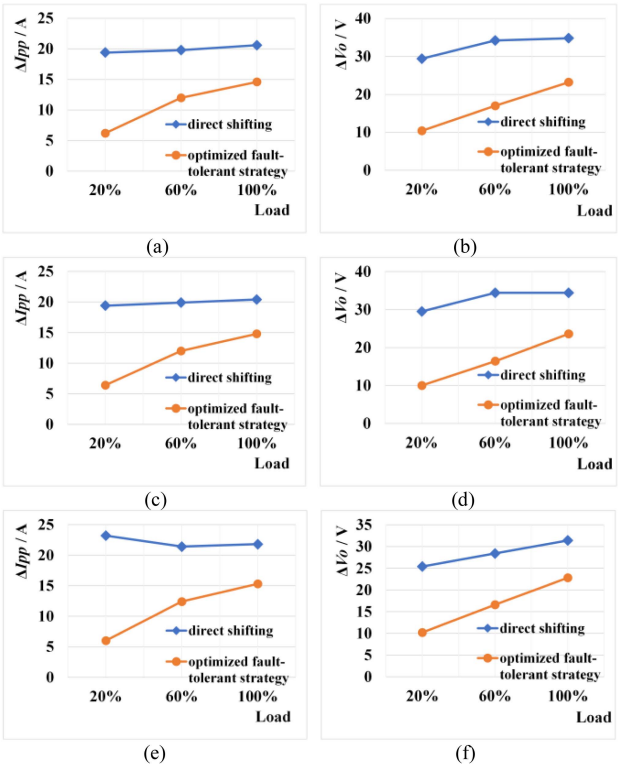

Fig. 20. Curves of ΔI_{pp} and ΔV_o versus load at various shifting positions. (a) Variation curve of ΔI_{pp} at current zero-crossing shifting. (b) Variation curve of ΔV_o at current zero-crossing shifting. (c) Variation curve of ΔI_{pp} at half peak current shifting. (d) Variation curve of ΔV_o at half peak current shifting. (e) Variation curve of ΔI_{pp} at peak current shifting. (f) Variation curve of ΔV_o at peak current shifting.

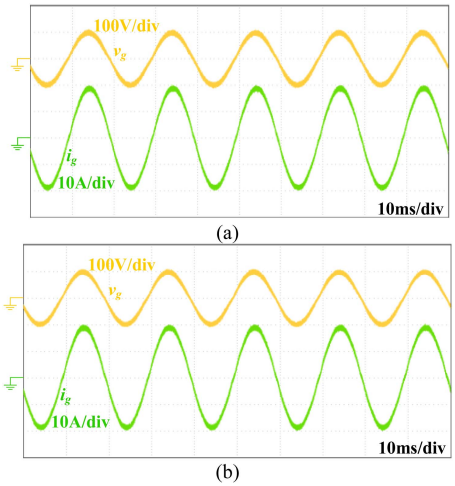

Fig. 21. Steady-state waveforms before and after fault-tolerant shift. (a) Before the shift (b) after the shift.

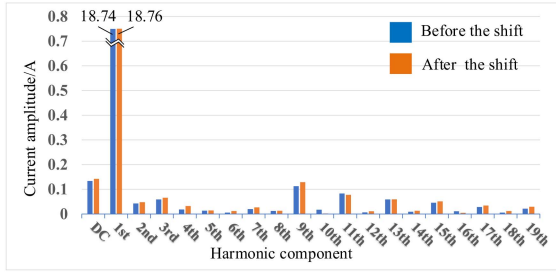

Fig. 22. Analysis of the harmonic components of input current before and after SST fault-tolerant shift.

The experimental waveforms shown above were obtained under the rated load ($R_L = 16\,\Omega$). To validate the effectiveness of the proposed strategy under different load conditions, experiments were also conducted at 20% load ($R_L = 80\,\Omega$) and 60% load ($R_L = 26.67\,\Omega$). The resulting values of ΔI_{pp} and ΔV_o are presented in Fig. 20.

As can be seen from Fig. 20, under different current shifting positions and different loads, after adopting the optimized fault-tolerant control strategy studied in this article, the input current fluctuation ΔI_{pp} and the output voltage fluctuation ΔV_o are smaller than those under direct shifting, which proves the effectiveness of the optimized fault-tolerant strategy studied in this article under different load conditions.

The steady-state waveforms of input current i_g, grid voltage v_g before and after fault-tolerant shift are shown in Fig. 21. From Fig. 21, it can be seen that the SST operates normally and stably both before and after fault-tolerant shift, and there are no significant changes in the waveforms of input current i_g. For a more precise verification, fast Fourier transform was applied to i_g to analyze their harmonic components, with the results shown in Fig. 22.

Fig. 22 illustrates the harmonic components of the input current. The THD of the input current before fault-tolerant shifting is 2.89%, and the THD of the input current after shifting is 2.90%. Therefore, the input current exhibits similar harmonic components in the stable states before and after the fault-tolerant shift. This indicates that the optimized fault-tolerant strategy proposed in this article can ensure the SST system fully recovers to its normal operating state after the shift.

VI. Conclusion

In order to reduce the current surge in the cold redundancy fault-tolerant shifting scheme, a fault-tolerant control method based on dynamically adjusting modulation voltage has been proposed. The strategy adjusts the modulation voltage amplitudes of the normal operating module in real-time based on feedback from the bus voltages and the original modulation voltage signal during fault-tolerant control, reducing voltage and current fluctuations during the shifting process. The principle of the proposed optimized fault-tolerant control strategy to suppress current surge is analyzed in detail. On the basis of the proposed control strategy, the control mode is changed during fault-tolerant shifting to achieve smooth transition. A prototype with two normal operating modules and one redundant module was built. Both theoretical analysis and experimental results showed that the proposed optimized fault-tolerant control strategy can effectively suppress the current surge during the module fault of the SST.

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