A Partially Rated Interlinking Converter With Distributed Energy Storage for Active Power Sharing in DC Microgrids

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***Abstract*—Partially rated dc interlinking converters are recognized for their high-gain power regulation capabilities, which effectively synergize active power across dc microgrids (DCMGs). Integrating energy storage units (ESUs) to address the intermittent nature of renewables in DCMGs has become an enhanced requirement for these converters. This article proposes a partially rated multiport interlinking converter (PMIC) that incorporates a distributed ESU. The PMIC controls a floating voltage and a bidirectional shunt current on the dc line, ensuring full galvanic isolation for the ESU while operating at a low dc-link voltage. It regulates multidirectional power flow and balances power during peak and off-peak periods. A decentralized droop-based power flow control strategy is proposed for the PMIC, which distributes renewable energy generation, load consumption, and ESU utilization proportionally across the system. The control strategy includes two tailored continuously differentiable activation functions, Sigmoid and hyperbolic tangent, to facilitate autonomous global power-sharing and seamless ESU engagement. Simulation and experimental case studies confirm the PMIC's capability to smooth renewable energy fluctuations and enhance the power and voltage profiles of DCMGs.**

***Index Terms*—DC microgrid (DCMG), partially converter, power flow controller, triple-active-bridge (TAB).**

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I. Introduction

THE more dc microgrids (DCMGs) lean toward decarbonization, the more system strength is required. As the share of renewable distributed generation (DG), such as photovoltaics and wind, continues to increase in the energy mix, local islanded DCMGs will play a critical role in maintaining a reliable power supply. However, the variability of renewables and fluctuating loads pose challenges to system robustness [1]. In off-grid regions, interconnecting islanded DCMGs enables the coordinated operation of DG assets, energy storage units (ESUs), and loads. However, the interconnection through tie-lines complicates power flow regulation when bus voltages equalize [2], [3]. DC interlinking converter technology plays a crucial role in regulating power flow within interconnected systems, providing the flexibility needed to balance energy distribution dynamically. As part of a holistic energy strategy, ESUs complement renewable energy sources by mitigating power fluctuations. When interlinking converters are integrated with ESUs, they further improve DCMG flexibility, optimize the utilization of on-site renewables, and strengthen overall system robustness.

DC interlinking converters are categorized into fully rated and partially rated designs. Fully rated designs include back-to-back (B2B) [4], dual-active-bridge (DAB) [5], [6], and triple-active-bridge (TAB) converters [7]. To enhance system resiliency, an ESU can be connected to the dc-link of the B2B through a dc/dc converter. However, this approach does not provide galvanic isolation for the ESU, a requirement in specific applications such as high-power stationary battery energy storage systems as per IEC 62786-3 [8], [9]. The TAB-based design is characterized by the use of a three-winding transformer to provide more dc interfaces, which has been proven in versatile applications such as dc distribution systems [10] and the dc energy router for medium-voltage dc systems [11]. TAB offers an additional isolated port for the ESU [see Fig. 1(a)], giving it an advantage over the DAB-based design. However, all fully rated converters need to be sized according to the maximum expected load and DG variations. These converters must use high-voltage and high-current components, resulting in bulky dimensions and increased costs [12], [13].

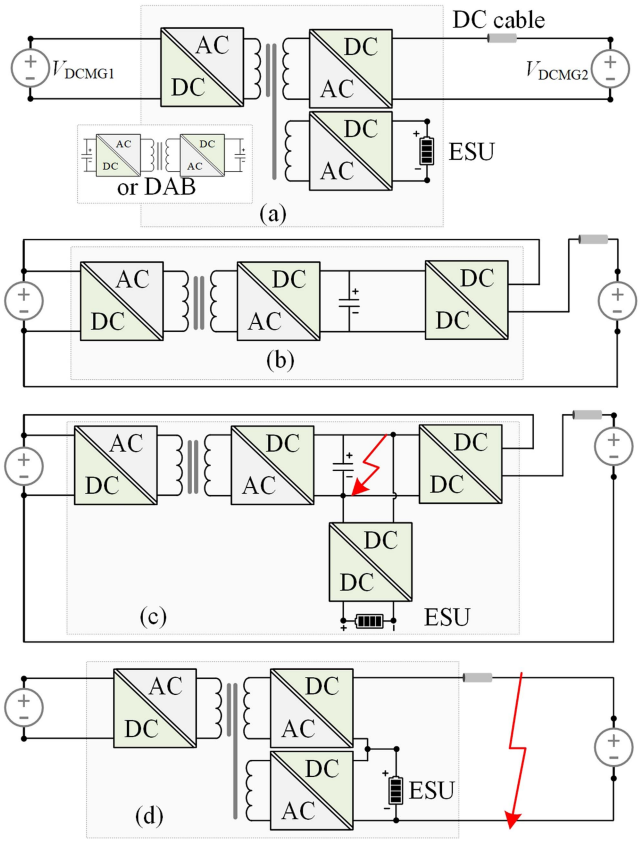

Fig. 1. Equivalent circuits of various interlinking converters. (a) Fully rated power flow controller with and/or without ESU. (b) Partially rated power flow controller (PFCC). (c) PFCC integrated with an ESU. (d) Three-port partial power converter (3P-PPC).

The partially rated design is cost-effective and highly efficient [12]. Partially rated converters only process a small portion of the power while the majority of the power is directly delivered from input to output. For example, the PFCC presented in [14] manages bidirectional power by regulating a bipolar series voltage across a virtual resistance in the interconnection cables [see Fig. 1(b)]. By deploying a solid-state dc circuit breaker (DCCB) between two dc grids, the PFCC achieves short-circuit withstand capability [2]. However, the PFCC lacks the capability to provide a dc port for an ESU. Therefore, deploying a PFCC typically requires each DCMG to be equipped with a high-capacity ESU to ensure system stability [15]. In certain scenarios, such as ring-type islanded microgrid clusters [16], EV charging stations with shared ESUs [17], or small isolated islands [18], a relocatable and scalable distributed ESU allows for incremental ESU capacity support for the entire system during peak periods.

Various approaches have been proposed to integrate an ESU with a partially rated design. For example, this can be achieved by adding a dc/dc converter with an ESU into the dc-link of the PFCC, as depicted in Fig. 1(c). However, this approach may increases the dc-link voltage. In a 400 V dc system, the PFCC's normal dc-link voltage ranges from 40 to 50 V [14], [19]. By contrast, integrating an ESU will raise the voltage above 110 V, which could diminish the benefits of using low-power components, as the converter must account for the maximum line current in its power rating design [20]. Integrating an ESU can be achieved by utilizing a multiport dc/dc converter. For instance, the partial power converter (PPC) combines boost cells with a DAB [13]. Nevertheless, the PPC still requires a high dc-link voltage up to 150 V. The three-port PPC (3P-PPC) employs a TAB converter to charge EVs, as shown in Fig. 1(d) [9]. As illustrated in Fig. 1(c) and (d), the lack of full galvanic isolation of the ESU makes the PFCC+ESU and 3P-PPC unsuitable for DCMG interconnection since dc faults in the dc-link or DCMG can jeopardize both the system and the ESU. This limitation is also observed in other series-connected PPCs in [21], [22], and [23].

Partially interlinking converters should be equipped with tailored power flow control strategies that consider the characteristics of DCMGs and the ESU. A key requirement for the interlinking converter is to achieve global power-sharing (GPS) operation, which ensures that the total load in the system is proportionally shared by each DCMG according to its capacity [24]. This is achieved by equalizing the normalized dc bus voltages using proportional–integral (PI) controllers [25], [26]. In addition, decentralized droop control facilitates effective management of the ESU [27], [28]. For example, the variable droop control proposed in [29] enables dynamic power allocation for the ESU based on different state-of-charge (SoC) conditions. However, charging and discharging ESU often rely on either using a piecewise function-based mode selector that includes a dead zone [30], [31], or by establishing voltage deviation margins [25]. These methods may increase the risk of frequent ESU mis-triggering at boundary conditions [32]. Therefore, additional switching timing selections are necessary to ensure seamless mode transitions when the system operates near these constraints $|V_{\text{bus}}| \leq \varepsilon$. As a result, the ESU control becomes complex and may require a multilayer structure [33]. To facilitate seamless transitions under sudden load changes, the sigmoid function is utilized to formulate the droop constant in [34]. However, the sigmoid function maintains a nonzero output throughout its domain, limiting its flexibility to activate or deactivate the ESU according to the voltage profile of the interconnected system. In addition, the steepness and weight initialization of the sigmoid function are not optimized for the output of DCMGs. Therefore, the activation function design must consider bus voltage fluctuations, ESU engagement constraints, and the SoC of distributed ESUs.

This article presents a simple yet highly tailored solution for the interconnection of DCMGs. The proposed partially rated multiport interlinking converter (PMIC) integrates an ESU with full galvanic isolation while significantly reducing the dc-link voltage. Furthermore, the article introduces a GPS control strategy leveraging the droop characteristics of each DCMG, enabling the PMIC to achieve autonomous, flexible, and seamless multidirectional active power regulation among DCMGs and ESU. The key contributions of this work are summarized as follows.

1) The proposed PMIC ensures full galvanic isolation for the ESU from the DCMGs while maintaining a low dc-link voltage and optimized step-down ratios. This design combines the benefits of safely integrating ESUs with an

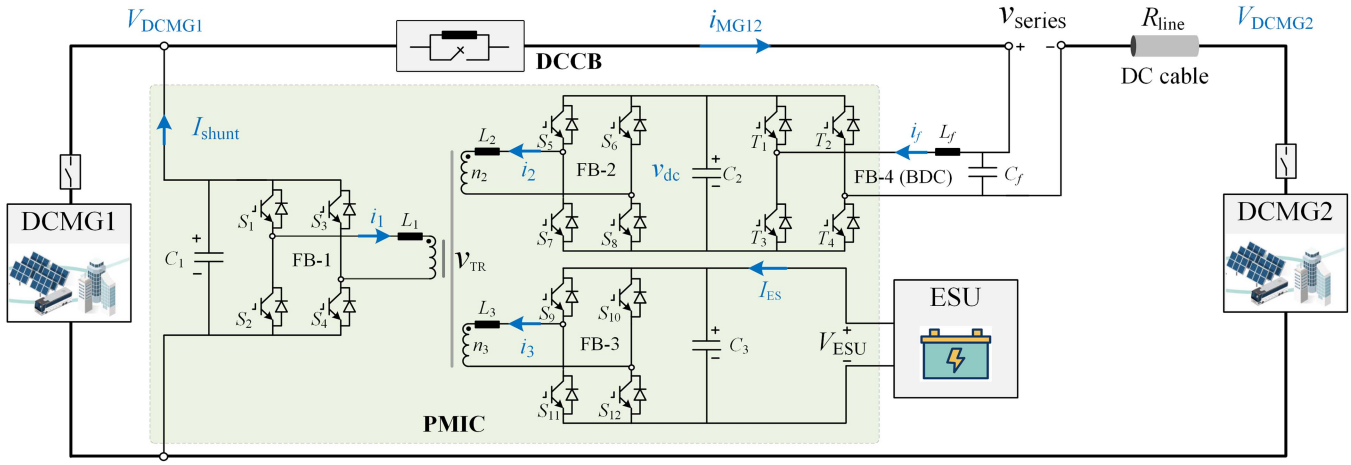

Fig. 2. PMIC-based DCMGs interconnection configuration.

efficient, high-gain partial power process utilizing low-power components.

2) The PMIC incorporates a normalized and decentralized global V–P droop control strategy tailored for DCMG interconnections. This control ensures autonomous and proportional power distribution among interconnected DCMGs and the ESU, effectively accommodating fluctuations in renewable power generation and load demand.
3) Two participation factors are proposed based on customized sigmoid and hyperbolic tangent activation functions, which achieve seamless ESU activation and SoC optimization under varying system operating conditions.

II. PMIC-Based DC Microgrid Interconnection Configuration

A. PMIC-Based DCMG Interconnection

Fig. 2 shows the configuration of the proposed PMIC, which interlinks two DCMGs. The PMIC comprises a TAB and a bipolar dc/dc module (BDC). Notably, full-bridge-1 (FB-1) is connected to the dc bus of DCMG1. FB-2 maintains the voltage on the dc-link capacitor, which connects to the BDC. The BDC injects a controllable bipolar dc voltage in series with the interconnection line to regulate power flow between DCMG1 and DCMG2. FB-3 provides a dedicated interface for a distributed ESU, which helps balance significant power imbalances among the network. In this scheme, FB-1 is the high-voltage (HV) input of the PMIC, while FB-2, FB-3, and FB-4 are LV sides. A step-down three-winding transformer is utilized to provide galvanic isolation and voltage turn ratios between HV and LV components of the PMIC. A DCCB is implemented between the two DCMGs to provide ultra-fast fault current interruption, ensuring the fault-tolerance capability of the PMIC [2].

According to Fig. 2, the power flow P_{MG12} between two DCMGs can be represented as

$$P_{MG12} = \frac{(V_{MG1} - V_{series} - V_{MG2})\, V_{MG2}}{R_{line}} \tag{1}$$

where V_{MG1}, V_{MG2}, and V_{series} are the dc bus voltages of DCMG1 and DCMG2, and the series voltage generated by the BDC, respectively; R_{line} is the dc line resistance. Considering the participation of the ESU, the total power processed by the PMIC is given by

$$\begin{aligned} P_{PMIC} &= \left(\frac{1}{\eta_{PMIC}}\right)\left(P_{ESU} + \frac{P_{MG12} V_{series}}{V_{MG2}}\right) \\ &= \frac{P_{ESU}}{\eta_{PMIC}} + \frac{(V_{MG1} + V_{series} - V_{MG2})\, V_{series}}{\eta_{PMIC} R_{line}} \end{aligned} \tag{2}$$

where η_{PMIC} represents the total efficiency of the PMIC. Moreover, the I_{shunt}, either injected into or absorbed from the system is given by the following:

$$I_{shunt} = \frac{P_{PMIC}}{\eta_{PMIC} V_{MG1}}. \tag{3}$$

According to a proven method detailed in [9], efficiencies for basic cells in the PMIC can be estimated, including the nonisolated BDC $\eta_{BDC} = 98\%$ [35] and the TAB $\eta_{TAB} = 97.5\%$ [36]. Therefore, the round-trip efficiency η_{PMIC} can be estimated as follows:

$$\eta_{PMIC} = \eta_{BDC} \cdot \eta_{TAB}^2 = 93.2\%. \tag{4}$$

Therefore, the PMIC maintains a round-trip efficiency comparable to the 3P-PPC ($\eta_{3P-PPC} = 92.2\%$, [9]) while achieving full galvanic isolation for the ESU. Compared to the PFCC ($\eta_{PFCC} = 93.6\%$), its slight efficiency reduction is offset by significant advantages in integrating the ESU for DCMGs. According to (2), the proposed PMIC can optimize the power profile of the DCMG system by regulating V_{series} and I_{ESU}.

B. Power Transmission of PMIC

The power processed by the PMIC can be represented as $P_{PMIC} = P_{ESU} + P_{BDC}$. According to the Δ equivalent circuit of the TAB [37], the equivalent inductance L_{ij} between any two

FBs in the PMIC is given by

$$L_{ij}=\frac{L_iL_j+L_iL_k+L_jL_k}{L_k},L_i=L_{iS}\left(\frac{n_1}{n_i}\right)^2,k\neq i,j \tag{5}$$

where L_i is the leakage inductance of each FB refers to FB-1. Therefore, the power of the BDC and ESU controlled by the PMIC can be given as

$$\begin{aligned}P_{\text{BDC}}&=i_{\text{MG12}}V_{\text{series}}\\&=\frac{n_1V_{\text{MG1}}V_{\text{dc}}\left(-\varphi_{12}\right)\left(\pi-|\varphi_{12}|\right)}{2n_2\pi^2fL_{12}}\\&\quad+\frac{n_1^2V_{\text{ESU}}V_{\text{dc}}\left(\varphi_{23}\right)\left(\pi-|\varphi_{23}|\right)}{2n_2n_3\pi^2fL_{23}}\end{aligned} \tag{6}$$

$$\begin{aligned}P_{\text{ESU}}&=\frac{n_1V_{\text{MG1}}V_{\text{ESU}}\left(-\varphi_{13}\right)\left(\pi-|\varphi_{13}|\right)}{2n_3\pi^2fL_{13}}\\&\quad-\frac{n_1^2V_{\text{ESU}}V_{\text{dc}}\left(\varphi_{23}\right)\left(\pi-|\varphi_{23}|\right)}{2n_2n_3\pi^2fL_{23}}\end{aligned} \tag{7}$$

$$P_{\text{PMIC}}^{\max}=\frac{n_1V_{\text{DCMG1}}V_{\text{dc}}}{8n_2fL_{12}}+\frac{n_1V_{\text{DCMG1}}V_{\text{ESU}}}{8n_3fL_{13}} \tag{8}$$

where φ_{12}, φ_{13}, and φ_{23} are the phase-shift (PS) ratios among the TAB. The maximum power of PMIC appears when $\varphi_{12}=\varphi_{13}=|\pi/2|$, as given in (8). According to the design of leakage inductances for the TAB module [38], L_1 can be initially designed to be smaller than L_2 and L_3 to ensure L_{23} being larger than L_{12} and L_{13}, which facilitates power decoupling between FB-2 and FB-3. According to (7), the processed partial power of the PMIC is $V_{searies}/V_{\text{DCMG2}}$ times less than that of the conventional TAB-based interlinking converter when i_{MG12} is transmitted between two DCMGs. Therefore, this allows for a reduced power rating for the three-winding transformer within the PMIC.

The proposed PMIC configuration preserves a reduced capacity while offering a high-gain power flow regulation capability like the PFCC as the series voltage V_{series} constitutes a minor portion of the dc bus voltage. The autonomous control of power flow between interconnected DCMGs and ESU power exchange will be addressed through a dedicated GPS strategy.

III. Droop-Based GPS Control Strategy for the PMIC

In each DCMG, decentralized droop control for multiple DGs achieves local power-sharing without a centralized management [25]. In primary control, the dynamic among DGs and loads within each DCMG is reflected by its dc bus voltage. The GPS control enables the PMIC to proportionally distribute power-sharing throughout the interconnected system. Considering the participation of ESU, a GPS control strategy is designed to coordinate the activation sequence of each component.

A. GPS for Interconnected DCMGs

The dc bus voltage of each DCMG can be normalized according to its combined droop characteristic [25], [39]. Assuming $(V_{\text{MG}i}^{\max}-V_{\text{MG}i}^{\text{rate}})=(V_{\text{MG}i}^{\text{rate}}-V_{\text{MG}i}^{\min})$, the droop relationship between the normalized bus volatge $V_{\text{MG}i}^{\text{pu}}$ and the combined output current $I_{\text{MG}i}$ of all DGs in ith MG is

$$V_{\text{MG}i}^{\text{pu}}=1+\frac{2\left(V_{\text{MG}i}^{\min}-V_{t\text{MG}i}^{\max}\right)I_{\text{MG}i}}{I_{\text{MG}i}^{\max}\left(V_{\text{MG}i}^{\max}-V_{\text{MG}i}^{\min}\right)},i\in1,2 \tag{9}$$

where $V_{\text{MG}i}^{\max}$, $V_{\text{MG}i}^{\min}$, and $V_{\text{MG}i}^{\text{rate}}$ are the maximum, minimum, and rated values of DCMG bus voltage, respectively; $I_{\text{MG}i}^{\max}$ is the maximum value of the output current, which refers to the capacity of each DCMG. The PMIC manages the system to enable two DCMGs to proportionally share power variations. Therefore, the desired voltage profile of the system should always maintain $V_{\text{MG1}\_des}^{\text{pu}}=V_{\text{MG2}\_des}^{\text{pu}}$. By combining (9) into this constraint, the objective function for the system optimization can be rewritten as follows:

$$\text{Objective}:=\frac{I_{\text{MG2\_des}}}{I_{\text{MG1\_des}}}=\frac{I_{\text{MG2}}^{\max}}{I_{\text{MG1}}^{\max}}. \tag{10}$$

Assuming the ESU is not required for the involvement in this stage, the power balance within the interconnected system should be achieved internally. Therefore, the relationship between the DG and load consumption is given as follows:

$$\frac{I_{\text{MG1\_des}}I_{\text{MG2}}^{\max}}{I_{\text{MG1}}^{\max}}+I_{\text{MG1\_des}}=I_{\text{load1}}+I_{\text{load2}}. \tag{11}$$

The load current $I_{\text{load}i}$ in each DCMG can be calculated according to normalized droop characteristics, is given as follows:

$$I_{\text{load}i}=-\frac{\left(V_{\text{MGi}}^{\text{pu}}-1\right)I_{\text{MGi}}^{\max}}{2}. \tag{12}$$

By combining (9), (10), and (11), the desired output current of DCMG1 is derived as follows:

$$\begin{aligned}&I_{\text{MG1\_des}}=\\&-\frac{\left(I_{\text{MG1}}^{\max}V_{\text{MG1}}^{\text{pu}}+I_{\text{MG2}}^{\max}V_{\text{MG2}}^{\text{pu}}-I_{\text{MG1}}^{\max}-I_{\text{MG2}}^{\max}\right)I_{\text{MG1}}^{\max}}{2\left(I_{\text{MG1}}^{\max}+I_{\text{MG2}}^{\max}\right)}.\end{aligned} \tag{13}$$

By using the PMIC to regulate the desired current flow $I_{\text{MG12\_des}}$ between DCMG1 and DCMG2, the relationship is given as follows:

$$I_{\text{MG12\_des}}=I_{\text{MG1\_des}}-I_{\text{load1}}=I_{\text{MG1\_des}}-\left(I_{\text{MG1}}-I_{\text{MG12}}\right). \tag{14}$$

Combining (12), (13), and (14), the desired current flow can be rewritten as follows:

$$I_{\text{MG12\_des}}=I_{\text{MG12}}+\frac{\left(V_{\text{MG1}}^{\text{pu}}-V_{\text{MG2}}^{\text{pu}}\right)I_{\text{MG1}}^{\max}I_{\text{MG2}}^{\max}}{2\left(I_{\text{MG1}}^{\max}+I_{\text{MG2}}^{\max}\right)}. \tag{15}$$

This current is achieved by using the BDC to control the series voltage. Therefore, (2) is rewritten as follows:

$$V_{\text{series\_des}}=-I_{\text{MG12\_des}}R_{\text{line}}+V_{\text{MG1}}-V_{\text{MG2}}. \tag{16}$$

The proposed GPS control strategy integrates normalized droop characteristics of DCMGs, specifically designed for scenarios with acceptable power variations. As a result, voltage profiles will accurately aligned with predefined objectives. However, the voltage level may be compromised under severe conditions, such as significant curtailment or surges in DG output and load fluctuations. Under such circumstances, the ESU's participation is crucial to support the entire system. Nevertheless, the

participation and availability of the ESU must be meticulously planned and designed.

B. Participation of ESU

The inconsistent availability is one of the biggest hurdles of DGs in DCMGs. By engaging the ESU during peak periods, the need for DG power will be flattened to below the thresholds of the curtailment of DG generation or load shedding. However, minimizing frequent charging and discharging of the ESU and optimizing the SoC is essential to extend its lifespan. Therefore, it is necessary to design a proper participation factor for the ESU to reconcile the GPS and voltage profiles.

It is assumed that the bus voltages of the two DCMGs meet the objective given in (10). The loadability of the entire interconnected system is reflected by $V_{\text{sys}}^{\text{pu}} = 0.5\left(V_{\text{MG1}}^{\text{pu}} + V_{\text{MG2}}^{\text{pu}}\right)$. Therefore, the corner boundaries and regions for the participation of ESU are given as

$$\begin{aligned} &\text{Region1}: 0 < |V_{\text{sys}}^{\text{pu}}| < |V_{ES}^{\text{pu}}| \\ &\text{Region2}: |V_{ES}^{\text{pu}}| \le |V_{\text{sys}}^{\text{pu}}| \le 1 \end{aligned} \tag{17}$$

where $|V_{ES}^{pu}|$ is the actuation boundary of ESU. The ESU will be actuated only when the interconnected system operates within Region2. To enable the PMIC seamless transition to Region2, a Hyperbolic Tangent activation function is designed for the PMIC controller.

The standard expression of Hyperbolic Tangent function is given in (19). It allows the controller to handle both positive and negative input values, which can lead to more stable weight updates and improved convergence. The standard function is symmetrical and zero-centered around the point (0, 0), meaning that $Tanh\left(V_{\text{sys}}^{\text{pu}}\right) = Tanh\left(-V_{\text{sys}}^{\text{pu}}\right)$. This characteristic aligns the charging and discharging operations of the ESU according to the normalized system voltage profile $V_{\text{sys}}^{\text{pu}}$. In addition, the function is continuous over its entire domain and range, which prevents the introduction of nondifferentiable inflection points that could cause the control system to oscillate near the transition intervals. Although the output value between $(-1, 1)$ matches the range of the normalized system voltage, it achieves its maximum values only as the input approaches positive or negative infinity

$$\text{Tanh}(x) = \frac{e^{x} - e^{-x}}{e^{x} + e^{-x}}. \tag{18}$$

To address this issue, a participation factor, $k_{\text{pf\_ES}}$, is incorporated into the PMIC control strategy. This factor is derived from a modified hyperbolic tangent activation function, enabling the ESU to operate at maximum capacity as system voltages approach the upper or lower limits and to deactivate when the system voltage stabilizes within *Region*1. $k_{\text{pf\_ES}}$ is defined as

$$k_{\text{pf\_ES}} = \tanh\left(\frac{1}{V_{\text{ES}}^{\text{pu}}} \cdot V_{\text{sys}}^{\text{pu}}\right)^{\left(2 \cdot S_{\text{pf\_ES}}+1\right)}, S_{\text{pf\_ES}} \in \mathbf{N}^{*} \tag{19}$$

where $S_{\text{pf\_ES}}$ a coefficient that fine-tunes the rate of change of $k_{\text{pf\_ES}}$ as $V_{\text{sys}}^{\text{pu}}$ approaches $|V_{ES}^{pu}|$. Equation (21) provides a straightforward approach to determining $S_{\text{pf\_ES}}$. For example, $S_{\text{pf\_ES}} \approx 1$ can be derived by selecting $|V_{ES}^{pu}| = 0.1$

$$\frac{\partial^2}{\partial\left(2 \cdot S_{\text{pf\_ES}} + 1\right)^2}\left(k_{\text{pf\_ES}}\right) = 0. \tag{20}$$

Nonetheless, $k_{\text{pf\_ES}}$ can be tailored to meet various operational needs. As shown in Fig. 4, the value of $k_{\text{pf\_ES}}$ and its derivative function vary depending on the $S_{\text{pf\_ES}}$ settings. For instance, $k_{\text{pf\_ES}}$ remains nearly zero within Region =1 when setting $S_{\text{pf\_ES}} = 10$. However, once $V_{\text{sys\_pu}}$ exceeds $|V_{ES}^{pu}|$, $k_{\text{pf\_ES}}$ changes sharply, activating the ESU for charging or discharging. In contrast, setting $S_{\text{pf\_ES}} = 1$ allows $k_{\text{pf\_ES}}$ to achieve its maximum rate of change when $|V_{ES}^{pu}| = 0.1$.

In practice, persistent imbalances between DG output and load demands can lead to overcharging or deep discharging of the ESU. To mitigate this, the PMIC control incorporates a participation factor, $k_{\text{pf\_SoC}}$, to optimize the SoC. $k_{\text{pf\_SoC}}$ is derived by a modified Sigmoid function. Eqs. (22) and (23) are standard and modified Sigmoid functions, respectively. Eq. (22) features an S-shaped curve symmetric around the point (0, 0.5). Its output gradually approaches 1 or 0 as input values move toward positive or negative infinity. This characteristic makes the Sigmoid function ideal for applications requiring a binary-like output behavior

$$\sigma(x) = \frac{1}{1 + e^{-x}} \tag{21}$$

$$k_{\text{pf\_SoC}} = \frac{1}{1 + \mathrm{e}^{-a \cdot (\text{SoCavg} - \text{SoC}_{\text{THR}}) \cdot \text{mode}}}. \tag{22}$$

In (23), SoC_{avg} is the average value of SoC that received from the ESU controller. SoC_{THR} represents the SoC threshold values of the ESU, corresponding SoC_{max} and SoC_{min}, respectively. The coefficient mode $= -1/1$ indicates the charge/discharge mode. The coefficient a adjusts the rate of change of $k_{\text{pf\_SoC}}$ when SoC_{avg} hits SoC_{THR}. A higher value of a leads to a more sharp rate of change at the threshold values. This coefficient a is specifically designed to match the characteristics of different ESUs. As shown in Fig. 5, with $a = 1$ and SoC_{avg} within the threshold range, the ESU is fully utilized as nearly $k_{\text{pf\_SoC}} = 1$. Conversely, $k_{\text{pf\_SoC}}$ is dramatically decreased to curtail the usage of ESU when SoC_{avg} exceeds the threshold range.

The ESU is designed to compensate for the system according to the unified loadability $V_{\text{sys\_pu}}$. Thanks to the participation factors $k_{\text{pf\_ES}}$ and $k_{\text{pf\_SoC}}$, the PMIC prioritizes direct power balancing between DCMGs when the interconnected system operates within Region1. By combining (20) and (23), the relationship between the interconnected system and the ESU current can be established as

$$\begin{aligned} I_{\text{ES\_des}} &= I_{\text{MG1\_ES}} + I_{\text{MG2\_ES}} \\ &= \frac{k_{\text{pf\_ES}} k_{\text{pf\_SoC}}\left(V_{\text{MG1}}^{\text{pu}} + V_{\text{MG2}}^{\text{pu}}\right) I_{\text{ESU}}^{\max}}{2}. \end{aligned} \tag{23}$$

The proposed activation functions are embedded in the GPS droop control of the PMIC. Therefore, the PMIC can autonomously enable the involvement of ESU without using mode

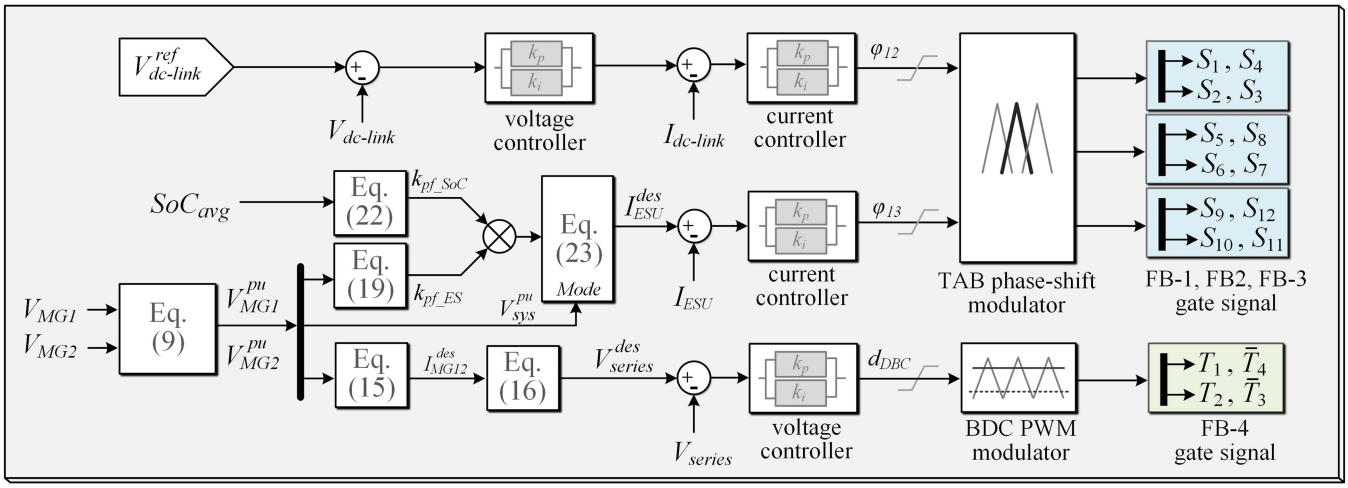

Fig. 3. Overall control structure for the PMIC.

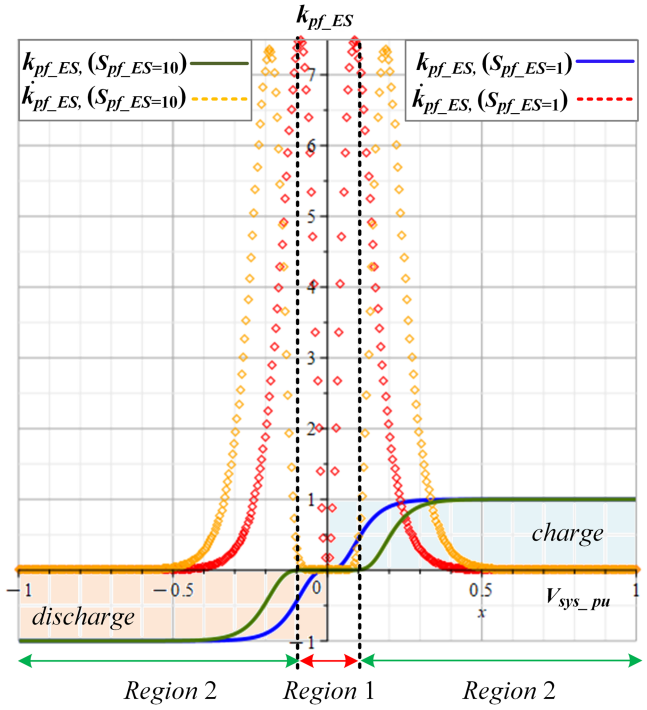

Fig. 4. Output of $k_{\text{pf\_ES}}$ and its change of rate for different $S_{\text{pf\_ES}}$ values when $|V^{pu}_{ES}| = 0.1$ p.u.

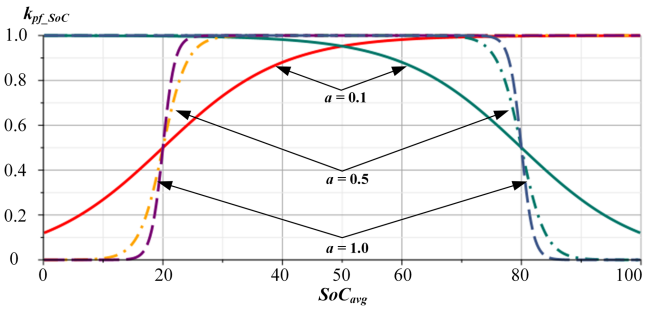

Fig. 5. Output of $k_{\text{pf\_SoC}}$ under different selections of a when $\text{SoC}_{\text{THR}} \in (20, 80)$.

selection algorithms. This approach solely monitors bus voltages, which can simplify the control system and avoid undesirable oscillations at corner boundaries.

C. Overall Control Structure of the PMIC

The overall control structure for the PMIC is shown in Fig. 3. FB-1 operates with a fixed 50% phase-shift (PS) ratio to set the PS reference for FB-2 and FB-3. A constant voltage reference value $V^{\text{ref}}_{\text{dc-link}}$ is given through a dual-loop voltage–current structure to enable FB-2 to maintain the dc-link voltage. The bus voltages of the DCMGs, V_{MG1} and V_{MG2}, are normalized per (9). The normalized voltage $V^{\text{pu}}_{\text{MG1}}$ and $V^{\text{pu}}_{\text{MG2}}$ are given to (20) with a predefined coefficient $S_{\text{pf\_ES}}$. The ESU's SoC is acquired and fed into (23) with predefined coefficients a and SoC_{THR}. As a result, the participation factors, $k_{\text{pf\_ES}}$ and $k_{\text{pf\_SoC}}$, are dynamically adjusted based on the system and ESU conditions and fed into (24). This adjustment determines the desired ESU current, $I^{\text{des}}_{\text{ESU}}$, which is regulated by FB-3's single-loop current controller to manage ESU charging and discharging. The BDC operates under a single-loop voltage control where its target value, $V^{\text{des}}_{\text{series}}$, is computed using (15) and (16).

The proposed GPS strategy takes advantage of decentralized control of the droop characteristic, which only measures the dc bus voltage of DCMGs. As the dc bus voltage of each DCMG is controlled by its droop-based master–slave control [40]. In addition, I_{MG12}, v_{series}, SoC_{avg}, and $V^{\text{ref}}_{\text{dc-link}}$ are measured locally within the PMIC. The PMIC controller processes and controls the power flow for the interconnected system, avoiding peer-to-peer communications with other controllers in each DCMG. As a result, the signaling of dc bus voltages can be transmitted via low-bandwidth communication networks, which minimizes system costs and communication complexity. Alternatively, dc bus voltage signaling can be integrated into existing distribution network operator (DNO) communication infrastructures, such as LTE M2M, WiMAX, or WiFi, without incurring additional costs. In addition, to implement nonlinear Sigmoid and Hyperbolic Tangent active functions in embedded systems without

introducing excessive computational demands, approximation methods such as the coordinate rotation digital computer algorithm, lookup tables, and piecewise linear approximations can be adopted. These techniques enhance efficiency and enable real-time performance in resource-constrained environments by balancing computational complexity and accuracy.

This section presents the droop-based GPS control strategy for the PMIC. The current between two DCMGs is controlled by two variables, the series voltage V_{series} and the ESU current I_{ES}. The proposed GPS control strategy autonomously enables the PMIC to proportionally distribute the power, ensuring two DCMGs mutually support each other as an entire system. By selecting proper coefficients, two activation functions ensure a stable involvement of the ESU under different SoC conditions. As a result, the utilization of DG can be efficiently enhanced without frequent curtailment or load shaving. In addition, it is important to carefully design the capacity of the ESU in accordance with grid codes to ensure that it consistently meets the power fluctuations in two DCMGs over extended periods.

IV. Generalized Average Model of the PMIC

To enhance comprehension of the proposed PMIC, a generalized average model is developed by using the dynamic phasor modeling method. For simplification, this model does not account for switching transients, power losses, or the dead-time of the power switches in the TAB and BDC. In addition, the transformer's magnetizing inductance is assumed to be large enough. Given the PMIC's close connection to the dc bus of DCMG1, the line resistance at the input of FB-1 is not considered. The dynamics of the bus voltages of DCMG1, DCMG2, and the ESU are deemed negligible.

A. Generalized Average Model

During the operation of the PMIC, the single-PS and bipolar pulsewidth modulation (PWM) are applied on the TAB and BDC, respectively. Therefore, the switching functions of the FB-1 ($s_1(\tau)$), FB-2 ($s_2(\tau)$), FB-3 ($s_3(\tau)$), and the BDC ($s_{\text{BDC}}(\tau)$) can be formulated as follows:

$$s_1(\tau)=\begin{cases}1 & 0\le\tau<\frac{T}{2}\\ -1 & \frac{T}{2}\le\tau<T\end{cases} \tag{24}$$

$$s_2(\tau)=\begin{cases}1 & \frac{\varphi_{12}T}{2}\le\tau<\frac{\varphi_{12}T}{2}+\frac{T}{2}\\ -1 & 0\le\tau<\frac{\varphi_{12}T}{2},\frac{\varphi_{12}T}{2}+\frac{T}{2}\le\tau<T\end{cases} \tag{25}$$

$$s_3(\tau)=\begin{cases}1 & \frac{\varphi_{13}T}{2}\le\tau<\frac{\varphi_{13}T}{2}+\frac{T}{2}\\ -1 & 0\le\tau<\frac{\varphi_{13}T}{2},\frac{\varphi_{13}T}{2}+\frac{T}{2}\le\tau<T\end{cases} \tag{26}$$

$$s_{\text{BDC}}(\tau)=\begin{cases}1 & 0\le\tau<Td\\ -1 & Td\le\tau<T\end{cases} \tag{27}$$

where φ_{12} and φ_{13} represent the PS ratios of FB-2 and FB-3 relative to FB-1, respectively; d_{BDC} is the duty cycle of the BDC; T is the switching period of the PMIC. Therefore, state equations can be developed to illustrate the operational dynamics

$$C_2\frac{dV_{\text{dc}}(\tau)}{d\tau}=S_{\text{BDC}}(\tau)\,i_f(\tau)-S_2(\tau)\,i_2(\tau) \tag{28}$$

$$L_2\frac{di_2(\tau)}{d\tau}=S_2(\tau)\,V_{\text{dc}}(\tau)-n_2v_{\text{TR}}(\tau) \tag{29}$$

$$L_3\frac{di_3(\tau)}{d\tau}=S_3(\tau)\,V_{\text{ESU}}-n_3v_{\text{TR}}(\tau) \tag{30}$$

$$C_f\frac{dv_{\text{series}}(\tau)}{d\tau}=\frac{V_{\text{DCMG1}}-V_{\text{DCMG2}}-v_{\text{series}}(\tau)}{R_{\text{line}}}-i_f(\tau) \tag{31}$$

$$L_f\frac{di_f(\tau)}{d\tau}=v_{\text{series}}(\tau)-s_{\text{BDC}}(\tau)\,v_{\text{dc}}(\tau). \tag{32}$$

In this context, i_1, i_2, and i_3 represent the currents of the leakage inductors of the transformer in the PMIC; v_{dc} denotes dc-link voltage; n_2 and n_3 represent the transformer's turns ratio for FB-2 and FB-3, referring to FB-1; v_{TR} denotes the transformer winding voltage; and i_f refers to the current on the output inductor of the BDC.

B. Fourier Series Modeling

The state variables in the above equations can be averaged to establish the linearized model of the PMIC. According to [41], the derivative Fourier series representation for k_{th} coefficient of each state variable can is given as

$$\frac{d\langle x\rangle_k(\text{t})}{dt}=\left\langle\frac{dx}{dt}\right\rangle_k(t)-j\omega_s\langle x\rangle_k(t) \tag{33}$$

where $\omega_s=2\pi f_{\text{sw}}$, with f_{sw} being the switching frequency of the PMIC. In addition, the k_{th} coefficient of the product of two variables is

$$\langle xy\rangle_k=\sum_{i=-\infty}^{\infty}\langle x\rangle_{k-i}\langle y\rangle_i. \tag{34}$$

By applying (33) and (34) to (28)–(32), the average states, including the dc and fundamental components ($k=0,-1,1$), can be established as

$$\frac{d\langle V_{\text{dc}}\rangle_0}{dt}=-\frac{2}{C_2}\langle s_2\rangle_{1R}\langle i_2\rangle_{1R}-\frac{2}{C_2}\langle s_2\rangle_{1I}\langle i_2\rangle_{1I}+\frac{1}{C_2}\langle s_{\text{BDC}}\rangle_0\langle i_f\rangle_0 \tag{35}$$

$$\frac{d\langle i_2\rangle_{1R}}{dt}=\omega_s\langle i_2\rangle_{1I}+\frac{1}{L_2}\langle s_2\rangle_{1R}\langle v_{\text{dc}}\rangle_0-\frac{n_2}{L_2}\langle v_{\text{TR}}\rangle_{1R} \tag{36}$$

$$\frac{d\langle i_2\rangle_{1I}}{dt}=-\omega_s\langle i_2\rangle_{1R}+\frac{1}{L_2}\langle s_2\rangle_{1I}\langle v_{\text{dc}}\rangle_0-\frac{n_2}{L_2}\langle v_{\text{TR}}\rangle_{1I} \tag{37}$$

$$\frac{d\langle i_3\rangle_{1R}}{dt}=\omega_s\langle i_3\rangle_{1I}+\frac{1}{L_3}\langle s_3\rangle_{1R}V_{\text{ESU}}-\frac{n_3}{L_3}\langle v_{\text{TR}}\rangle_{1R} \tag{38}$$

$$\frac{d\langle i_3\rangle_{1I}}{dt}=-\omega_s\langle i_3\rangle_{1R}+\frac{1}{L_3}\langle s_3\rangle_{1I}V_{\text{ESU}}-\frac{n_3}{L_3}\langle v_{\text{TR}}\rangle_{1I} \tag{39}$$

$$\frac{d\langle v_{\text{series}}\rangle_0}{dt}=\frac{1}{R_{\text{line}}C_f}V_{\text{DCMG1}}-\frac{1}{R_{\text{line}}C_f}V_{\text{DCMG2}}$$

$$-\frac{1}{R_{\text{line}}C_f}\langle v_{\text{series}}\rangle_0-\frac{1}{C_f}\langle i_f\rangle_0 \tag{40}$$

$$\frac{d\langle i_f\rangle_0}{dt}=\frac{1}{L_f}\langle v_{\text{series}}\rangle_0-\frac{1}{L_f}\langle s_{\text{DBC}}\rangle_0\langle V_{\text{dc}}\rangle_0 \tag{41}$$

where "R" and "I" denote the real and imaginary components of the state variables. In addition, by applying (34) and (35) to (25)–(28), the first coefficients of $s_2(\tau)$ and $s_3(\tau)$ are given as

$$\langle s_2\rangle_{1R}=-\frac{2\sin(d_{12}\pi)}{\pi} \tag{42}$$

$$\langle s_2\rangle_{1I}=-\frac{2\cos(d_{12}\pi)}{\pi} \tag{43}$$

$$\langle s_3\rangle_{1R}=-\frac{2\sin(d_{13}\pi)}{\pi} \tag{44}$$

$$\langle s_3\rangle_{1I}=-\frac{2\cos(d_{13}\pi)}{\pi}. \tag{45}$$

The zeroth coefficient of the switching function for s_{BDC} is detailed in [12] and is given as follows:

$$\langle s_{\text{BDC}}\rangle_0=2d_{\text{BDC}}-1 \tag{46}$$

According to (25)–(28), it is also important to develop the fundamental components of the transformer voltage v_{TR} which has been done in [41]. Considering the input voltages of the PMIC, the fundamental components of real and imaginary parts are given as

$$\begin{aligned}\langle v_{\text{TR}}\rangle_{1R}=&\frac{2L_{2I}V_{\text{DCMG1}}}{\pi}\\&+\frac{2\left(L_{3I}\cos(d_{12}\pi)-L_{3R}\sin(d_{12}\pi)\right)\langle v_{\text{dc}}\rangle_0}{\pi n_2}\\&+\frac{2\left(L_{1I}\cos(d_{13}\pi)-L_{1R}\sin(d_{13}\pi)\right)V_{\text{ESU}}}{\pi n_3}\end{aligned} \tag{47}$$

$$\begin{aligned}\langle v_{\text{TR}}\rangle_{1I}=&-\frac{2L_{2R}V_{\text{DCMG1}}}{\pi}\\&-\frac{2\left(L_{3R}\cos(d_{12}\pi)+L_{3I}\sin(d_{12}\pi)\right)\langle v_{\text{dc}}\rangle_0}{\pi n_2}\\&-\frac{2\left(L_{1R}\cos(d_{13}\pi)+L_{1I}\sin(d_{13}\pi)\right)V_{\text{ESU}}}{\pi n_3}.\end{aligned} \tag{48}$$

The generalized average model of the PMIC is described as follows:

$$\begin{aligned}&\frac{\mathrm{d}}{\mathrm{d}t}\bar{x}=A\bar{x}+B\bar{u}\\&\bar{x}=\begin{bmatrix}v_{\mathrm{dc}} & i_{2,1R} & i_{2,1I} & i_{3,1R} & i_{3,1I} & v_{\text{series}} & i_f\end{bmatrix}^T,\\&\bar{u}=\begin{bmatrix}V_{\mathrm{DCMG1}} & V_{DCMG2} & V_{\mathrm{ESU}}\end{bmatrix}^T.\end{aligned} \tag{49}$$

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS OF THE INTERCONNECTED SYSTEM, PMIC AND ESU

DCMG 1 Parameters	Simulation Value	Experimental Value
DC bus voltage V_{MG1}	200 ± 20 V	200 ± 20 V
DG power $P^{\text{rate}}_{\text{MG1}}$ /$P^{\text{max}}_{\text{MG1}}$	50 kW/100 kW	10 kW (equivalent)
Load power $P^{\text{rate}}_{\text{laod1}}$ /$P^{\text{max}}_{\text{laod}}$	50 kW/100 kW	10 kW (equivalent)
DCMG 2 Parameters	Simulation Value	Experimental Value
DC bus voltage V_{MG2}	200 ± 20 V	200 ± 20 V
DG power $P^{\text{rate}}_{\text{MG2}}$/$P^{\text{max}}_{\text{MG2}}$	25 kW/50 kW	5 kW (equivalent)
Load power $P^{\text{rate}}_{\text{laod1}}$/$P^{\text{max}}_{\text{laod}}$	25 kW/50 kW	5 kW (equivalent)
PMIC Parameters	Simulation Value	Experimental Value
Power rating $P^{\text{max}}_{\text{PMIC}}$	25 kW	1.5 kW
DC-link voltage V_{DClink}	50 V	50 V
Turns ratio $N1:N2:N3$	2:1:1	2:1:1
Leakage inductances $L_{1,2,3}$	5 uH	100;40;100 uH
Input capacitance $C_{1,2}$	410 uF	410 uF
DC-link capacitance C_{DClink}	820 uF	820 uF
BDC filter inductance L_f	0.5 mH	0.5 mH
BDC filter capacitance C_f	40 uF	40 uF
Interlinking resistance R_{line}	0.657 Ω	5 Ω
ESU Parameters	Simulation Value	Experimental Value
ESU power/current $P^{\text{max}}_{\text{ESU}}$	20 kW	± 20 A (equivalent)
Output voltage V_{ESU}	200 V	100 V
Initial SoC SoC_{int}	50%/ 22%	50% (equivalent)
SoC thresholds $\text{SoC}_{\text{Min, Max}}$	20%, 80%	20%, 80%

TABLE II
SIMULATION AND EXPERIMENTAL PARAMETERS OF THE PMIC CONTROLLER

Parameters	Simulation Value	Experimental Value
PMIC swtiching frequency f	10 kHz	10 kHz
Voltage loop cut-frequency f_{c_V}	40 Hz	40 Hz
Current loop cut-frequency f_{c_I}	600 Hz	600 Hz
ESU boundary $\lvert V_{ES\_pu}\rvert$	0.1 p.u.	0.1 p.u.
ESU coefficient $S_{\text{pf\_ES}}$	10	5
SoC coefficient a	0.5	0.5

C. Small-Signal Modeling

The small-signal model of the PMIC is based on the small-signal deviations of (50) as

$$\frac{d}{dt}\Delta\bar{x}=\boldsymbol{A}\Delta\bar{x}+\boldsymbol{B}\Delta\bar{u}+\boldsymbol{N}\Delta\bar{w}. \tag{50}$$

In (50), $\Delta\bar{w}$ represents the small-signal state of d_{12}, d_{13}, and d_{DBC}, respectively. Therefore, by substituting (42)–(46) and (37)–(48) into (36)–(41) and (50), the matrices **A**, **B**, and **N** are given in (51), and (52), and (53), shown at the bottom of the next page, respectively.

It is known that the BDC is a constant power load with respect to the TAB module [42]. The current and voltage control parameters for the TAB module are configured based on the steady-state conditions where maximum power transfer is achieved, as outlined in Table I. Therefore, the transfer function for the TAB module is assessed independently. The PI controller parameters are comprehensively detailed in Table II. Fig. 6(a) verifies the open-loop transfer function from d_{13} to I_{ESU}, which behaves as a constant. Accordingly, the loop gain design for the current loop in Fig. 6(b) shows a well match between simulation sweeps and theoretical results at a cut-off frequency of 600 Hz. Notably,

FB-2 and FB-3 in TAB module are configured identically, resulting in identical current controller parameters. The bandwidth of the outer voltage loop in Fig. 3(b) designed as 40 Hz. This ensures the compensated voltage-loop gain in Fig. 6(c) features adequate phase margins over 45 dB. Therefore, the analysis presents an accurate continuous full-order large-signal model of the proposed PMIC using the Fourier series representation.

V. Simulation and Experimental Results

To validate the effectiveness of the proposed PMIC and its control strategy, a PMIC-interconnected DCMG system is developed on PLECS/Plexim. Table I shows the system and PMIC parameter settings. The PMIC controller parameters are given in Table II.

The system comprises two DCMGs which have rated loads of 50 and 25 kW, with maximum capacities of 100 and 50 kW, respectively. As stipulated in (9), the power generation meets the maximum load demand when the dc bus voltage is at its minimum value. For instance, in DCMG1, the DG supplies the maximum load of $P_{\text{load}}^{\max} = 100$ kW as the bus voltage drops to $V_{\text{MG1}}^{\min} = 180$ V.

The design of ESU's rated power and capacity follows an optimized ESU configuration for DCMGs outlined in [43]. The ESU's rated power is set at 0.254 p.u. of the DG's rated power, which results in $P_{\text{ESU}}^{\max} = 20$ kW. In addition, the capacity of ESU is set as 0.131 p.u. This configuration achieves an 80% confidence degree and a cost-benefit ratio of approximately 9.62. The setting $S_{\text{pf\_ES}} = 10$ is designed to ensure that the ESU will be fully disigned during minor fluctuations in dc bus voltages. The simulation model is validated under seven operation states.

A. Simulation Results

In state 1, the total load in each DCMG is set to the rated value, with $P_{\text{load1}} = 50$ kW and $P_{\text{load2}} = 25$ kW, as shown in Fig. 7. Therefore, the actual dc bus voltage of each DCMG is the rated voltage, resulting in the normalized voltage being zero. Since the load is proportionally in line with the preset capacity ratio of the two DCMGs, the PMIC only maintains the dc-link

$$A=\begin{bmatrix}
0 & \frac{4\sin(D_{12}\pi)}{C_2\pi} & \frac{4\cos(D_{12}\pi)}{C_2\pi} & 0 & 0 & 0 & \frac{(2D_{\text{BDC}}-1)}{C_2}\\
\frac{2((L_{3R}-1)\sin(D_{12}\pi)-L_{3I}\cos(D_{12}\pi))}{L_2\pi} & 0 & \omega_s & 0 & 0 & -\frac{2L_{3R}\sin(D_{12}\pi)}{L_2\pi} & 0\\
\frac{2((L_{3R}-1)\cos(D_{12}\pi)+L_{3I}\sin(D_{12}\pi))}{L_2\pi} & -\omega_s & 0 & 0 & 0 & \frac{2L_{3I}\sin(D_{12}\pi)}{L_2\pi}+\frac{2L_{3R}\cos(D_{12}\pi)}{L_2\pi} & 0\\
-\frac{2n_3L_{3I}\cos(D_{12}\pi)}{n_2L_3\pi}+\frac{2n_3L_{3R}\sin(D_{12}\pi)}{n_2L_3\pi} & 0 & 0 & 0 & \omega_s & -\frac{2n_3L_{3I}\cos(D_{12}\pi)}{n_2L_3\pi}+\frac{2n_3L_{3R}\sin(D_{12}\pi)}{n_2L_3\pi} & 0\\
\frac{2n_3L_{3I}\sin(D_{12}\pi)}{n_2L_3\pi}+\frac{2n_3L_{3R}\cos(D_{12}\pi)}{n_2L_3\pi} & 0 & 0 & -\omega_s & 0 & \frac{2n_3L_{3I}\sin(D_{12}\pi)}{n_2L_3\pi}+\frac{2n_3L_{3R}\cos(D_{12}\pi)}{n_2L_3\pi} & 0\\
0 & 0 & 0 & 0 & 0 & -\frac{1}{R_{\text{line}}C_f} & -\frac{1}{C_f}\\
-\frac{(2D_{\text{BDC}}-1)}{L_f} & 0 & 0 & 0 & 0 & \frac{1}{L_f} & 0
\end{bmatrix} \tag{51}$$

$$B=\begin{bmatrix}
0 & 0 & 0\\
-\frac{2n_2L_{2I}}{L_2\pi} & 0 & \frac{2n_2L_{1R}\sin(D_{13}\pi)}{n_3L_2\pi}-\frac{2n_2L_{1I}\cos(D_{13}\pi)}{n_3L_2\pi}\\
\frac{2n_2L_{2R}}{L_2\pi} & 0 & \frac{2n_2L_{1I}\sin(D_{13}\pi)}{n_3L_2\pi}+\frac{2n_2L_{1R}\cos(D_{13}\pi)}{n_3L_2\pi}\\
-\frac{2n_3L_{2I}}{L_3\pi} & 0 & -\frac{2(L_{1I}\cos(D_{13}\pi)-(L_{1R}-1)\sin(D_{13}\pi))}{L_3\pi}\\
\frac{2n_3L_{2R}}{L_3\pi} & 0 & \frac{2(L_{1I}\sin(D_{13}\pi)+(L_{1R}-1)\cos(D_{13}\pi))}{L_3\pi}\\
\frac{1}{R_{\text{line}}C_f} & -\frac{1}{R_{\text{line}}C_f} & 0\\
0 & 0 & 0
\end{bmatrix} \tag{52}$$

$$N=\begin{bmatrix}
\frac{4\cos(D_{12}\pi)I_{21R}}{C_2}-\frac{4\sin(D_{12}\pi)I_{21I}}{C_2} & 0 & \frac{2I_{f0}}{C_2}\\
\frac{2L_{3R}\cos(D_{12}\pi)V_{\text{dc}}}{L_2}-\frac{2\cos(D_{12}\pi)V_{\text{dc}}}{L_2}+\frac{2L_{3I}\sin(D_{12}\pi)V_{\text{dc}}}{L_2}-\frac{2L_{3R}\cos(D_{12}\pi)V_{series}}{L_2} & \frac{2V_{\text{ESU}}n_2L_{1R}\cos(D_{13}\pi)}{n_3L_2}+\frac{2V_{\text{ESU}}n_2L_{1I}\sin(D_{13}\pi)}{n_3L_2} & 0\\
\frac{2\sin(D_{12}\pi)V_{\text{dc}}}{L_2}+\frac{2L_{3I}\cos(D_{12}\pi)V_{\text{dc}}}{L_2}+\frac{2L_{3I}\cos(D_{12}\pi)V_{\text{series}}}{L_2}-\frac{2L_{3R}\sin(D_{12}\pi)V_{\text{series}}}{L_2} & \frac{2n_2V_{\text{ESU}}L_{1I}\cos(D_{13}\pi)}{n_3L_2}-\frac{2n_2V_{\text{ESU}}L_{1R}\sin(D_{13}\pi)}{n_3L_2} & 0\\
\frac{2n_3L_{3I}\sin(D_{12}\pi)V_{\text{series}}}{n_2L_3}+\frac{2n_3L_{3R}\cos(D_{12}\pi)V_{\text{series}}}{n_2L_3}+\frac{2n_3L_{3R}\cos(D_{12}\pi)V_{\text{dc}}}{n_2L_3}+\frac{2n_3L_{3I}\sin(D_{12}\pi)V_{\text{dc}}}{n_2L_3} & \frac{2V_{\text{ESU}}L_{1I}\sin(D_{13}\pi)}{L_3}+\frac{2V_{\text{ESU}}L_{1R}\cos(D_{13}\pi)}{L_3}-\frac{2V_{\text{ESU}}\cos(D_{13}\pi)}{L_3} & 0\\
\frac{2n_3L_{3I}\cos(D_{12}\pi)V_{\text{series}}}{n_2L_3}-\frac{2n_3L_{3R}\sin(D_{12}\pi)V_{\text{series}}}{n_2L_3}+\frac{2n_3L_{3I}\cos(D_{12}\pi)V_{\text{dc}}}{n_2L_3}-\frac{2n_3L_{3R}\sin(D_{12}\pi)V_{\text{dc}}}{n_2L_3} & \frac{2V_{\text{ESU}}L_{1I}\cos(D_{13}\pi)}{L_3}-\frac{2V_{\text{ESU}}L_{1R}\sin(D_{13}\pi)}{L_3}+\frac{2V_{\text{ESU}}\sin(D_{13}\pi)}{L_3} & 0\\
0 & 0 & 0\\
0 & 0 & -\frac{2V_{dc}}{L_f}
\end{bmatrix} \tag{53}$$

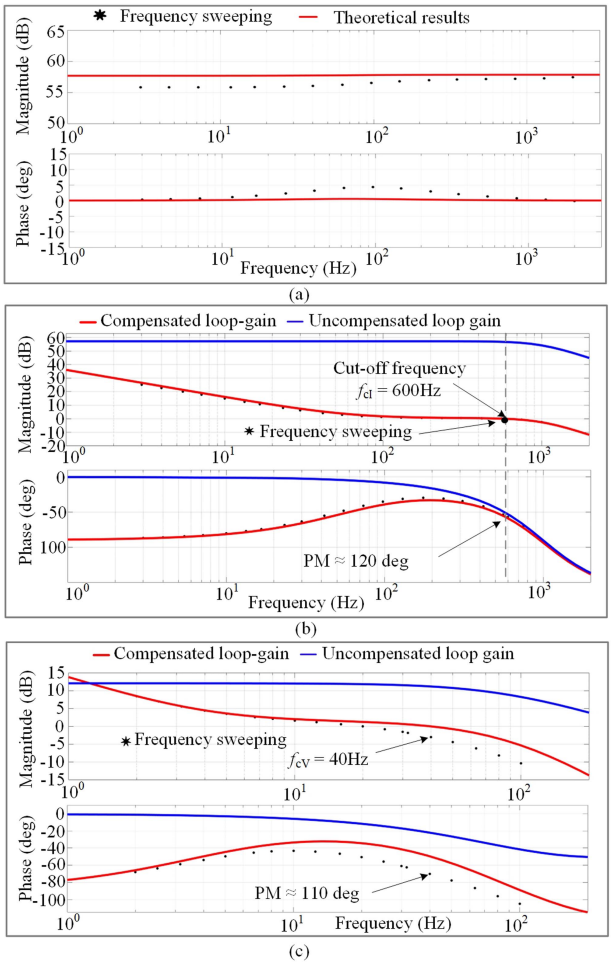

Fig. 6. Calculated and simulated control-to-output gains and phases of the PMIC. (a) The constant open-loop transfer function from d13 to IESU, (b) current loop result, and (c) voltage loop result.

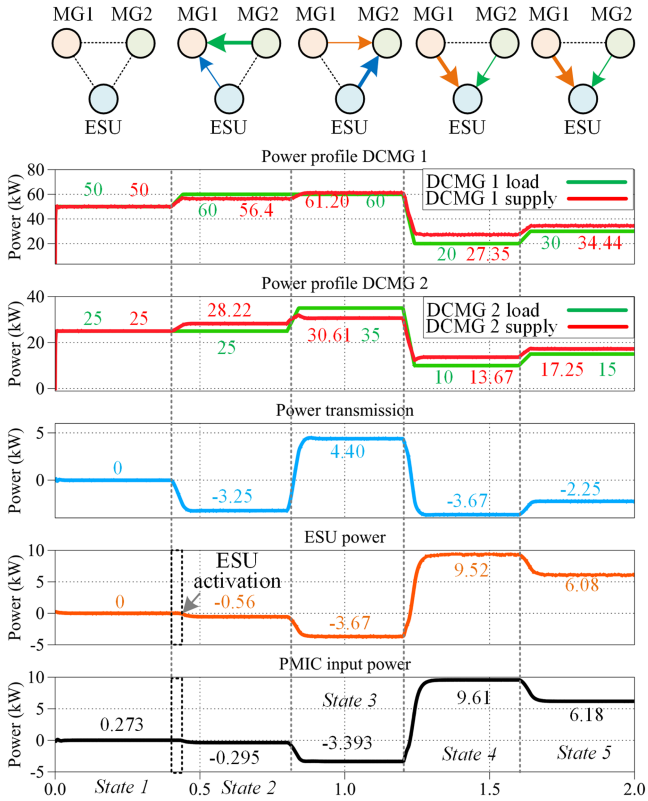

Fig. 7. Power profiles and power regulation results.

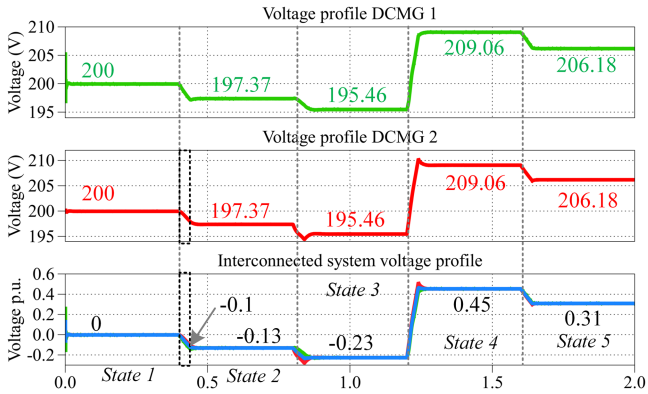

Fig. 8. Voltage profiles of DCMG1, DCMG2, and the interconnected system.

voltage at $V_{\text{DClink}} = 50$ V, while the BDC and ESU operations are not necessitated in this state. As observed in Fig. 9, the output voltage of the BDC and the ESU current are both zero, indicating no participation from the PMIC.

State 2 begins at $t = 0.4$ s. The load in DCMG1 increases to $P_{\text{load1}} = 60$ kW after a duration of $\Delta t = 0.05$ s. In Fig. 9, the output voltage of BDC increases to $V_{\text{series}} = 10.75$ V accordingly. The PMIC regulates the power transferred from DCMG2 to DCMG1 as $P_{MG12} = -3.25$ kW. During this interval, the combined system voltage profile crosses and then stabilizes around $V_{\text{sys\_pu}}$ =-0.13 which is near the predefined ESU activation threshold. Therefore, the ESU lightly engages to inject $P_{\text{ESU}} = -0.56$ kW into the system as shown in Fig. 7. It can be observed that no oscillations occur when the combined system voltage is around the ESU boundaries. The ESU output current $I_{\text{ESU}} = -2.68$ A. Thanks to the design of the participation factor $k_{\text{pf\_ES}}$, there is a time delay for the activation of ESU before $V_{\text{sys\_pu}}$ decreases into the ESU operation Region2. As a result, the power supplies in DCMG1 and DCMG2 are $P_{\text{MG1}} = 56.4$kW and $P_{MG2} = 28.22$ kW, respectively. The values rigorously follow the power ratio which is $P_{\text{MG1}}^{\max} : P_{\text{MG2}}^{\max} = 2 : 1$. This demonstrates that DCMG2 and the ESU proportionally supply a fraction of the increased load in DCMG1 according to (11) and (23).

State 3 begins at $t = 0.8$ s. The load in DCMG2 increases to $P_{\text{load2}} = 35$ kW. It results in a notable increase of $k_{\text{pf\_ES}} = -0.79$, enabling the ESU to inject $P_{\text{ESU}} = 3.67$ kW into the system. Meanwhile, the output voltage of BDC reverses, applying a series voltage $V_{\text{series}} = -14.74$ V. The series voltage adjusts the total power externally supplied to DCMG2 as $P_{\text{MG12}} = 4.40$ kW. In this case, the load mismatch in DCMG2 is mainly supplied by the ESU since the loadability of DCMG1 is much smaller than DCMG2. As a result, DCMG1 only supplies 1.2 kW to DCMG2 and the rest of the power is provided by the ESU. The power supplied by DCMG1 and DCMG2 are $P_{MG1} = 61.2$ kW and $P_{\text{MG2}} = 30.61$ kW, respectively. As

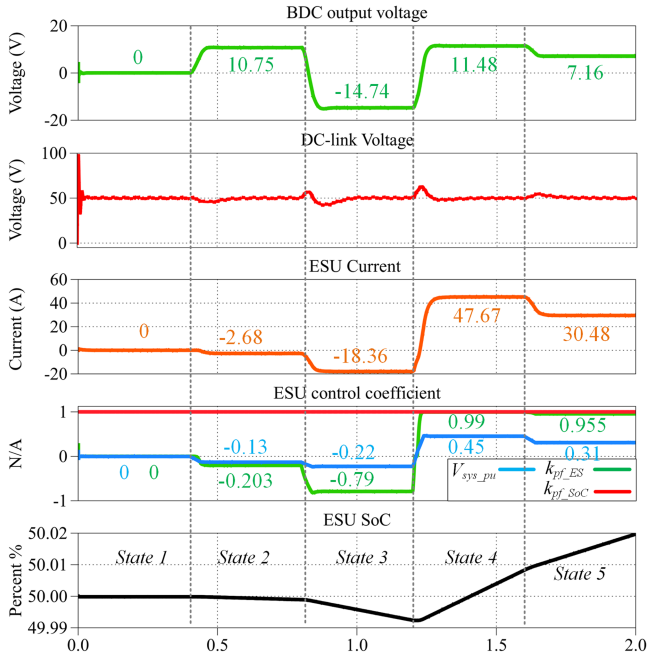

Fig. 9. PMIC waveforms and coefficients.

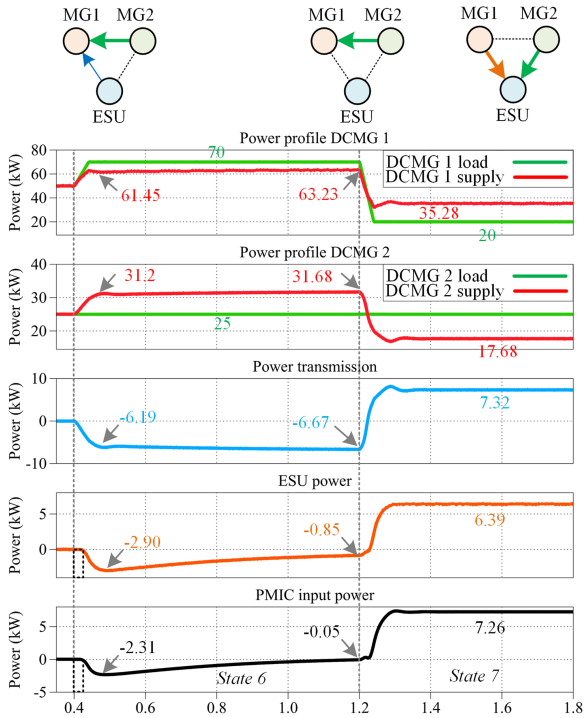

Fig. 10. Voltage profiles of DCMG1, DCMG2, and the interconnected system under the initial condition of $\mathrm{SoC_{int}} = 22\%$.

shown in Fig. 8, the normalized voltage profile of each DCMG exhibits $V_{\mathrm{MG1\_pu}} = V_{\mathrm{MG2\_pu}} = -0.23$, which indicates that the PMIC has effectively synchronized both DCMGs under identical load conditions.

State 4 begins at $t = 1.2$ s. During this interval, the loads in DCMG1 and DCMG2 are decreased to $P_{\mathrm{load1}} = 20$ kW and $P_{\mathrm{load1}} = 10$ kW, respectively. This implies that the interconnected system enters a light load condition. To preserve an acceptable voltage profile, the ESU coefficient undergoes a sharp reversal, eventually rising to $k_{\mathrm{pf\_ES}} = 0.99$. The PMIC adjusts the output voltage of the BDC to $V_{\mathrm{series}} = 11.48$ V and the PS ratios of the TAB module. This allows the system to charge the ESU with a total power of $P_{\mathrm{ESU}} = 9.52$ kW. The PMIC regulates $P_{\mathrm{MG12}} = 3.67$ kW from DCMG2 through the dccable to the input of FB-1. Due to power losses, the ESU receives approximately $P_{\mathrm{MG2\_ES}} = 3.2$ kW from DCMG2, while the remaining power is provided by DCMG1. As shown in Fig. 8, the voltage of each DCMG is $V_{\mathrm{MG1}} = V_{\mathrm{MG2}} = 209.06$ V, which remains within the acceptable range.

State 5 begins at $t = 1.6$ s. During this interval, the loads in DCMG1 and DCMG2 are $P_{\mathrm{load1}} = 30$ kW and $P_{load1} = 15$ kW, respectively. The two values remain below their rated values but inherently align with the power ratio 2:1. Therefore, the BDC only regulates the line power to proportionally distribute the charging power from each DCMG to the ESU. It leads to a total ESU charging power of $P_{\mathrm{ESU}} = 6.08$ kW, in which DCMG1 contributes 4.44 kW and DCMG2 contributes 2.25 kW.

The above results demonstrate that the PMIC can autonomously manage both the line power and the ESU power in accordance with the system's demands. In particular, the ESU participation factor $k_{\mathrm{pf\_ES}}$ is dynamically adjusted to align with the changing voltage profiles. However, it can be seen from Fig. 9 that the SoC factor consistently maintains $k_{\mathrm{pf\_SoC}} = 1$ since the SoC does not undergo dramatic changes over short-term periods in practical. A specific case is conducted to thoroughly validate the design of k_{pf_SoC}. In this case, the initial SoC is set as $\mathrm{SoC_{int}} = 22\%$, while the rate of change of the SoC is scaled up 1000 times.

During State 6, the load in DCMG1 and DCMG2 are $P_{load1} = 70$ kW and $P_{load2} = 25$ kW, respectively. This necessitates the discharge of the ESU to optimize the overloaded system. The initial value of $k_{\mathrm{pf\_SoC}}$ is 0.6. However, the SoC is decreasing because of the gradual discharge of the ESU. This leads to a curtailment in the ESU output power, as shown in Figs. 10 and 11. In response, the output voltage of the BDC incrementally increases to offset this power reduction. By the end of this interval, the output power of the ESU is reduced to $P_{\mathrm{ESU}} = 0.85$ kW with the SoC $= 16.44\%$. It can be seen that the gradual decrease of the ESU power is synchronized with the adjustment of the participation coefficients without oscillations throughout the dynamic process. It verifies the effectiveness of $k_{\mathrm{pf\_SoC}}$ and $k_{\mathrm{pf\_ES}}$. When the system transitions to State 7, the load in DCMG1 reduces to $(P_{\mathrm{load1}}) = 20$ kW. This requires the PMIC to control the ESU being charged. Accordingly, the participation factor $k_{\mathrm{pf\_SoC}}$ shifts from 0.14 to 1, which enables the PMIC to maximize the charging of ESU. As shown in Fig. 10, the ESU charging power reaches $P_{\mathrm{ESU}} = 6.39$ kW, which leads to a rapid increase in the SoC.

B. Experimental Results

To validate the proposed PMIC, experimental tests are performed on a 1.5 kW PMIC prototype. The experimental platform and PMIC setup are shown in Fig. 12. Two California

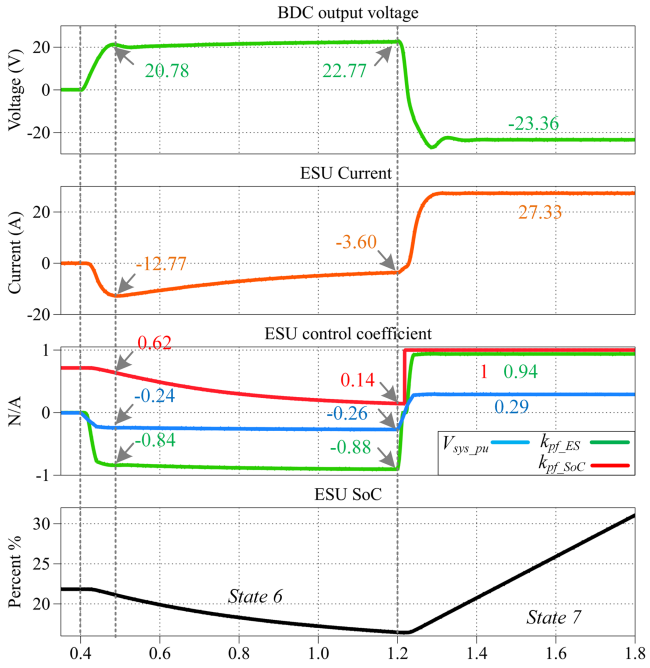

Fig. 11. PMIC waveforms and coefficients under the initial condition of $SoC_{int} = 22\%$.

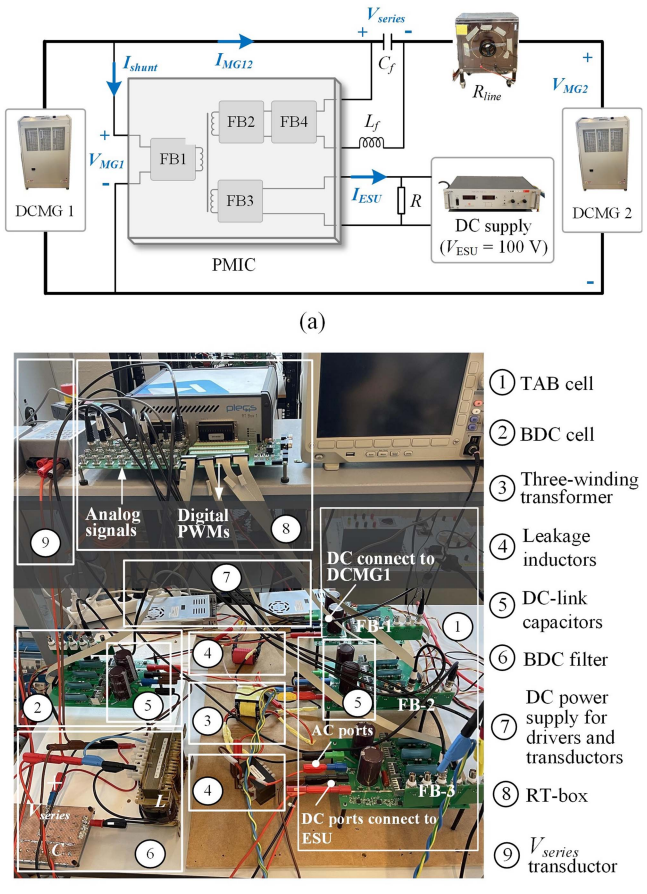

Fig. 12. Experimental platform: (a) System connection scheme. (b) The PMIC setup.

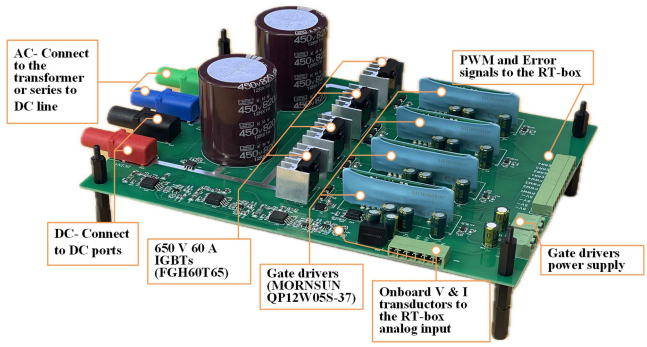

Fig. 13. FB module of the PMIC.

Instruments MX programming grid simulators are deployed to emulate DCMGs. A 2 kW dc power supply paired with a 10 Ω resistor is connected to FB-3 to simulate the charging and discharging of the ESU. The proposed GPS control strategy is implemented in the RT-box 1 controller, which operates on a Xilinx Zynq Z-7030 system-on-chip featuring two embedded CPU cores within an FPGA [44]. Specifically, the activation functions are programmed in a C-script module with a discretization step size set to one-tenth of the PMIC switching period. It should be noted that the grid simulators can only provide voltage steps to mimic DCMG voltage variations and do not replicate the V–P relationships. In addition, the SoC is predefined in the PMIC control. Fig. 13 shows the FB module, where each FB utilizes four 650 V/60 A insulated-gate bipolar transistors (IGBT, FBH60T65), driven by the MORNSUN QP12W05S-37 gate drivers.

Four cases are conducted to validate the effectiveness of the PMIC. Case 1 and case 2 focus on testing the line current controllability, power compensation capability, and the modified Hyperbolic tangent activation function of the PMIC when the system transitions from Region 1 to Region 2 as depicted in (18). For both cases, the equivalent SoC is set at 50 % to enable full charging and discharging of the ESU. Cases 3 and 4 are designed to verify the effectiveness of the modified Sigmoid activation function factor in preventing overcharging and overdischarging of the ESU. In both cases, the equivalent SoC signals embedded in the RT-box are ramped to either 15 % and 85 %, respectively, and sent to the PMIC control.

Case 1 - DCMG1 supplies DCMG2 and ESU; ESU supplies system

In case 1, the dc bus voltages of DCMG1 and DCMG2 initially start at 200 V. At $t = t_1$, the voltage of DCMG1 rises to $V_{\text{DCMG1}} = 210$ V, while the voltage of DCMG2 drops to $V_{\text{DCMG2}} = 195$V. According to the maximum current capability and voltage range that specified in Table I, the normalized voltages of DCMG1 and DCMG2 are $V_{\text{MG1}}^{\text{pu}} = 0.5$ and $V_{MG2}^{\text{pu}} = -0.25$, respectively. These voltage variations emulate the surplus power in DCMG1 and power shortage in DCMG2. However, the system loadability, V_{sys}^{pu}, reaches only 0.125, which approaches the ESU activation boundary between Regions 1 and 2. Therefore, from t_1 to t_2, the power shortage of DCMG2 is mainly supplied by DCMG1 with the help of PMIC which

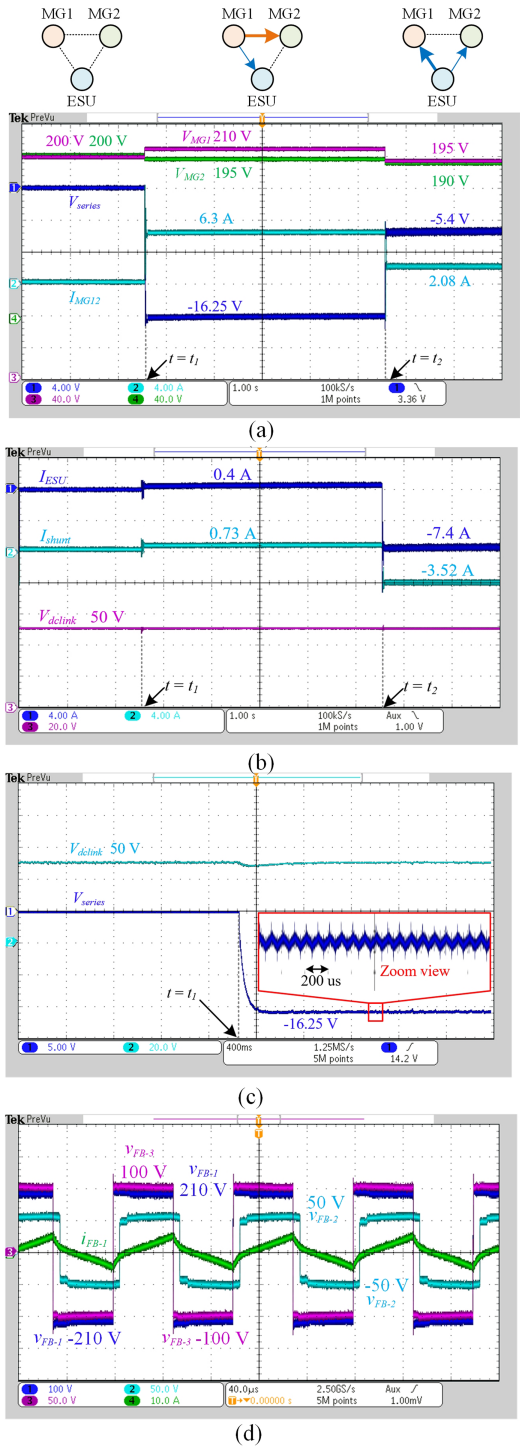

Fig. 14. Experimental case 1: (a) BDC output series voltage and line current waveforms when DCMG1 and DCMG 2 voltage changes. (b) PMIC shunt current, dc-link voltage, and ESU current waveforms. (c) Transient responses at $t = t_1$ of the BDC, and (d) High-frequency voltages and current of FB-1, FB-2, and FB-3 within the TAB module of the PMIC.

features a power regulation ratio of $V_{\text{series}}/V_{\text{MG2}} \approx -0.083$. As per (16), the BDC generates the series voltage of $V_{\text{series}} = -16.25$ V, as shown in Fig. 14(a). During this period, the PMIC regulates the ESU to absorb an $I_{\text{ESU}} = 0.4$ A from the system, as shown in Fig. 14(b). As a result, the total current externally supplied to DCMG2 is $I_{\text{MG12}} = 6.3$A, resulting in the total power delivered to DCMG2 is approximately $P_{MG12} = 1228$ W. According to (2), the power delivered by the PMIC is calculated as $P_{\text{PMIC}} = -(P_{\text{BDC}} + P_{\text{ESU}}) = -142.4$ W. The shunt current is given in Fig. 14(b), indicating the input power of the PMIC during this period is approximately $P^{\text{in}}_{\text{PMIC}} = 153.3$ W. Fig. 14(c) shows the transient responses of the dc-link voltage and the output voltage of the BDC at $t = t_1$. Fig. 14(d) illustrates the high-frequency voltages, FB-1's current, and PS ratios of the TAB module within the proposed PMIC. The PS ratio, φ_{12}, is approximately $\pi/10$ which indicates that FB-1 supplies the BDC (FB-2) to sustain the series voltage. It can be observed that FB-1 is also responsible for power injection to FB-3, as evidenced by the voltages of FB-1 ($\pm$210 V) and FB-3 ($\pm$100 V).

At $t = t_2$, the voltages of DCMG1 and DCMG2 decrease to $V_{\text{DCMG1}} = 195$ V and $V_{DCMG2} = 190$ V, respectively. The system loadability drops to -0.375, which indicates a significant power shortage in the interconnected system. Therefore, the PMIC controls the ESU to inject 7.4 A into the system, supplying $P_{\text{ESU}} = 740$ W to DCMG1 and DCMG2. Meanwhile, the series voltage is adjusted to -5.4 V, regulating the line current $I_{\text{MG12}} = 2.08$ A. As a result, DCMG2 receives 395.2W, and DCMG1 receives 291.2W. During this period, the efficiency of the PMIC setup is 94.3%.

Case 2 - DCMG2 supplies DCMG1; System charges ESU

In case 2, the grid simulators initiate changes at $t = t_1$. As depicted in Fig. 15(a), the dc bus voltage of DCMG1 drops to $V_{\text{DCMG2}} = 188$ V, while DCMG2's voltage increases to 205 V. This shift results in the normalized voltage of DCMG1 and DCMG2 are $V^{\text{pu}}_{\text{MG1}} = -0.6$ and $V^{\text{pu}}_{\text{MG2}} = 0.25$, respectively. The PMIC thus regulates the surplus power in DCMG2, transferring it to DCMG1 by generating a series voltage of $V_{\text{series}} = 18.3$ V, as shown in Fig. 15(a). Meanwhile, the ESU supplies the current of $I_{\text{ESU}} = -1.87$ A. As a result, the total current injected into to DCMG1 is $I_{\text{MG12}} = -7.1$ A, which indicates approximately 1334.8 W is received by DCMG1. During this period, the power in the PMIC can be calculated as: $P_{\text{BDC}} = -129.93$ W, $P_{\text{ESU}} = 187$ W, and $P^{\text{in}}_{\text{PMIC}} = -45.12$ W. In addition, the dc-link voltage stabilizes at 50 V during this period.

At $t = t_2$, the voltages of DCMG1 and DCMG2 increase to $V_{\text{DCMG1}} = 201$ V and $V_{\text{DCMG2}} = 210$ V, respectively. The system loadability increases to 0.525. Therefore, the PMIC controls the ESU to absorb the surplus power from the interconnected system. As shown in Fig. 15(b), the ESU absorbs approximately $P_{\text{ESU}} = 503$ W from the system with a current of 5.03 A. Meanwhile, the series voltage is autonomously adjusted to $V_{\text{series}} = 9.7$ V to ensure DCMG2 supplies 3.75 A to DCMG1 and the PMIC. During this period, the PMIC input power is 564.8 W.

Case 3 - ESU over-discharging

This case is designed to verify the proposed activation functions for the ESU. Specifically, at $t = t_2$, a ramped change in the SoC signal is enabled in the control system in the RT-box to emulate SoC conditions for managing the ESU current. Prior to $t = t_2$, the equivalent SoC (SoC_{eq}) was set at 50%. During this period, the PMIC manages the interconnected system by controlling the ESU current to inject 7.4 A, supplying $P_{\text{ESU}} = -740$ W

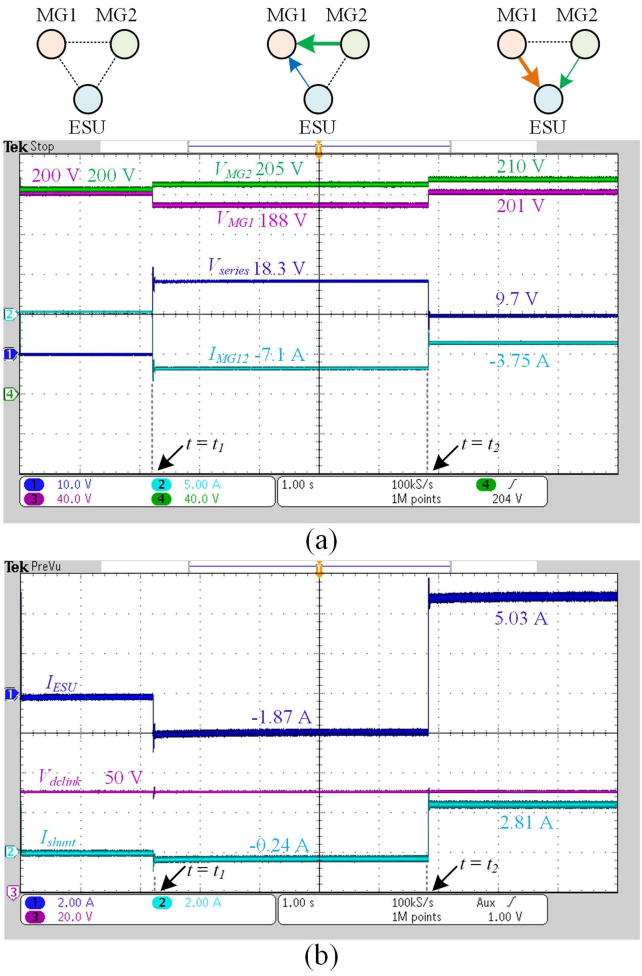

Fig. 15. Experimental case 2: (a) BDC output series voltage and line current waveforms when DCMG1 and DCMG 2 voltage changes. (b) PMIC shunt current, dc-link voltage, and ESU current waveforms.

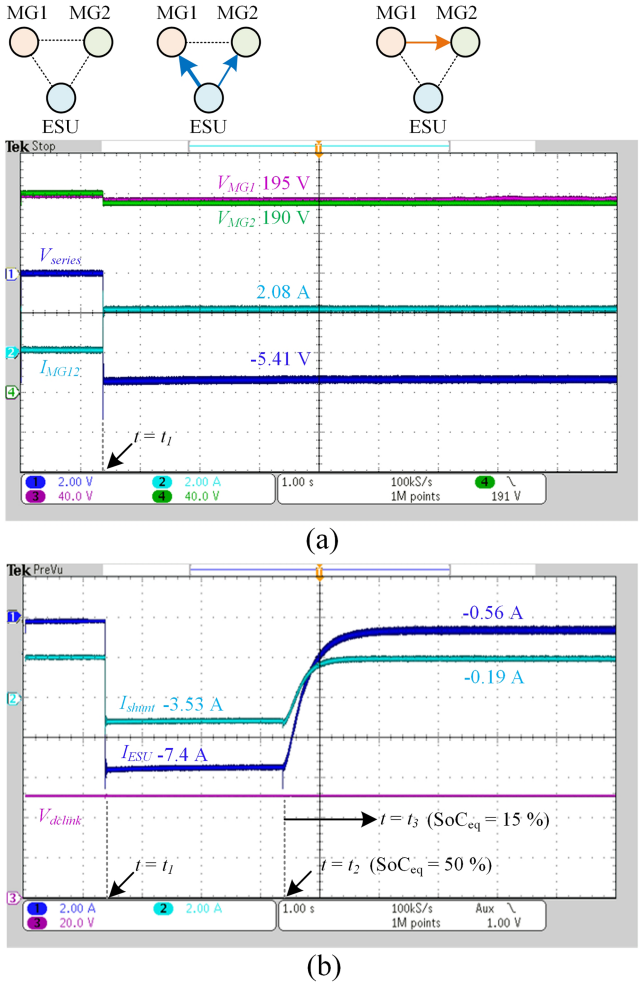

Fig. 16. Experimental case 3: (a) BDC output series voltage and line current waveforms when DCMG1 and DCMG 2 voltage changes. (b) PMIC shunt current, dc-link voltage, and ESU current waveforms.

to both DCMG1 and DCMG2. At $t = t_2$, SoC_{eq} begins to decrease, taking 1.6 s to drop to 15%. Concurrently, the PMIC enables the ESU current curtailment. By $t = t_3$, the ESU current stabilizes at $I_{\text{ESU}} = -0.56$ A, contributing only -56 W to the system. As shown in Fig. 16, this reduction in power prevents overdischarging of the ESU. It is noteworthy that no power oscillations occur on the ESU from t_1 to t_2, demonstrating the effectiveness of the proposed SoC activation factor. However, the grid simulators cannot replicate the V–P droop characteristics of a DCMG. The DCMG voltages remain stable even as ESU power is reduced, resulting in unchanged series voltage.

Case 4 - ESU overcharging

Fig. 17 illustrates the process of the PMIC manages the ESU current to prevent overcharging when the equivalent SoC increases from 50% to 85%. Before $t = t_2$, the PMIC controls the system's surplus power by charging the ESU with a current of 8.9 A, thereby absorbing $P_{\text{ESU}} = 890$ W from both DCMG1 and DCMG2. At $t = t_2$, the SoC_{eq} starts to increase, reaching 85% within 2 s. During this period, the PMIC accordingly reduces the ESU charging current. It stabilizes around 0.68 A without oscillations, drawing only 68 W from the system. This case demonstrates that the proposed modified Sigmoid activation function can smoothly moderate the charge power to avoid overcharging the ESU.

Fig. 18 illustrates the efficiency of the proposed PMIC across different experimental cases. The tested PMIC setup achieved an average efficiency of approximately 94.3%, which aligns with the round-trip efficiency analysis given in (4). The tested PMIC prototype is developed to validate the concept of the proposed PMIC and its GPS control. The efficiency of the PMIC can be improved by incorporating an embedded transformer, optimizing thermal management, and using low on-resistance transistors. Notably, the experimental results demonstrate that PMIC's high gain of power regulation capability. For instance, it utilizes only 153 W to effectively regulate the transmission of 1323 W between the two DCMGs in case 1, thus achieving a remarkable power gain of 8.5 times.

C. Comparison of Different Interlinking Converter Solutions

The comparision among the proposed PMIC and recently proposed interlinking converters for different applications is given in Table. III. Three critical factors are evaluated in the following.

TABLE III
COMPARARIVE ASSESSMENT OF INTERLINKING CONVERTER SOLUTIONS

Type of DC Power Flow Controller	ESU Integration	ESU and DC Grid Isolation	Power Flow	Power regulation ratio $G_{pr} = P_{\text{cov}}/P_{\text{MG12}}$	Number of Components (S/HT/W)	DC-Link	Multi-region Seamless Control	Power Loss	Ref.
Fully Rated	Yes	Yes / Yes	Multidirectional wide range	1	12/1/3	No	No	+++	[10]
Partially Rated	No	– / DCCB	Bidirectional limited range	$\frac{V_{series}}{V_{MG2}}$	12/1/2	50 V	No	++	[2]; [12]
Partially Rated	No	– / DCCB	Bidirectional limited range	$1-\frac{V_{MG1}}{V_{MG2}}$	10/1/1	No	No	+	[14]
Partially Rated	No	– / DCCB	Bidirectional limited range	$1-\frac{V_{MG1}}{V_{MG2}}$	6/1/3	No	No	+	[45]
Partially Rated	Yes	No / No	Multidirectional wide range	$\frac{P_{ESU}}{I_{MG12}V_{MG2}}+\frac{V_{series}}{V_{MG2}}$	14/1/2	110 V	No	++	[20]
Modular Partially Rated	Yes	No / No	Multidirectional wide range	Up to 0.75	12/1/2	150 V	Yes	++	[13]
Modular Hybrid Rated	No	– / Yes	Bidirectional wide range	1	4n/n/2n	No	No	++	[46]
Modular Partially Rated	No	– / DCCB	Multidirectional limited range	$\frac{V_{series}}{V_{MG2}}$	8n/-/-	$\frac{V_{series}}{n}$	No	++	[47]
Modular Partially Rated	Yes	No / No	Multidirectional wide range	$\frac{P_{ESU}}{I_{MG12}V_{MG2}}$	14/1/2	nV_{MG}	No	++	[3]
Partially Rated	**Yes**	**Yes** / DCCB	Multidirectional wide range	$\frac{V_{series}}{V_{MG2}}$ (**Rg.1**) $\frac{P_{ESU}}{I_{MG12}V_{MG2}}+\frac{V_{series}}{V_{MG2}}$ (**Rg.2**)	16/1/3	**50 V**	**ESU+GPS**	++	PMIC

S: power switches; HT: High-frequency transformers; W: Transformer windings; n: number of modulars; Rg: Operational regions of the PMIC defined in (17).

1) ESU Integration and Galvanic Isolation: In Table III, the integration of the ESU offers extensive multidirectional power flow control capabilities for interlinking converters. However, it also brings additional costs. As demonstrated in experimental case 1 after $t = t_2$, the PMIC addresses the power shortages of both DCMG1 and DCMG2, which cannot be achieved by the DAB-based PFCC [12], S-PPC [14], and DCPFC [47]. While similar capabilities are observed in the UAPFC [20], multiport PPC [13], 3P-PPC [9], and MER [3], the PMIC ensures galvanic isolation between the ESU and DCMGs. This design prevents direct electrical connections between the ESU and DCMGs protects the ESU from the rapid propagation of dc short-circuit faults across the system.

2) Power Regulation and Seamless Mode Transition: In Table III, the DAB-based PFCC and DCPFC exhibit low G_{pr}, enabling them to regulate bidirectional power flow efficiently with minimal power usage. The power regulation range of the S-PPC is constrained by its dependence on voltage differences between two interconnected systems. In contrast, the UAPFC, multiport PPC, and MER extend their capabilities by integrating ESU's power, providing an additional reserve for the system but compromising by higher G_{pr} due to P_{ESU}. Taking these advantages, the proposed PMIC with the GPS control strategy supports seamless transitions across two operational regions. In Region 1, the PMIC achieves a low G_{pr} similar to that of the PFCC, actively managing power flow When additional ESU power is needed, it transitions seamlessly to Region 2 (e.g., experimental case 2, after $t = t_2$). This adaptability is driven by the proposed participation factors $k_{\text{pf\_ES}}$ and $k_{\text{pf\_SoC}}$, which are customized to the normalized droop characteristics of interconnected DCMGs the ESU. This approach offers a more refined control than the Sigmoid function used in PV-battery DCMGs [34], dynamically adjusting to both power needs and ESU usage while ensuring optimal operation under varying conditions.

3) Techno-Economic Feasibility and Applicability: In Table III, the push–pull PPC [45] uses six power switches and a three-winding transformer, offering high efficiency at a lower cost. By eliminating the dc-link, it enhances power density and improves economic viability. It is a suitable choice for integrating renewables within a single DCMG. The ISO-IDCPFC in [47] features a modular design without transformers, allowing low-power components to be used across multiple modules. This design makes it ideal for high-voltage or medium-voltage dc networks. Interlinking converters with ESUs require additional components, increasing system costs but provide expanded power reserves and improved robustness. The UAPFC connects an ESU to a 110 V dc-link. It is ideal for the integration of high-voltage ESUs. The multiport PPC and MER efficiently connect multiple dc sources to a dc bus or an ESU for the LVDC networks without the galvanic isolation requirement.

The proposed PMIC with its GPS control strategy provides a practical solution for interconnecting islanded DCMGs with a distributed ESU. It enables partial power processing, seamless power regulation, and adaptive power regulation ratios. However, the use of a multiwinding transformer and two additional power switches relatively increases implementation

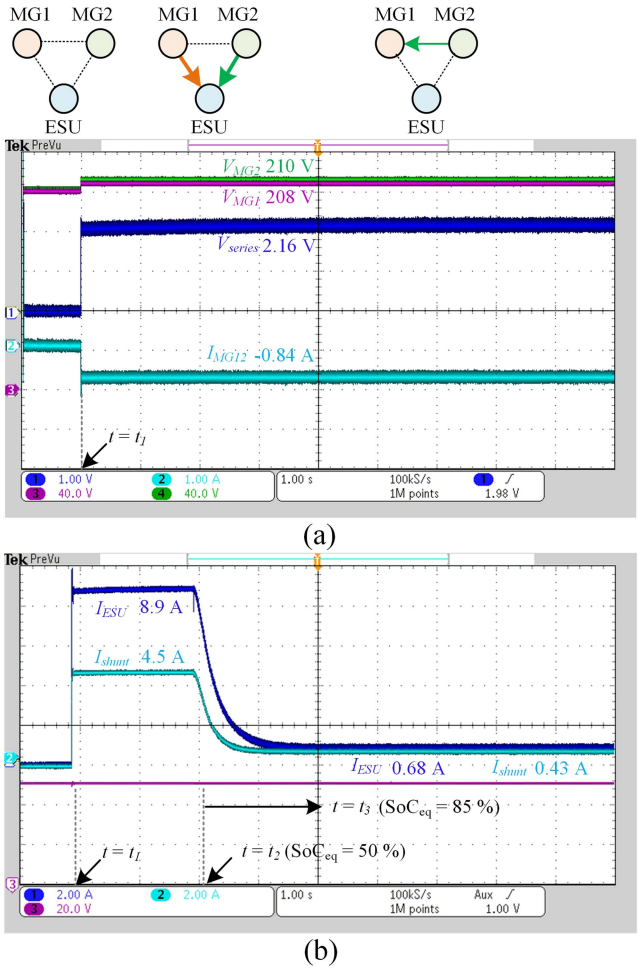

Fig. 17. Experimental case 4: (a) BDC output series voltage and line current waveforms when DCMG1 and DCMG 2 voltage changes. (b) PMIC shunt current, dc-link voltage, and ESU current waveforms.

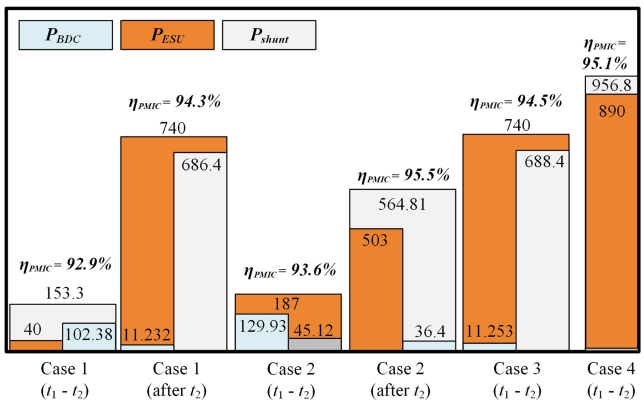

Fig. 18. Experimental efficiency map of the tested PMIC prototype under different cases.

costs. Despite this, the PMIC enhances fault tolerance, reduces the dc-link voltage, and ensures stable operation under varying conditions. These features make the PMIC a tailored choice for islanded DCMG applications requiring ESU support and galvanic isolation.

VI. Conclusion

This article presents a novel PMIC with a tailored GPS control strategy. It enables proportional load sharing among interconnected DCMGs and seamless ESU power management under varying conditions. By leveraging partial power processing, a low dc-link voltage, and full galvanic isolation for the ESU, the PMIC achieves efficient multidirectional power flow regulation with minimal energy consumption. Customized Sigmoid and Hyperbolic Tangent activation functions facilitate dynamic and continuous ESU participation, adapting to flexible power regulation gains based on system voltage profiles without complex optimization at boundary conditions. The generalized average model outlines the PMIC's dynamic behavior and controller design. Simulation and experimental results validate its effectiveness in power flow regulation and ESU management, ensuring stable operation of interconnected DCMGs, maximizing RES utilization, and improving economic efficiency. Future research may focus on advanced modeling and control strategies, optimized ESU capacity planning, and reconfiguring the PMIC for high- and medium-voltage dc applications to expand its applicability.

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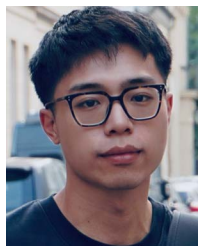

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