A High-Sensitive Online T_j Extracting Method Based on Electrothermal Interaction and Linear-Mode Current Response for Power MOSFET Devices

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***Abstract*—Accurate online junction temperature (T_j) extraction is crucial to power MOSFETs' reliability and health management. However, most temperature-sensitive electrical parameters in silicon carbide (SiC) power MOSFETs exhibit relatively low temperature sensitivity, which limits extracting accuracy and increases the bandwidth requirements of measurement circuits. To address these challenges, this article proposes a high-sensitive online T_j extracting method, called linear-mode current response (LMCR). A theoretical formula is proposed for the first time to reveal the electrothermal characteristics of the drain current in linear mode. Then, technology computer aided design (TCAD) simulations and experimental results verify its high sensitivity to T_j and controllability. To apply for T_j extraction, this article details the implementation of the LMCR-based T_j extracting unit and strategy. By injecting a narrow current pulse into the device, the T_j can be determined from the LMCR. Calibrations using double pulse test are introduced and demonstrate the method's advantages, including high T_j sensitivity, spontaneous injection, minimal additional losses, and low dependence on load current and bus voltage. Finally, the effectiveness of the proposed method is further validated through experiments with a SiC power boost converter. The results show that narrow pulse injection does not affect the load or other components, and this method provides high measurement sensitivity, low invasive interference, and eliminates the need for high-bandwidth circuits.**

***Index Terms*—Junction temperature sensing, power conversion, power semiconductor, reliability, silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET).**

I. Introduction

In RECENT years, the widespread adoption of silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) has driven the development of power electronics towards higher power density and broader operating temperature ranges. Simultaneously, the online T_j extracting method has gained increasing attention. This is for two primary reasons: over 50% of semiconductor failures result from T_j fluctuations and overheating [1]; and while SiC MOSFETs can operate at temperatures up to 550 °C [2], their smaller die area results in higher heat flux density, leading to greater T_j fluctuations and harsher thermal conditions. Therefore, online T_j extraction is crucial for real-time protection, reliability assessment, and health management of power devices [3]. There are four traditional methods for online T_j extraction. Physical contact methods, such as thermistors and thermocouples, are simple but features invasive and complex [4], [5]. Optical methods offer higher accuracy but are limited by encapsulation materials. Thermal network modeling is an indirect approach to determine T_j, but is influenced by multiple parameters, such as heat dissipation conditions and aging effects [6]. In contrast, the TSEP method provides fast response, high accuracy, and the ability to reflect the bare die's T_j. Due to these advantages, the TSEP method has been widely used for online T_j extraction in silicon insulated-gate bipolar transistors (Si IGBTs).

The TSEP method's most significant techniques are based on switching transient parameters and threshold voltage of diodes [7], [8]. However, the temperature sensitivity and operating characteristics of SiC power MOSFET is significantly different from Si-IGBT, i.e., lower temperature sensitivity and higher switching speed. Table I gives the typical TSEPs for comparison

TABLE I
COMPARISON WITH TYPICAL TEMPERATURE SENSITIVE ELECTRICAL PARAMETERS

TSEPs	1200V SiC MOSFET	Si IGBT
Voltage Rising Time	8.87 ps/°C [2]	2 ns/°C [9]
Turn-on Delay Time / Turn-off Delay Time	13.26 ps/°C; 99.18 ps/°C [2]	1 ns~2 ns/°C; 2 ns/°C [9]
Drain Current Slew Rate	1.2 A/(μs·°C) [2]	3 A/(μs·°C) [9]
Gate Threshold Voltage	5 mV/°C [2]	8 mV/°C [9]
On-state Resistance	0.6181 mΩ/°C [10]	/

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with the SiC MOSFET [2] and Si IGBTs [9]. Several research has been conducted on SiC MOSFET TSEPs and their application in online T_j extraction. Common static TSEPs include ON-state resistance, gate threshold voltage, and Miller plateau voltage, etc. ON-state resistance is used for online T_j extraction with aging compensation, demonstrating a temperature sensitivity of 0.6181 mΩ/°C, with values ranging from 64.004 to 156.719 mΩ [10]. Similarly, ON-state voltage mapping has been employed for T_j measurement [8], yielding significant improvements in accuracy and frequency. Jiang et al. [11] also proposes using threshold voltage, with a temperature sensitivity of 5.2 mV/°C and a strong linear relationship.

Typical transient-related TSEPs include the slew rate of drain current/drain-source voltage, switching delay time, and gate current. For example, gate current has been utilized as a highly accurate TSEP, with a temperature sensitivity of 31.6 μA/°C and values ranging from 10 to 14 mA [12]. An online T_j extraction and correction method based on parasitic parameters has been proposed, significantly improving accuracy [13]. A method uses turn-OFF delay time as the TSEP and employs a gate impedance regulation circuit to enhance temperature sensitivity to 736 ps/°C, with measured values ranging from 0 to 90 ns [14].

Despite achieving satisfactory expectations, challenges remain in online T_j extraction due to the high thermal stability and fast-switching speed (*di/dt* and *dv/dt*) of SiC MOSFETs, specifically:

1) *Lower Temperature Sensitivity and Smaller Measured Values:* While SiC devices excel in high-frequency, wide-temperature operations, their TSEPs exhibit lower temperature sensitivity and smaller measured values [15], [16], [17]. The concentrated electrothermal stress and complex electromagnetic operating conditions of SiC applications further complicate T_j extraction.
2) *Difficulty Obtaining Transient TSEPs and High Bandwidth Requirements:* The fast-switching speed of SiC MOSFETs makes it difficult to measure transient-related TSEPs, such as turn-ON/OFF delay times, which span tens of picoseconds per degree Celsius. This requires high-resolution, high-bandwidth measurement circuits, leading to increased costs.

To address these challenges, this article proposes a novel linear-mode current response (LMCR) method for online T_j extraction using a high-sensitive TSEP to reduce measurement error and cost. The narrow current pulse injected in LMCR is influenced by T_j-related factors, including threshold voltage (V_th) and channel mobility (μ_CH), and is controlled by the gate-source voltage (V_GS). The LMCR method is verified through double pulse test (DPT) and boost power converter experiments, with its advantages discussed.

The rest of this article is organized as follows. Section II introduces theoretical analysis and experimental verification. Section III presents the T_j extracting strategy using the novel online extraction unit. Section IV details the DPT used to calibrate the injected current-T_j curve. Based on this curve, Section IV further demonstrates online T_j extraction experiments in a SiC power boost converter using LMCR, and finally, Section V concludes this article.

II. Theoretical Basis of the Relationship Between Linear-Mode I_D and T_J

A. Analysis of Electrothermal Interaction Mechanism

The linear-mode SiC power MOSFET operates in the saturation region at low V_GS and drain-source voltage (V_DS). The drain current (I_D) follows the equation:

$$I_\mathrm{D} = \frac{W\mu_\mathrm{CH}C_\mathrm{OX}}{2L}(V_\mathrm{GS}-V_\mathrm{th})^2(1+\lambda V_\mathrm{DS}), \quad V_\mathrm{DS} > V_\mathrm{GS}-V_\mathrm{th}\ . \tag{1}$$

In this equation, I_D is directly controlled by low-level V_GS, which is why many manufacturers [18], [19], [20], [21], [22], [23] refer to this as linear-mode operation. This mode is widely applied in precise current/voltage control, protection, programmable electronic loads, etc. Although both linear-mode operation and short-circuit failure occur in the saturation region, their operating conditions and characteristics differ significantly, as detailed in Appendix A.

The term $(1+\lambda V_\mathrm{DS})$ accounts for channel length modulation, where V_DS has a slight influence on I_D. For the SiC MOSFET used in this article, λ is calculated as only 0.029 at T_j of 25 °C. Generally, this term can be ignored [24]. Therefore, the temperature sensitivity of the drain current, $\partial I_\mathrm{D}/\partial T$, is expressed as:

$$\frac{\partial I_\mathrm{D}}{\partial T} = \frac{WC_\mathrm{OX}(V_\mathrm{GS}-V_\mathrm{th})^2}{2L}\frac{\partial \mu_\mathrm{CH}}{\partial T} - \frac{W\mu_\mathrm{CH}C_\mathrm{OX}(V_\mathrm{GS}-V_\mathrm{th})}{L}\frac{\partial V_\mathrm{th}}{\partial T}. \tag{2}$$

Setting this equation to zero yields the transition point (TP) of temperature sensitivity, where the correlation between temperature and I_D switches from positive to negative. The expression for I_D at the TP is given by

$$I_\mathrm{D\_TP} = \frac{2WC_\mathrm{OX}\mu_\mathrm{CH}^3}{L}\left(\frac{\partial V_\mathrm{th}}{\partial T}\right)^2\left(\frac{\partial \mu_\mathrm{CH}}{\partial T}\right)^{-2}. \tag{3}$$

Substituting (3) into (1), the gate-source voltage at the TP ($V_\mathrm{GS\_TP}$) can be derived as

$$V_\mathrm{GS\_TP} = 2\mu_\mathrm{CH}\frac{\partial V_\mathrm{th}}{\partial T}\left(\frac{\partial \mu_\mathrm{CH}}{\partial T}\right)^{-1} + V_\mathrm{th}. \tag{4}$$

It is evident that both $I_\mathrm{D\_TP}$ and $V_\mathrm{GS\_TP}$ are influenced by the channel mobility (μ_CH) and the threshold voltage (V_th). However, (4) does not fully explain the electrothermal interaction mechanism.

Using (1) to rearrange (3), and get the following theoretical expression:

$$\frac{\partial I_\mathrm{D}}{\partial T} = \sqrt{\frac{2WC_\mathrm{OX}}{L}}\sqrt{\mu_\mathrm{CH}I_\mathrm{D}}\left|\frac{\partial V_\mathrm{th}}{\partial T}\right| - \frac{I_\mathrm{D}}{\mu_\mathrm{CH}}\left|\frac{\partial \mu_\mathrm{CH}}{\partial T}\right| = g_m\left|\frac{\partial V_\mathrm{th}}{\partial T}\right| - \frac{I_\mathrm{CH}}{\mu_\mathrm{CH}}\left|\frac{\partial \mu_\mathrm{CH}}{\partial T}\right|$$

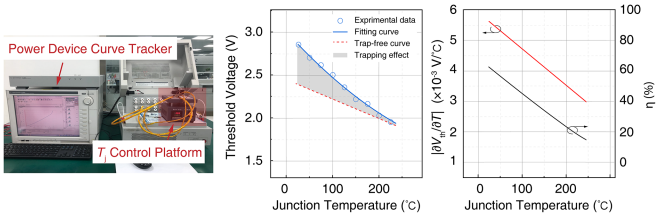


Fig. 1. Temperature sensitivity of the threshold voltage in SiC MOSFET with part number CREE QPM3-1200-0013D (obtained from experiments). (a) Measurement setup. (b) Relationship between the $V_{\rm th}$ and T_j. The trap-free curve is plotted based on the conclusion that $V_{\rm th}$ is unaffected by the trapping effect at high T_j [26]. (c) Relationship between $|\partial V_{\rm th}/\partial T|$, η and T_j.

$$= g_m \left(\underbrace{\left| \frac{\partial V_{\rm th}}{\partial T} \right|}_{\text{positive}} - \theta_{\rm T} \underbrace{\left| \frac{\partial \mu_{\rm CH}}{\partial T} \right|}_{\text{negative}} \right) \tag{5}$$

where the transconductance of the SiC MOSFET is

$$g_m\left(V_{\rm GS}\right) = \frac{\mu_{\rm CH} W C_{\rm OX}\left(V_{\rm GS} - V_{\rm th}\right)}{L} \tag{6}$$

and the acceleration factor of electrothermal interaction is

$$\theta_T\left(V_{\rm GS}\right) = \frac{V_{\rm GS} - V_{\rm th}}{2\mu_{\rm CH}}. \tag{7}$$

Using (5), $\partial I_{\rm D}/\partial T$ of the SiC MOSFET can be deduced. The following conclusions can be drawn: $\partial I_{\rm D}/\partial T$ is influenced by $|\partial V_{\rm th}/\partial T|$, $|\partial \mu_{\rm CH}/\partial T|$, and $\theta_{\rm T}$; and θ_T affects both the polarity (positive or negative) and intensity of $\partial I_{\rm D}/\partial T$.

From the relationship between $I_{\rm D}$ and T_j, it can be concluded that

$$I_{\rm D} = f\left[T_j,\ \theta_T\left(V_{\rm GS}\right)\right]. \tag{8}$$

B. Specific Analysis

1) Positive-Related Term $|\partial V_{\rm th}/\partial T|$: For the SiC power MOSFET, $V_{\rm th}$ can be expressed as [24], [25]

$$V_{\rm th} = \sqrt{4\varepsilon_{\rm S} kTN_A \ln\left(\frac{N_A}{n_i}\right)}/C{\rm ox} + \frac{2kT}{q}\ln\left(\frac{N_{\rm A}}{n_i}\right) + V_{\rm p,S} - \frac{Q{\rm ox}}{C{\rm ox}} \tag{9}$$

where $V_{p,S}$ is the potential difference between poly-Si and SiC, Q_{OX} is the charge due to oxide traps. The positive temperature coefficient of intrinsic carrier concentration (n_i) leads to a negative temperature coefficient of $V_{\rm th}$. The measured $|\partial V_{\rm th}/\partial T|$ is shown in Fig. 1(c) (obtained using Keysight B1505A). At higher T_j, the decrease in $V_{\rm th}$ slows down. This occurs because interface traps become occupied by electrons, increasing the interface state charge at the elevated T_j. Further, this is primarily because the elevated T_j enhances the electron emission effect of the traps, weakening the trapping effect. The grey shaded area, shown in Fig. 1(b), illustrates that the $\Delta V_{\rm th}$ caused by traps decreases rapidly with elevated T_j. To make this clearer, η is

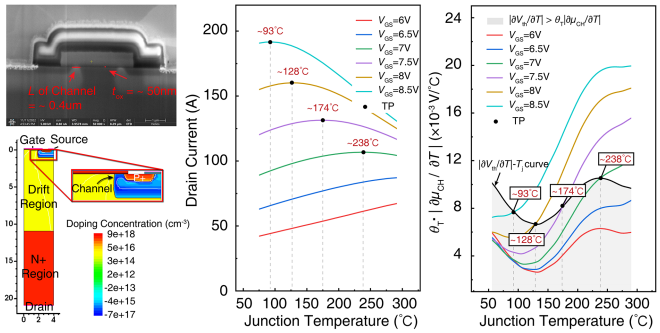


Fig. 2. Illustrations for the TP of TCAD simulations. (a) Cell structure obtained from FIB-SEM system and simulation structure of DUT. (b) Darin current with elevated T_j at $V_{\rm DS} = 8$V. (c) $\theta_T \cdot |\partial \mu_{\rm CH}/\partial T|$ and $|\partial V_{\rm th}/\partial T|$ with TP.

defined as

$$\eta = \frac{V_{\text{th, fitting}} - V_{\text{th, trap-free}}}{\Delta V_{\text{th, trap-free}}} \times 100\% \tag{10}$$

where $V_{\rm th,fitting}$ and $V_{\rm th,trap\text{-}free}$ represent the $V_{\rm th}$ values obtained from the fitting curve and the trap-free curve, respectively. $\Delta V_{\rm th,trap\text{-}free}$ is the $V_{\rm th}$ reduction caused by the semiconductor material. The η quantifies the contribution of trapping effect to the total factor in $\Delta V_{\rm th}$. After T_j exceeds 100 °C, the $\Delta V_{\rm th}$ caused by traps no longer dominates. This is the primary reason why the positive-related term diminishes as elevated T_j.

2) Negative-Related Term $|\partial \mu_{\rm CH}/\partial T|$ and Acceleration Factor $\theta_{\rm T}$: As T_j increases, stronger lattice vibrations and phonon scattering reduce $\mu_{\rm CH}$. The acceleration factor (θ_T), primarily determined by $V_{\rm GS}$, enhances the influence of the negative-related term in (5). The composition of θ_T indicates its dependence on the $V_{\rm th}$, $\mu_{\rm CH,}$ and the external circuit parameters $V_{\rm GS}$ [refer to (7)]. It is evident that θ_T increases as the T_j rises. Thus, θ_T acts as the acceleration factor for SiC MOSFETs. Therefore, θ_T plays a crucial role in $|\partial I_{\rm D}/\partial T|$.

C. Verification of the Theoretical Formula

1) Technology Computer Aided Design (TCAD) Simulations: This subsection primarily utilizes TCAD of semiconductor physics simulation called Sentaurus (Version. O), to verify the electrothermal interaction predicted by theoretical (5). In the TCAD simulations, a half-cell structure is used to improve simulation speed, as shown in Fig. 2(a). Clearly, the simulations do not allow for quantitative interpretation of DUT's electrothermal interaction, because the accurate doping parameters and process parameters of DUT cannot be obtained as they are proprietary to the manufacturer. The simulation model is structured to approximate the DUT, where some structural parameters are obtained through FIB-SEM system (Thermo Scientific Helios 5 UX).

The TCAD simulation conditions are as follows: $V_{\rm DS} = 8$ V, $V_{\rm GS}$ is scanned from 6 to 8.5 V in 0.5 V steps. To validate (5), the $I_{\rm D}$-T_j curves are extracted to obtain the TP [see Fig. 2(b)] and compared with the TP derived using (5) [see Fig. 2(c)]. Specifically, the TP point can be determined from the relationship

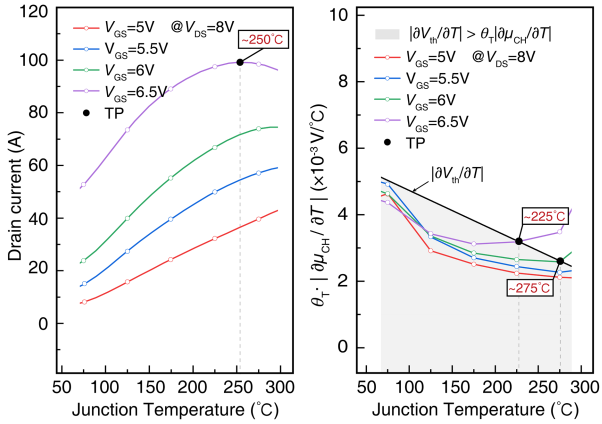


Fig. 3. Illustrations for the TP of experiments. (a) Darin current with elevated T_j at $V_{\mathrm{DS}} = 8$ V. (b) $\theta_T \cdot |\partial\mu_{\mathrm{CH}}/\partial T|$ and $|\partial V_{\mathrm{th}}/\partial T|$ with TP.

$dI_{\mathrm{D}}/dT = 0$, which can be directly obtained from the I_{D}-T_j curves. The TP point can also be determined using (5). When $dI_D/dT = 0$, (5) can be rearranged into "$|\partial V_{\mathrm{th}}/\partial T| = \theta_T|\partial\mu_{\mathrm{CH}}/\partial T|$". This equation represents the intersection of $|\partial V_{\mathrm{th}}/\partial T|$-$T_j$ curve and $\theta_T|\partial\mu_{\mathrm{CH}}/\partial T|$-$T_j$ curves, which determines the TP point. The simulation results show consistent TP values between both methods, indicating that (5) accurately describes the linear-mode electrothermal interaction.

2) Experiments Based on Power Device Curve Tracer: The DUT is experimentally tested using a power device curve tracer (Keysight B1505A) to validate the accuracy of (5). Fig. 3(a) displays the curves of drain current with elevated T_j. The experimental data are then processed using (5) to obtain TP, shown in Fig. 3(b). While the actual TP does not exactly match the TP derived from (5), both fall within a similar range. This discrepancy is due to measurement errors and approximations during data processing. The TCAD simulations, which eliminate most of these errors, show TP points that are essentially identical between the two methods. In summary, the similar TP values experimentally verify the accuracy of (5).

Furthermore, as shown in Figs. 2(c) and (c), higher V_{GS} values result in a lower TP temperature. In other words, the higher the V_{GS}, the lower the temperature at which the curves for $\theta_T|\partial\mu_{\mathrm{CH}}/\partial T|$ and $|\partial\mu_{\mathrm{CH}}/\partial T|$ intersect, i.e., the TP temperature. This verifies the control effect of V_{GS} on linear-mode electrothermal interaction.

By now, the mechanism of temperature sensitivity of the linear-mode drain current and the controllability of the external circuit parameter V_{GS} have been clarified, as demonstrated in theoretical (5) and (8).

III. Proposed T_{J} Extraction Strategy

A. Basic Principle

The basic principle of the LMCR method is that the real-time T_j of the SiC device can be obtained by injecting a narrow current pulse (I_{M}) and then measuring the response (representing the DUT's reaction to the pulse at T_j). I_{M} is provided by the proposed online I_{M} extraction unit, as shown in Fig. 4. The relationship

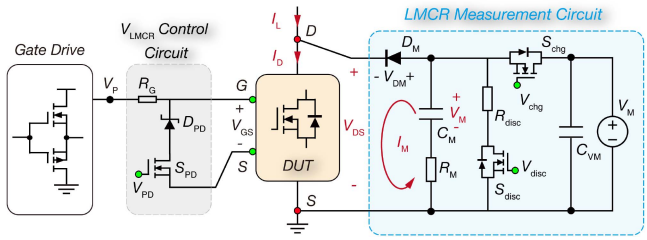


Fig. 4. Diagram of the proposed T_j online extraction unit consisting of LMCR measurement circuit and V_{LMCR} control circuit.

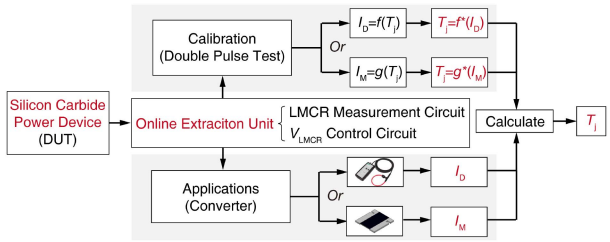


Fig. 5. Illustrations for the proposed online T_j extracting strategy.

between I_{D} and T_j is constrained by (8) and can be determined through a calibration process. Since I_{M} is equal to I_{D} minus the load current (I_{L}), it can also be used to measure T_j. Given that the V_{GS} is clamped to V_{LMCR} by the control circuit, θ_T is solely related to T_j. Thus, (8) can be rewritten as

$$I_{\mathrm{M}} = g\left(T_j\right). \tag{11}$$

The diagram of the T_j extracting strategy is shown in Fig. 5.

B. Online $\mathrm{T_j}$ Extracting Unit for Injecting Current

The proposed online T_j extracting unit is implemented using two circuits, as shown in Fig. 4. The first is the V_{LMCR} control circuit, which clamps V_{GS} to V_{LMCR} using Zener diode D_{PD} and is controlled by switch S_{PD}. Different V_{LMCR} values correspond to different I_{D} or I_{M} values and their temperature sensitivities. The second is the LMCR measurement circuit, which provides the narrow current pulse I_{M} via capacitor C_{M} and C_{VM}. In this circuit, S_{chg} controls the charging process of C_{M}, while S_{disc} controls its discharging. D_{M} blocks voltage from the power circuit to the LMCR measurement circuit.

C. Execution Process

1) Overall Control Logic: The control logic of LMCR is illustrated in Fig. 6 and described as follows. The LMCR stage begins spontaneously at the end of the DUT's turn-ON transients and continues until the device turns OFF. Before turning ON the DUT, the V_{LMCR} control circuit clamps V_{GS} to V_{LMCR} ($<V_{\mathrm{M}}$), and C_{M} is charged to V_{M} in preparation for injecting a narrow current pulse. During most of the DUT's turn-ON transients, D_{M} is reverse biased because V_{DS} is greater than V_{M}. When V_{DS} drops below V_{M}, D_{M} becomes forward biased and clamps V_{DS} near V_{M}, while C_{M} and C_{VM} inject the narrow current pulse into the DUT. At this stage, the DUT operates in linear mode

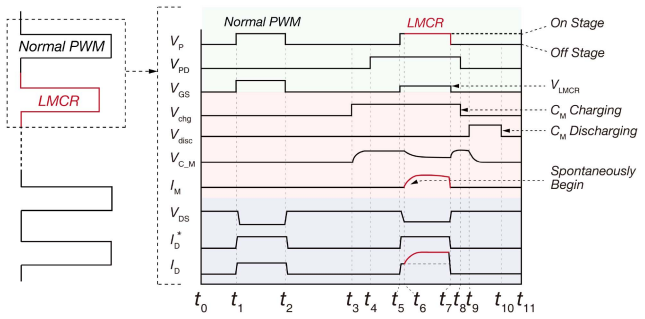


Fig. 6. Illustrations for the control logic of the LMCR.

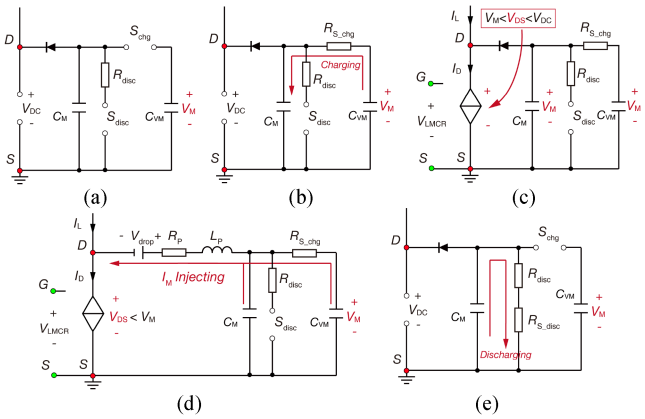


Fig. 7. Illustrations for equivalent circuit during LMCR. (a) $t_2<t<t_3$. (b) $t_3<t<t_5$. (c) $t_5<t<t_6$. (d) $t_6<t<t_7$. (e) $t_9<t<t_{10}$.

(V_{LMCR}-$V_{\mathrm{th}}<V_{\mathrm{DS}}$, low V_{GS} and V_{DS}), and the injected narrow current pulse follows (9). The equivalent circuit for LMCR during this key period is shown in Fig. 7. The T_j of the DUT can be obtained by measuring I_{D} or I_{M}.

2) Detailed Execution: The detailed execution process of LMCR is as follows.

$t_0 \sim t_3$: PWM Operation Stage. The DUT operates in a normal PWM state. The load is inductive, and the current rises linearly.

$t_3 \sim t_5$: LMCR Preparatory stage. V_{chg} turns to high level during $t_3 \sim t_4$. As a result, S_{chg} turns ON, and C_{M} is charged to V_{M} for subsequent current pulse injection. At t_4, S_{PD} turns ON, and D_{PD} clamps V_{GS} from $V_{\mathrm{GS(on)}}$ to V_{LMCR}. V_{LMCR} determines the value of I_{D} (or I_{M}) and its temperature sensitivity.

$t_5 \sim t_6$: DUT Turn-On Transients. At t_5, the DUT turns ON, and I_{D} begins to increase until I_{L}. V_{DS} then decreases from V_{DC} until reaching V_{M} at t_6.

$t_6 \sim t_7$: LMCR Execution stage. After t_6, the relationship between V_{DS} and V_{M} follows:

$$V_{\mathrm{DS}} \leq V_{\mathrm{M}} - V_{\mathrm{DM}}. \tag{12}$$

Thus, the LMCR stage begins spontaneously without additional control, and I_{M} is injected into the DUT. At t_7, the DUT turns OFF, ending the LMCR stage.

$t_7 \sim t_{10}$: Post-Execution Stage. At t_8, V_{C} and V_{chg} switch to low. During $t_9 \sim t_{10}$, V_{disc} turns to high and discharging C_{M} through R_{disc}. Thus, this ensures that the DUT will not be injected with C_{M} current in the next PWM cycle.

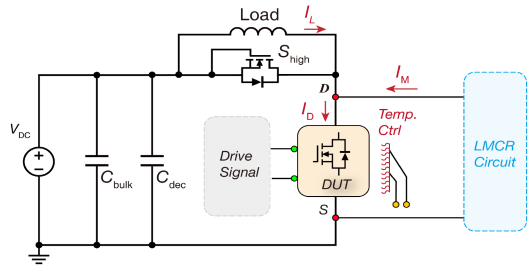


Fig. 8. Circuit of double pulse test.

D. Obtain the Real-Time T_j

During the LMCR execution process ($t_6 \sim t_7$), the equivalent circuit diagram of the measurement circuit is shown in Fig. 7(d). Key features include.

1) The characteristics of current pulse I_{M} mainly depends on DUT's I_{D} during the LMCR stage, i.e., $I_{\mathrm{M}} = I_{\mathrm{D}}$-$I_{\mathrm{L}}$.
2) During the LMCR stage, two factors vary with elevated T_j: $V_{\mathrm{th}}(T_j)$, and $\mu_{\mathrm{CH}}(T_j)$. According to the analysis in Section II.A, the value of I_{D} (or I_{M}) depends on these two T_j-related factors, as well as θ_T or V_{GS}, following (8).
3) Therefore, under constant $V_{\mathrm{GS}} = V_{\mathrm{LMCR}}$, different T_j values correspond to different responses to the injected narrow current pulse (i.e., I_{M} or I_{D}).

Based on these features, by measuring I_{M} (or I_{D}), the T_j of the DUT during the LMCR stage can be determined using the relationship between I_{M} and T_j (or I_{D} and T_j).

IV. Online Experiments for Calibration Based on Double Pulse Test

A. Experiment Setups

1) Operating Principle: The experimental verification and calibration of the LMCR method are based on the DPT shown in Fig. 8. DPT accurately replicates the operating conditions of the converter to investigate the DUT's performance, and is widely adopted in industry standards such as IEC [27], AQG [28], and JEDEC [29], as well as in academic research [2], [10], [30].

The control logic of the DUT follows Fig. 6. During normal PWM operation, the DUT turns ON, allowing current I_{D} to flow through the load L and the DUT, increasing linearly to the preset current I_{L}. When the DUT turns OFF, I_{L} flows through the body diode of S_{high}. During LMCR, I_{L} commutates to the DUT, simulating preset voltage and current conditions. This entire process occurs within microseconds, preventing significant T_j rise due to minimal self-heating, thus facilitating control of the DUT's T_j during the DPT.

2) Key Experimental Parameters: The experimental setup is shown in Fig. 9, and the main equipment is given in Table II. Important parameters for the DPT include: bus voltage is 400 V, load current is about 50 A, T_j varies from 30 to 150 °C with

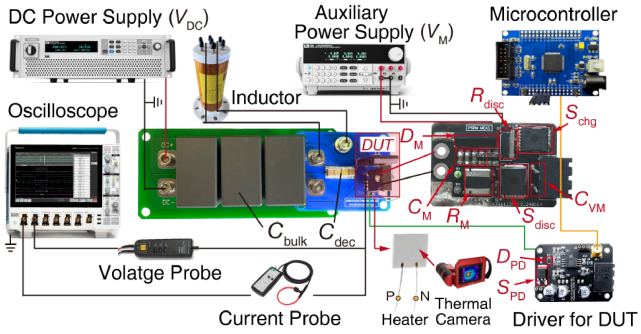


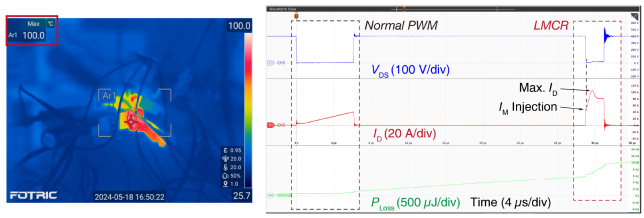
Fig. 9. Equipment of DPT experiment.

TABLE II
DETAILS OF MAIN EXPERIMENTAL EQUIPMENT

Objective	Details
Power Supply	ITECH IT6527D, 1000 V/10A; ITECH IT6036D-1500-80, 1500 V/80A
Power Electronic Load	IT8918A-600-1260, 600V/1260A
Oscilloscope	Tektronix MSO54, 500 MHz, 12bits
Voltage Probe	Tektronix THDP0200 200 MHz Tektronix TPP0500B 500 MHz
Current Probe	CWTMini50HF 06/B, 50 MHz, ±0.2%; Tektronix TCP0150 DC-20 MHz WSL36372L000DEA, 2 mΩ, ±0.5%
Inductor	200 μH (DPT); ~313 μH (converter)
Heater	Metal Ceramic Heater (MCH) 48 W with blackbody material coating
Thermal Camera	FOTRIC 288+, precision ±2%
DUT	CREE C3M0016120K, 1200 V/16 mΩ
S_{chg}, S_{disc}	Infineon IPT007N06N, 60 V/0.75 mΩ
Microcontroller	TMS320F28035PNT, 32-bit, 60 MHz

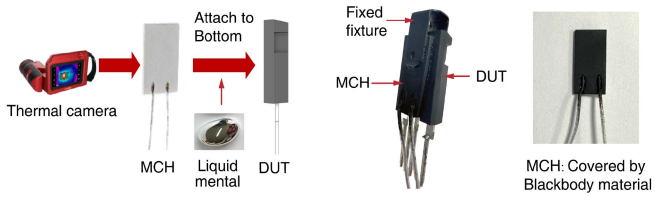
step of 10 °C, the period of LMCR is 2 μs, the charging time of C_M is 4 μs, the discharging time of C_M is 0.5 μs, $V_M = 15$ V, $C_M = 50$ μF, $C_{VM} = 470$ μF, $V_{LMCR} = 7$ V, $R_{disc} = 500$ mΩ, $R_G = 1$ Ω.

3) Calibration Process: The DUT's T_j is controlled using a metal-ceramic heater coated with blackbody material to enhance measurement accuracy. Liquid metal is used as a thermal interface material between the DUT and heater to reduce thermal resistance. T_j is obtained using a thermal camera [see Fig. 11(a)] and corrected by $P{\cdot}R_{th} = \Delta T$. Each measurement is taken after maintaining the target T_j for 10 min to ensure thermal steady state. The oscilloscope is set to single-trigger mode to capture the rising edge of the double pulse. If I_D is measured, it is directly recorded by a Rogowski coil probe. For I_M measurements, the maximum voltage V_{R_M} across shunt resistor R_M is measured, and I_M is calculated as V_M/R_M. Since $I_M = I_D$-I_L and I_L is constant, both methods are valid.



(a) (b)

Fig. 11. Illustrations for the DPT experiment results at $V_{DC} = 400$ V, $I_L = 50$ A, $T_j = 100$ °C, $V_{LMCR} = 7$ V. (a) Diagram of the temperature distributions. (b) Experimental waveforms.



(a) (b) (c)

Fig. 10. Illustration for the DUT temperature control. (a) Relationship between key components. Liquid metal as TIM is used as a thermal interface material to reduce contact thermal resistance. (b) Overall view. Covering the surface with blackbody material to improve emissivity and reduce optical measurement errors. (c) MCH covered with blackbody material.

4) Measurement Errors Analysis: I_D is measured using a noninvasive Rogowski coil probe, I_L is measured with an AC/DC current probe, and I_M is measured across the shunt resistor R_M using a passive voltage probe. The oscilloscope's vertical resolution is 50 mA, and the Rogowski coil probe has an accuracy of ±0.2%, yielding a measurement error of 0.002 I_D ± 0.05 A. The current shunt resistor has a tolerance of ±0.5%, resulting in an I_M measurement error of 0.005 I_M ± 0.05 A.

B. Calibration Results Analysis

Fig. 10 shows the DPT waveforms at $T_j = 100$°C. During the normal PWM stage, I_D increases linearly to 50 A within 6 μs. The LMCR stage begins near the end of the turn-ON transient and lasts for 2 μs. Under the influence of T_j and V_{LMCR}, I_M reaches a specific value, represented by the maximum current during LMCR.

Fig. 12(a) shows I_D waveforms at different T_j (from 30 to 150 °C with 10 °C increments), while Fig. 12(b) illustrates the linear relationship between maximum I_D and T_j. The fitting results show high temperature sensitivity (0.3568 A/°C) and a strong linear correlation (Pearson's $r = 0.9964$). This relationship can be linearized as

$$I_D = f(T_j) = 0.3568T_j + 69.2816. \tag{13}$$

Then, T_j can be expressed as

$$T_j = f^*(I_D) = 2.8027I_D - 194.1749. \tag{14}$$

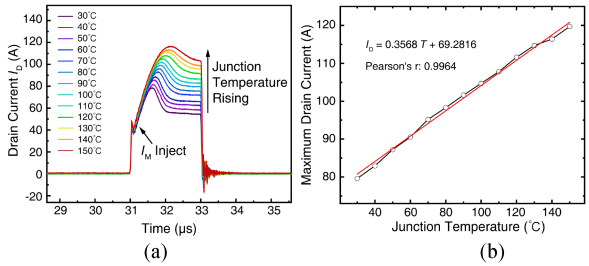


Fig. 12. Temperature sensitivity of I_D in LMCR. (a) Experimental waveforms of I_D at 30 °C∼150 °C. (b) Linear relationship between the maximum I_D and T_j.

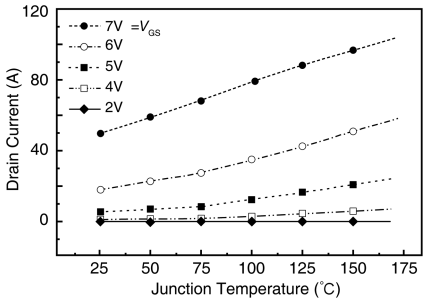


Fig. 13. Relationship between I_D and T_j in linear mode operation.

When I_M is measured, T_j can be expressed as

$$T_j = g^*(I_M) = 2.8474 I_M - 194.031. \tag{15}$$

The errors of T_j extraction are given by the following:

$$\varepsilon(T_j \sim I_D) = 0.0056 I_D \pm 0.1401. \tag{16}$$

$$\varepsilon(T_j \sim I_M) = 0.014 I_M \pm 0.1424. \tag{17}$$

With these calibrations, (14) and (15) can now be used for online T_j extraction.

C. Features and Advantages of LMCR Measurement

1) Electro-thermal Control Effect: Equation (5) reveals the control effect of θ_T on I_D in the SiC MOSFET operating in linear mode. V_{GS} is the main factor influencing θ_T. During calibration, $V_{LMCR} = 7$ V is selected for V_{GS} as it provides satisfactory temperature sensitivity for I_D in LMCR. Fig. 13 shows I_D changes under different V_{LMCR} values. The temperature sensitivity of I_D obtained through static parameter extraction is slightly different from that in the LMCR circuit but follows the same trend. Fig. 13 serves as a benchmark for selecting V_{LMCR} for the DUT.

2) Spontaneous Injection: The injection timing is determined by the relationship between V_{DS} and V_M. Fig. 14 shows the experimental waveforms. Before t_6, D_M is reverse biased ($V_{DS} > V_M$). When V_{DS} falls from V_{DC} to below V_M at t_6, D_M becomes forward biased, and C_M and C_{VM} spontaneously inject I_M into the DUT, eliminating the need for high-bandwidth control circuits. This feature makes LMCR cost-effective and suitable for high-frequency applications.

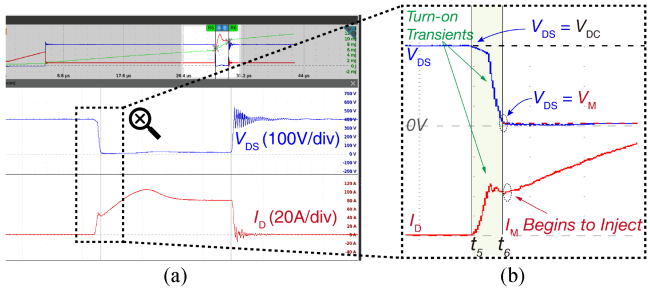


Fig. 14. Illustrations for the spontaneous injection. (a) Injection transients. (b) Enlarged diagram.

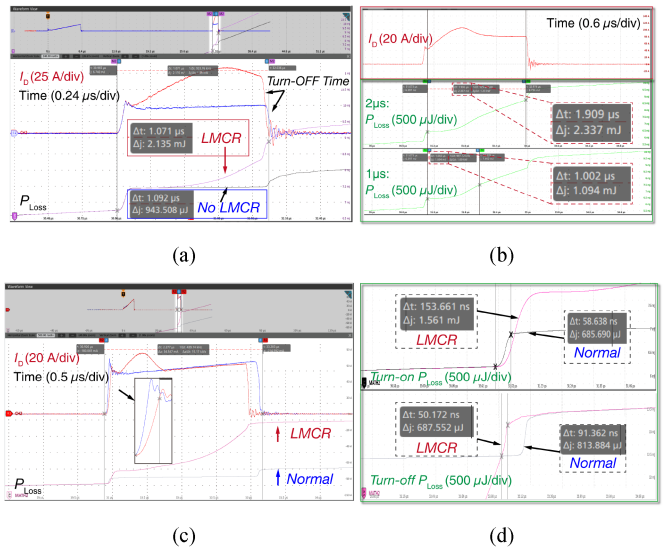


Fig. 15. Illustrations for the induced additional losses by LMCR. (a) Comparison between injected current and no injected current under LMCR setup. (b) Comparison of conduction losses. (c) Comparison between LMCR and normal conditions. (d) Comparison of conduction losses.

3) Low Additional Losses: Fig. 15(a) compares the total losses (switching and conduction) with and without injected current under LMCR conditions. Turn-ON switching losses before injection are unaffected by LMCR. The total loss with LMCR is 2.135 mJ, while without it, the loss is 943.508 μJ, mainly due to increased conduction losses and reduced turn-OFF losses. Fig. 15(b) shows that LMCR duration significantly affects conduction losses. For a 2 μs duration, the loss is 2.337 mJ, while for a 1 μs duration, it drops to 1.094 mJ. These losses are negligible compared to DUT's rated turn-ON losses of 2.3 mJ [31]. Further, the switching losses with and without LMCR are compared in Fig. 15(c) and (d). The turn-ON and turn-OFF losses with LMCR are 1.6 mJ and 688 μJ, while those without LMCR are 686 and 814 μJ. Thus, the turn-ON loss of LMCR increases, the turn-OFF loss decreases, but the total switch loss increases.

4) Multistage Capacitor Configuration: LMCR uses a multistage capacitor configuration to provide stable I_M, ensuring minimal V_{DS} and V_M fluctuations under different I_M and T_j values. The configuration consists of a high-frequency ceramic capacitor C_M (50 μF) and a medium-frequency electrolytic

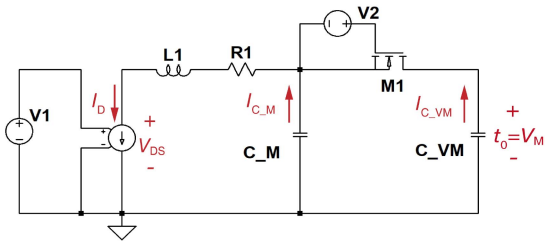


Fig. 16. Simulation circuits.

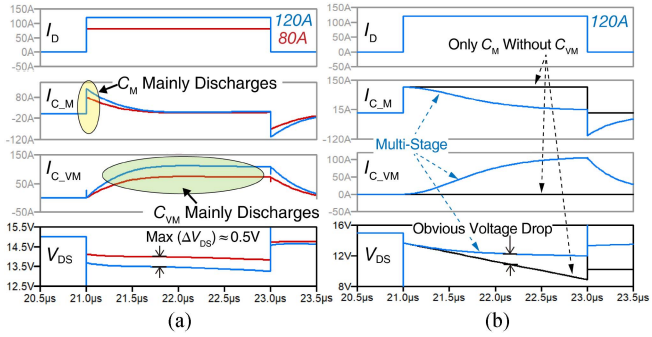


Fig. 17. Simulation explains for the multi-stage caps. (a) Effect of Mixed-use caps on different current levels. (b) Comparison between using and not using multistage caps.

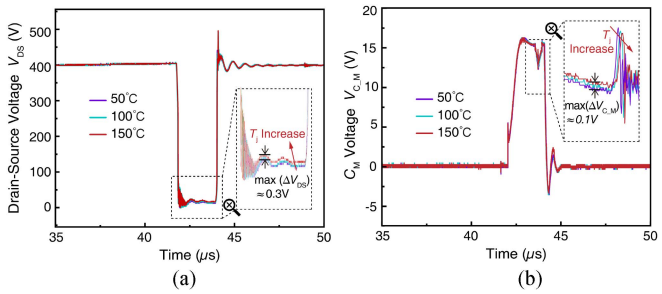


Fig. 18. Illustrations for the impact of T_j on the LMCR measurement. The waveforms are obtained from the double pulse test. (a) V_{DS} at different T_j. (b) V_{C_M} at different T_j.

capacitor C_{VM} (470 μF). LTSpice is used to simulate the charging process of multistage capacitors in LMCR (see Fig. 16). The results show that C_M mainly provides electric charge for I_M at high *di/dt* [yellow shadow in Fig. 17(a)], while C_{VM} supplies charge for low *di/dt* (green shadow). The use of both capacitors reduces V_{DS} fluctuations compared to using only C_M [see Fig. 17(b)]. Experimental results (see Fig. 18) show that V_{DS} drift due to different T_j is only 0.3 V. Considering the channel length modulation effect, the error is calculated as

$$\varepsilon\left(T_j \sim \lambda \Delta V_{DS}\right) = \lambda \Delta V_{DS} \cdot I_M = 0.0087 I_M \tag{18}$$

where λ is 0.029. Therefore, the extra errors are small enough.

5) Low Dependence From Load Current and Bus Voltage: The different I_L affects the value of I_M. Multistage capacitor configuration makes LMCR method insensitive to I_L. According to the above analysis, the I_M varies by nearly 40 A within the 50 to 150 °C. But the experimental waveforms in Fig. 18 shows

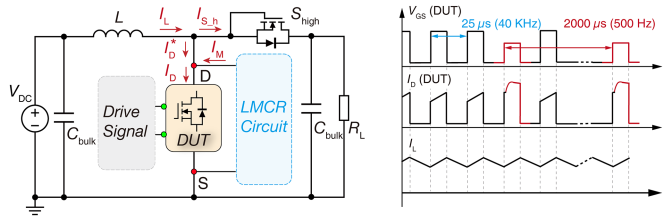


Fig. 19. Illustrations for power boost converter experiment. (a) Equivalent circuit. (b) Diagram of LMCR's sampling frequency and typical operation waveforms of boost converter.

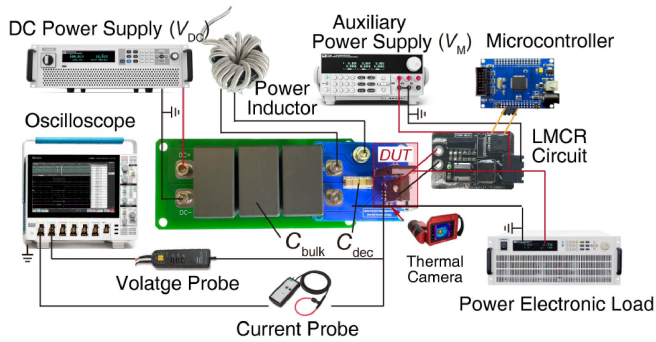


Fig. 20. Illustrations for boost converter experimental setups.

that the maximum offset between the V_{DS} and the voltage of C_M is very small, which is only 0.3 and 0.1 V, respectively.

As for the bus voltage, LMCR is executed during the period from the end of turn-ON switching transients to conduction and is therefore independent of the turn-OFF voltage.

V. Online Experiments Based on DC/DC Converter

A. Online Experimental Setups

The LMCR online T_j extraction is implemented using a boost power converter (see Fig. 19). The experimental setup is illustrated in Fig. 20. Key parameters of the boost converter include a bus voltage of 400 V, a load current of approximately 50 A, a switching frequency of 40 kHz, and an LMCR sampling frequency of 500 Hz [see Fig. 19(b)]. The LMCR period is 2 μs, with a charging time for C_M of approximately 4 μs and a discharging time of 0.5 μs. Additional parameters are as follows: $V_M = 15$ V; $C_M = 50$ μF; $C_{VM} = 470$ μF; $V_{LMCR} = 7$ V; $R_{disc} = 500$ mΩ; and $R_G = 1$ Ω.

B. Analysis of Online Extraction Experimental Results

Fig. 21 presents the experimental waveforms of the boost converter, while Fig. 22 provides detailed waveforms on the same time axis, offering further insight and verification of the LMCR method in a practical boost converter.

The online T_j extracting strategy (see Fig. 5) for the boost converter follows the calibration curve obtained through a double pulse test (DPT), represented as $T_j = f^*(I_D)$ or $T_j = g^*(I_M)$ [see (14) or (15)]. The I_D is measured using a noninvasive Rogowski coil current probe, while the injected current I_M is measured using an invasive current shunt resistor. In the experiments, both

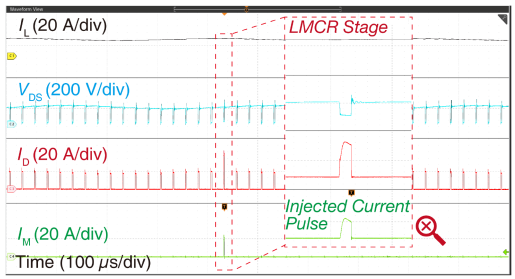


Fig. 21. Illustrations for power converter experiment. (a) Boost converter circuit. (b) Switching waveforms containing LMCR stage.

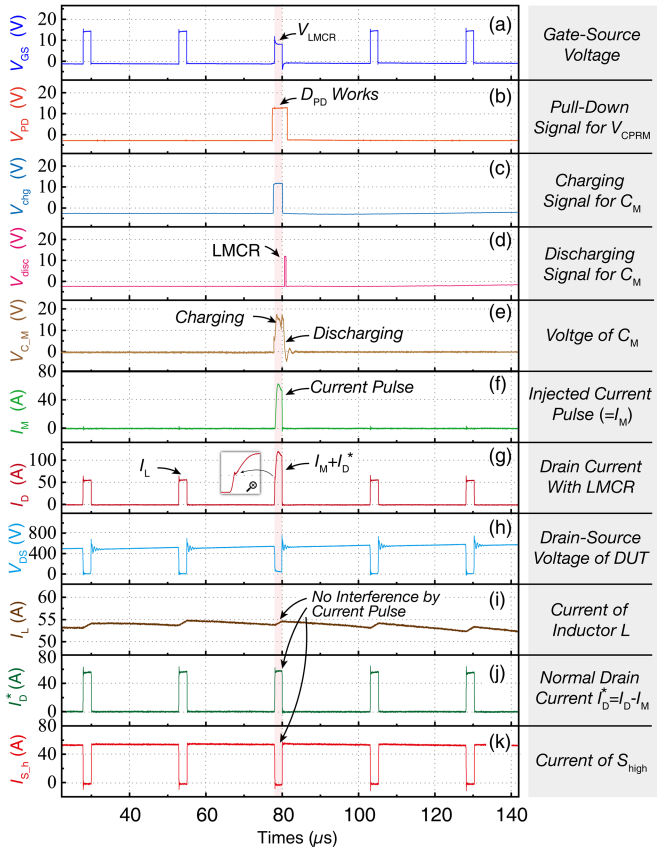


Fig. 22. Measured waveforms of power boost experiment. The waveform details are provided on the right side (gray shadow).

I_{D} and I_{M} are recorded, and (12) and (13) are used to calculate the real-time T_j. For example, when measuring I_{M}, the T_j at the LMCR measurement point in Fig. 22 is 120.60 °C, with an error margin of 0.7323 to 1.0125 °C, according to (16).

C. Verification Based on Optical Measurement

In high-voltage and high-power converter experiments, removing the packaging material of the DUT to perform optical measurement directly on the bare die is not feasible, as it would compromise insulation capabilities and pose a significant risk of short-circuits. Therefore, the following verification method is adopted: the load current is derated (approximately reduced to 5A) to limit the DUT's power dissipation to below 5W in

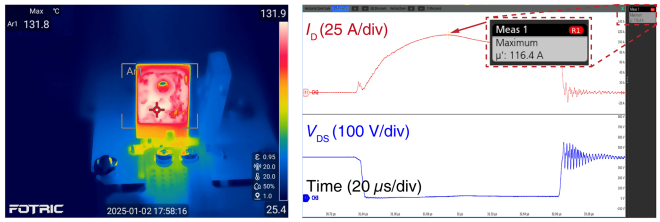


Fig. 23. Validation of LMCR method using thermal camera. (a) Temperature distribution of DUT drain metal under conditions without additional heat dissipation methods. (b) Current and voltage waveforms obtained using LMCR method.

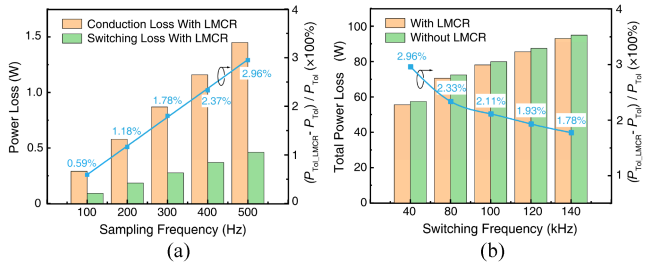


Fig. 24. Comparison of the power losses with and without LMCR. (a) Comparison of sampling frequency with LMCR and its losses. (b) Comparison of switching frequency and the total power losses with/without LMCR.

operation converter, while keeping other conditions unchanged. No additional cooling methods are applied to reduce the DUT's convective heat exchange with the environment, ensuring that no significant temperature gradient exists inside the device (further details are provided in the Appendix B). Under these conditions, the DUT's T_j is consistent with the drain metal temperature. The LMCR I_{D} is measured when the converter reaches a stable operation. As shown in Fig. 23(b), $I_{\mathrm{D\_max}}$ is 116.4 A. According to (14), the calculated T_j is 132.06 °C, which differed from the thermal camera measurement of 131.8 °C by only 0.26 °C [see Fig. 23(a)].

D. Analysis of Losses With Switching Frequency

The losses induced by the LMCR during the DPT are discussed in Section IV-C. The results show that the power loss introduced by the LMCR is negligible. An estimation of additional losses in the boost converter operating at 40 kHz is also conducted. Without LMCR, the switching and conduction losses of the DUT are 18.25 W and 37.32 W, respectively. With LMCR and a sampling frequency of 500 Hz, these losses increase to 18.48 W (1.26% increase) and 38.73 W (3.78% increase), respectively. The additional power loss ratio δ is defined as

$$\delta = \frac{P_{\mathrm{LMCR}}}{P_{\mathrm{Tol\_loss}}} \times 100\%. \tag{19}$$

where $P_{\mathrm{Tol\_loss}}$ is the total power loss without LMCR, and P_{LMCR} is the additional loss due to LMCR. The value of δ is calculated to be 2.951%, which is small enough to be considered negligible. Furthermore, Fig. 24 compares power losses with and without LMCR under different sampling frequencies and switching frequencies of the DUT, showing that the LMCR

TABLE III
COMPARISON WITH MEASUREMENT SENSITIVITY RATIO OF TYPICAL TSEPS

TSEPs	S (%/°C)	TSEPs	S (%/°C)
Turn-ON delay time	0.029	Short-circuit current (Si-IGBT)	0.17 [34]
Turn-ON delay time (R_G=160 Ω, I_L=6.5 A)	0.135 [13]	Dynamic threshold voltage	0.1773
Turn-OFF delay time	0.054	ON-state resistance	0.3944 [10]
Turn-OFF delay time (R_G=150 Ω, I_L=5 A)	0.118 [14]	Gate current	0.2257 [12]
Turn-OFF delay time (R_G=150 Ω, I_L=25 A)	0.123 [14]	Proposed LMCR method	0.5097

method consistently results in minimal and negligible additional losses.

E. No Interference to Other Elements of Converter

The current pulses injected during LMCR do not interfere with other components of the power converter. Fig. 22(a), (b), (c), (d), (e), (f), (g), (h), (i), (j), and (k) illustrates the experimental waveforms of the boost converter, containing one LMCR and four adjacent normal PWM cycles. In particular, Fig. 19(h), (i), (j), and (k) demonstrates that LMCR does not affect other PWM signals or electrical waveforms during the LMCR stage, such as the inductor current (I_{L}), S_{high} current ($I_{\mathrm{S\_h}}$), and I_{D}^{*}. The inductor current and the injected narrow current pulse intersect within the DUT without mutual interference.

F. Comparison Between the Proposed Method and Typical TSEP Extraction

1) Comparison of Time-Related TSEPs: For time-related TSEPs of SiC devices, such as switching time and switching delay time, the typical range is 10 to 50 ns. According to the "5 times rule" [32], the required bandwidth and sampling frequency must exceed 125 MHz to limit the measurement error to ±2%. For most transient TSEPs, a bandwidth exceeding 500 MHz is necessary, posing a significant cost challenge. In contrast, the time constant of the LMCR method is in the microsecond range, and the initiation timing is spontaneous (see Section IV-C), without requiring ns-level control or measurement circuit equipment which makes expensive high-bandwidth hardware unnecessary.

2) Comparison of Temperature Sensitivity: The temperature sensitivity of different types of TSEPs (time- and voltage-related) can be compared using a measurement sensitivity ratio [7], expressed as

$$S = \frac{|s|}{|Val_{\max}|} \times 100\%. \tag{20}$$

where S is the measurement sensitivity ratio, s is the temperature sensitivity, and $Val_{\max}$ is the maximum measured value of the TSEPs. The S of proposed method is calculated as 0.5097%/°C, with the comparative values for other TSEPs given in Table III. This demonstrates that the LMCR method offers the highest sensitivity, highlighting its superior temperature sensitivity and accuracy.

VI. CONCLUSION

This article proposes a novel method for online T_j extraction, namely LMCR. The primary objective is to utilize the high-sensitivity linear-mode current as a TSEP for real-time T_j extraction in SiC applications, improving both accuracy and reducing costs. The main contributions of this article are as follows.

1) The electrothermal interactions and temperature sensitivity of the linear-mode current in SiC power MOSFETs is investigated. For the first time, a theoretical formula is proposed and validated through TCAD simulations and experiments, demonstrating the high sensitivity and controllability of the linear-mode current.
2) An online T_j extracting unit and strategy is introduced and experimentally validated through DPT and boost converter experiments. Results show that the temperature sensitivity of the proposed method is 0.3568 A/°C with the measurement sensitivity ratio of 0.5097%/°C, significantly surpassing that of other TSEPs.
3) The impact of the method on power losses and its invasiveness is also examined. In boost converter experiments, the total losses of the DUT increased by only 2.951% due to the proposed method. Further analysis across different sampling and switching frequencies confirms its low-loss characteristics. Additionally, the method causes no interference with other elements of the converter.

In summary, the proposed method operates spontaneously, eliminating the need for high-bandwidth and expensive control or measurement circuits. Consequently, it offers high sensitivity, low interference, and cost-effectiveness. Additionally, this method holds great promise for applications in complex topologies, lifetime monitoring, and optimization.

APPENDIX

A. Comparison Between Linear Mode and Short-Circuit

The primary difference between linear-mode operation and short-circuit conditions lies in the regions of the device involved in electrothermal interactions. In linear mode, Section II presents a theoretical formula incorporating the device's threshold voltage and channel electron mobility, which has been validated through TCAD simulations and experimental data. This formula involves only the device's channel region, indicating that this is the key region in linear-mode operation. However, existing literature shows that short-circuit conditions are primarily influenced by intrinsic carriers in the drift region, which differs from the focus on the "channel region" in linear-mode operation [37].

This article utilizes TCAD simulations to compare linear-mode operation (V_{DS} = 15 V, V_{GS} = 7 V) with short-circuit conditions (V_{DS} = 500 V, V_{GS} = 15 V). The results reveal distinct current density distributions (see Fig. 25) and varying electron mobility distributions across different regions (see

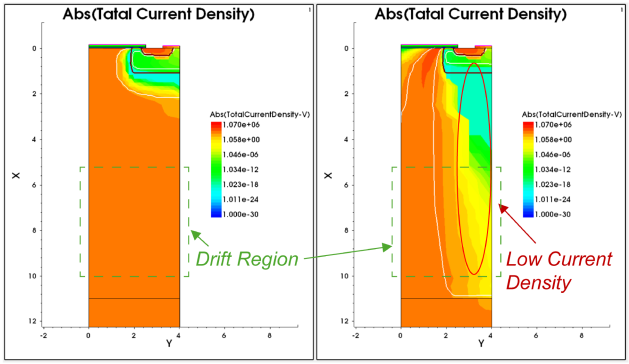


Fig. 25. Comparison of the current density distribution of MOSFET cell in linear mode and short-circuit condition. (a) Linear mode operation at $V_{DS} = 15$ V, $V_{GS} = 7$ V. (b) Short-circuit condition at $V_{DS} = 500$ V, $V_{GS} = 15$ V.

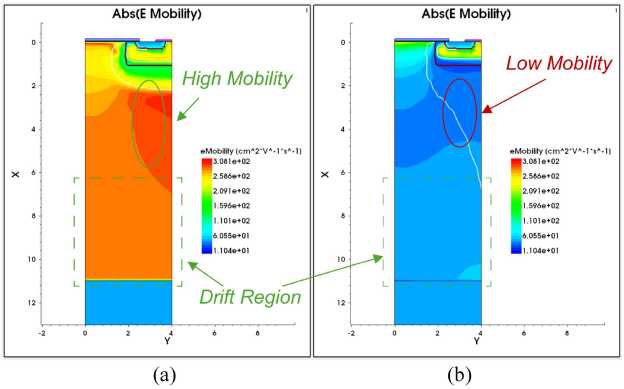


Fig. 26. Comparison of the electron mobility distribution of MOSFET cell in linear mode and short-circuit condition. (a) Linear mode operation at $V_{DS} = 15$ V, $V_{GS} = 7$ V. (b) Short-circuit condition at $V_{DS} = 500$ V, $V_{GS} = 15$ V.

Fig. 26). These differences indicate that the device's operational behavior and characteristics are fundamentally different under linear-mode and short-circuit conditions.

B. Comparison of Internal DUT Temperature Gradients Under Different Cooling Conditions

The external cooling conditions of power devices determine the internal temperature gradient. Without additional cooling, there is no significant temperature gradient within the power device. As a result, the temperature distribution at the device's bottom (drain mental), measured using a thermal camera, can accurately and indirectly reflect the T_j of the internal bare die.

To demonstrate the differences under cooling and uncooling conditions, finite element analysis simulations are conducted. The simulation conditions are given in Table IV. The boundary conditions are set as shown in. The results under cooling conditions are shown in Fig. 27, indicating a temperature difference of 7.58 °C between the junction and the bottom. Under uncooling conditions, the absence of effective heat transfer eliminates any significant temperature gradient along the heat dissipation path, making T_j nearly equal to the bottom drain mental temperature (ΔT_j is only 0.29 °C).

TABLE IV
DETAILS OF FINITE ELEMENT ANALYSIS SIMULATIONS

	With cooling	*Without cooling*
Position of nature cooling htc=50 W/(m^2·°C)	Case and terminal of DUT	Bottom, case and terminal of DUT
Position of forced water cooling htc=3000W/(m^2·°C)	Bottom of DUT	/
Bare die of power losses	50W	5W

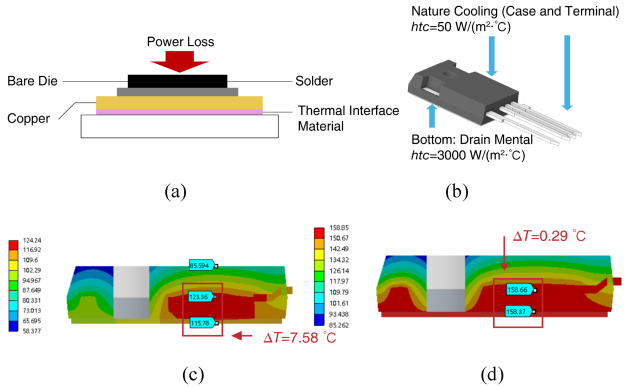


Fig. 27. Internal temperature distribution of power devices with or without additional cooling. (a) and (b) explanation of simulation model and applied boundary conditions. (c) Internal temperature distribution with additional cooling. (d) Internal temperature distribution without additional cooling.

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